Tungsten Hammer

Work Plan

by

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CSCI 320 Projec 2

Contents

Roles

Team Member:

A Team Member is an individual of the team. They should be dedicated and devoted to seeing the team succeed. They are expected to try there best and abide by the rules described in the Team Contract.

Organization

This team is comprised of three team members. Each team member holds equal weight in decision making of the team. When there are any conflicts involved, a simple vote can resolve the issues.

Schedule

Date	Milestone	Description
Thu 09/22	Team Assembly	Work on team contract and project plan. Initial work on Activity 06
Thu 09/29	Contract/Plan/Act 06 Due - 1st check in/team report	Finish/submit team contract, plan and Activity 06 - Single cycle MIPS CPU. Finish assigning the project individual modules
Thu 10/06	2nd check in/team report	Having individual base modules “completed”, start testing and integrating
Fri 10/07	Fall Break begins	Crunch time begins - Work hard
Wed 10/12	Fall Break ends	No more break
Thu 10/13	3rd check in/team report	Wrapping up the module integration. Testing with the 3 required programs. Start the Presentation.
Wed 10/19	The night before	Should finish up all work by now
Thu 10/20	Project due/Presentation	Present the work

Testing Plan

Individual modules or sets of modules should have accompanying functionality test files (up to the responsible team member to make sure that the assigned module has required behaviors, with timing requirements in mind).

Stages of the pipeline should have tests to verify its behaviors and interactions with other stages, keeping the forwarding buffers in mind.

The whole pipelined CPU would need to pass all the test programs, with correct pipeline timing and forwarding. Evolution by evolution, the CPU needs to pass each of the testing stages (NOPs -> Hello World - Fibonacci - Advanced Third Program)

Team Contract Analysis

Goals

Our goals are to learn a lot about the MIPS CPU architecture. We hope to gain an in depth knowledge about the material and be able to talk professionally about it. We also hope to develop our skills working on a team as well as our skills developing computer architecture in verilog.

Expectations

We have high expectations for every member of the team. We expect them to be punctual, communicate frequently, and strive to achieve the best project possible.

We would like all team members to attend meetings on time and finish their assigned work before it is due. This will help the projects operations be efficient and effective. We believe that strong communication is vital in having a working team environment, thus any issues should be expressed as soon as possible before they cannot be resolved.

Policies and Procedures

We will have weekly meetings at roughly the time of the lab sessions to discuss our progress for the last week as well as planning tasks for the upcoming week. Codes in crucial part of the project will be reviewed peer-to-peer. Each team member is responsible for his own assigned work and has to take initiative in order to produce the highest-quality work. They are also responsible for updating to other team members about their progress and being transparent when problems arise.

Consequences

Our team is understanding that college life can be chaotic and priorities can be lost. Therefore, before we decide to carry out any disciplinary actions, we will notify the members causing the issues about their faults. This gives them a chance to resolve the issues and it helps maintain a friendly team environment.