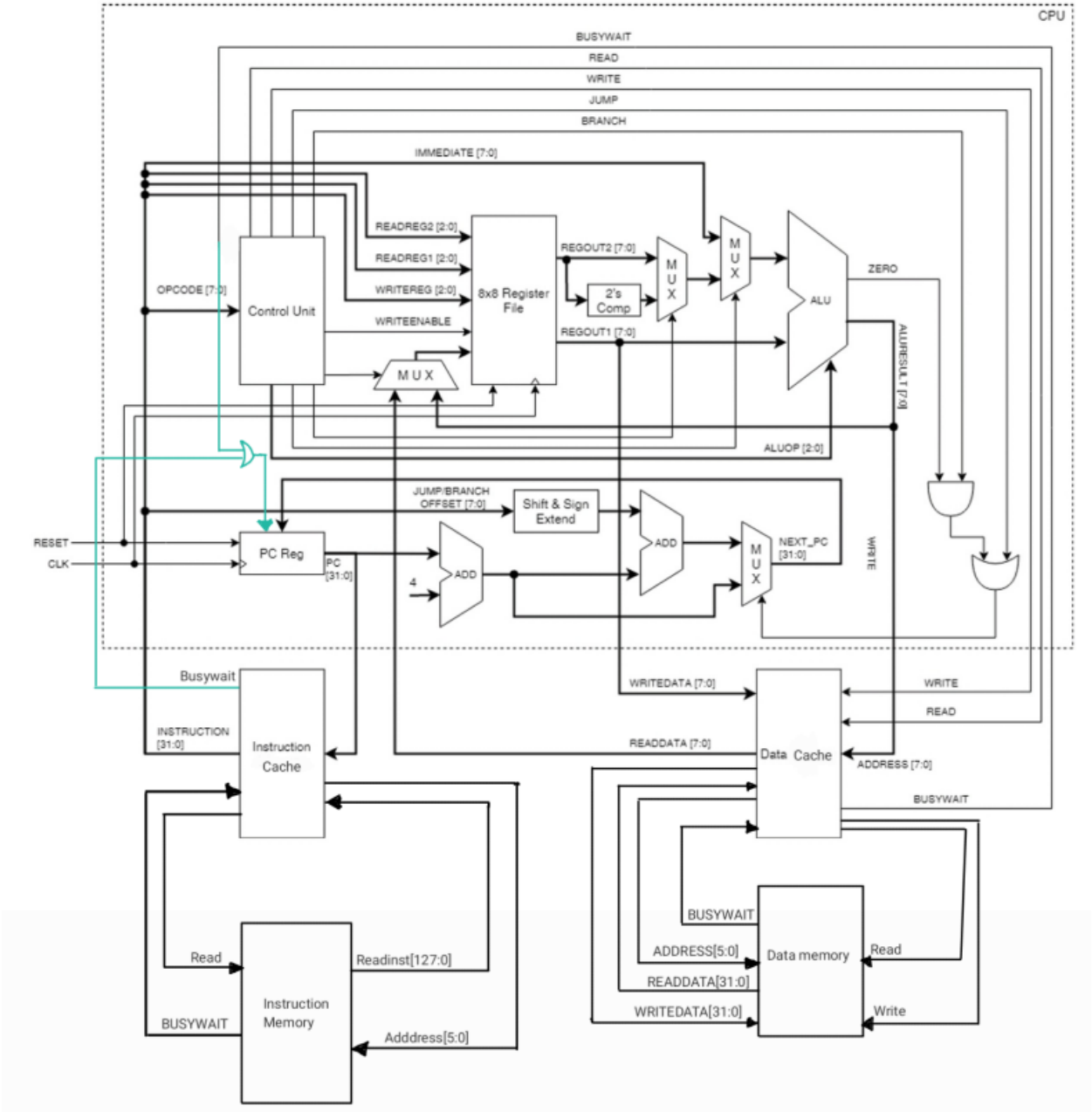
Lab 6 part 3

Group 19

E/20/100, E/20/280

The new design architecture for data cache memory and instruction cache memory presents a comprehensive approach to enhancing system performance.

Design architecture for Data cache memory and instruction cache memory,



Given program

```
1    loadi 0 0x09 // r0 = 9
2    loadi 1 0x01 // r1 = 1
3    swd 0 1 // m1 = r0 = 9
4    swi 1 0x00 // m0 = r1 = 1
5    lwd 2 1 // r2 = m1 = 9
6    lwd 3 1 // r3 = m1 = 9
7    sub 4 0 1 // r4 = r0 - r1 = 8
8    swi 4 0x02 // m2 = r4 = 8
9    lwi 5 0x02 // r5 = m2 = 8
10   swi 4 0x20 // m20 = r4 = 8
11   lwi 6 0x20 // r6 = m20 = 8
12
```

Time diagram for given program,