FD6287T

Three phases250Vgate driver

Overview

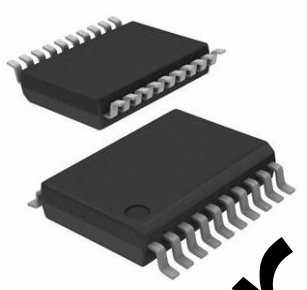
FD6287T is a half-bridge that integrates three independent Gate drive integrated circuit chip, designed for high voltage and high speed drive dynamic MOSFET design, Can operate up to +250V.

FD6287T built-in VCC/VBS undervoltage (UVLO) protection Protection function to prevent the power tube from working at too low voltage.

FD6287T has built-in shoot-through prevention and dead time to prevent Prevents the driven high- and low-side MOSFETs from passing through, effectively protecting power component.

FD6287T has built-in input signal filtering to prevent input Noise interference.

encapsulation



TSSOP-2

Features

- Suspension absolute voltage +250V
- Power supply operating voltage range: 7~20V
- Integrated three independent half-bridge drivers
- Output current +1.5A/-1.8A
- 3.3V/5V input logic compatible
- VCC/VBS undervoltage protection (U O)
- Built-in pass-through prevention tion
- Built-in 200ns de time
- Built-in i ut filte function
- High and low end nnel ma ng
- The high-e tput is in phase with the input, the low-end output is in phase with the input rse phase

pplication

Three-phase motor drive

1.Absolute maximum ratings(Unless otherwise specified, all pins areCOMas a reference point)

parameter		symbol	scope	unit
High side floating absolute voltage		$V_{B1,2,3}$	- 0.3~275	V
High-side floating offset voltage		$V_{S1,2,3}$	$V_{B1,2,3}$-25~$V_{B1,2,3}$+0.3	V
High side output voltage		$V_{HO1,2,3}$	$V_{S1,2,3}$-0.3~$V_{B1,2,3}$+0.3	V
Low side supply voltage		V_{CC}	- 0.3~25	V
Low side output voltage		$V_{LO1,2,3}$	- 0.3~V_{CC}+0.3	V
Logic input voltage (HIN, LIN*)		V_{IN}	- 0.3~V_{CC}+0.3	V
Offset voltage slew rate range		dVs/dt	≤50	V/ns
Power dissipation@T_A≤25-C	TSSOP-20	P_D	≤1.25	W
Thermal resistance to ambient	TSSOP-20	R_{AHr}	≤100	-C/W
Junction temperature range		T_j	≤150	-C
Storage temperature range		T_{stg}	- 55~15	-C

Note1: In any case, do not exceedP_D.

Note2: Voltage exceeding absolute maximum ratings may damage the chip.

2. Recommended working conditions(All voltages are inCOMas a reference point)

parameter	symb	imum value	maximum value	unit
High side floating absolute voltage		$V_{S1,2,3}$+7	$V_{S1,2,3}$+20	V
Static high-side floating offset voltage	$V_{S1,2,3}$	COM-2(Note1)	250	V
Dynamic high-side floating offset voltage	$V_{2,3}$	- 50(Note2)	250	V
High side output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Low side supply voltage	V_{CC}	7	20	V
Low side output voltage	$V_{LO1,2,3}$	0	V_{CC}	V
Logic input voltage (HIN, L*)	V_{IN}	0	V_{CC}	V
ambient temperature	T_A	- 40	125	-C

Note1:$V_{S1,2}$or(COM-2V)arri250Vhour,HOnormal work.$V_{S1,2,3}$for(COM-2V)arrive(COM-V_{BS})hour,HOLogical state is maintained.

Note2:$V_{S1,2,3}$for(COM-2V),Width50nsof transient negative voltage,HOnormal work.

Note3: If the chip works above the recommended working conditions for a long time, its reliability may be affected. It is not recommended that the chip be operated above the recommended operating conditions for an extended period of time.

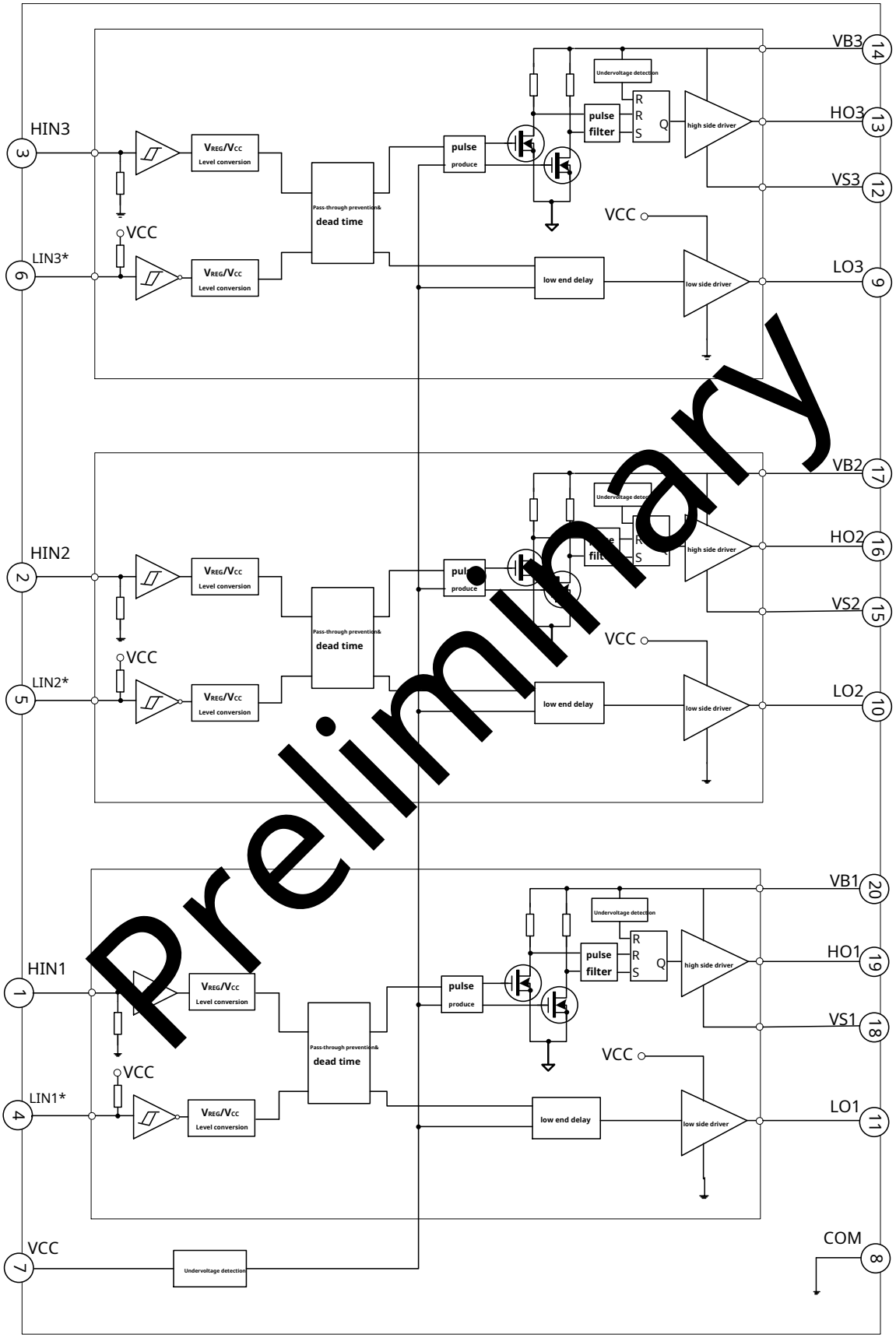
3. Static electrical parameters(Unless otherwise noted, otherwiseT_A=25-C,V_{CC}=$V_{BS1,2,3}$=15V,V_S=COM)

parameter	symbol	Test Conditions	minimum value	Typical value	maximum value	unit
High level input threshold voltage	V_{IH}		2.7	- -	- -	V
Low level input threshold voltage	V_{IL}		- -	- -	0.8	V
V_{CC}Undervoltage protection trip voltage	V_{CCUV+}		5.8	6.4	7.0	V
V_{CC}Undervoltage protection reset voltage	V_{CCUV-}		5.4	6.0	6.6	V
V_{CC}Undervoltage protection hysteresis voltage	V_{ccUVH}		0.3	0.4	- -	V
V_{BS}Undervoltage protection trip voltage	V_{BSUV+}		5.8	6.4	7.0	V
V_{BS}Undervoltage protection reset voltage	V_{BSUV-}		5.4	6.0	6.6	V
V_{BS}Undervoltage protection hysteresis voltage	V_{BSUVH}		0.3	0.4	- -	V
Floating power supply leakage current	I_{LK}	$V_{B1,2,3}$=$V_{S1,2,3}$=250V	- -	0.1	5.0	μA
V_{BS}Quiescent Current	I_{QBS}	V_{IN}=0Vor5V	- -	180	270	μA
V_{BS}dynamic current	I_{PBS}	$f_{HIN1,2,3}$=20kHz	- -	180	270	μA
V_{CC}Quiescent Current	I_{QCC}	V_{IN}=0Vor5V	- -	330	500	uA
V_{CC}dynamic current	I_{PCC}	$f_{LIN1,2,3}$=20kHz	- -	330	500	uA
LIN*High-level input bias current	I_{LIN+}	V_{LIN}=0V	- -	20	40	μA
LIN*Low level input bias current	I_{LIN-}	V_{LIN}=5V	- -	- -	2	μA
HINHigh-level input bias current	I_{HIN+}	V_{HIN}=5V	- -	20	40	μA
HINLow level input bias current	I_{HIN-}	V_{HIN}=0V	- -	- -	2	μA
Input pull-down resistor	R_{IN}		200	260	320	KΩ
High level output voltage	V_{OH}	I_O=10	- -	0.6	0.9	V
Low level output voltage	V_{OL}	I_O=00mA	- -	0.3	0.45	V
High level output short circuit pulse current	I_{OH}	V_O=0V,V_{IN}=5V,PWD≤10μs	1.1	1.5	1.9	A
Low level output short circuit pulse current	I_{OL}	V_O=15V,V_{IN}=0V,PWD≤10μs	1.3	1.8	2.3	A
$V_S$static negative pressure			- -	- 6.0	- -	V

4. Dynamic electrical parameters(Unless otherwise noted, otherwiseT_A=25-C,V_{CC}=$V_{BS1,2,3}$=15V,V_S=COM)

parameter	symbol	Test Conditions	minimum value	Typical value	maximum value	unit
Output rising edge transfer time	t_{on}		- -	300	450	ns
Output falling edge transfer time	t_{off}		- -	100	160	ns
Output rise time	t_r	C_L=1000pF	- -	12	- -	ns
Output fall time	t_f	C_L=1000pF	- -	12	- -	ns
High and low side delay matching	MT		- -	- -	50	ns
dead time	DT		100	200	300	ns

5. Circuit diagram



6. Chip pin configuration

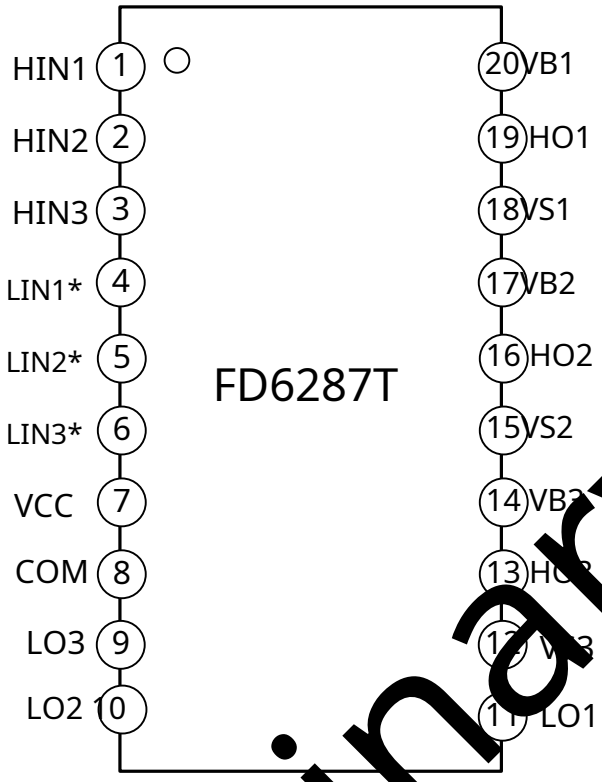
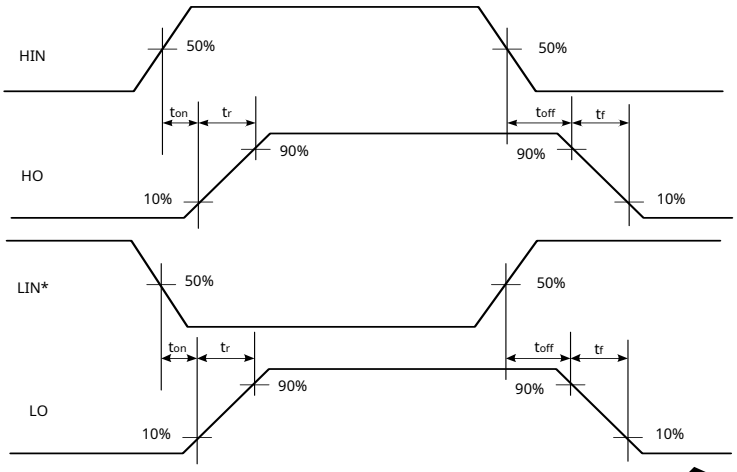


Figure 6-1 Package pin diagram

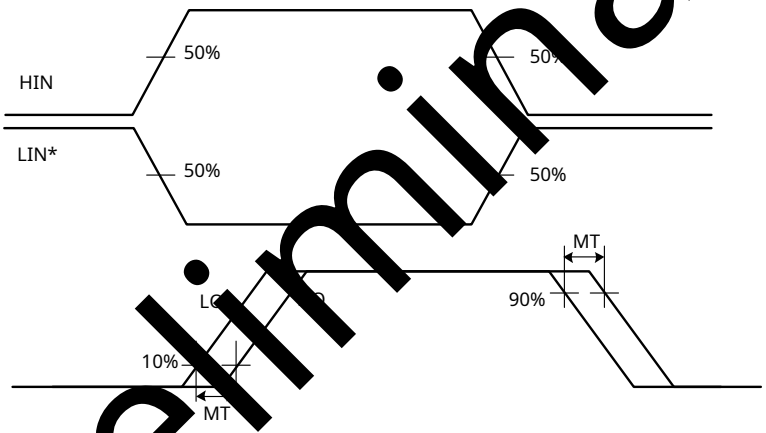
Table 6-1 Pin description

Pin number	Pin name	Pin description
1,2,3	HIN1,HIN2,HIN3	high side input
4,5,6	LIN1*,LIN2*,LIN3*	low side input
7	VCC	Low side supply voltage
8	COM	ground
9,10,11	LO3,LO2,LO1	low side output
12,15,18	VS3,VS2,VS1	High-side floating offset voltage
13,16,19	HO3,HO2,HO1	high side output
14,17,20	VB3,VB2,VB1	High side floating absolute voltage

7. Switching time test standards



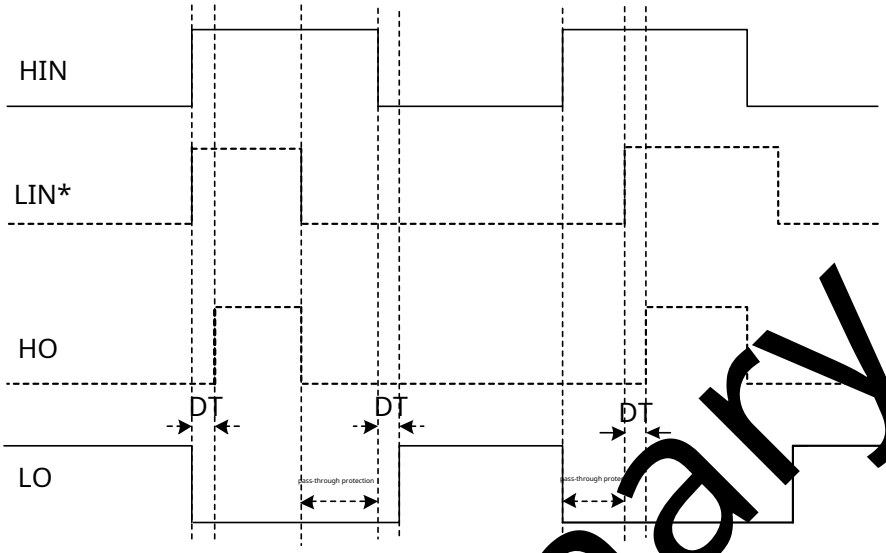
8. Transmission time matching test standards



9. Pass-through prevention function

The chip's internal design is specifically designed to prevent power tube cut-through protection circuitry, which can effectively prevent high-side and low-side input signals from being interfered with.

Direct damage to the power tube caused by interference. The figure below shows how the shoot-through prevention circuit protects the power tube.



10. Dead zone function

A fixed dead time protection circuit is set up inside the chip. During the dead time, both the high-side and low-side outputs are set low.

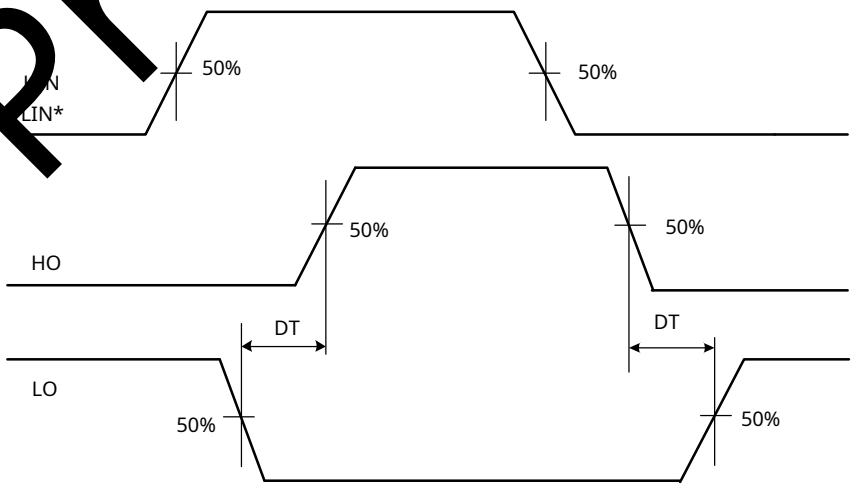
The set dead time must ensure that after one power tube is turned off, another power tube is turned on to effectively prevent the occurrence of upper and lower power tubes.

pass-through phenomenon. If the external dead time set by the logic input is greater than the dead time set internally in the chip, the

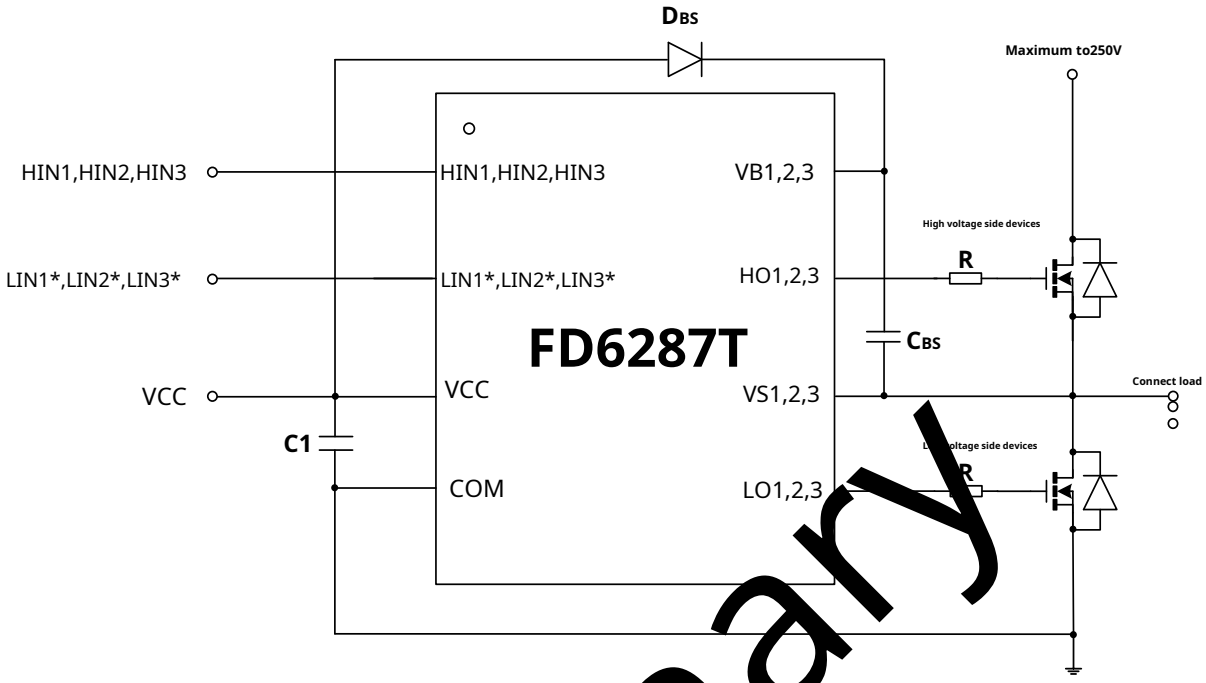
The external dead time is the chip output dead time; if the external dead time set by the logic input is less than the dead time set internally in the chip

time, the dead time output by the chip is the dead time set internally in the chip. The following figure depicts the dead time, input signal and driver

Timing relationship of output signals.



11. Typical application circuit



C1: Power supply filter capacitor, 10μF~100μF can be selected according to the circuit conditions, as close as possible to the chip pin.

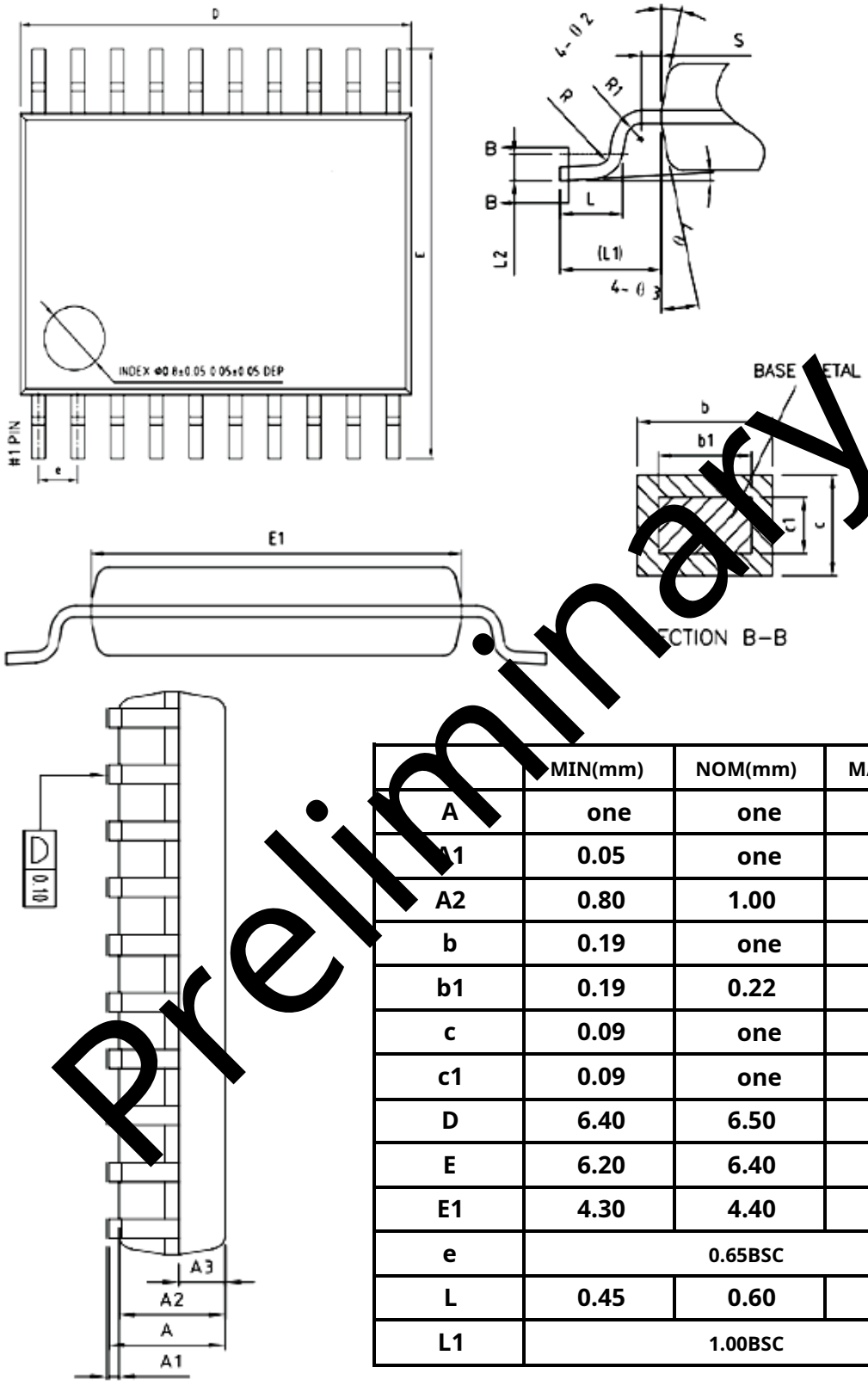
R: Gate drive resistor, the resistance value depends on the driven device and the application.

Dbs: Bootstrap diode, Schottky diode with high reverse breakdown voltage and short recovery time should be selected.

Cbs: Bootstrap capacitor, ceramic capacitor or tantalum capacitor should be selected, 1μF~50μF can be selected, as close as possible to the chip pin.

Note: The above circuits and parameters are for reference only. The parameters of the actual application circuit should be set based on the actual measurement results.

12. Package size (TSSOP-20)



	MIN(mm)	NOM(mm)	MAX(mm)
A	one	one	1.20
A1	0.05	one	0.15
A2	0.80	1.00	1.05
b	0.19	one	0.30
b1	0.19	0.22	0.25
c	0.09	one	0.20
c1	0.09	one	0.16
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		

Product number	Package form	Marking	Packing	quantity
FD6287T	TSSOP20	FD6287T	Tape&Reel	3000

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