UNIT I VHDL DESIGN

CARRERRIDE

1. An Assert is _____ command. Answer: b. Concurrent
2. The 'next' statements skip the remaining statement in the _____ iteration of loop and execution starts from first statement of next iteration of loop. Answer: c. Current (present)
3. Which among the following wait statement execution causes the enclosing process to suspend and then wait for an event to occur on the signals? Answer: b. Wait on x, y, z
4. In composite data type of VHDL, the record type comprises the elements of _____data types. Answer: b. Different
5. Which among the following is pre-defined in the standard package as one-dimensional array type comprising each element of BIT type? Answer: b. Bit_vector type
6. In VHDL, which class of scalar data type represents the values necessary for a specific operation? Answer: d. Enumerated types
7. Which data type in VHDL is non synthesizable & allows the designer to model the objects of dynamic nature? Answer: b. Access
8. In VHDL, which object/s is/are used to connect entities together for the model formation? Answer: c. Signal
9. In Net-list language, the net-list is generated _____synthesizing VHDL code. Answer: c. After
10. Among the VHDL features, which language statements are executed at the same time in parallel flow? Answer: a. Concurrent

SANFOUNDRY

1. Which of the following language can describe the hardware? Answer: d) VHDL
2. What do VHDL stand for? Answer: b) VHSIC hardware description language
3. What does VHSIC stand for? Answer: a) very high speed integrated chip
4. Each unit to be modelled in a VHDL design is known as Answer: c) design entity
5. Which of the following are capable of displaying output signal waveforms resulting from stimuli applied to the inputs? Answer: a) VHDL simulator

6. Which of the following describes the connections between the entity port and the local component? Answer: a) port map
7. Who proposed the CSA theory? Answer: c) Hayes
8. Which of the following is a systematic way of building up value sets? Answer: a) CSA theory
9. Which of the following is an abstraction of the signal impedance? Answer: b) strength
10. Which of the following is an abstraction of the signal voltage? Answer: a) level

TESTBOOKS

1. Which modeling style in VHDL uses 'process' & sequential statements Answer: a) Behavioral modeling
2. Which of the following is a key feature of VHDL Answer: a) It supports sequential & concurrent execution
3. Which data object in VHDL is used to represent interconnection wires and is declared in entity, architecture, or package declarations? Answer: c) Signal
4. Which modeling style describes a circuit using interconnected components and their structure? Answer: c) Structural
5. Which of the following is NOT a valid VHDL concurrent statement? Answer: c) if-else inside a process
6. In a Moore machine, the outputs depend on: Answer: a) The present state only
7. What is the purpose of a test bench in VHDL? Answer: b) To verify the functionality of the design by providing inputs and checking outputs
8. Which package defines the std_logic and std_ulogic data types? Answer: b) std_logic_1164
9. What is metastability in digital circuits? Answer: c) A condition where a flip-flop settles into an unpredictable state due to timing violations
10. What is the primary difference between std_logic and std_ulogic data types? Answer: c) std_logic automatically resolves conflicting logic levels, while std_ulogic does not
11. Which of the following is a user-defined data type in VHDL? Answer: c) Enumerated type (e.g. type state is (st0, st1, st2))

12. What is the primary use of the TEXTIO package in VHDL? Answer: b) To read/write test vectors from/to a text file
13. Which of the following is NOT a solution to metastability? Answer: a) Using a faster clock
14. Which of the following is Not the feature of HDLs Answer: c) Used for creating analog circuits
15. What is the purpose of 'testbench' in HDL design Answer: b) To simulate behaviour of design

UNIT II PLD ARCHITECTURE AND APPLICATIONS

CARRERRIDE

1. Which level of routing resources are supposed to be the dedicated lines allowing output of each tile to connect directly to every input of eight surrounding tiles? Answer: a. Ultra-fast local resources
2. In spartan-3 family architecture, which programmable functional element accepts two 18 bit binary numbers as inputs and computes the product? Answer: d. Multiplier Blocks
3. An antifuse element initial provides _____ between two conductors in absence of the application of sufficient programming voltage. Answer: b. Insulation
4. Which type of CPLD packaging comprises pins on all four sides that wrap around the edges of chip? Answer: b. Quad Flat Pack (QFP)
5. Simple Programmable Logic Devices (SPLDs) are also regarded as _____. Answer: d. All of the above (Programmable Array Logic (PAL), Generic Array Logic (GAL), Programmable Logic Array (PLA))
6. Which among the following is/are not suitable for in-system programming? Answer: a. EPROM
7. The devices which are based on fusible link or antifuse are _____time/s programmable. Answer: a. one
8. Which programming technology/ies is/are predominantly associated with SPLDs and CPLDs? Answer: d. All of the above (EPROM, EEPROM, FLASH)
9. In fusible link technologies, the undesired fuses are removed by the pulse application of _____voltage & current to device input. Answer: c. High
10. An Antifuse programming technology is predominantly associated with _____. Answer: b. FPGAs

11. Which among the following statement/s is/are not an/the advantage/s of Programmable Logic Devices (PLDs)? Answer: b. Increased space requirement
12. What do the Programmable Logic Devices (PLDs) designed specially for the combinational circuits comprise? Answer: a. Only gates
13. In JTAG programming, JTAG stands for _____ Answer: d. Joint Test Action Group
14. What would happen, if smaller logic modules are utilized for performing logical functions associated with FPGA? Answer: c. A & D (Propagation delay will increase, Number of interconnected paths in device will decrease)
15. What is/are the configurable functions of each and every IOBs connected around the FPGA device from the operational point of view? Answer: d. All of the above (Input operation, Tristate output operation, Bi-directional I/O pin access)
16. Which type of CPLD packaging can provide maximum number of pins on the package due to small size of the pins? Answer: d. BGA
17. How many logic gates can be implemented in the circuit by complex programmable logic devices (CPLDs)? Answer: d. 10000
18. Which gates are used on the output side as buffers in order to provide a programmable output polarity in PAL 16 P8 devices? Answer: c. EX-OR
19. If the number of nichrome fuse links in PAL are equal to 2M xn, then what does 'n' represent in it? Answer: d. Number of product terms
20. Which among the following are used in programming array logic (PAL) for reducing the loading on inputs? Answer: a. Input buffers

SANFOUNDRY (First set)

1. The inputs in the PLD is given through _____ Answer: d) AND gates
2. PAL refers to _____ Answer: c) Programmable Array Logic
3. Outputs of the AND gate in PLD is known as _____ Answer: a) Input lines
4. PLA contains _____ Answer: a) AND and OR arrays
5. PLA is used to implement _____ Answer: c) A complex combinational circuit
6. A PLA is similar to a ROM in concept except that _____ Answer: c) It doesn't provide full decoding to the variables
7. For programmable logic functions, which type of PLD should be used? Answer: a) PLA

8. The complex programmable logic device contains several PLD blocks and _____ Answer: c) Global interconnection matrix
9. Which type of device FPGA are? Answer: d) PLD
10. The difference between a PAL & a PLA is _____ Answer: b) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
11. If a PAL has been programmed once _____ Answer: d) It cannot be reprogrammed
12. The FPGA refers to _____ Answer: b) Field Programmable Gate Array
13. The full form of VLSI is _____ Answer: c) Very Large Scale Integration
14. In FPGA, vertical and horizontal directions are separated by _____ Answer: b) A channel
15. Applications of PLAs are _____ Answer: d) All of the Mentioned (Registered PALs, Configurable PALs, PAL programming)

SANFOUNDRY (Second set)

1. What is memory decoding? Answer: b) The process of Memory IC used in a digital system is selected for the range of address assigned
2. The first step in the design of memory decoder is _____ Answer: c) Address assignment
3. How many address bits are required to select memory location in the Memory decoder? Answer: c) 12 KB
4. How memory expansion is done? Answer: c) By connecting Memory ICs together
5. IC 4116 is organised as _____ Answer: b) 16 * 1
6. To construct 16K * 4-bit memory, how many 4116 ICs are required? Answer: d) 4
7. How many 1024 * 1 RAM chips are required to construct a 1024 * 8 memory system? Answer: c) 8
8. How many 16K * 4 RAMs are required to achieve a memory with a capacity of 64K and a word length of 8 bits? Answer: a) 2
9. The full form of PLD is _____ Answer: c) Programmable Logic Devices

10. PLD contains a large number of _____ Answer: b) Gates
11. Logic circuits can also be designed using _____ Answer: c) PLD
12. In PLD, there are provisions to perform interconnections of the gates internally, because of _____ Answer: c) The desired logic implementation
13. Why antifuses are implemented in a PLD? Answer: d) As a switching devices
14. How many types of PLD is? Answer: b) 3
15. PLA refers to _____ Answer: c) Programmable Logic Array

TEXTBOOK

1. The FPLA is a programmable logic that combines the characteristics of Answer: 3. RAM and PAL
2. Downloading means Answer: 1. Transferring programs from a programming device to a PLC
3. Select the correct statement about PLA (Programmable logic array) Answer: iii) In PLA both AND and OR gate plane are programmable
4. Programmable logic array has Answer: 4. Programmable AND gate followed by a programmable OR gate
5. A. HDL Coding /RTL Design B. Synthesis C. Static Timing Analysis D. Place and Route E. Programming file generation What is the correct order of the FPGA design flow? Answer: 1. A, B, C, D, E
6. What is a primary advantage of using PLDs in digital circuit design? Answer: c) Customizable logic implementation
7. Which PLD is typically used in applications requiring high-speed and low-latency operations? Answer: c) FPGA
8. Which of the following statements is true about FPGAs? Answer: a) They are programmed using only hardware description languages
9. In a CPLD, what is the function of the macrocell? Answer: c) To implement logic functions

UNIT III BASIC MOS THEORY

SANFOUNDRY

1. In negative logic convention, the Boolean Logic [1] is equivalent to: Answer: b) 0 V
2. In positive logic convention, the true state is represented as: Answer: a) 1
3. In CMOS logic circuit the n-MOS transistor acts as: Answer: c) Pull down network
4. In CMOS logic circuit the p-MOS transistor acts as: Answer: b) Pull up network
5. In CMOS logic circuit, the switching operation occurs because: Answer: c) N-MOSFET transistor turns ON, and p-MOSFET transistor turns OFF for input '1' and N-MOS transistor turns OFF, and p-MOS transistor turns ON for input '0'
6. When both nMOS and pMOS transistors of CMOS logic design are in OFF condition, the output is: Answer: c) High impedance or floating(Z)
7. When both nMOS and pMOS transistors of CMOS logic gates are ON, the output is: Answer: c) Crowbarred or Contention(X)

CAREERRIDE

1. nMOS devices are formed in _____ Answer: c) p-type substrate of moderate doping level
2. Source and drain in nMOS device are isolated by _____ Answer: b) two diodes
3. In depletion mode, source and drain are connected by _____ Answer: b) conducting channel
4. What is the condition for non saturated region? Answer: c) Vds lesser than Vgs -- Vt
5. In enhancement mode, device is in _____ condition. Answer: b) non conducting

TEXTBOOK

1. Which one of the following is not a basic MOSFET device type? Answer: 3. Narrow P-channel MOSFET
2. Which type of the MOSFETs is exclusively used by MOS digital ICs? Answer: 1. Enhancement MOSFET
3. For an n-channel E-MOSFET Vth = 5V, what is the condition to turn ON the device? Answer: 3. VGs > 5V
4. Power dissipation is negligibly small in: Answer: 4. CMOS
5. Which of the following is the fastest switching device? Answer: 3. MOSFET

6. Which of the following statements is true for E-MOSFET? Answer: 3. The E-MOSFET is capable of operating only in the enhancement mode
7. Why is an N-channel MOSFET preferred over a P-channel MOSFET? Answer: 1. Because it allows fast switching
8. Enhancement mode is present in Answer: 4. MOSFET
9. The (Id - Vgs) characteristics of a MOSFET in the saturation region is: Answer: 2. quadratic
10. What is the condition for non conducting mode? Answer: d) Vgs = Vds = Vs = 0
11. nMOS is _____ Answer: b) acceptor doped
12. Inversion layer in enhancement mode consists of excess of _____ Answer: b) negative carriers
13. What is the condition for linear region? Answer: b) Vgs greater than Vt
14. As source drain voltage increases, channel depth _____ Answer: b) decreases
15. Electrical charge flows from _____ Answer: a) source to drain
16. Enhancement mode device acts as ____ switch, depletion mode acts as ____ switch. Answer: a) open, closed
17. Depletion mode MOSFETs are more commonly used as _____ Answer: b) resistors
18. In n channel MOSFET _____ is constant. Answer: c) channel depth
19. MOS transistors consist of which of the following? Answer: d) all of the mentioned

UNIT IV DIGITAL CMOS CIRCUITS AND ISSUSES

TEXTBOOK

1. Which one of the following statements is not correct for CMOS technology in comparison with bipolar technology? Answer: 4. CMOS technology has high output drive current
2. The full forms of the abbreviations TTL and CMOS in reference to logic families are Answer: 3. Transistor Transistor Logic and Complementary Metal Oxide Semiconductor
3. The typical quiescent power dissipation of low-power CMOS units is Answer: 3. 2 nW

4. Which circuit takes the less chip area in large scale integration? Answer: 4. CMOS circuits
5. As compared to TTL, CMOS logic has Answer: 4. none of the above
6. The main advantage of CMOS is its Answer: 4. Low power consumption
7. In which one of the following IC technology, the switch implementation is good? Answer: b) CMOS
8. What is the standard form of PDN? Answer: b) Pull Down Network
9. In a CMOS Inverter, which of the following is true? Answer: b) There is one PMOS and one NMOS Transistor
10. Which statement/s is/are considered to be precise regarding the operational behaviour of MOS transistor? Answer: d) All of the above

CARRERRIDE

1. In accordance to the scaling technology, the total delay of the logic circuit depends on _____ Answer: d. All of the above
2. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance? Answer: b. Dynamic dissipation
3. In high noise margin (NMH), the difference in magnitude between the maximum HIGH output voltage of driving gate and the maximum HIGH voltage is recognized by the _____gate. Answer: a. Driven
4. Which factor/s play/s a crucial role in determining the speed of CMOS logic gate? Answer: d. All of the above
5. For complex gate design in CMOS, OR function needs to be implemented by _____ connection/s of MOS. Answer: b. Parallel
6. In pull-up network, PMOS transistors of CMOS are connected in parallel with the provision of conducting path between output node & Vdd yielding _____ output. Answer: a. 1
7. In CMOS inverter, the propagation delay of a gate is the/an _____ transition delay time for the signal during propagation from input to output especially when the signal changes its value. Answer: b. Average
8. In DIBL, which among the following is/are regarded as the source/s of leakage? Answer: d. All of the above

9. In enhancement MOSFET, the magnitude of output current _____ due to an increase in the magnitude of gate potentials. Answer: a. Increases
10. Which type of MOSFET exhibits no current at zero gate voltage? Answer: b. Enhancement MOSFET
11. What is the effect on the power supply voltage due to substantial reduction in the duration of propagation delay and noise margin of CMOS circuit? Answer: b) Power supply voltage decreases
12. How is the configuration strategy of p-type and n-type units in two-input CMOS NAND gate circuit? Answer: b) Two p-type units in parallel & two n-type units in series
13. What is the output level of two-input CMOS NOR gate circuit configuration when all inputs are at low logic level? Answer: a) high
14. TTL and CMOS stands for? Answer: c) Transistor Transistor Logic and Complementary Metal Oxide Semiconductor
15. The CMOS inverter can be used as an amplifier when Answer: c) Both PMOS and NMOS are in saturation
16. Which of the following characteristics does an active loaded MOS differential circuit possess? Answer: a) high CMRR
17. If the output of a CMOS inverter gets accidently shorted to ground Answer: c) The current drain for the supply will increase, which may damage the p-channel load MOSFET

SANFOUNDRY

1. The full form of CMOS is _____ Answer: c) Complementary metal oxide semiconductor
2. The full form of COS-MOS is _____ Answer: a) Complementary symmetry metal oxide semiconductor
3. CMOS is also sometimes referred to as _____ Answer: c) Complementary symmetry metal oxide semiconductor
4. CMOS technology is used in _____ Answer: d) Both microprocessor and digital logic
5. Two important characteristics of CMOS devices are _____ Answer: d) Both high noise immunity and low static power consumption

6. CMOS behaves as a/an _____ Answer: c) Inverter
7. An important characteristic of a CMOS circuit is the _____ Answer: b) Duality
8. CMOS logic dissipates _____ power than NMOS logic circuits. Answer: b) Less
9. Semiconductors are made of _____ Answer: a) Ge and Si
10. Which chip were the first RTC and CMOS RAM chip to be used in early IBM computers, capable of storing a total of 64 bytes? Answer: c) The Motorola 146818

UNIT V VLSI TESTING AND ANALYSIS

CARRERRIDE

1. Basically, an observability of an internal circuit node is a degree to which one can observe that node at the _____ of an integrated circuit. Answer: b. Outputs
2. High observability indicates that _____number of cycles are required to measure the output node value. Answer: c. Less
3. Due to the limitations of the testers, the functional test is usually performed at speed _____the target speed. Answer: a. Lower than
4. Which among the following is/are responsible for the occurrence of 'Delay Faults'? Answer: d. All of the above
5. Which among the following serves as an input stage to most of the op-amps due to its compatibility with IC technology? Answer: a. Differential amplifier
6. PSSR can be defined as the product of the ratio of change in supply voltage to change in output voltage of op-amp caused by the change in power supply & _____ of op-amp. Answer: a. Open-loop gain
7. According to the principle of current mirror, if gate-source potentials of two identical MOS transistors are equal, then the channel currents should be _____ Answer: a. Equal
8. In two-stage op-amp, what is the purpose of compensation circuitry? Answer: d. To achieve stable closed-loop performance
9. In accordance to the scaling technology, the total delay of the logic circuit depends on _____ Answer: d. All of the above
10. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance? Answer: b. Dynamic dissipation

11. The poor controllability circuits are: Answer: d) all of the mentioned
12. The circuits with poor observability are: Answer: d) All of the mentioned
13. Which among the following is/are responsible for the occurrence of 'Delay Faults'? Answer: d) All of the above

SANFOUNDRY

1. VLSI technology uses _____ to form integrated circuit. Answer: a) transistors
2. Medium scale integration has _____ Answer: c) hundred logic gates
3. The difficulty in achieving high doping concentration leads to _____ Answer: a) error in concentration
4. _____ is used to deal with effect of variation. Answer: a) chip level technique
5. As die size shrinks, the complexity of making the photomasks _____ Answer: a) increases
6. _____ architecture is used to design VLSI. Answer: c) system on a chip
7. What is the design flow of VLSI system? Answer: a) ii-i-iii-iv
8. _____ is used in logic design of VLSI. Answer: b) FIFO
9. Which provides higher integration density? Answer: c) transistor transistor logic
10. Physical and electrical specification is given in _____ Answer: c) system design
11. Which is the high level representation of VLSI design? Answer: a) problem statement
12. Gate minimization technique is used to simplify the logic. Answer: a) true
13. High resistance short present between drain and ground of n-MOSFET inverter acts as: Answer: b) Logical fault as output is stuck at 1
14. The fault simulation detects faults by: Answer: d) All of the mentioned
15. The ease with which the controller establishes specific signal value at each node by setting input values is known as: Answer: c) Controlability
16. The ease with which the controller determines signal value at any node by setting input values is known as: Answer: b) Observability

TEXTBOOK

1. The p-type epitaxial layer grown over an n-type substrate for fabricating a bipolar transistor will function as Answer: 2. The base of an n-p-n transistor
2. An MSI chip contains Answer: 3. lesser than 1000 and greater than 100
3. The p-type epitaxial layer grown over an n-type substrate for fabricating a bipolar transistor will function as Answer: 2. The base of an n-p-n transistor
4. In the fabrication process SiO2 act as a/an Answer: 4. All of these
5. The purpose of Design for Test (DFT) process in ASIC design flow is Answer: 2. To capture manufacturing defects
6. The dopants are introduced in the active areas of silicon by using which process? Answer: d) Either diffusion or Implantation process
7. In nMOS fabrication, etching is done using_____ Answer: a) plasma
8. Design for testability is considered in production for chips because: Answer: c) Many chips are required to be tested within short interval of time which yields timely delivery for the customers
9. The functions performed during chip testing are: Answer: d) All of the mentioned
10. Delay fault is considered as: Answer: b) Logical fault