Chittagong University of Engineering and Technology

Department of Electrical and Electrical Engineering

EEE 490: VLSI Technology Sessional

Report on

16 Bit Bit Counter

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ABSTRACT

This experiment introduces **Cadence Virtuoso Software** which provides an environment to simulate our Verilog codes and test whether it works as it has to. Using this we designed the schematic of a 16 bit Bit counter and layout by using 2 input NAND gate.

KEYWORDS

2 input NAND Gate, D-flip flop, 16-bit counter

INTRODUCTION

This experiment introduces to use Cadence Virtuoso Software to design a 16 bit Bit Counter. It helps us to create a library to create schematic and layout of 16 bit Bit counter and clear all design rule errors and layout to schematic verification. A counter comprises a number of flip-flops, whose outputs are interpreted as a number. The counter circuit has to be able to increment or decrement the number. These circuits can be designed using D flip-flops. We used negative edge triggered Master/slave D-type flip-flip D flip flop to implement a 16 bit down counter.

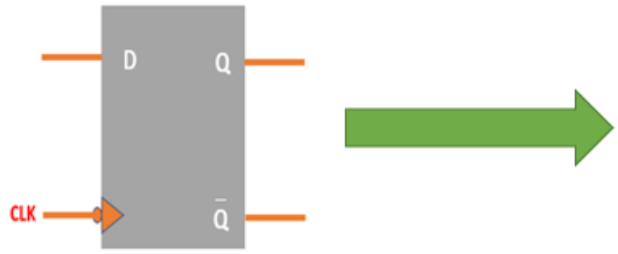

FIG.1. Graphical symbol

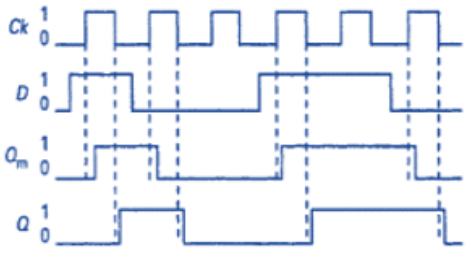

FIG.2. Timing diagram

For designing negative edge Master/slave D-type flip-flop, we need 11 Nand gate which produces an output which is false only if all its inputs are true.

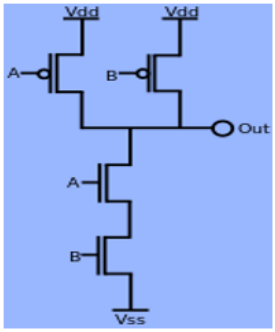

FIG.3. A CMOS two-input NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

FIG.4. Truth table of NAND gate

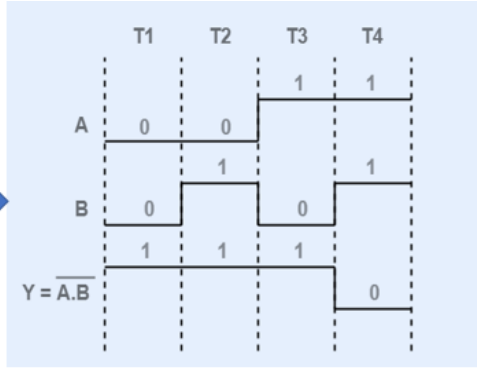

FIG.5. Timing diagram of NAND gate

For designing 16 bit bit counter 17 negative edge triggered D flipflop is used and the connection must be like the figure below.

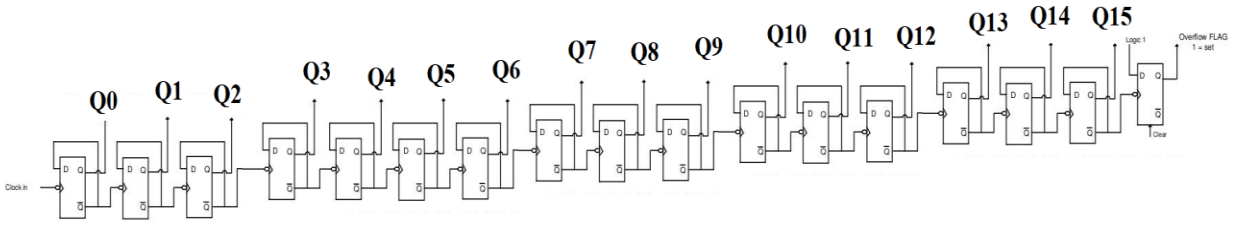

Fig.6. 16 bit bit counter

OBJECTIVES:

The objective of this experiment are

1. To design a a 16 bit Bit Counter (Schematic and Layout) using CMOS Technology and create symbol.

2. To observes DRC and LVS simulation and verify it with schematics diagram.

REQUIRED EQUIPMENT:

1. Laptop

2. MS Word 2019

3. CADENCE Workstation Software.

4. Snipping Tools.

SCHEMATIC DIAGRAM

Nand Gate

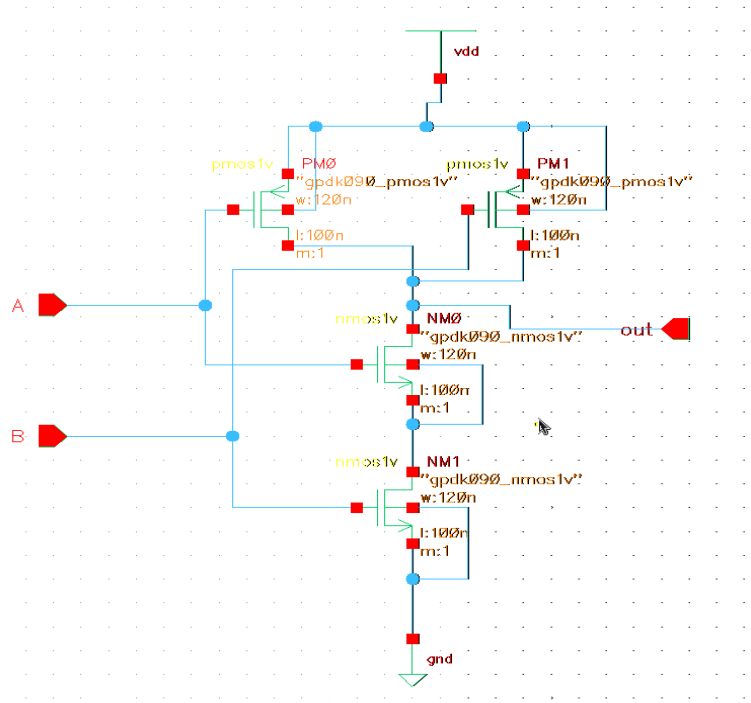

FIG.8. Schematic Diagram of Nand gate

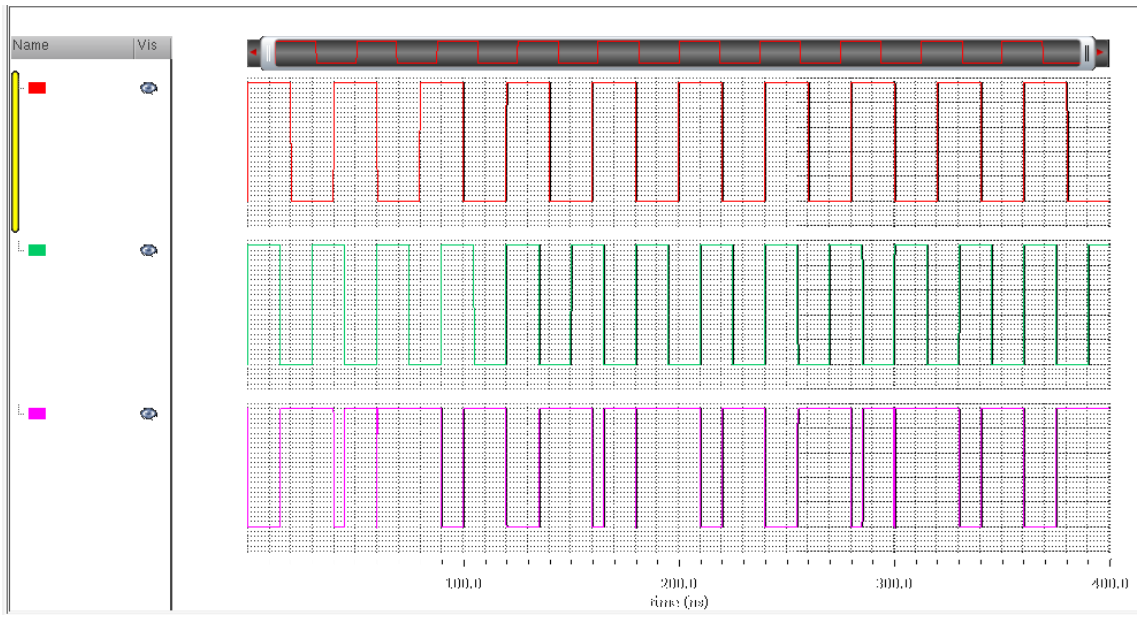

FIG.9. Timing diagram of Nand gate

D-flipflop

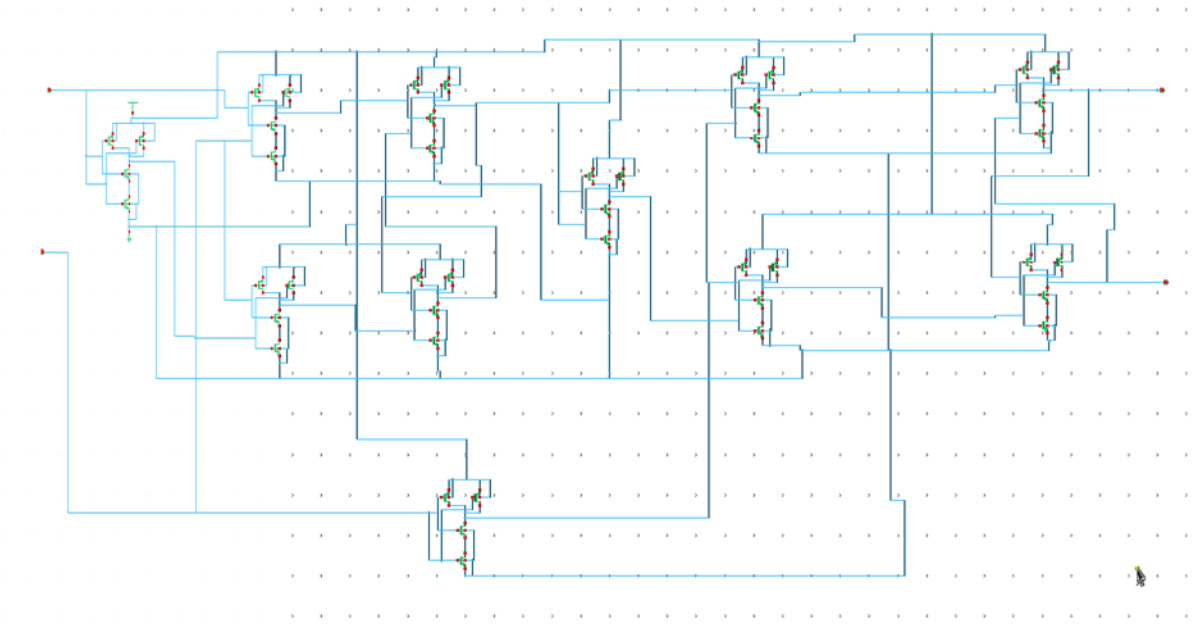

FIG.10. Schematic Diagram of D-flipflop gate

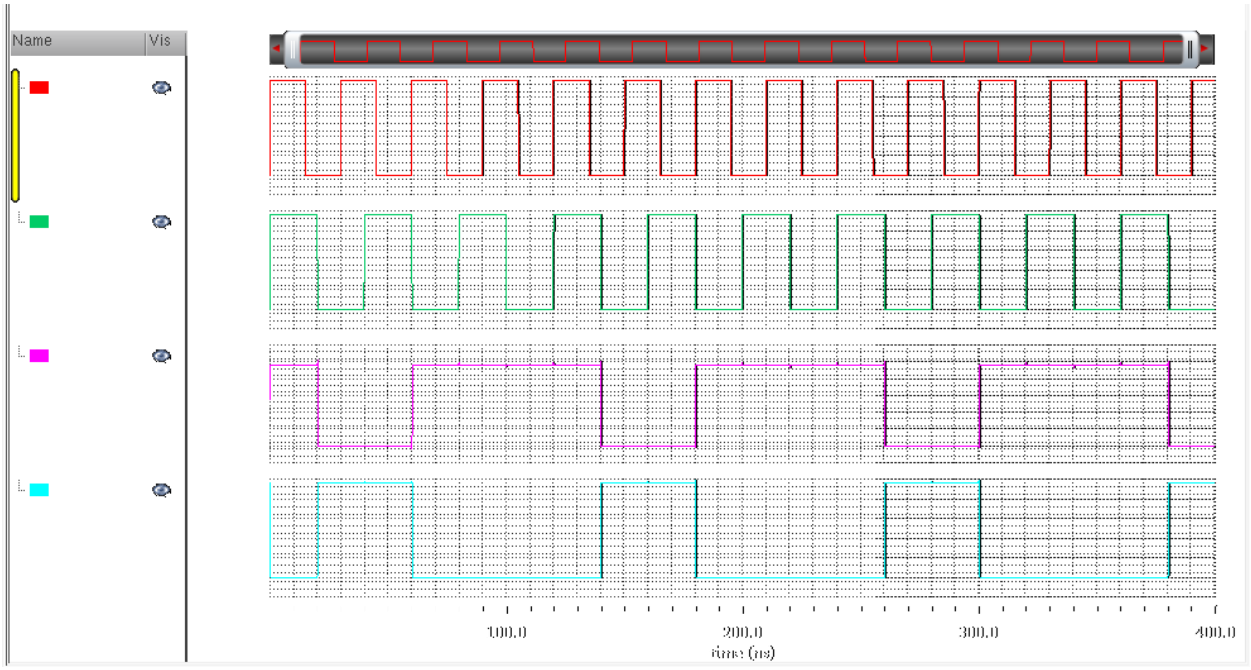

FIG.11. Timing Diagram of D-flipflop gate

16 bit bit counter

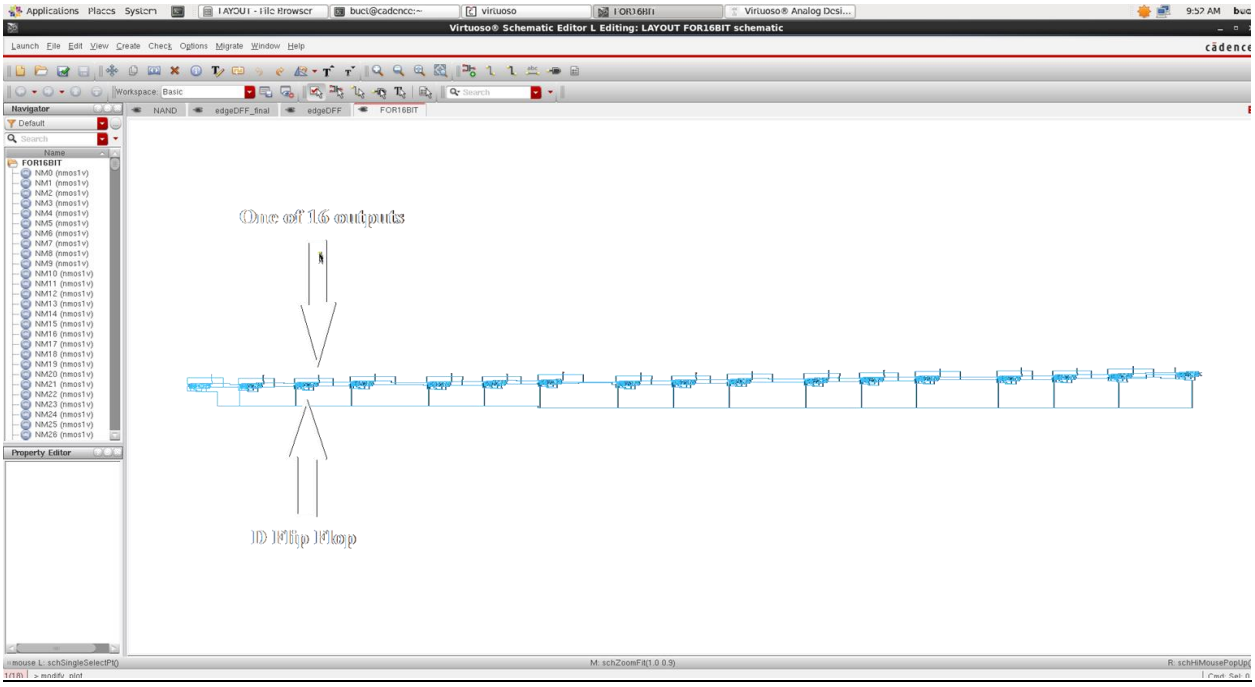

FIG.12. Schematic Diagram of 16 bit bit counter.

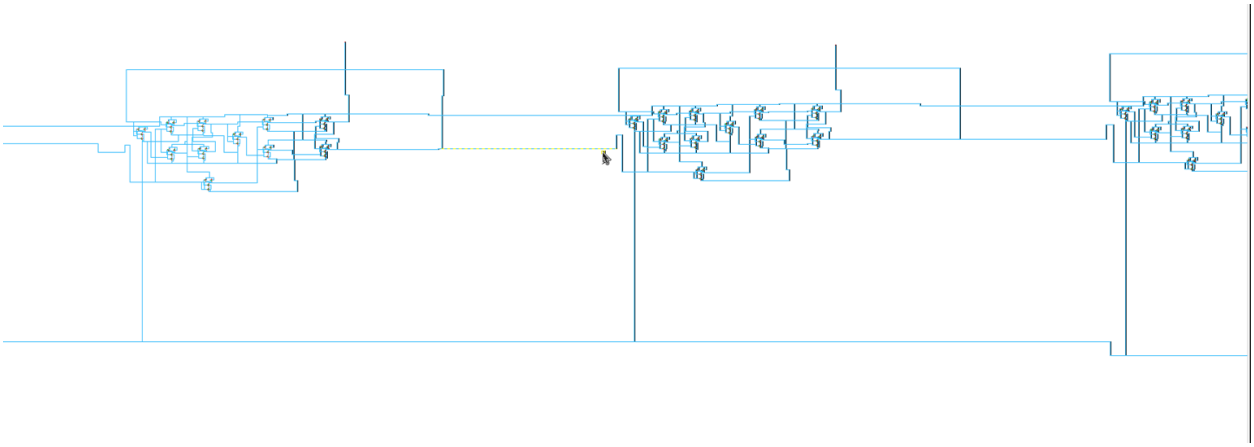

FIG.13. Schematic Diagram of 16 bit bit counter zoom in.

FIG.14. Timing Diagram of 16 bit bit counter.

Symbol of 16 bit bit counter

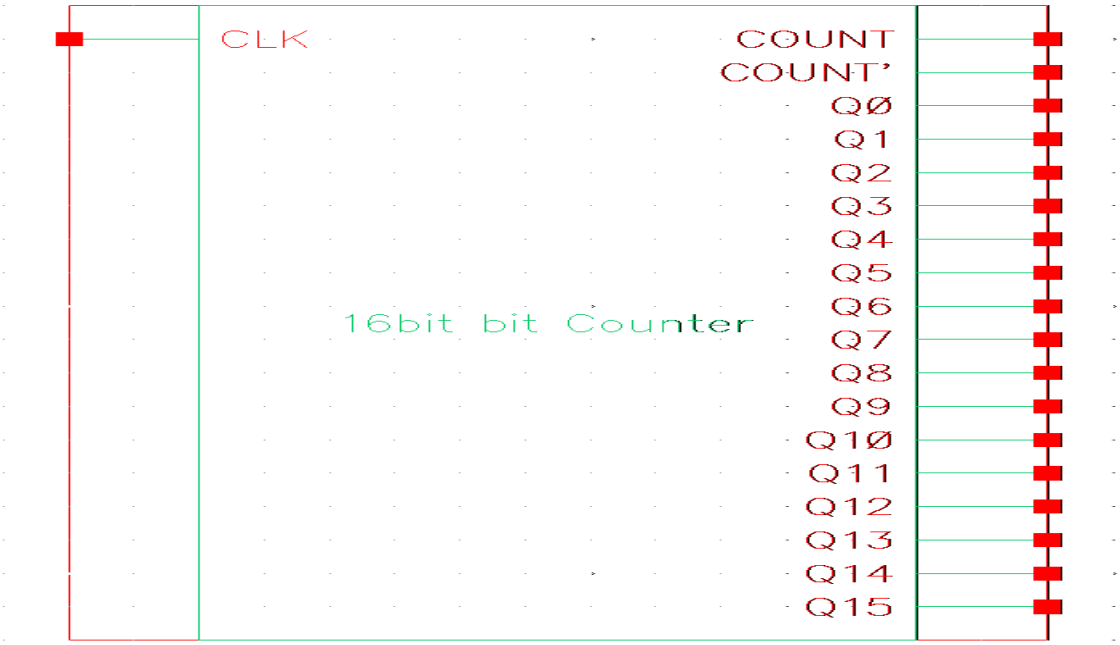

FIG.15. Symbol of 16 bit bit counter.

Layout design of NAND gate

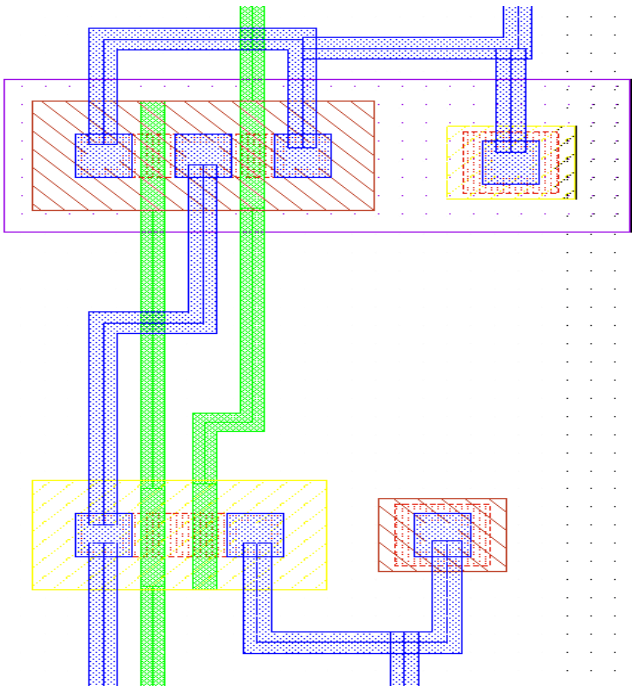

FIG.16. Layout design of NAND gate

Layout design of D-flipflop

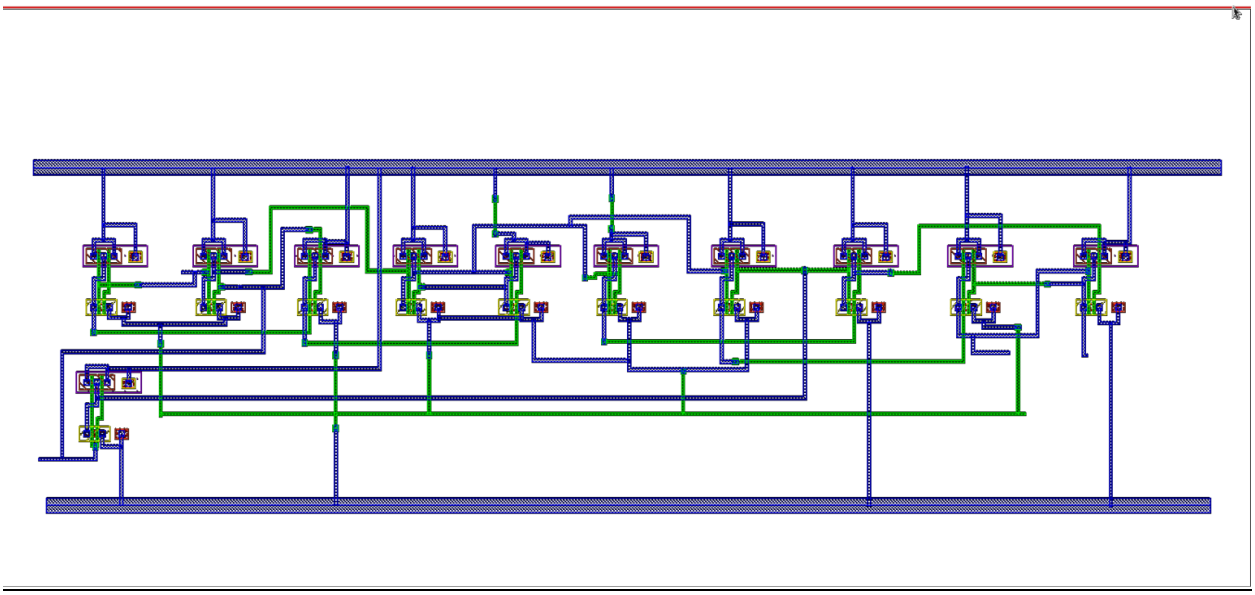

FIG.17. Layout design of D-flipflop

Layout design of 16 bit bit counter

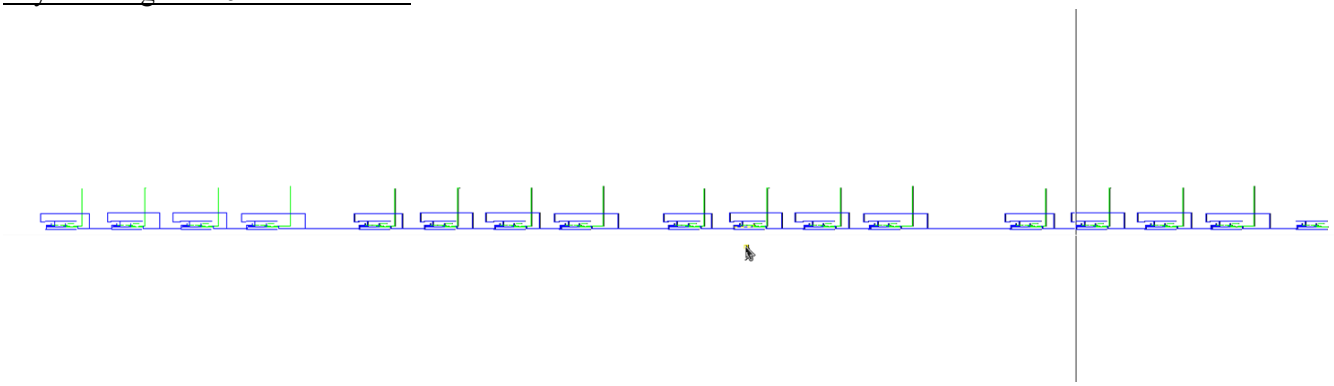

FIG.18. Layout design of 16 bit bit counter

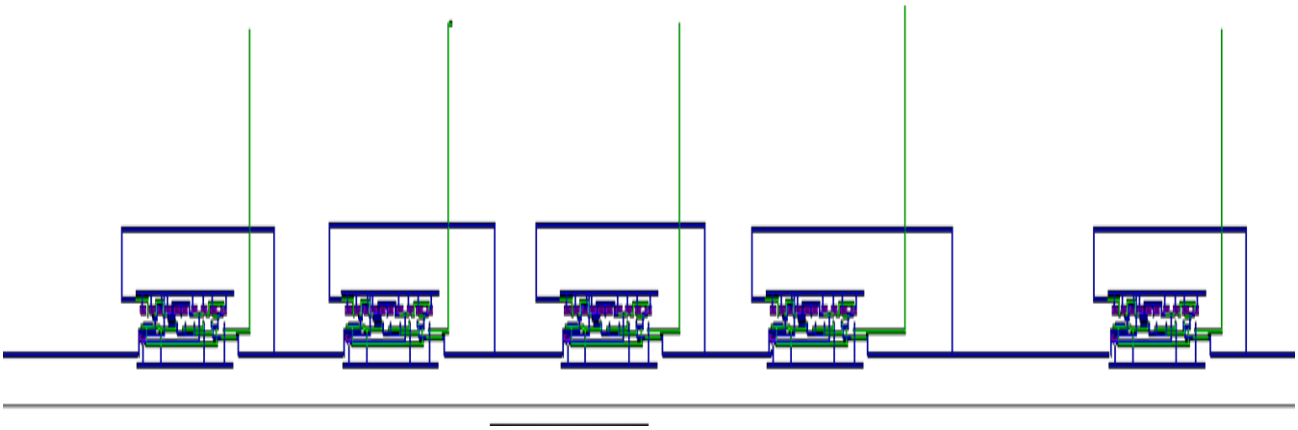

FIG.19. Layout design of 16 bit bit counter with zoom in

DRC simulation

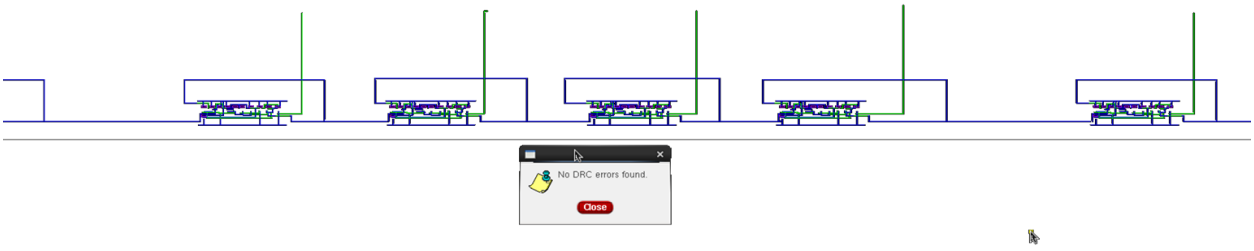

FIG.20. Layout design of 16 bit bit counter with no DRC error

LVS simulation

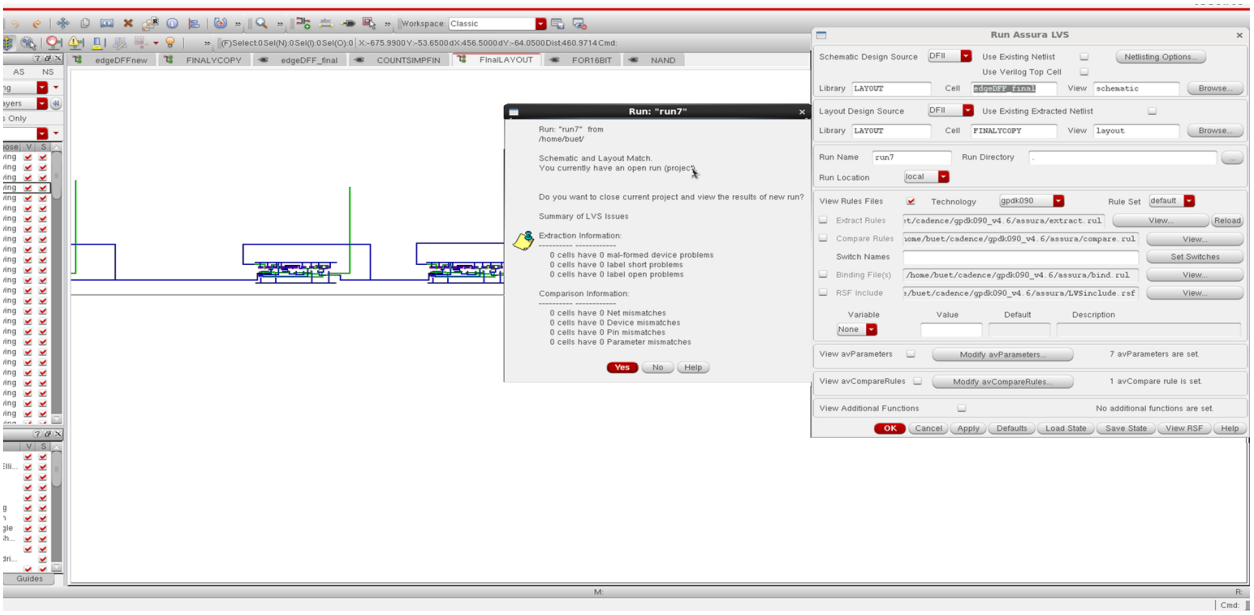

FIG.21. LVS simulation with mismatch

Conclusion:

The objective of the experiment was to design 16 bit bit count and then create it's symbol. We have checked the DRC and LVS from ASSURA. We were required to uphold the stated standard. Nevertheless, by adhering to the parameters, we were able to create the appropriate circuit. Before the LVS tab indicated no mismatch between the schematic and the layout, there was initially some DRC issue, which we were able to correct effectively.