Product SPEC

of

WM-SG-SM-42 LoRa Module

Introduction

The WM-SG-SM-42 LoRa module which refers as "module" is a small size module and consists of a SEMTECH SX1272, an authorization chip and a U.FL connect. The WM-SG-SM-42 provides for the highest-level integration for electronic accessories, featuring integrated Lora.

The small size & low profile physical design makes it easier for system design to enable high performance LoRa connectivity without space constrain. This multi-functionality and board-to-board physical interface provides UART interface options.

For the software and driver development, USI provides extensive technical document and reference software code for the system integration under the agreement of SEMTECH and ST.

Hardware evaluation kit and development utilities will be released base on listed OS and processors to OEM customers.

Features

Semtech SX1272

- Provides LoRa communication
- High sensitivity: down to -137 dBm
- Low power operation supporting

ST STM32L052 Microprocessor

- ARM 32-bit Cortex-M0+ CPU
- CPU frequency up to 32MHz
- Embedded 8K SDRAM and 64K Flash
- 20 General Purpose IOs multiplexed with other interfaces
- Hardware division and fast multiplier
- Little-endian memory space

WM-SG-SM-42 LoRa Module

- Featuring integrated LoRa modem
- Low power consumption & excellent power management performance extend battery life.
- Small size suitable for low volume system integration.
- Easy for integration into mobile and handheld device with flexible system configuration.
- Lead Free design which supporting Green design requirement, RoHS Compliance.
- FCC/CE/LoRaWAN certified

Device Package

12.0x13.0x2.0 mm

Change Sheet					
Rev.	Date	Description of change			Approval & Date
		Page	Par	Change(s)	
0.1	12/08/16			Initial release	Kimi
0.2	12/09/16			Update specification	Chintang
0.3	3/1/17			Update specification	Chintang

TABLE OF CONTENTS

1 EXECUTIVE SUMMARY

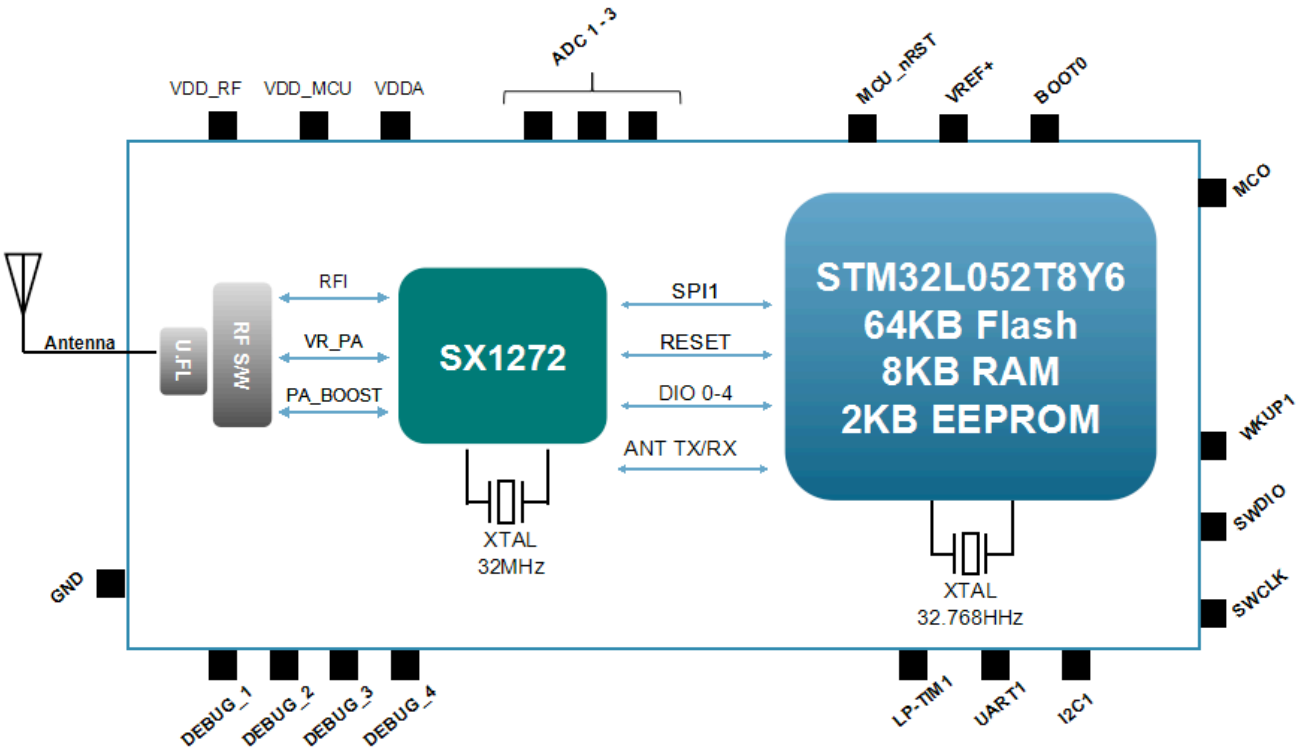
The WM-SG-SM-42 module - is one of the product families in UG's product offering, targeting for system integration requiring a smaller form factor. It also provides the standard migration to high data rate to UG's current customers.

The purpose of this document is to define the product specification for LoRa RF module WM-SG-SM-42. All the data in this document is based on SX1272 and STM32L052 datasheet and other documents provided from Semtech and STM. The data will be updated after implementing the measurement of the module.

2 BLOCK DIAGRAM

The WM-SG-SM-42 module is designed based on SX1272 and STM32L052 solution. It supports generic UART interface to connect the RF to the host processor. A simplified block diagram of the WM-SG-SM-42 module is depicted in the Fig. below.

WM-SG-SM-42 Block Diagram



3 DELIVERABLES

The following products and software will be part of the product.

- WM-SG-SM-42 Module with packaging
- Evaluation kits (with UART interface)
- Software utility which supporting customer for integration, performance test and homologation. Capable of testing, loading (firmware) and configuring (MAC, CIS) for the WM-SG-SM-42 module.
- Unit Test / Qualification report
- Product Specifications.
- Agency certification test report base on adapter boards

4 REFERENCE DOCUMENTS

C.I.S.P.R. Pub. 22	"Limits and methods of measurement of radio interference characteristics of information technology equipment." International Special Committee on Radio Interference (C.I.S.P.R.), Third Edition, 1997.
CB Bulletin No. 96A	"Adherence to IEC Standards: “Requirements for IEC 950, 2nd Edition and Amendments 1 (1991), 2(1993), 3 (1995) and 4(1996). Product Categories: Meas, Med, Off, Tron." IEC System for Conformity Testing to Standards for Safety of Electrical Equipment (IECEE), April 2000.
CFR 47, Part 15-B	"Unintentional Radiators". Title 47 of the Code of Federal Regulations, Part 15, FCC Rules, Radio Frequency Devices, Subpart B.
CFR 47, Part 15-C	"Intentional Radiators". Title 47 of the Code of Federal Regulations, Part 15, FCC Rules, Subpart C. URL: http://www.access.gpo.gov/nara/cfr/waisidx_98/47cfr15_98.html
CSA C22.2 No. 950-95	"Safety of Information Technology Equipment including Electrical Business Equipment, Third Edition." Canadian Standards Association, 1995, including revised pages through July 1997.
EN 60 950	"Safety of Information Technology Equipment Including Electrical Business Equipment." European Committee for Electrotechnical Standardization (CENELEC), 1996, (IEC 950, Second Edition, including Amendment 1, 2, 3 and 4).
IEC 950	"Safety of Information Technology Equipment Including Electrical Business Equipment." European Committee for Electrotechnical Standardization, Intentional Electrotechnical Commission. 1991, Second Edition, including Amendments 1, 2, 3, and 4.
IEEE 802.11	“Wireless LAN Medium Access Control (MAC) And Physical Layer (PHY) Specifications.” Institute of Electrical and Electronics Engineers. 1999.

5 TECHNICAL SPECIFICATION

5.1 ABSOLUTE MAXIMUM RATING

Supply Power	Max +3.6 Volt	
Non Operating Temperature	- 40° to 105° Celsius	
Voltage ripple	+/- 2%	Max. Values not exceeding Operating voltage

5.2 RECOMMENDABLE OPERATION CONDITION

5.2.1 TEMPERATURE, HUMIDITY

The WM-SG-SM-42 module has to withstand the operational requirements as listed in the table below.

Operating Temperature	-40° to 85° Celsius	
Humidity range	Max 85%	Non condensing, relative humidity

The maximum operating ambient temperature range can up to 85degC, but exposure to absolute-maximum-rated conditions may cause performance degradation and affect device reliability.

5.2.2 VOLTAGE

Power supply for the WM-SG-SM-42 module will be provided by the host via the power pins

Symbol	Parameter	Min	Typ	Max	Unit
VDD_3V3	Power supply for MCU	2.0	3.3	3.6	V
VDDA	Power supply for MCU	2.0	3.3	3.6	V
VREF+	Power supply for MCU	2.0	3.3	3.6	V
VDD_RFS	Power supply for RFS	2.0	3.3	3.6	V

5.2.3 CURRENT CONSUMPTION

The WM-SG-SM-42 on TX mode output current consumption:
(Typical spec is defined **@3.3V 25°C BW125kHz**)

Table 5-1 Current consumption

Mode	**TYP.**	**Max.**
Standby mode	7mA	10mA
RX	17mA	25mA

Table 5-2 Output power of TX Power Setting

TX Power Setting	**Output Power (dBm)**		**TYP. Current (mA)**		**Max. (mA)**
	868MHz	**915MHz**	**868MHz**	**915MHz**	**1GHz**
5	5.7	5.6	47	48	58
6	6.7	6.6	49	51	61
7	7.8	7.8	51	53	64
8	8.8	8.8	53	56	66
9	10.0	9.8	56	59	71
10	11.0	10.9	60	63	74
11	11.9	11.8	64	66	77
12	12.9	12.8	68	71	83
13	13.9	13.9	73	76	88
14	14.8	14.8	79	82	94
15	15.7	15.7	86	89	101
16	16.5	16.4	95	97	109
17	17.2	17.2	104	106	118
18	17.9	17.8	112	115	125
19	18.5	18.5	120	123	133
20	19.0	18.8	126	127	140

5.3 RF SPECIFICATIONS

The WM-SG-SM-42 module complies with the following features and standards;
(Typical spec is defined **@3.3V 25°C**)

Features	**Description**
RF Standards	LoRa® Technology modulation
Frequency Band	863.000 MHz to 870.000 MHz 902.000 MHz to 928.000 MHz
Bandwidth	125KHz, 250KHz, 500KHz
Frequency Tolerance	-25ppm to +25ppm
RF TX Power	Adjustable up to max. +18.5 dBm*

* When Module in the high, low voltage and high, low temperature, TX power will be up to 16dBm

Sensitivity Characteristics	**TYP.**	**MAX.**	**Unit**
1% PER, Rx Sensitivity @ SF=7,BW=125KHz	-124**	-119	dBm
1% PER, Rx Sensitivity @ SF=12,BW=125KHz	-137**	-132	dBm
1% PER, Rx Sensitivity @ SF=7,BW=250KHz	-122**	-117	dBm
1% PER, Rx Sensitivity @ SF=12,BW=250KHz	-135**	-130	dBm
1% PER, Rx Sensitivity @ SF=7,BW=500KHz	-116**	-111	dBm
1% PER, Rx Sensitivity @ SF=12,BW=500KHz	-129**	-124	dBm

**Follow Semtech spec

6 CPU AND FLASH MEMORY

6.1 ARM CORTEX-M0+ CPU CORE

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:
.

- A simple architecture that is easy to learn and program
- Ultra-low power, energy-efficient operation
- Excellent code density ·
- Deterministic, high-performance interrupt handling ·
- Upward compatibility with Cortex-M processor family ·
- Platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L052x6/8 are compatible with all ARM tools and software.

6.2 MEMORIES

The STM32L052x6/8 devices have the following features: ·

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses). ·
- The non-volatile memory is divided into three arrays:
  – 32 or 64 Kbytes of embedded Flash program memory
  – 2 Kbytes of data EEPROM
  – Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

· **Level 0**: no protection ·

· **Level 1**: memory readout protected. The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected ·

· **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The firewall protects parts of code/data from access by the rest of the code that is executed outside of the protected area. The granularity of the protected code segment or the non-volatile data segment is 256 bytes (Flash memory or EEPROM) against 64 bytes for the volatile data segment (RAM).

The whole non-volatile memory embeds the error correction code (ECC) feature.

7 I/O PORT CHARACTERISTICS

Unless otherwise specified, the parameters given as below *Table*.

For detail information of I/O injection parameters and conditions, please refer to STM32L052x6/8 I/0 manual.

Table7-1 I/O Static Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Unit
V_{IL}	Input low Voltage		-	0.3 V_{DD}	V
V_{IH}	Input High Voltage		0.7 V_{DD}	-	V
R_{PU}	Input Pull-Up Resistance	V_{IN} - V_{SS}	30	60	KΩ
R_{PD}	Input Pull-Down Resistance	V_{IN} - V_{DD}	30	60	KΩ
V_{OL}	Output Low Voltage	CMOS port I_{IO} = +8 mA 2.7V≤V_{DD} ≤ 3.6V	-	0.4	V
V_{OH}	Output High Voltage		V_{DD}-0.4	-	V
V_{OL}	Output Low Voltage	TTL port, I_{IO} =+ 8 mA 2.7V≤V_{DD} ≤ 3.6V	-	0.4	V
V_{OH}	Output High Voltage	TTL port I_{IO} = -6 mA 2.7V≤V_{DD} ≤ 3.6V	2.4	-	V
V_{OL}	Output Low Voltage	I_{IO} = +15 mA 2.7V≤V_{DD} ≤ 3.6V	-	1.3	V
V_{OH}	Output High Voltage	I_{IO} = -15 mA 2.7V≤V_{DD} ≤ 3.6V	V_{DD}-1.3	-	V
V_{OL}	Output Low Voltage	I_{IO} = +4 mA 1.65V≤V_{DD} ≤ 3.6V	-	0.45	V
V_{OH}	Output High Voltage	I_{IO} = +4 mA 1.65V≤V_{DD} ≤ 3.6V	V_{DD}-0.45	-	V

8 INTERFACE

Several peripheral are multiplexed GPIOs.

8.1 LPUART interface

The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication. The LPUART has a clock domain independent from the CPU clock. It can wake up the system from Stop mode using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be: ·

- Start bit detection ·
- Or any received data frame ·
- Or a specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.
LPUART interface can be served by the DMA controller.

8.2 I2C Interface

WM-SG-SM-42 Module I2C interface can operate in multi-master or slave modes. .
I2C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

Table 8-1 STM32L052x6/8 I2C implementation

I2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X(2)
Independent clock	X	-
SMBus	X	-
Wakeup from STOP	X	-

1. X = supported.
2. See for the list of I/Os that feature Fast Mode Plus capability

8.3 ADC Interface

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L052x6/8 device. It has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference). Three channels, PA0, PA4 and PA5, are fast channels, while the others are standard channels.
The ADC performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.
The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed.
The ADC consumption is low at all frequencies (~25 µA at 10 kSPS, ~200 µA at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.
The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.
The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).
An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.
The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

8.4 GPIO Interface

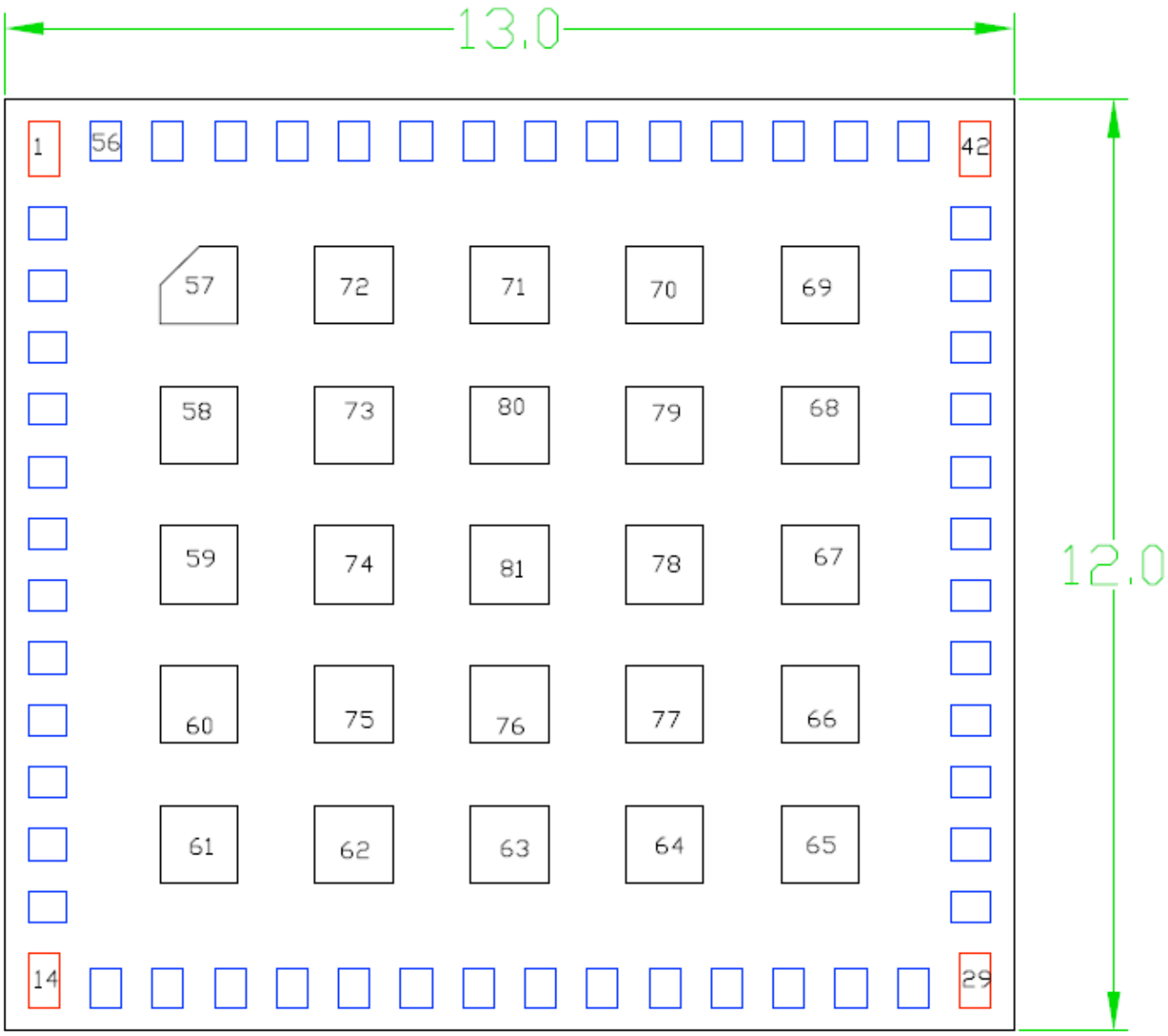
Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

9 DIMENSIONS, WEIGHT AND MOUNTING

The following paragraphs provide the requirements for the size, weight and mounting of the WM-SG-SM-42 module.

9.1 Dimensions

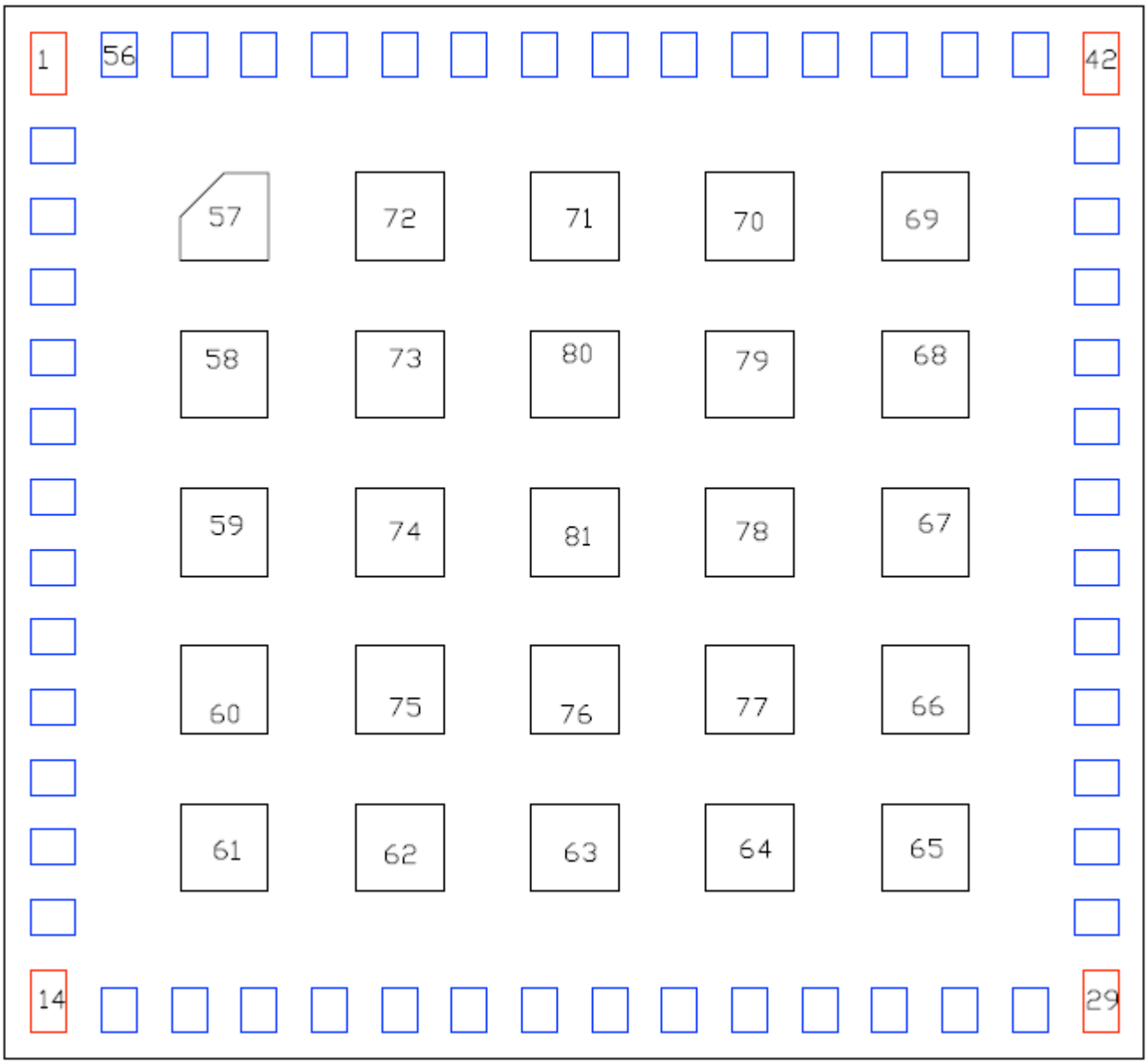
The size and thickness of the WM-SG-SM-42 module is “12mm (W) x 13 mm (L) x 2.0 mm (H) +/- 0.1mm “ (Including metal shielding)



TOP View

9.2 Pin Out and Pin Description

PIN OUT



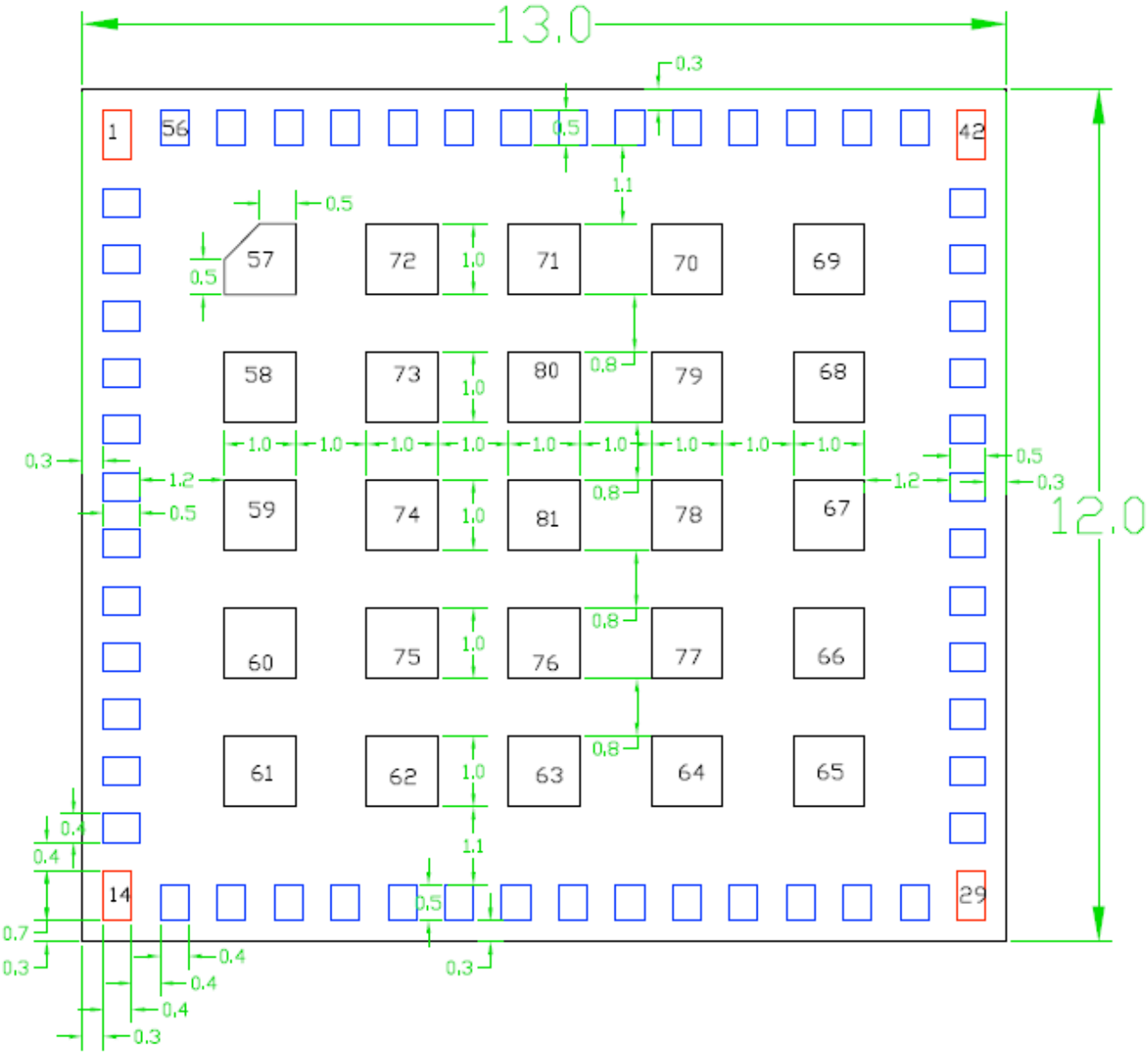
Top View

Pin Description

Pin-Number	Pin-Define	Type	Description
1	GND	--	Ground
2	PA8/RCC_MCO	--	GPIO connect MCU PA8
3	PB10/LPUART_TX	--	LPUART_TX
4	PB2/LPTIM1_OUT		GPIO connect MCU PB2
5	PA7/ADC_IN7		GPIO connect MCU PA7
6	PA1/COMP1_INP	--	GPIO connect MCU PA1
7	VREF+		VREF+ power supply
8	GND		Ground
9	VDDA	--	VDDA power supply
10	PB5/LPTIM1_IN1		GPIO connect MCU PB5
11	PA0/SYS_WKUP1		GPIO connect MCU PA0
12	GND		Ground
13	GND		Ground
14	GND		Ground
15	GND		Ground
16	GND		Ground
17	GND		Ground
18	GND	--	Ground
19	GND		Ground
20	MICRO_RST_N	--	External system reset active low
21	PA9/RF_RST	--	Module internal use
22	PA2/DIO0	--	Module internal use
23	PA3/DIO1	--	Module internal use
24	PA5/DIO2		Module internal use
25	PA6/DIO3		Module internal use
26	PA1/DIO4		Module internal use
27	DIO5		Module internal use
28	BOOT0	--	BOOT Pin
29	GND		Ground
30	VDD_RFS	--	VDD_RFS power supply

31	VDD_RFS		VDD_RFS power supply
32	GND		Ground
33	VDD_3V3		VDD_3V3 power supply
34	VDD_3V3		VDD_3V3 power supply
35	GND		Ground
36	PB3/SPI1_SCK		Module internal use
37	PB4/SPI1_MISO		Module internal use
38	PA12/SPI1_MOSI		Module internal use
39	PA15/SPI1_NSS		Module internal use
40	GND		Ground
41	GND		Ground
42	GND		Ground
43	PB8/RF_SW_CTRL2		Module internal use
44	PA4/RF_SW_CTRL1		Module internal use
45	GND	--	Ground
46	GND		Ground
47	RF_OUT		RF_OUT Test pin
48	GND		Ground
49	PB7/I2C1_SDA	--	GPIO connect MCU PB7
50	PB6/I2C1_SCL		GPIO connect MCU PB6
51	PA13/SWDIO		SWDIO
52	PA14/SWCLK		SWCLK
53	PB1/ADC_IN9		GPIO connect MCU PB1
54	PA11/COMP1_OUT		GPIO connect MCU PA11
55	PB11/LPUART_RX		LPUART_RX
56	PB0/ADC_IN8		GPIO connect MCU PB0
57~81	GND		Ground

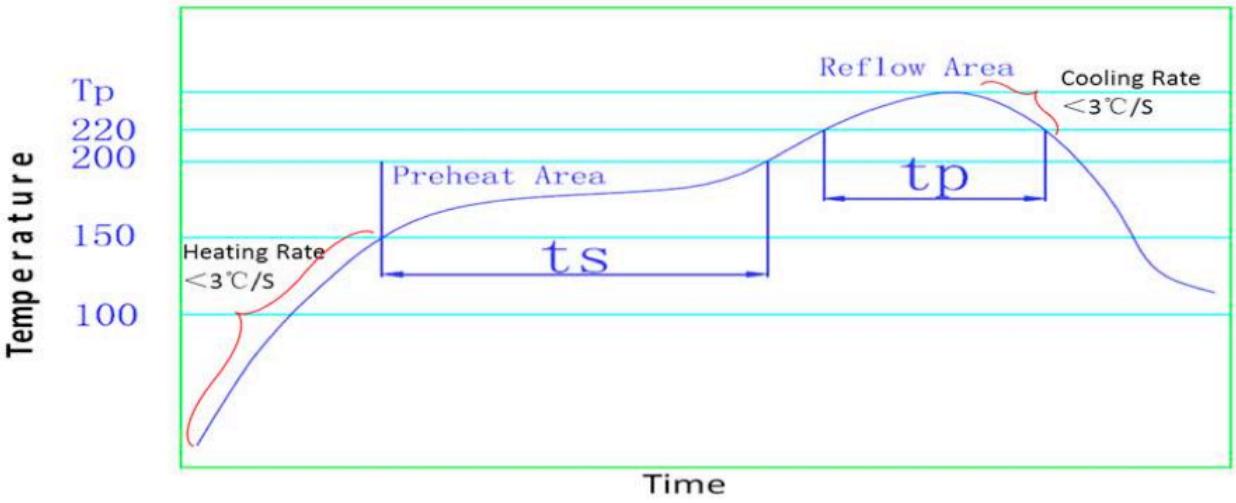
9.3 Recommend Footprint



Unit: mm +/- 0.1mm

Top View

10 RECOMMEND REFLOW PROFILE



Recommended Reflow Profile

1 Solder paste alloy: SAC305(Sn96.5/Ag3.0/Cu0.5).
2 Pre-heat Temp: 150~200℃; Soak time(ts): 60~120sec.
3 Peak temp(Tp) ≤ 260℃.
4 Time above 220℃ (tp): 40~90sec.
5 Optimal cooling rate < 3℃/sec, from peak to 220℃.
6 The oxygen concentration < 2000 ppm.

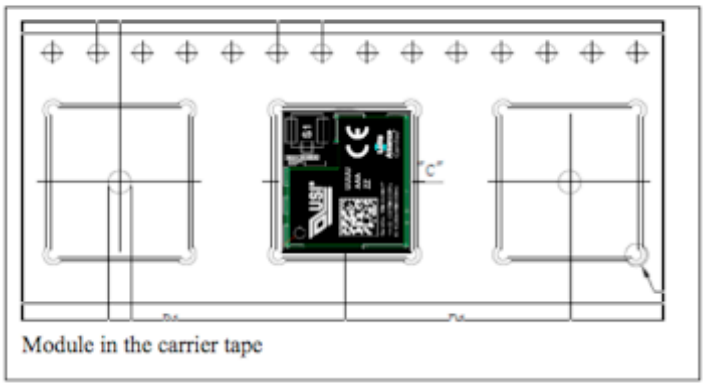
11 PACKAGE AND STORAGE CONDITION

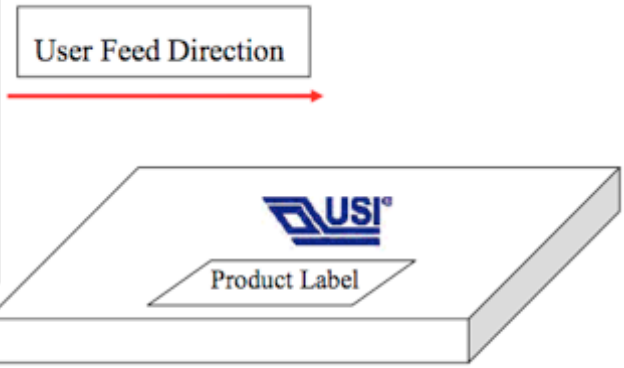
11.1 PACKAGE AND MARKING SPECIFICATION

WM-SG-SM-42	PACKAGING SPECIFICATION	

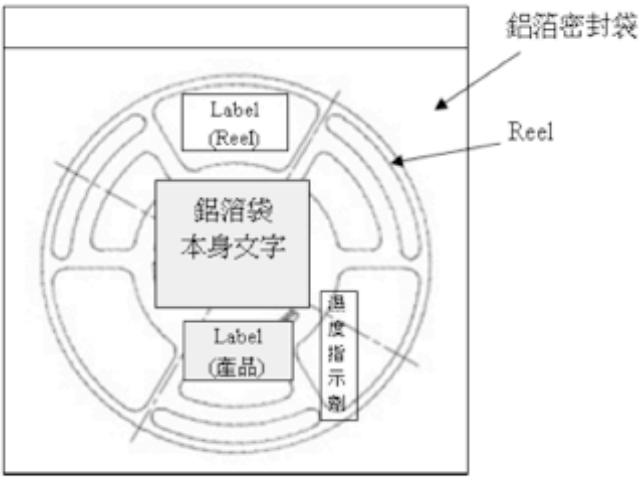
Package method:

1. Tape and Reel





Package Quantity:
Per REEL: 1200PCS;
Per Carton: 3600PCS。



PART NAME: (PDM Description)
MODULE NAME: BWM-BAN-BM-16
USI P/N: **8501-601080-01**
DATE CODE: YYWW
QTY: XXXX
REEL ID: [SFIS CONTROL]
COUNTRY OF ORIGIN: CHINA

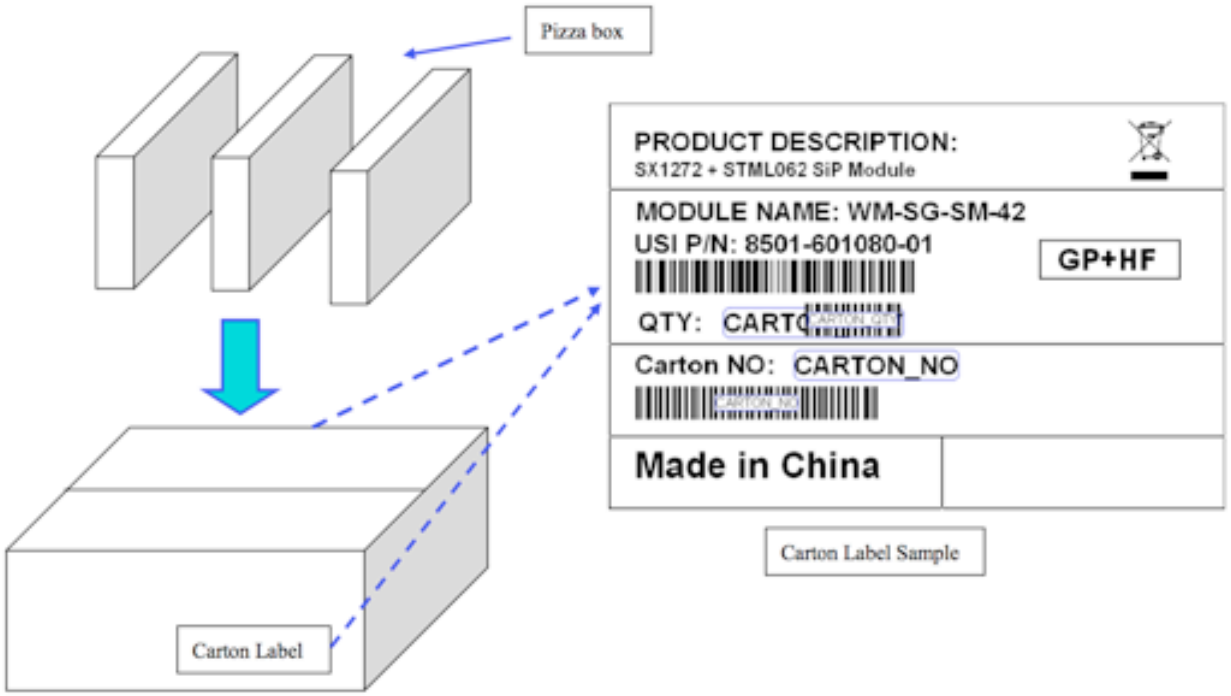
Product Label

TITLE	Packaging Laser Spec for WM-SG-SM-42	DOC NO.			
		SHEET	1/3	REV.	31

WM-SG-SM-42	PACKAGING SPECIFICATION	

3. MSL Label

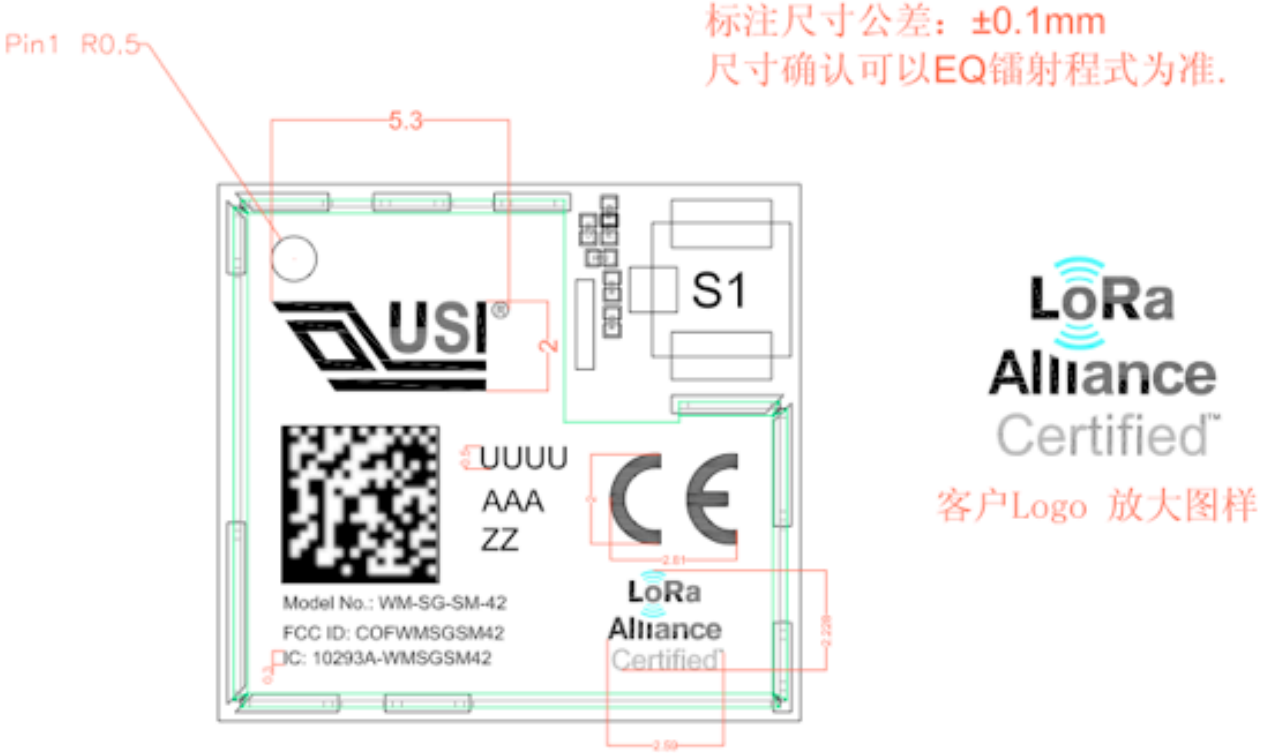
4. Carton package



TITLE	Packaging Laser Spec for WM-SG-SM-42	DOC NO.			
		SHEET	2/3	REV.	31

WM-SG-SM-42	PACKAGING SPECIFICATION	

4. Marking specification:



8501-601080-01/02

条码内容: UUUUXXXAAAZZYYMMDDNNNNNSSS

UUUUXXXAAAZZ为USI机种名去掉中间横线

YYMMDD为年月日代码,NNNNN为Panel序列号五位十进制

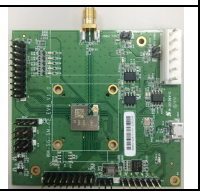
SSS为板子在Panel顺序，三位十进制.

二维码类型：Datamatrix，最小3.5X3.5mm，正方形，ECC200

字体维持正常比例.所有内容距离铁壳边缘不低于0.5mm.

TITLE	Packaging Laser Spec for WM-SG-SM-42	DOC NO.			
		SHEET	3/3	REV.	31

11.2 ORDERING INFORMATION

USI Project Code	USI P/N	Description	Remark
WM-SG-SM-42	8501-601080-01	SM-42 w RF output by u.FL connector/AT CMD	
	8501-601080-02	SM-42 w RF output by LGA Pad/AT CMD	TBA
Evaluation Board	8885-019387-01	Evaluation board w SM-22 LGA sku/AT CMD	

12 ESD LEVEL

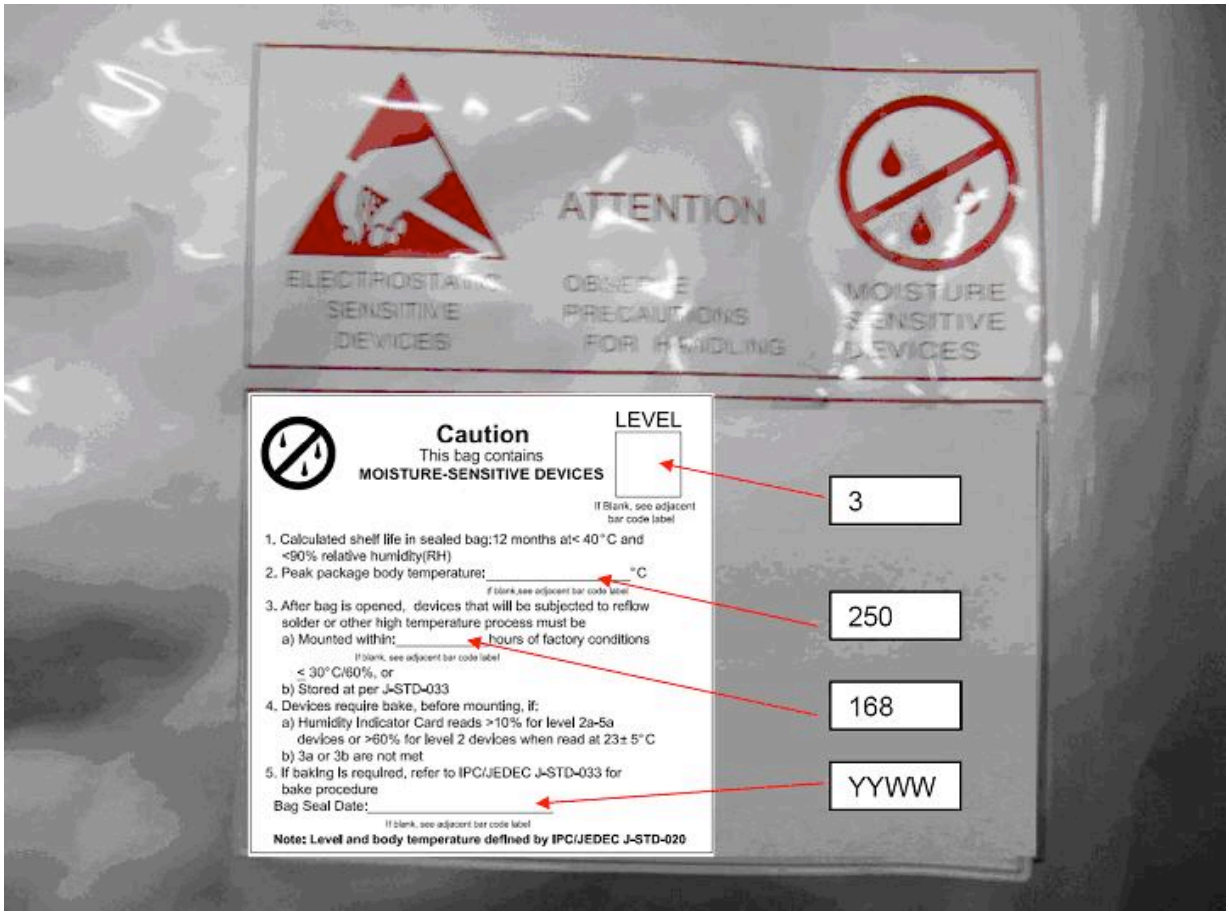
Note:
1. Surface Resistivity:
   Interior:10^{9}~10^{11}Ω/SQUARE
   EXTERIOR:10^{8}~10^{12}Ω/SQUARE
2. Dimension:475*420mm
3. Tolerance:+5,0mm
4. Color:
   Background : Gray
   Text : Red

Length leader / trailer tape:
Leader tape: ≥550mm which includes ≥100mm of carrier tape with empty compartments and covered with tape; remaining part might be of cover tape only.
Trailer tape: ≥160mm with empty compartments and covered with tape.

NOTES:

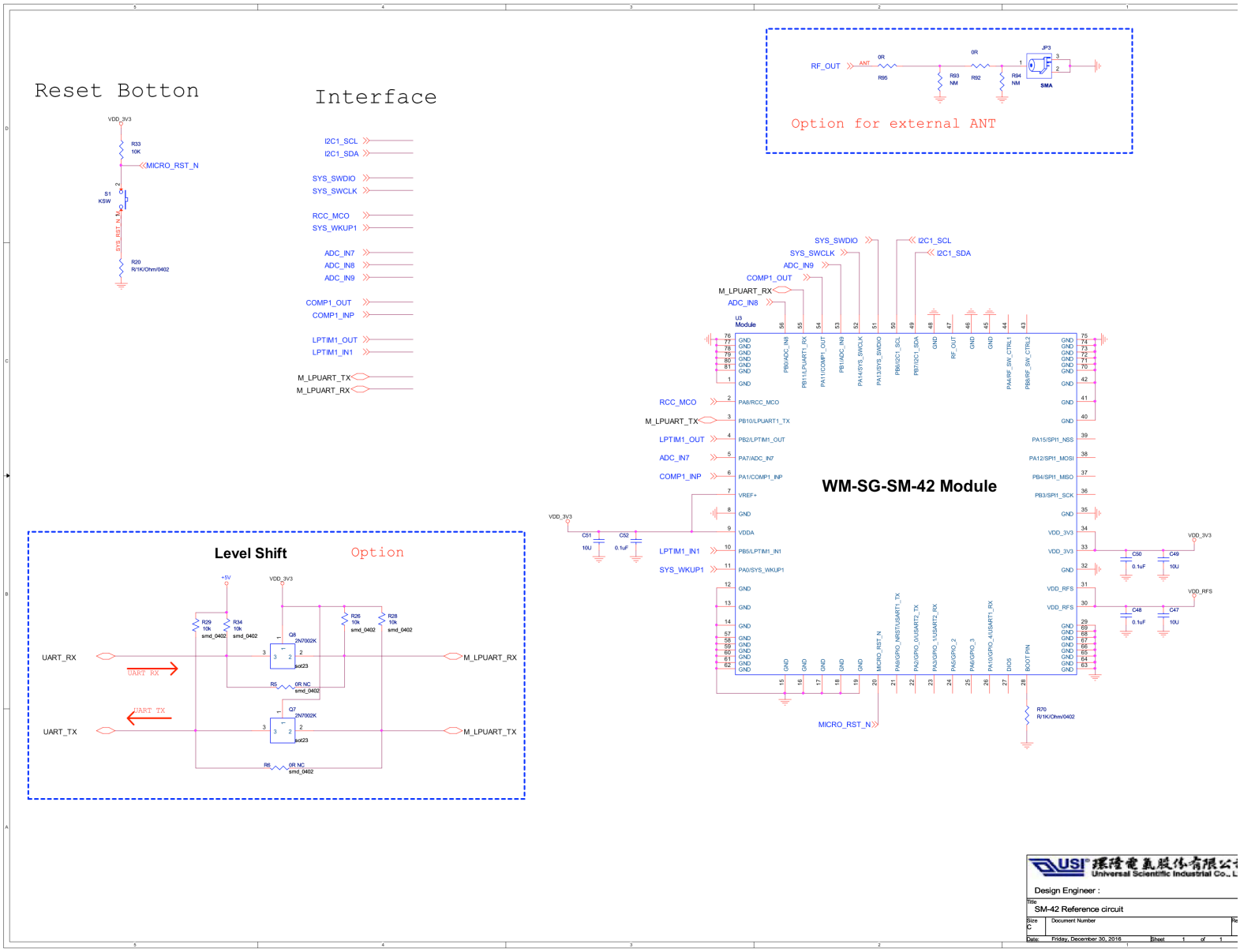
1. **Material: Conductive Polystyrene (Recycle)**
2. **Color: Black**
3. **Surface resistance: 10^{6} Ohms/square 以下.**
   Cumulative tolerance per 10 pitches (P_0) is ±0.2mm.
   A_0 & B_0 are measured on the plane by 0.3mm above the bottom of the pocket.
4. **K_0 is measured from the Inside bottom of the pocket to the top surface of the carrier.**
5. **Pocket position relative to sprocket hold is measured as true position of pocket, not sprocket hold.**

13 MSL LEVEL / STORAGE CONDITION



Life cycle: 1 years

14 APPLICATION REFERENCE DESIGN



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