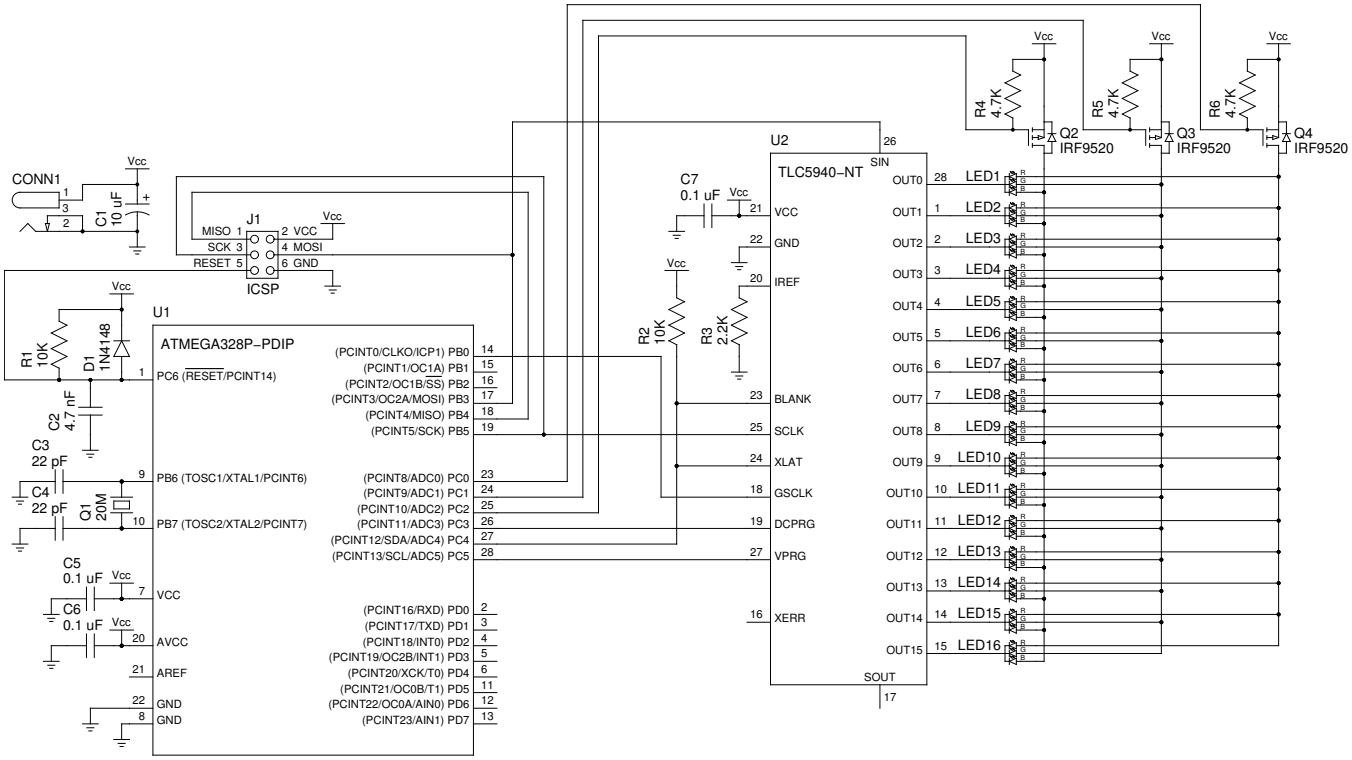

Fixed pins: GSCLK (PB0), SIN (PB3), SCLK (PB5)
Remappable pins: BLANK (PC4), XLAT (PC4), DCPRG (PC3), VPRG (PC5), ROW0_PIN (PC0), ROW1_PIN (PC1), ROW2_PIN(PC2)
Optional pins (see documentation): DCPRG (PC3), VPRG (PC5)
Restricted pins (see below): PB2, PB4, ROW0_PIN (PC0), ROW1_PIN (PC1), ROW2_PIN (PC2)

Pins marked "remappable" in the above list may be remapped to unused pins, or swapped with other remappable pins in the Makefile configuration.

Due to hardware limitations when using this SPI mode, PB2 must always remain an output pin, and PB4 must always remain an input pin, but both may be used for other purposes as long as those conditions are met.

All multiplexing pins in use (ROW0_PIN, ROW1_PIN, and ROW2_PIN) must belong to the same PORT.

Makefile configuration:
TLC5940_N = 1
TLC5940_ENABLE_MULTIPLEXING = 1
TLC5940_MULTIPLEX_N = 3
TLC5940_SPI_MODE = 0
BLANK_PIN = PC4
XLAT_PIN = PC4
DCPRG_PIN = PC3
VPRG_PIN = PC5
ROW0_PIN = PC0
ROW1_PIN = PC1
ROW2_PIN = PC2

For optimal performance, BLANK_PIN and XLAT_PIN should belong to the same PORT, and XLAT_PIN should belong to the same PORT as the multiplexing pins (ROW0_PIN, ROW1_PIN, and ROW2_PIN).

R1 is optional, but protects against accidental resets due to noise.
D1 is optional, but provides ESD protection for the $\overline{\text{RESET}}$ pin.
C2 is optional, but provides additional noise protection for the $\overline{\text{RESET}}$ pin. (If debugWire or PDI is being used, C2 cannot be present.)

Q1, C3, and C4 are optional if the fuse bits are changed appropriately to use the internal oscillator.

LED1–16 are common cathode RGB LEDs.

The IRLML9303 is a much better choice for Q2, Q3, and Q4, but it is only available in a surface mount package.

