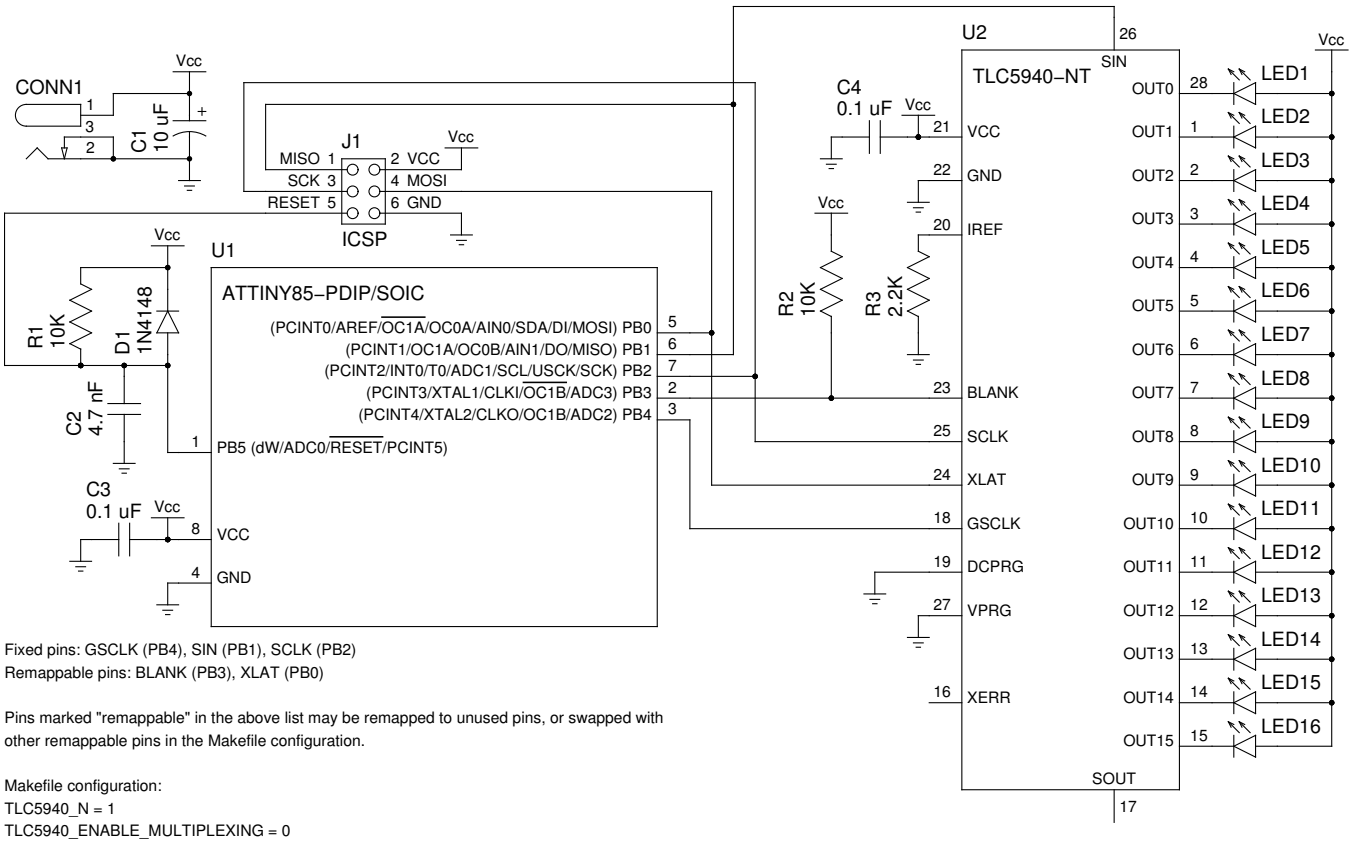

Fixed pins: GSCLK (PB4), SIN (PB1), SCLK (PB2)
Remappable pins: BLANK (PB3), XLAT (PB0)

Pins marked "remappable" in the above list may be remapped to unused pins, or swapped with other remappable pins in the Makefile configuration.

Makefile configuration:
TLC5940_N = 1
TLC5940_ENABLE_MULTIPLEXING = 0
TLC5940_SPI_MODE = 2
TLC5940_ISR_CTC_TIMER = 0
BLANK_PIN = PB3
XLAT_PIN = PB0
DCPRG_PIN = GND
VPRG_PIN = GND

To ensure the outputs remain off while reflashing the chip using this SPI mode, avoid mapping BLANK_PIN to PB0 (the ICSP uses PB0 for MOSI).

R1 is optional, but protects against accidental resets due to noise.
D1 is optional, but provides ESD protection for the $\overline{\text{RESET}}$ pin.
C2 is optional, but provides additional noise protection for the $\overline{\text{RESET}}$ pin. (If debugWire or PDI is being used, C2 cannot be present.)

