CME 433.3 (3L-3P alt. weeks)
Digital Systems Architecture

Department of Electrical and Computer Engineering
Fall 2014-15

Description: Components and architecture complement each other in the design of digital systems implemented in ASIC (Application Specific Integrated Circuit), ASSP (Application Specific Standard Product), FPGA/CPLD (Field Programmable Gate Array/Complex Programmable Logic Device), Microprocessor, DSP (Digital Signal Processor) and SOC (System on Chip). CME 341 and CME 435 teach how to build a system from components. CME 433 teaches guiding principles to organize a system using a top down design approach.

Prerequisites: CME331 and CME 341

Students are expected to be able to communicate in spoken and written English. "Developing and practicing communication skills is an essential experience requirement." – Experience Guideline 2 (Updated May 2009), Components of Acceptable Engineering Work Experience, APEGS

Pre- or Corequisites:

Instructor:
Seokbum Ko, Ph.D. P.Eng.
Professor, Department of Electrical and Computer Engineering
Office: 3B31
Telephone: 306.966.5456
Email: seokbum.ko@usask.ca

Lectures: Tuesday, Thursday, 10:00 a.m.–11:20 a.m., ENGR Room 2B53

Laboratory: L01: Friday alt. weeks, 2:30 p.m.–5:20 p.m., ENGR Room 2C61

Website: Assignments, solutions, lab schedules, general course information, and announcements will be posted on the course website. Students are responsible for keeping up-to-date with the information on the course website: PAWS

Course Reference Numbers (CRNs):
86575 (lectures)
90158 (L01)

Textbook:
Required
Morgan Kaufmann, David Patterson and John Hennessy, *Computer Organization and Design: The Hardware/Software Interface, 5th Ed*
Recommended
Morgan Kaufmann, John L. Hennessy and David A. Patterson, *Computer Architecture, 5th Ed.: A Quantitative Approach*
Behrooz Parhami, *Computer Architecture: From Microprocessors to Supercomputers* (Oxford, 2005)

Office Hours: The instructor has an open door policy and will talk to a student at any time. Students may also telephone/email the instructor and arrange a time to meet.

Reading List: none

Assessment: The methods of assessment and their respective weightings are given below:

Midterm Exam	20%
Final Exam	50%
Homework and Labs	20%
Quizzes and Literature Review	10%

Final Grades: The final grades will be consistent with the "literal descriptors" specified in the university's grading system.

http://students.usask.ca/current/academics/grades/grading-system.php

For information regarding appeals of final grades or other academic matters, please consult the University Council document on academic appeals.

http://www.usask.ca/university_secretary/honesty/StudentAcademicAppeals.pdf

Course Content:
Part 1: Basic fundamentals
Part 2: FPGA and logic synthesis
Part 3: Instruction set architecture
Part 4: Arithmetic logic unit for binary and decimal
Part 5: Data path and control
Part 6: Memory system design
Part 7: I/O interfacing
Part 8: Advanced architectures

Quiz: There will be 2 or 3 Quizzes, depending on the pace of the course lectures.

Assignments: There will be series of Assignments, depending on the pace of the course lectures. Assignments must be submitted on time in the class time. Late assignments will not be marked and will be given a mark of zero. Solutions to the assignments are posted to the course website when the marked assignments are returned.

Labs:
Lab1: FPGA design basics
Lab2: Carry look-ahead adder design
Lab3: Microprocessor pipeline and memory caching 1
Lab4: Microprocessor memory caching 2
Lab5: Microprocessor memory caching 3
Lab6: Graphics processing unit

Exams: There will be one midterm exam and one final exam. The midterm exam will be scheduled during the middle of October. All exams are closed book.

Important Dates: The important dates will be posted on the class website.

Student Conduct: Ethical behaviour is an important part of engineering practice. Each professional engineering association has a Code of Ethics, which its members are expected to follow. Since students are in the process of becoming Professional Engineers, it is expected that students will conduct themselves in an ethical manner.

The APEGS (Association of Professional Engineers and Geoscientists of Saskatchewan) Code of Ethics states that engineers shall "conduct themselves with fairness, courtesy and good faith towards clients, colleagues, employees and others; give credit where it is due and accept, as well as give, honest and fair professional criticism" (Section 20(e), The Engineering and Geoscience Professions Regulatory Bylaws, 1997).

The first part of this statement discusses an engineer's relationships with his or her colleagues.

One of the ways in which engineering students can demonstrate courtesy to their colleagues is by helping to maintain an atmosphere that is conducive to learning, and minimizing disruptions in class. This includes arriving on time for lectures, turning cell phones and other electronic devices off during lectures, not leaving or entering the class at inopportune times, and refraining from talking to others while the instructor is talking. However, if you have questions at any time during lectures, please feel free to ask (chances are very good that someone else may have the same question as you do).

For more information, please consult the University Council Guidelines for Academic Conduct.

http://www.usask.ca/university_secretary/council/reports_forms/reports/guide_conduct.php

Academic Honesty: The latter part of the above statement from the APEGS Code of Ethics discusses giving credit where it is due. At the University, this is addressed by university policies on academic integrity and academic misconduct. In this class, students are expected to submit their own individual work for academic credit, properly cite the work of others, and to follow the rules for examinations. Academic misconduct, plagiarism, and cheating will not be tolerated. Copying of assignments and lab reports is considered academic misconduct. Students are responsible for understanding the university's policies on academic integrity and academic misconduct. For more information, please consult the University Council Regulations on Student Academic Misconduct and the university's examination regulations.

http://www.usask.ca/university_secretary/honesty/StudentAcademicMisconduct.pdf
http://www.usask.ca/university_secretary/council/academiccourses.php

Safety: The APEGS Code of Ethics also states that Professional Engineers shall "hold paramount the safety, health and welfare of the public and the protection of the environment and promote health and safety within the workplace" (Section 20(a), The Engineering and Geoscience Professions Regulatory Bylaws, 1997).

Safety is taken very seriously by the Department of Electrical and Computer Engineering. Students are expected to work in a safe manner, follow all safety instructions, and use any personal protective equipment provided. Students failing to observe the safety rules in any laboratory will be asked to leave.

Laboratory Learning Outcomes:

Lab1 (FPGA design basics): Upon completion of this Lab the students should be able to:

- Demonstrate the basic coding skills of both Altera and Xilinx FPGA tools
- Implement the Shannon's expansion theorem and Davio expansion theorem

Lab2 (Carry look-ahead adder design): Upon completion of this Lab the students should be able to:

- Explain the advantages and disadvantages of different types of adders (i.e. ripple carry, carry-lookahead, carry-save, etc.)
- Design and build a 1-bit, 4-bit, 16-bit and 32-bit carry-lookahead adder.

Lab3 (Microprocessor pipeline and memory caching 1): Upon completion of this Lab the students should be able to:

- Implement a pipelined microprocessor architecture
- Implement the operation of suspending the microprocessor
- Explain the operations of a dual-port RAM

Lab4 (Microprocessor memory caching 2): Upon completion of this Lab the students should be able to:

- Implement the operation of a single-line cache for the program memory.
- Explain the advantages and disadvantages of using an instruction cache.

Lab5 (Microprocessor memory caching 3): Upon completion of this Lab the students should be able to:

- Implement memory cache initialization for the program memory cache.
- Implement the operation of a 4-line, 8-words per line cache for the program memory.
- Explain the advantages that the multi-line cache has over the single-line cache.

Lab6 (Graphics processing unit): Upon completion of this Lab the students should be able to:

- Explain the architecture of the NVIDIA GPU.
- Explain the interaction between the CPU and GPU in a computer.
- Write a basic CUDA program taking advantage of parallel programming.

Course Learning Outcomes:

Upon completing this course students will be able to:

1) Explain how to measure the digital system performance using Amdahl's law and Gustafson's law
2) Explain the advanced logic minimization techniques
3) Explain how Look-Up Table-based FPGAs work
4) Explain what key decisions should be made from instruction set architecture point of view
5) Explain what Arithmetic Logic Unit does for binary and decimal in digital systems
6) Explain how CPU works in detail
7) Explain the importance of memory hierarchy
8) Explain I/O interfacing
9) Explain the advanced architecture including Graphics Processing Unit and multicore.

Attribute Mapping:

*Level of Performance**

Learning Outcome	Attribute**											
	A1	**A2**	**A3**	**A4**	**A5**	**A6**	**A7**	**A8**	**A9**	**A10**	**A11**	**A12**
1	2	2			2							
2	3	3	3		3							
3	3	3	3		3							
4	3	3										
5	3				3							
6	3				3							
7	3	3	3									
8	2											
9	3	3										

******Attributes:

- **A1** Knowledge base for engineering
- **A2** Problem analysis
- **A3** Investigation
- **A4** Design
- **A5** Use of engineering tools
- **A6** Individual and team work
- **A7** Communication skills
- **A8** Professionalism
- **A9** Impact of engineering on society and the environment
- **A10** Ethics and equity
- **A11** Economics and project management
- **A12** Life-long learning

*Levels of Performance:

1 - **Knowledge** of the skills/concepts/tools but not using them to solve problems.

2 - **Using** the skills/concepts/tools to solve directed problems. (*"Directed" indicates that students are told what tools to use.*)

3 - **Selecting** and using the skills/concepts/tools to solve non-directed, non-open-ended problems. (*Students have a number of S/C/T to choose from and need to decide which to employ. Problems will have a definite solution.*)

4 - **Applying** the appropriate skills/concepts/tools to solve open-ended problems. (*Students have a number of S/C/T to choose from and need to decide which to employ. Problems will have multiple solution paths leading to possibly more than one acceptable solution.*)

Accreditation Unit (AU) Mapping: (% of total class AU)

Math	Natural Science	Complementary Studies	Engineering Science	Engineering Design
-	-	-	45.8 AU (100%)	-

Assessment Mapping:

Component	Weighting	Methods of Feedback***	Learning Outcomes Evaluated
Assignments	10	S	1,2,3,4,5,6,7,8,9
Labs	10	S	3,5,6,7,9
Quiz	10	S	1,2,3,4,5,6,7,8.9
Midterm exams	20	S	1,2,3,4,5
Final exam	50	S	1,2,3,4,5,6,7,8,9

***Methods of Feedback:

F – *formative* (written comments and/or oral discussions)

S – *summative* (number grades)