CME 342.3 (3L-1.5P)
VLSI Circuit Design

Department of Electrical and Computer Engineering
Fall 2013

Description: This is an introductory course in VLSI Systems and Design. CMOS logic circuits and fabrication process will be introduced first, followed by some advanced topics such as design optimization for speed, power and testing. At the completion of this course, a student should be able to design and analyze digital circuits. They should be able to design for low power and speed, and testability.

Prerequisites: EE221 and (EE 232 or EP 321)
Students are expected to be able to communicate in spoken and written English.

Corequisites: None

Instructor: Li Chen, Ph.D. P.Eng.
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Lectures: Monday-Wednesday-Friday, 12:30-13:30, Engineering Building, Room 2C01

Tutorials: N/A

Laboratory: Wednesdays, 8:30-11:20, Room 2C61

Website: Assignments, solutions, lab schedules, general course information, and announcements will be posted on the course website. Students are responsible for keeping up-to-date with the information on the course website:
http://www.engr.usask.ca/classes/CME/342/

Course Reference Numbers (CRNs): 89880 (lectures), 89881 (laboratory)

Textbook: The recommended text for this course is:
"CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Neil H.E. Weste & David M. Harris, 2006, Addison Wesley

Office Hours: The instructor has an open door policy and will talk to a student at any time. Students may also telephone/email the instructor and arrange a time to meet.

Reading List: None.

Assessment: The methods of assessment and their respective weightings are given below:

Assignments	15%
Labs	25%
Midterm Exam	20%
Final Exam	40%

Final Grades: The final grades will be consistent with the "literal descriptors" specified in the university's grading system.

http://students.usask.ca/current/academics/grades/grading-system.php

For information regarding appeals of final grades or other academic matters, please consult the University Council document on academic appeals.

http://www.usask.ca/university_secretary/honesty/StudentAcademicAppeals.pdf

Course Content:

Outline for the Class Lecture Material

1. MOS Transistor Theory (1 week)
2. CMOS Logic Circuits (1.5 week)
3. CMOS Layout and Processing Technology (2 week)
4. Circuit Simulation - SPICE Model and Simulation (1 week)
5. Speed - RC Delay, Logic Effort (1.5 week)
6. Power - Static Power, Dynamic Power, Optimization (1 week)
7. Sequential Logic Circuits (2 weeks)
8. Alternative Logic Structures (1 week)
9. Design for Testability (1 week)

Assignments and labs: There are 5 Assignments and 6 labs due bi-weekly. The assignments and lab reports will be marked and returned to the students.

Exams: There will be one midterm exam and one final exam.

Important Dates: The important dates will be posted on the class website.

Student Conduct: Ethical behaviour is an important part of engineering practice. Each professional engineering association has a Code of Ethics, which its members are expected to follow. Since students are in the process of becoming Professional Engineers, it is expected that students will conduct themselves in an ethical manner.

The APEGS (Association of Professional Engineers and Geoscientists of Saskatchewan) Code of Ethics states that engineers shall "conduct themselves with fairness, courtesy and good faith towards clients, colleagues, employees and others; give credit where it is due and accept, as well as give, honest and fair professional criticism" (Section 20(e), The Engineering and Geoscience Professions Regulatory Bylaws, 1997).

The first part of this statement discusses an engineer's relationships with his or her colleagues. One of the ways in which engineering students can demonstrate courtesy to their colleagues is by helping to maintain an atmosphere that is conducive to learning, and minimizing disruptions in class. This includes arriving on time for lectures, turning cell phones and other electronic devices off during lectures, not leaving or entering the class at inopportune times, and refraining from talking to others while the instructor is talking. However, if you have questions at any time during lectures, please feel free to ask (chances are very good that someone else may have the same question as you do).

For more information, please consult the University Council Guidelines for Academic Conduct.

http://www.usask.ca/university_secretary/council/reports_forms/reports/guide_conduct.php

Academic Honesty: The latter part of the above statement from the APEGS Code of Ethics discusses giving credit where it is due. At the University, this is addressed by university policies on academic integrity and academic misconduct. In this class, students are expected to submit their own individual work for academic credit, properly cite the work of others, and to follow the rules for examinations. Academic misconduct, plagiarism, and cheating will not be tolerated. Copying of assignments and lab reports is considered academic misconduct. Students are responsible for understanding the university's policies on academic integrity and academic misconduct. For more information,

please consult the University Council Regulations on Student Academic Misconduct and the university's examination regulations.

http://www.usask.ca/university_secretary/honesty/StudentAcademicMisconduct.pdf
http://www.usask.ca/university_secretary/council/academiccourses.php

Safety: The APEGS Code of Ethics also states that Professional Engineers shall "hold paramount the safety, health and welfare of the public and the protection of the environment and promote health and safety within the workplace" (Section 20(a), The Engineering and Geoscience Professions Regulatory Bylaws, 1997).

Safety is taken very seriously by the Department of Electrical and Computer Engineering. Students are expected to work in a safe manner, follow all safety instructions, and use any personal protective equipment provided. Students failing to observe the safety rules in any laboratory will be asked to leave.

Laboratory Learning Outcomes:

Overarching Learning Outcomes for the Laboratory Component

Upon completion of the CME342 labs the students will be able to:

1. Design logic gates using schematic entry and simulation with Cadence,
2. Develop the layout of digital circuits and perform DRC, LVS, and postlayout simulation,
3. Carry out logical effort analysis with simulation tool,
4. Explain SPICE simulation syntax and advanced features using Cadence,
5. Conduct logic synthesis using component library,
6. Place and route the digital components into a chip with the aid of Cadence tool.

Lab 1: Upon completion of this Lab the students should be able to:

1. Start Cadence and be familiar with the commands in Cadence for schematic entry,
2. Carry out schematic simulate and measure the delay using waveforms.

Lab 2: Upon completion of this Lab the students should be able to:

1. Develop the layout of the logic gates with Cadence,
2. Carry out DRC and LVS checking of the layout,
3. Perform postlayout simulation from the extracted view.

Lab 3: Upon completion of this Lab the students should be able to:

1. Derive the SPICE simulation files from schematic and text file,
2. Perform simulations using Cadence environment,
3. Advanced simulation techniques using Calculator functions in Cadence.

Lab 4: Upon completion of this Lab the students should be able to:

1. Obtain the logical effort and electrical efforts using schematic simulation,
2. Verify the logical efforts of Inverters and NAND gates.

Lab 5: Upon completion of this Lab the students should be able to:

1. Synthesis logic circuits with a component library,
2. Explain the procedures for logic synthesizing and select speed, area options.

Lab 6: Upon completion of this Lab the students should be able to:

1. Explain the back-end design flow for IC design
2. Develop the layout of a circuit using Cadence place and route tool

Course Learning Outcomes:

Upon completing this course students will be able to:

1) Explain the MOSFET transistor operation,
2) Explain the CMOS technology fabrication process,
3) Design combinational and sequential circuits with Complementary CMOS logic and alternative logic such as pass logic, and dynamic logic,
4) Explain the RC delay in logic circuits, and optimize the speed of a circuit design by using logical effort method,
5) Explain the major components in power consumptions and techniques to reduce it,
6) Design common combinational and sequential logic circuits,
7) Explain the design techniques for testability,
8) Perform schematic entry, schematic simulation, layout and postlayout simulation using Cadence tools,
9) Develop the layout of circuits using Cadence Place & Route tools.

Attribute Mapping:

*Level of Performance**

Learning Outcome	Attribute**											
	A1	**A2**	**A3**	**A4**	**A5**	**A6**	**A7**	**A8**	**A9**	**A10**	**A11**	**A12**
1	2	2			2							
2	2	2										
3	2	3		2								
4	2	4		3								
5	2	2										
6	2	2		2								
7	2	1										
8	2	2										
9	2	2		2								

******Attributes:

- **A1** Knowledge base for engineering
- **A2** Problem analysis
- **A3** Investigation
- **A4** Design
- **A5** Use of engineering tools
- **A6** Individual and team work
- **A7** Communication skills
- **A8** Professionalism
- **A9** Impact of engineering on society and the environment
- **A10** Ethics and equity
- **A11** Economics and project management
- **A12** Life-long learning

*Levels of Performance:

1 - **Knowledge** of the skills/concepts/tools but not using them to solve problems.

2 - **Using** the skills/concepts/tools to solve directed problems. (*"Directed" indicates that students are told what tools to use.*)

3 - **Selecting** and using the skills/concepts/tools to solve non-directed, non-open-ended problems. (*Students have a number of S/C/T to choose from and need to decide which to employ. Problems will have a definite solution.*)

4 - **Applying** the appropriate skills/concepts/tools to solve open-ended problems. (*Students have a number of S/C/T to choose from and need to decide which to employ. Problems will have multiple solution paths leading to possibly more than one acceptable solution.*)

Accreditation Unit (AU) Mapping: (% of total class AU)

Math	Natural Science	Complementary Studies	Engineering Science	Engineering Design
-	-	-	32.9 AU (72%)	12.8 AU (28%)

Assessment Mapping:

Component	Weighting	Methods of Feedback***	Learning Outcomes Evaluated
Assignment	15	S	2,3,4,5,6,8
Midterm exams	20	S	2,3,4,5,6,7,8
Labs	25	S	1,3,4,5,6,7
Final exam	40	S	2,3,4,5,6,7,8

***Methods of Feedback:

F – *formative* (written comments and/or oral discussions)

S – *summative* (number grades)