CME 341.3
Logic Design Using FPGAs

Department of Electrical and Computer Engineering
Fall 2014

Description: This course investigates techniques for designing large digital circuits with the Verilog Hardware Description Language (Verilog HDL). The course focuses on FPGAs; however, the techniques discussed are also applicable to the design of ASICs. The architectures of FPGAs are discussed in general with certain aspects of their internal operation discussed in detail. Emphasis is placed on connecting the Verilog HDL code to the hardware circuit that is constructed by the Verilog compiler and router.

Prerequisites: CMPT 116 and (EE 232 or EP 321)

Corequisites: None

Instructor: J. Eric Salt, Ph.D. P.Eng.
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Lectures: Monday-Wednesday-Friday, 2:30-3:30, Engineering Building, Room 1B79

Tutorials: As needed, Wednesday 6:00-700, Room 1B79

Laboratory: Wednesdays, 5:30-8:20, Room 1B79

Website: Assignments, solutions, lab schedules, general course information, and announcements will be posted on the course website. Students are responsible for keeping up-to-date with the information on the course website.

http://www.engr.usask.ca/classes/EE/431/

Course Reference Numbers (CRNs): 89880 (lectures), 89881 (laboratory)

Textbook: A text book would be helpful but is not necessary. Any textbook on Verilog 2001 or Verilog 2005 would be appropriate. The text would be used to look up the syntax of Verilog commands (much like a dictionary is used to look up the meaning of a word) so the textbook should have an extensive index. The same information can often be found by searching the web.

Office Hours: The instructor has an open door policy and will talk to a student at any time. Students may also telephone/email the instructor and arrange a time to meet.

Reading List: None.

Assessment: The methods of assessment and their respective weightings are given below(scores on the midterm are replaced with the score on the final exam if that score is greater):

Assignments	0% (unless final grade is between 40 and 49
Project	0%
Lab	30%
Midterm Exams	20%

Final Exam 50%

Final Grades: The final grades will be consistent with the "literal descriptors" specified in the university's grading system.

http://students.usask.ca/current/academics/grades/grading-system.php

For information regarding appeals of final grades or other academic matters, please consult the University Council document on academic appeals.

http://www.usask.ca/university_secretary/honesty/StudentAcademicAppeals.pdf

Course Content:

Outline for the Class Lecture Material

Part I

1. Principles of hardware description language synthesizers
2. Introduction to the Lab: DE2 board and tools
3. Designing Circuits with Verilog HDL
4. Using QUARTUS to synthesize circuits
5. Using Modelsim-Altera to debug circuits
    a. Principles of HDL simulators
    b. Simulation of circuits using Modelsim-Altera

Part II

1. Finite State Machines in Verilog HDL
2. Making timers and clock dividers for finite state machines
3. Operation of traffic light controllers

Part III

1. Design a 4-bit microprocessor for implementation in an FPGA
    a. Design the program sequencer
    b. Design the program memory
    c. Design the instruction decoder
    d. Design the computational unit
    e. Design the data memory
    f. Integrate the circuits to make the microprocessor
2. Debugging a microprocessor
    a. debugging strategies
    b. debugging examples
3. Compiler directives (including synthesizer directives)
4. Circuits that enhance the performance of a microprocessor

Assignments: There are 10 assignments. The assignments will not be marked unless the student term grade calculates to between 43 and 50%, in which case the assignments will be marked out of 10 and that mark will be added to the calculated grade to bring the term grade up to a maximum of 50%.

Attribute Mapping:

*Level of Performance**

Learning Outcome	Attribute**											
	A1	**A2**	**A3**	**A4**	**A5**	**A6**	**A7**	**A8**	**A9**	**A10**	**A11**	**A12**
1					4							
2					4							
3				3								
4				3								
5				3								
6				4								
7				4								
8				4								
9												
10												
11												

****Attributes:**

- **A1** Knowledge base for engineering
- **A2** Problem analysis
- **A3** Investigation
- **A4** Design
- **A5** Use of engineering tools
- **A6** Individual and team work
- **A7** Communication skills
- **A8** Professionalism
- **A9** Impact of engineering on society and the environment
- **A10** Ethics and equity
- **A11** Economics and project management
- **A12** Life-long learning

*Levels of Performance:

1 - **Knowledge** of the skills/concepts/tools but not using them to solve problems.

2 - **Using** the skills/concepts/tools to solve directed problems. (*"Directed" indicates that students are told what tools to use.*)

3 - **Selecting** and using the skills/concepts/tools to solve non-directed, non-open-ended problems. (*Students have a number of S/C/T to choose from and need to decide which to employ. Problems will have a definite solution.*)

4 - **Applying** the appropriate skills/concepts/tools to solve open-ended problems. (*Students have a number of S/C/T to choose from and need to decide which to employ. Problems will have multiple solution paths leading to possibly more than one acceptable solution.*)

Accreditation Unit (AU) Mapping: (% of total class AU)

Math	Natural Science	Complementary Studies	Engineering Science	Engineering Design
-	-	-	20	80

Assessment Mapping:

Component	Weighting	Methods of Feedback***	Learning Outcomes Evaluated
Midterm exams	30	S	1,3,4,6,8
Lab exams	20	S	1,2,3,4,5,7
Final exam	50	S	1,3,4,6,8

***Methods of Feedback:

F – *formative* (written comments and/or oral discussions)
S – *summative* (number grades)