CME 435.3 (3L – 3P alt weeks)
Verification of Digital Systems

Department of Electrical and Computer Engineering
Fall 2015

UNIVERSITY OF SASKATCHEWAN

Description:	Covers the verification of digital circuits and systems with emphasis on SystemVerilog, a verification language. It starts with the basics, such as functional verification methodologies, and SystemVerilog fundamentals, and gradually builds to more complex examples and advanced topics. At the end of the course, a complete verification system is created using SystemVerilog.
Prerequisite(s):	EE 431.3: Logic Design using FPGAs (taken) Students are expected to be able to communicate in spoken and written English. "Developing and practicing communication skills is an essential experience requirement." – Experience Guideline 2 (Updated May 2009) Components of Acceptable Engineering Work Experience, APEGS
Corequisite(s):	None
Instructors:	Anthony Rapley, M.Sc., P.Eng. Engineer, CNH Office: N/A Telephone: (306) 242-6766 Email: Anthony.Rapley@gmail.com
Lectures:	Tuesday-Thursday, 8:30-10:00 a.m., Engineering Building, Room 2B53
Tutorials:	Wednesday (alternate weeks), 3:30-6:30 p.m., Engineering Building, Room 2C61
Website:	Notes, assignments, solutions, tutorial schedules, general course information, and announcements will be posted on the course website. Students are responsible for keeping up-to-date with the information on the course website. http://www.engr.usask.ca/classes/CME/435/
Course Reference Numbers (CRNs):	86577(lectures), 87588 (tutorials)
Textbook:	There is no required textbook; however the following textbook is recommended: Chris Spear and Greg Tumbush, 2012, SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, 3rd Edition, Springer, New York, New York. Additional SystemVerilog Language information is available from the SystemVerilog Language Reference Manual (LRM). This reference material is available at http://www.eda.org/sv/SystemVerilog_3.1a.pdf
Reading List:	None
Office Hours:	For office hours, an "open-door" policy is maintained. Students are welcome to drop by the office at any time for help with the course material. Alternatively, students can contact the instructors by telephone or email to schedule a time to meet. Prof. Bolton's class schedule is posted on his office's bulletin board.
Assessment:	The methods of assessment and their respective weightings are given below: Assignments 6% Tutorials 24% Midterm Exam 20% Final Exam 50%
Final Grades:	The final grades will be consistent with the "literal descriptors" specified in the university's grading system. http://students.usask.ca/current/academics/grades/grading-system.php

For information regarding appeals of final grades or other academic matters, please consult the University Council document on academic appeals.

http://www.usask.ca/university_secretary/honesty/StudentAcademicAppeals.pdf

Course Content:

1. Introduction to Digital ASIC Functional Verification
    - Goal of Functional Verification
    - Verification Challenges
    - Verification Metrics
    - Verification Technologies
2. Functional Verification Planning
    - General Approaches
        - Black Box
        - White Box
        - Grey Box
    - Assertion Based Verification
    - Coverage Based Verification
    - Test Plans
    - CME 435 Methodology and Philosophy
3. Test bench Architecture and Interface Component Design
    - Interfaces and Ports
    - Driver and Monitors
    - Error Injection
    - Transaction Records
4. Introduction to SystemVerilog
    - History
    - Data Types
    - Procedural Statements
    - Functions and Tasks
    - Modules
5. Basic Stimulus Generation
    - Test bench construction
6. Constrained Random Generation
    - Random Variables
    - Constraints
7. Functional Coverage
    - Covergroups
    - Coverpoints
    - Binning
    - Cross Coverage
8. Enhancing Test Planning Skills
9. Practical SystemVerilog
    - Queues
    - Fork … Join
10. Stimulus Generation with Driver Components
    - Transaction Based Stimulus
11. Advanced Test benches
    - Hierarchy
    - Classes
12. Module Component Design
    - Transaction Records
13. Conclusions
    - Test Plans
    - Audits

Assignments:

Assignments will be handed out approximately every two weeks, depending on the pace of the course lectures. Assignments must be submitted on time in the assignment box outside 2C94E. Late assignments will not be marked and will be given a mark of zero.

Tutorials/Practicums: Tutorials/Practicums are held every two weeks. The purpose is to have students gain practical experience in the design of test benches and the use of Questa. Tutorials/Practicums must be submitted on time (usually electronically). Late Tutorials/Practicums will not be marked and will be given a mark of zero.

The Tutorials/Practicums are critical to the course as they build on the class lectures and incorporate design into the class.

Tutorial/Practicum Content: The labs associated with CME 435 are intended to familiarise students with use of SystemVerilog in developing test benches for use with the Questa software. They progress from simple introductory labs through to sophisticated randomized testing scenarios.

Lab 1:

Topic: Introduction to Functional Verification Using Questa and Altera Quartus ROM/RAM emulation

What: Set up a suitable directory structure for use with the CME 435 verification methodology and software (Questa). Design verilog modules to replace the Altera ROM/RAM intellectual property. Correct faulty Altera documentation.

End: Use a suitable directory structure template for CME 435 Questa software to allow it be able to be run efficiently and in a re-usable manner.. Verification of Altera ROM/RAM replacements of Altera ROM/RAM IP for use in CME 435. Determine the value of reuse.

Lab 2:

Topic: SystemVerilog test bench creation

What: Design a complete SystemVerilog test bench to evaluate their EE 431 microprocessor operation.

End: Have the ability to measure program timing of their EE 431 microprocessor. Apply various SystemVerilog constructs to a simple verification task. Reuse previous code from other test benches.

Lab 3:

Topic: Constrained Random Verification and Functional Coverage

What: Design a complete SystemVerilog test bench using constrained randomization to evaluate a module from their EE 431 microprocessor.

End: Have the ability to measure constrained randomization functional coverage. Apply various SystemVerilog constructs to a simple verification task. Reuse previous code from other test benches.

Lab 4, 5 & 6:

Topic: Advanced verification design (complex module)

What: Design a complete SystemVerilog test bench to evaluate a complex module implementing a supplied functional specification.

End: Have the ability to verify a complex module thorough the use of transaction records and module components and advanced object oriented programming. Reuse previous code from other test benches (where appropriate).

Examinations: The midterm exam is not forgivable. The midterm exam will normally be scheduled during the middle of October. Please plan to be in attendance during this time. All exams are closed book.

Important Dates: TBD

Student Conduct: Ethical behaviour is an important part of engineering practice. Each professional engineering association has a Code of Ethics, which its members are expected to follow. Since students are in the process of becoming Professional Engineers, it is expected that students will conduct themselves in an ethical manner.

The APEGS (Association of Professional Engineers and Geoscientists of Saskatchewan) Code of Ethics states that engineers shall "conduct themselves with fairness, courtesy and good faith towards clients, colleagues, employees and others; give credit where it is due and accept, as well as give, honest and fair professional criticism" (Section 20(e), The Engineering and Geoscience Professions Regulatory Bylaws, 1997).

The first part of this statement discusses an engineer's relationships with his or her colleagues. One of the ways in which engineering students can demonstrate courtesy to their colleagues is by helping to maintain an atmosphere that is conducive to learning, and minimizing disruptions in class. This includes arriving on time for lectures, turning cell phones and other electronic devices off during lectures, not leaving or entering the class at inopportune times, and refraining from talking to others while the instructor is talking. However, if you do have questions at any time during lectures, please feel free to ask (chances are very good that someone else may have the same question as you do).

For more information, please consult the University Council Guidelines for Academic Conduct.

http://www.usask.ca/university_secretary/council/reports_forms/reports/guide_conduct.php

Academic Honesty:

The latter part of the above statement from the APEGS Code of Ethics discusses giving credit where it is due. At the University, this is addressed by university policies on academic integrity and academic misconduct. In this class, students are expected to submit their own individual work for academic credit, properly cite the work of others, and to follow the rules for examinations. Academic misconduct, plagiarism, and cheating will not be tolerated. Copying of assignments and lab reports is considered academic misconduct. Students are responsible for understanding the university's policies on academic integrity and academic misconduct.

For more information, please consult the University Council Regulations on Student Academic Misconduct and the university's examination regulations.

http://www.usask.ca/university_secretary/honesty/StudentAcademicMisconduct.pdf
http://www.usask.ca/university_secretary/council/academiccourses.php

Safety:

The APEGS Code of Ethics also states that Professional Engineers shall "hold paramount the safety, health and welfare of the public and the protection of the environment and promote health and safety within the workplace" (Section 20(a), The Engineering and Geoscience Professions Regulatory Bylaws, 1997).

Safety is taken very seriously by the Department of Electrical and Computer Engineering. Students are expected to work in a safe manner, follow all safety instructions, and use any personal protective equipment provided. Students failing to observe the safety rules in any laboratory will be asked to leave.

Course Learning Outcomes:

1. Students will acquire a basic understanding of Functional Verification.
2. Students will acquire knowledge of the SystemVerilog verification language.
3. Students will use an industry standard functional verification tool: Questa.
4. Students will design constrained random generation and functional coverage to test systems.
5. Students will learn the fundamentals of test planning and test bench design.
6. Students will learn the need for "reuse" as a development approach.

Tutorial/Practicum Learning Outcomes:

1. Students will acquire a basic understanding of Functional Verification.
2. Students will acquire knowledge of the SystemVerilog verification language.
3. Students will use an industry standard functional verification tool: Questa.
4. Students will design constrained random generation and functional coverage to test systems.
5. Students will learn the fundamentals of test planning and test bench design.
6. Students will learn the need for "reuse" as a development approach.

Attribute Mapping:

Level of Performance[‡]

Learning Outcome	Attribute[†]											
	A1	**A2**	**A3**	**A4**	**A5**	**A6**	**A7**	**A8**	**A9**	**A10**	**A11**	**A12**
1	4	4	4	4	4						1	
2	4											

3					4							
4	4				4						1	
5		4	4									
6				3							2	

†Attributes:

A1 A knowledge base for engineering
A2 Problem analysis
A3 Investigation
A4 Design
A5 Use of engineering tools
A6 Individual and team work
A7 Communication skills
A8 Professionalism
A9 Impact of engineering on society and the environment
A10 Ethics and equity
A11 Economics and project management
A12 Life-long learning

‡Levels of Performance:

1 - **Knowledge** of the skills/concepts/tools but not needing to directly apply them to solve problems.
2 - **Application** of the skills/concepts/tools to directed problems. (*"Directed" indicates that students are told what tools to use.*)
3 - **Selecting and Using** the skills/concepts/tools to solve non-directed, non-open-ended problems. (*Students have a number of S/C/T to choose from and need to decide which to employ. Problems will have a definite solution.*)
4 - **Problem Solving** using the appropriate skills/concepts/tools for open-ended problems. (*Students have a number of S/C/T to choose from and need to decide which to employ. Problems will have multiple solution paths leading to possibly more than one acceptable solution.*)

Accreditation Unit (AU) Mapping: (% of total class AU)

Math	Natural Science	Complementary Studies	Engineering Science	Engineering Design
-	-	-	22.9	22.9

Assessment Mapping:

Component	Weighting	Methods of Feedback*	Learning Outcomes Evaluated
Assignments	6%	F, S	1, 2, 3
Tutorials	24%	F, S	1, 2, 3, 4, 5, 6
Midterm	20%	F, S	1, 2, 5
Final	50%	S	1, 2, 3, 4, 5, 6

*Methods of Feedback: **F** – *formative* (written comments and/or oral discussions)
S – *summative* (number grades)