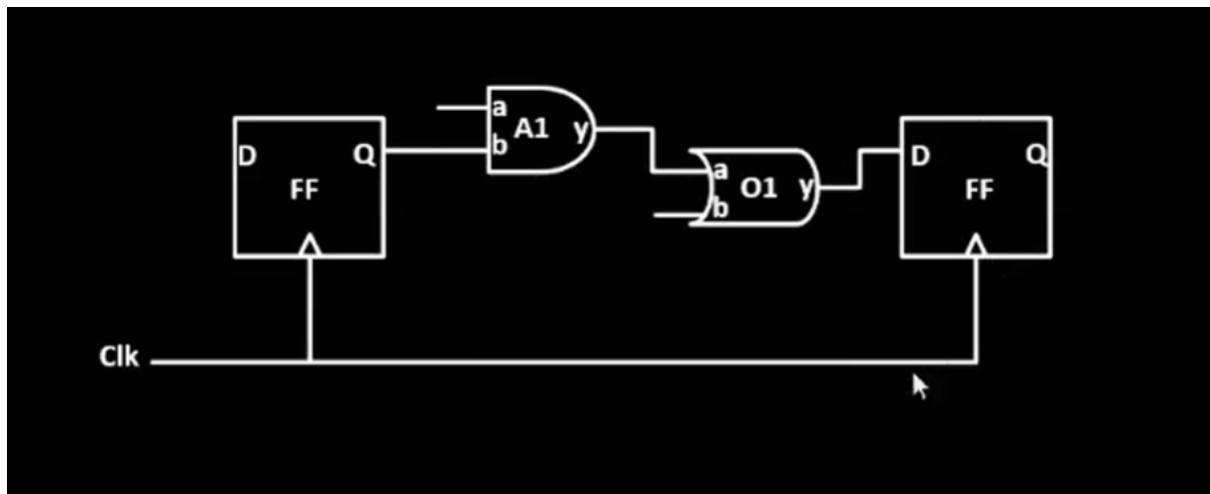


Day 2

Level 3

Define the width and height of core and die

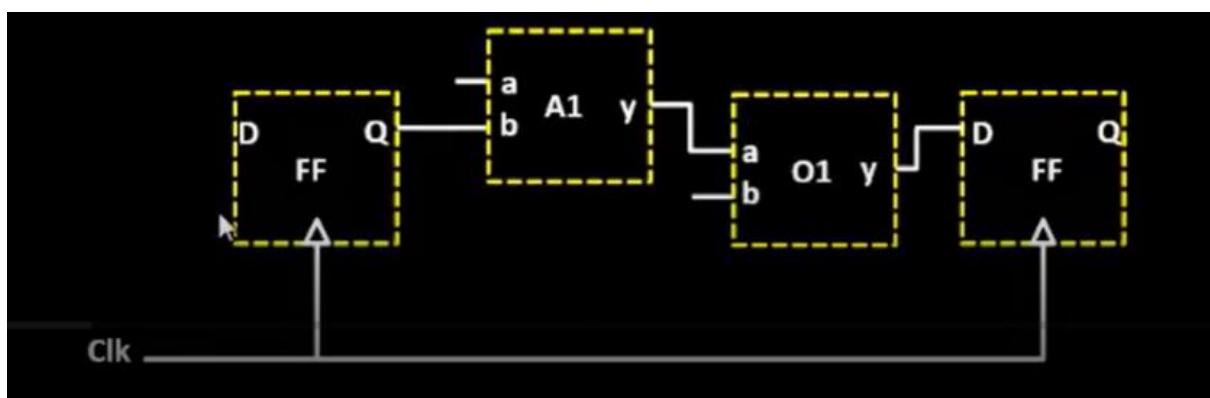
Netlist(A netlist describes the connectivity of an electronic design)



this is the netlist to define the width and height of core and die

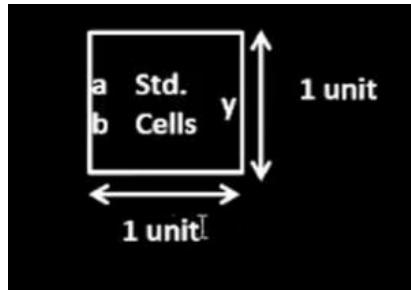
FF= flipflops

A1 O1=The logic gates



We will get this if we give proper dimensions to the logic gates

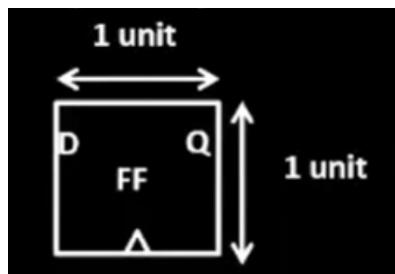
Now lets give every standard cell a rough value



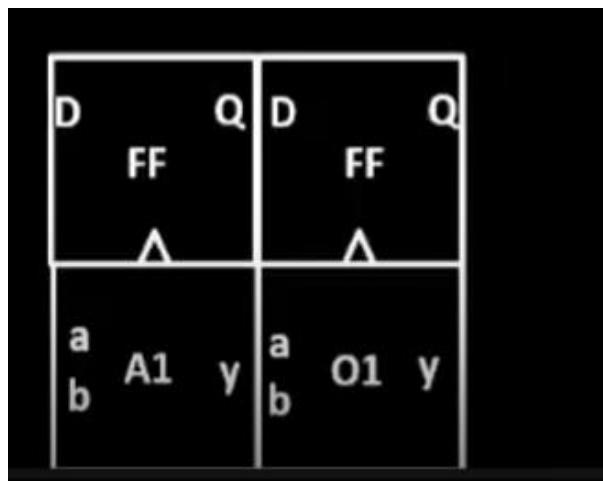
As of now it will be 1 unit on all the sides

The area will be 1 sq unit because $1 \times 1 = 1$

Lets assume the same for the FF

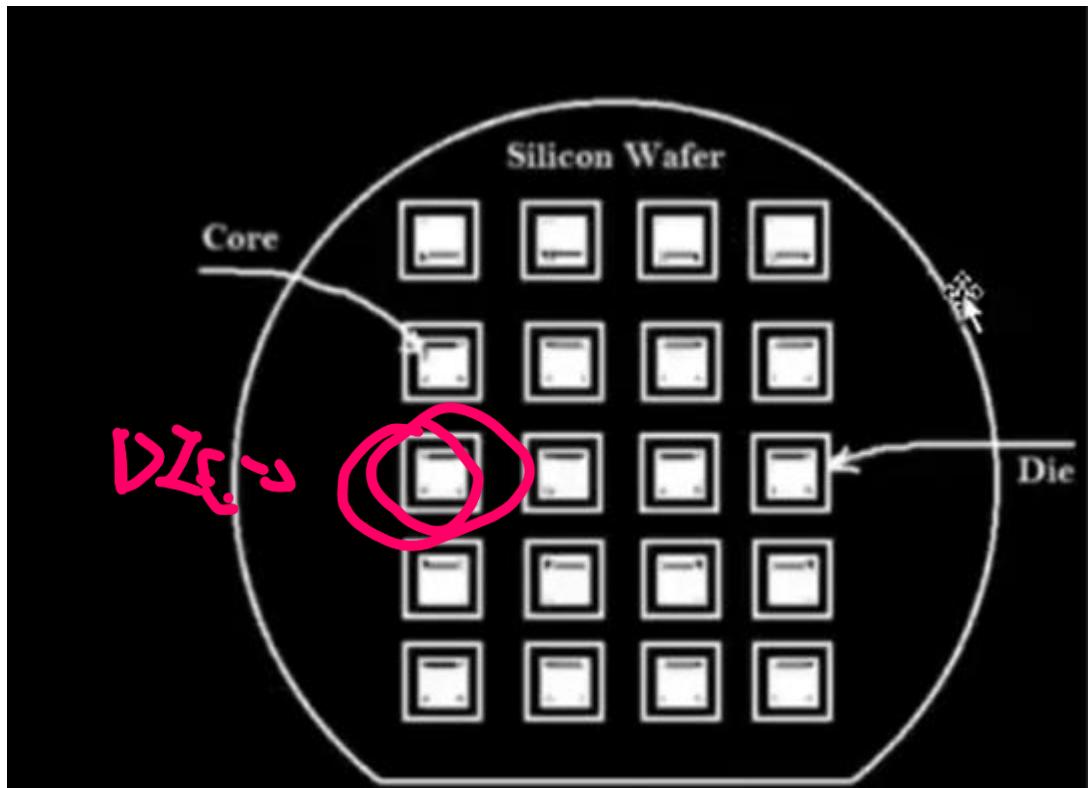


Now to calculate the total length and breadth we arrange in an order like this



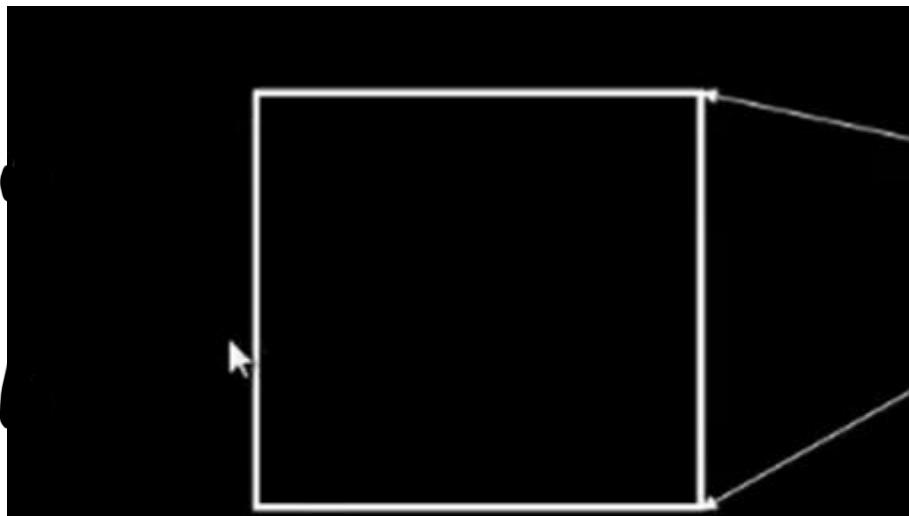
So each side has 2 units so the area will be 4 sq.units

Ok now lets see what is a core and die of a chip



So the silicon wafer is where all these logic stuff happens and

That red marked thingy is the die and inside we have the core



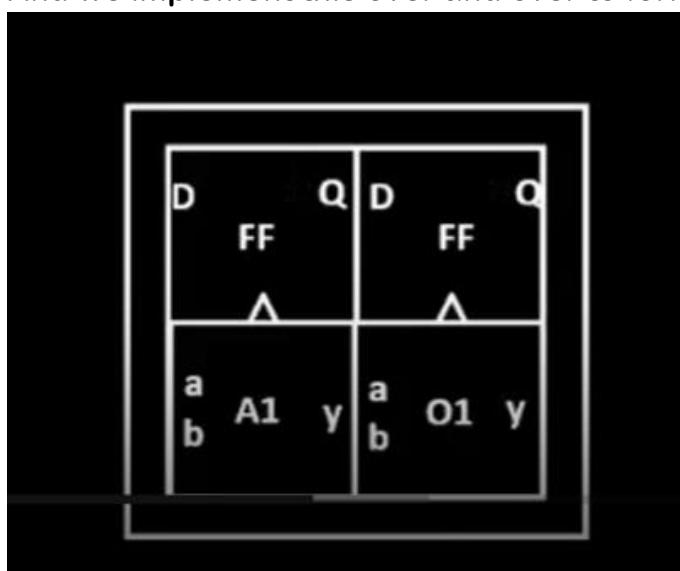
A 'core' is the section of the chip where the fundamental logic of the design is placed.



And the outer thing of it is the Die we saw  (FLASHBACKS)

It's a semiconductor it has the core inside

And we implement this over and over to form the silicon wafer



utilisation factor=  it says

area of netlist / area of core if the answer is 1 then its full

So the arrangement we did before will go to the core

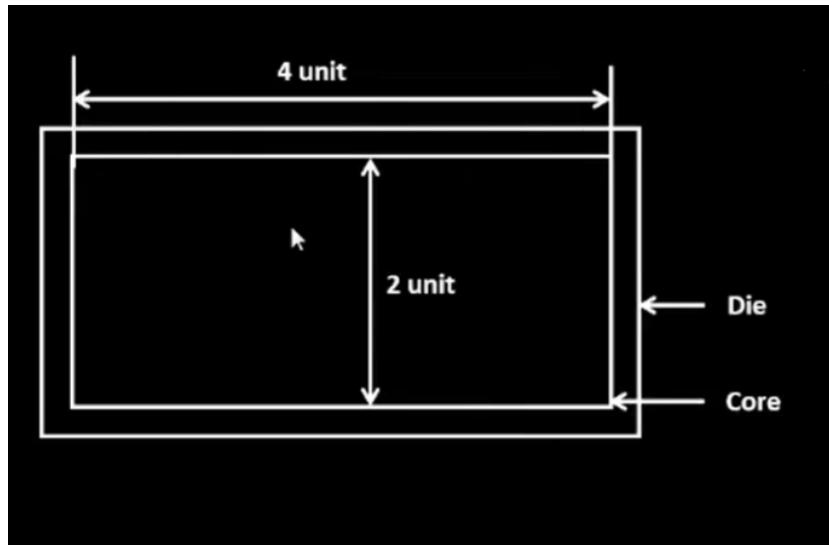
Here it occupies the entire core

It means it has 100% Utilised the core

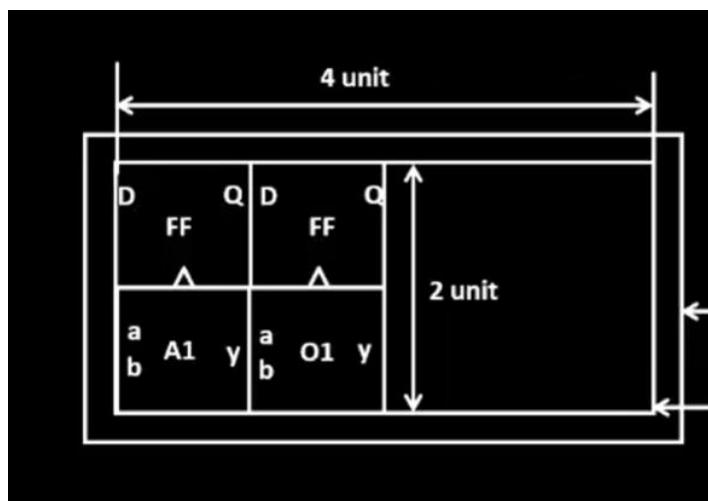
Another aspect ratio = H/B here its $2/2 = 1$

For another example lets take the H as 2unit and B as 4 unit

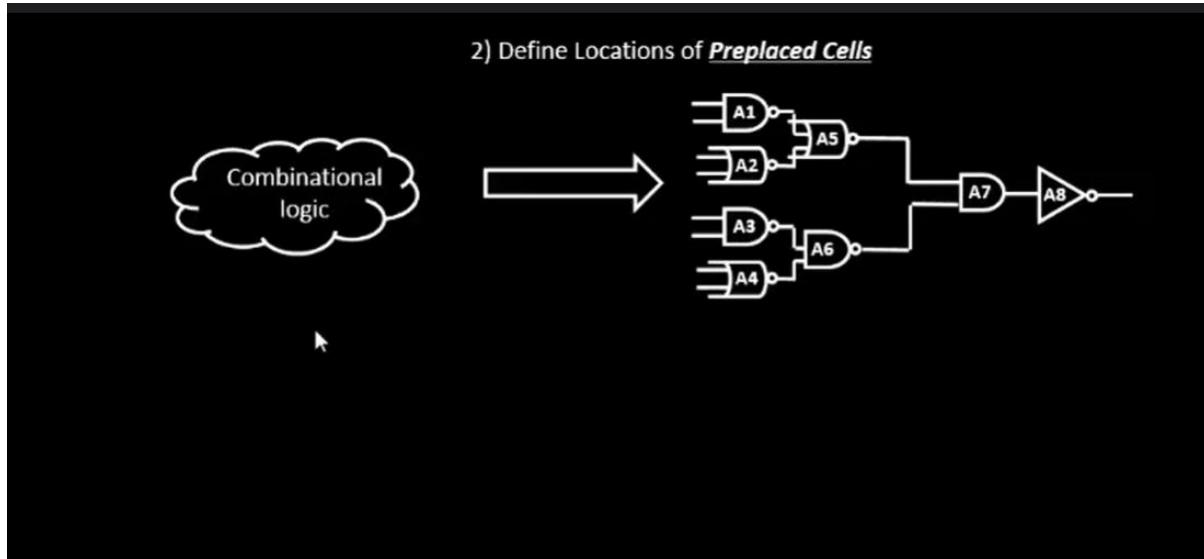
And with the same core as before



Here the utilisation- = 0.5 aspect ratio – 0.5



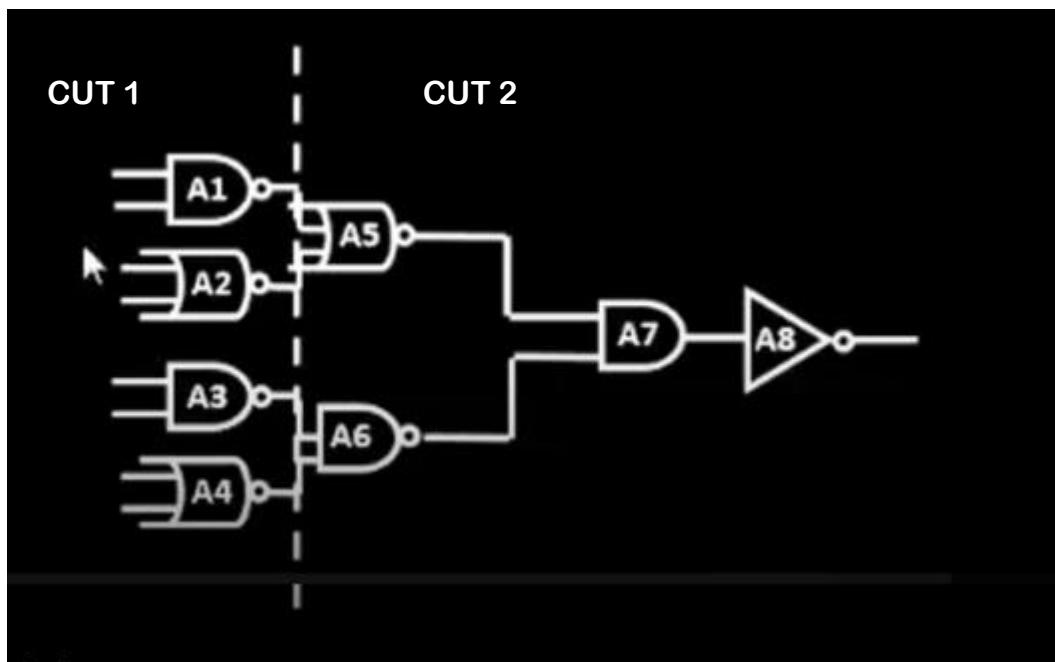
Define locations of pre placed cells

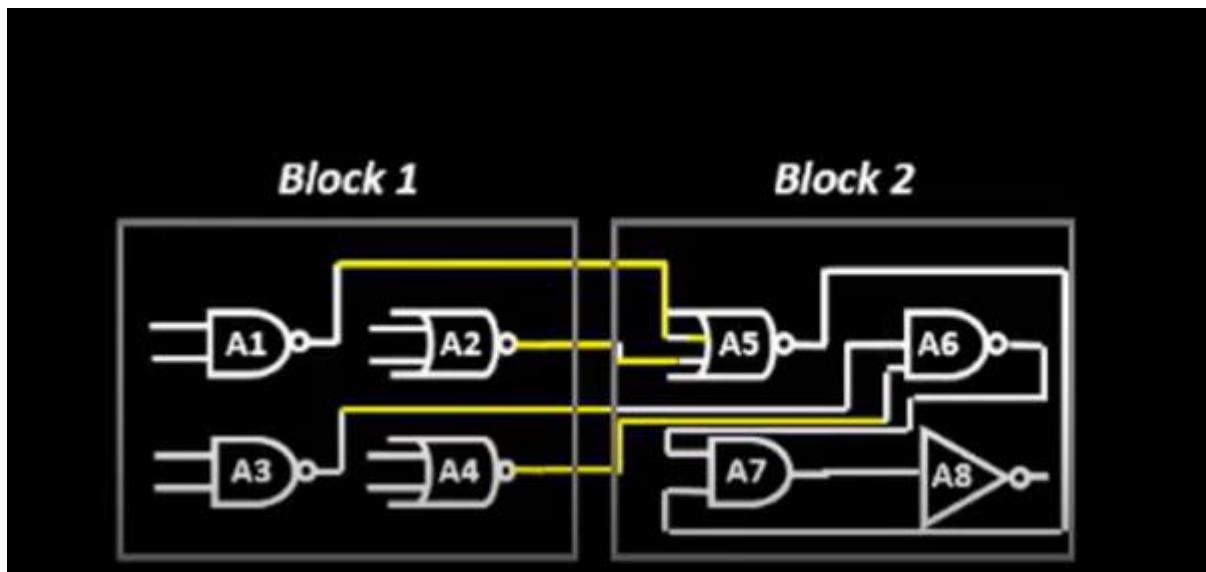


Assumption**

Lets

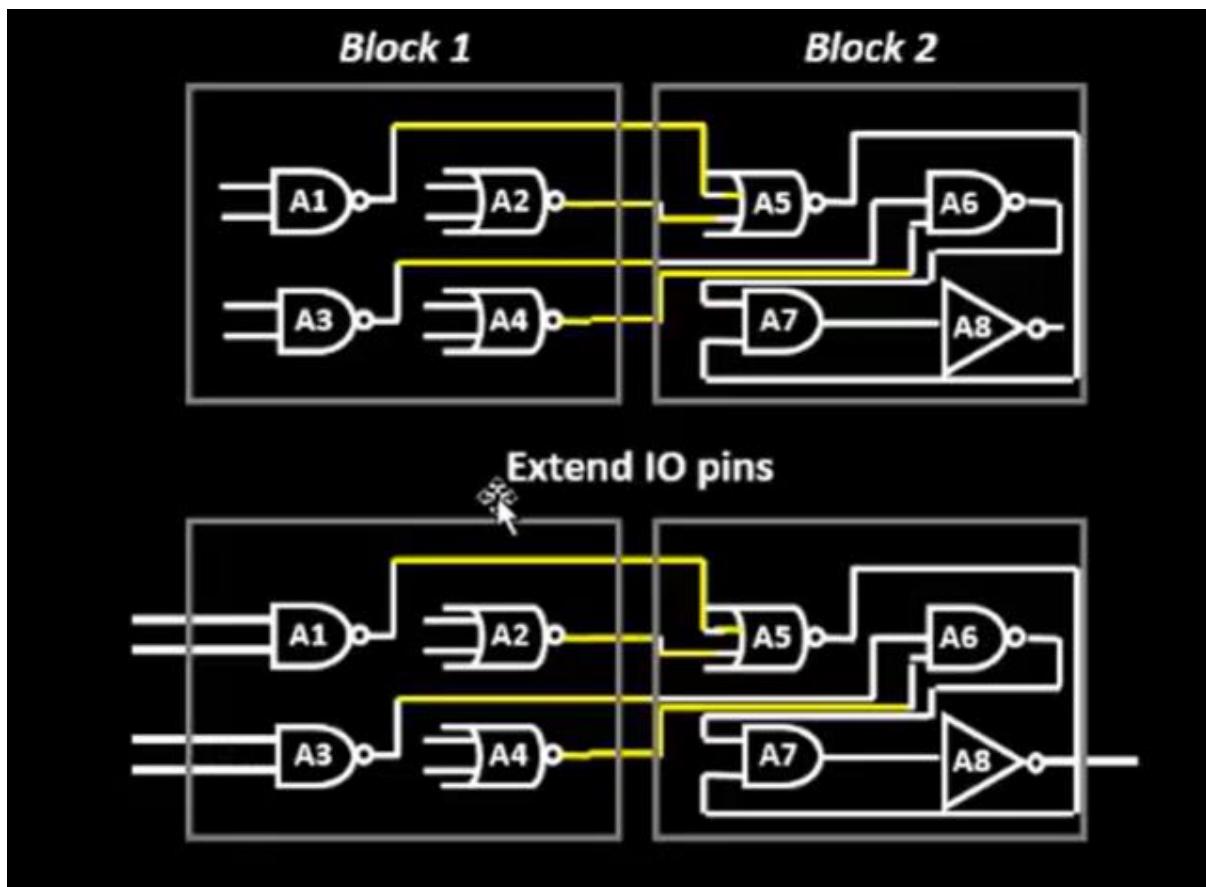
take the part of the circuit out and cut it 😊



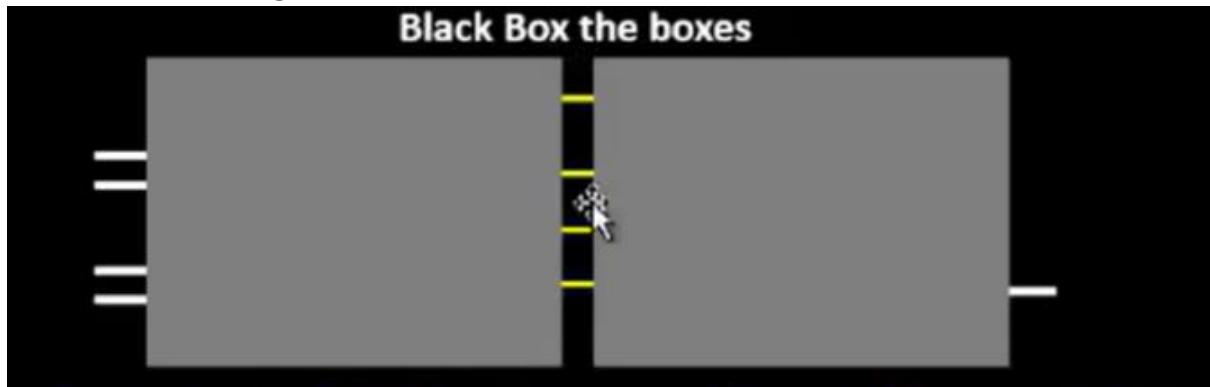


Too somthin like dis

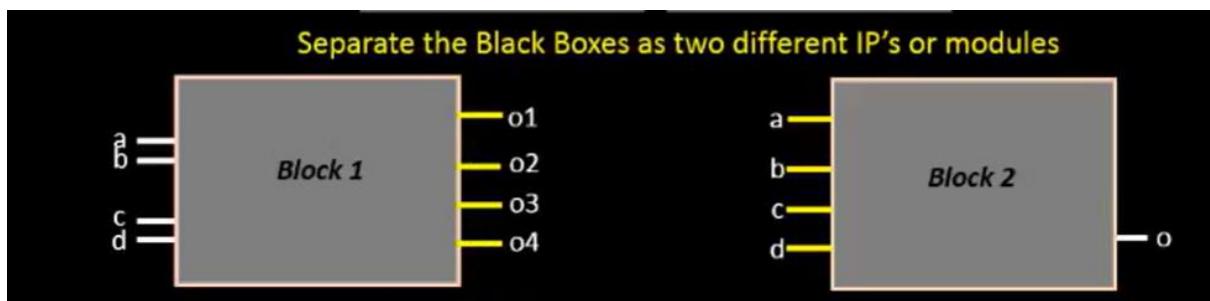
And if we extend the IO pins we get this



After black boxing



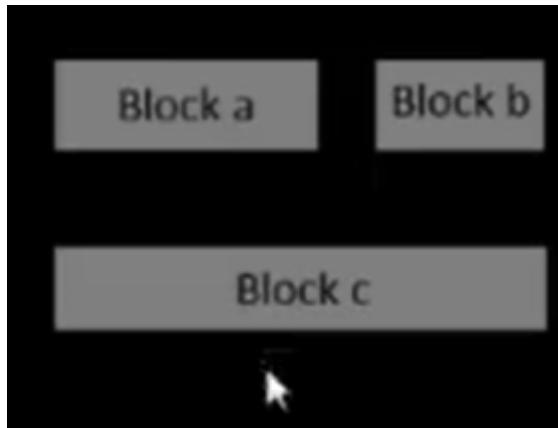
Then splitting them



Then we send these blocks to diff users to implement them

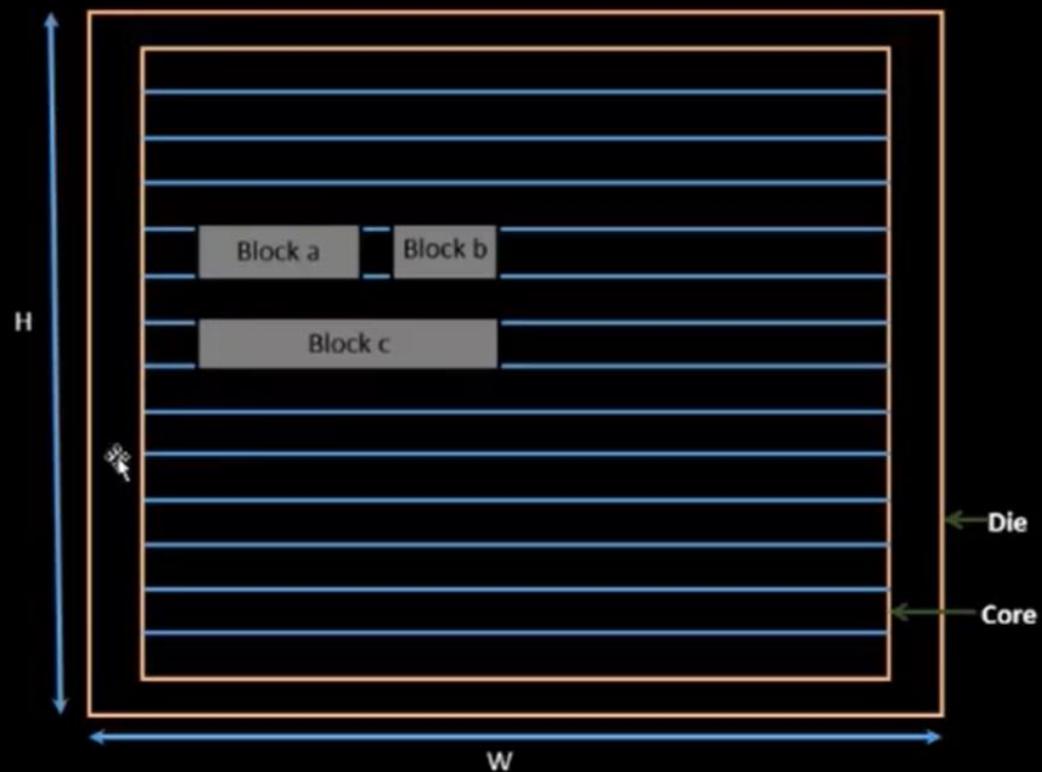
- The arrangements of ip" in a chip is known as floor planning

Now lets take block 1,2,3 to put in a core



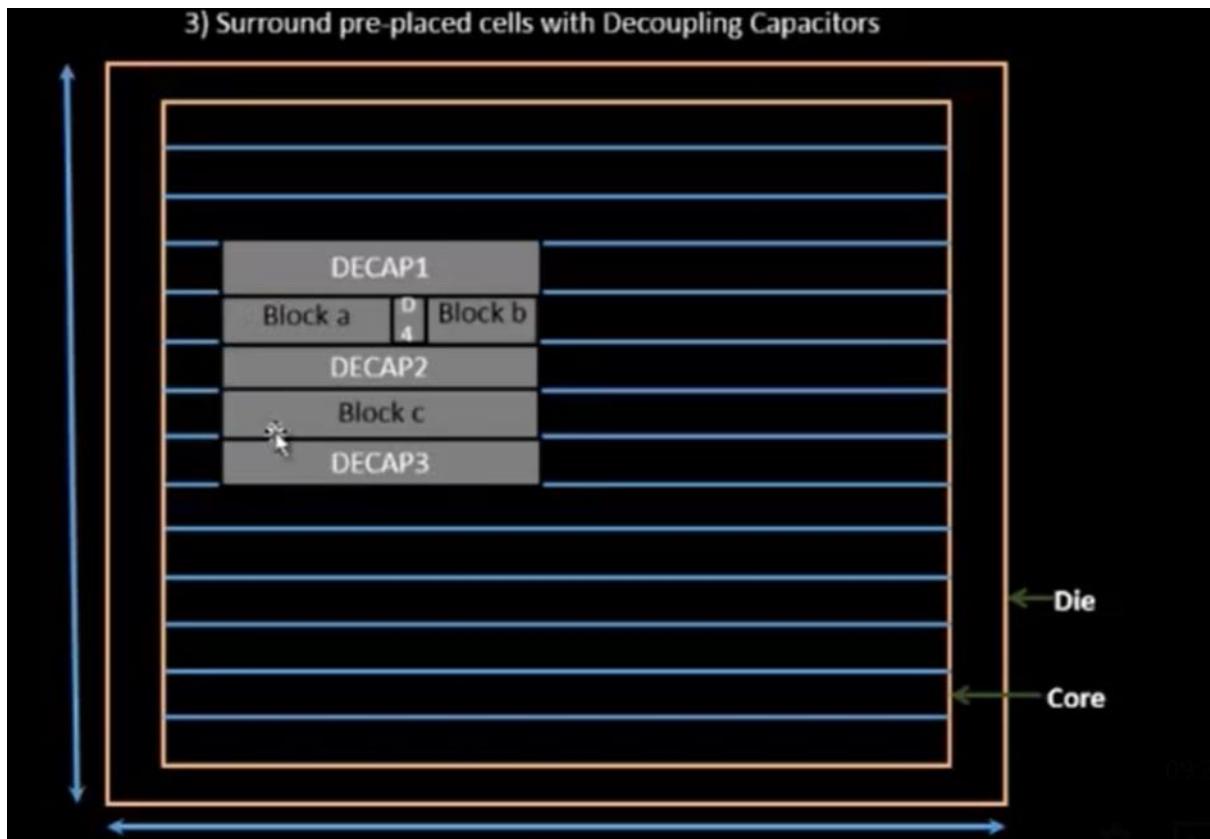
Done 😊

2) Define Locations of Preplaced Cells



Now they r a preplaced cells

Now we have to surround them with decoupling capacitors

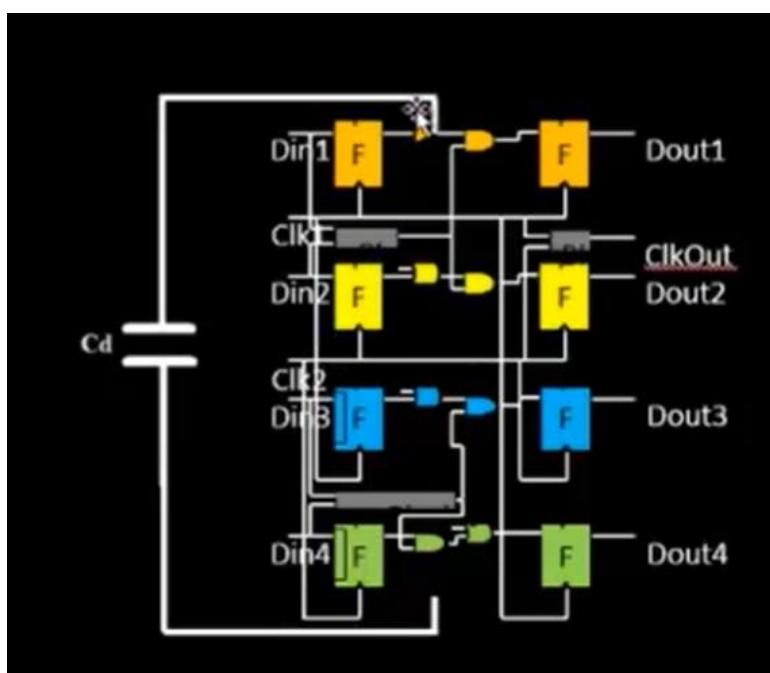


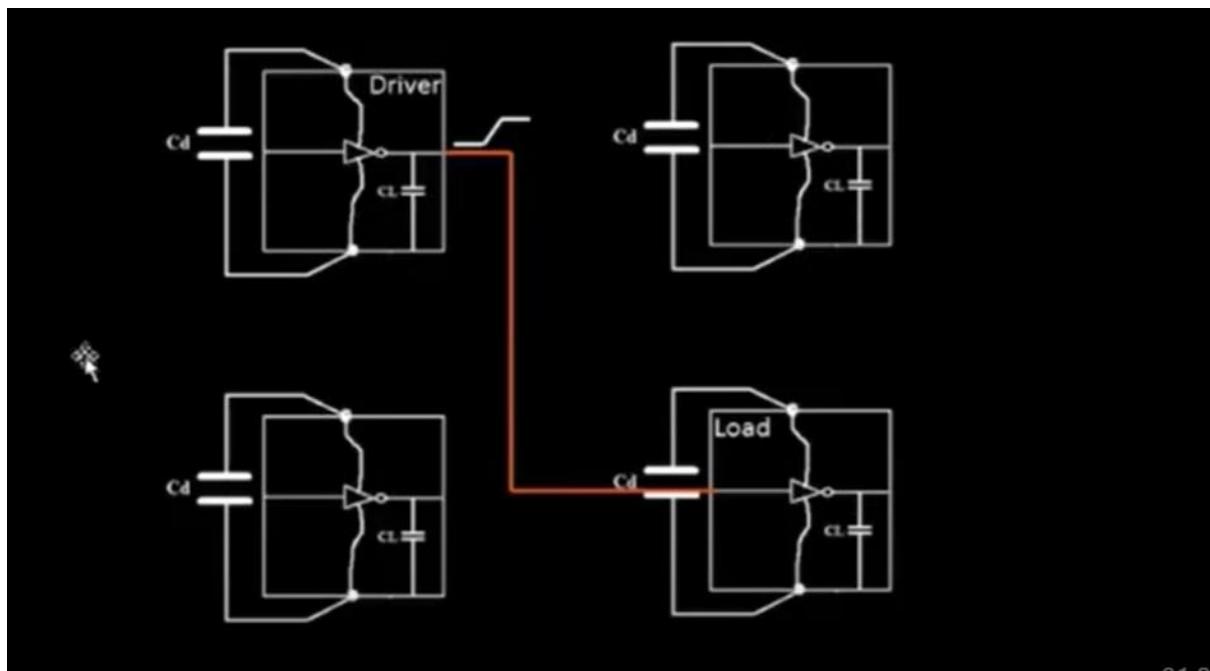
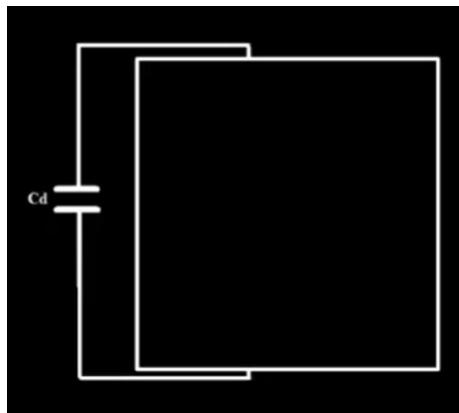
Like this

Their short form is Decap

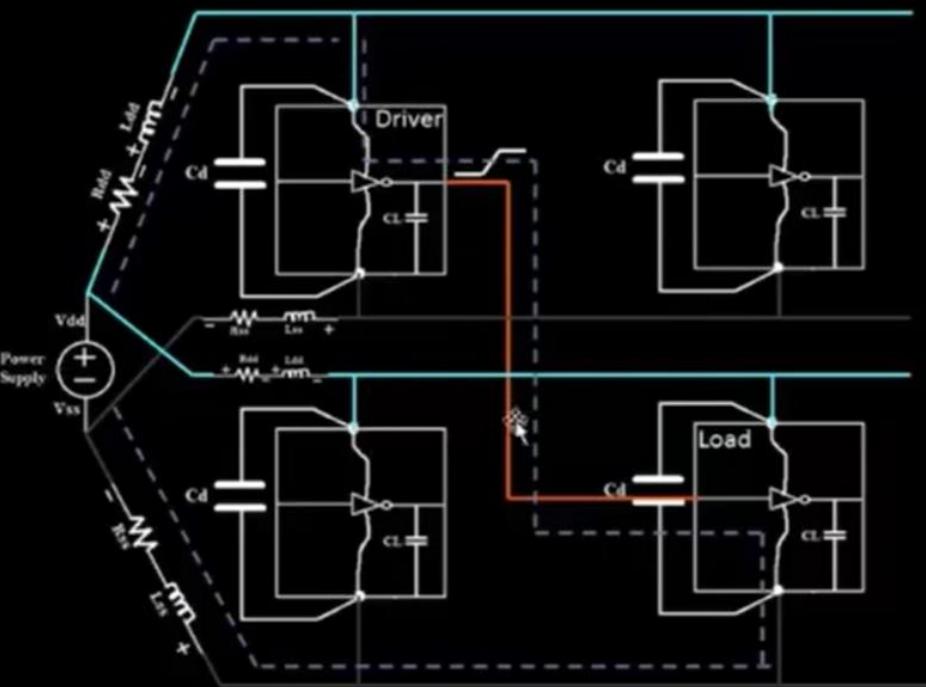
Power planning

Lets take this and turn it into a black box – macro





Lets think the macro has been repeated this many times



Assume, the 'Blue' path is a 16-bit bus

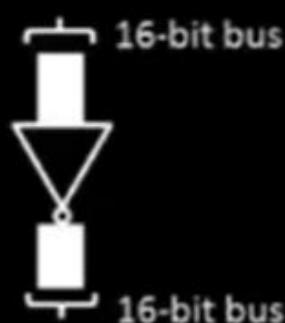
now we do this

Assume the red line as 16 bits

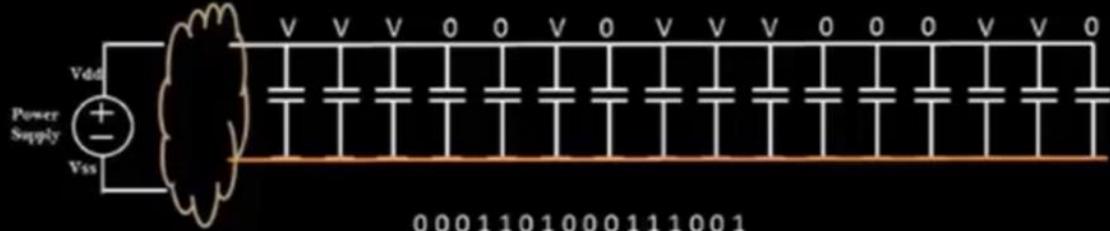
Now lets take the stuff of a 16 bit bus

Now, Lets the output of 16 – bit bus, is connected to an inverter

1 1 1 0 0 1 0 1 1 1 0 0 0 1 1 0

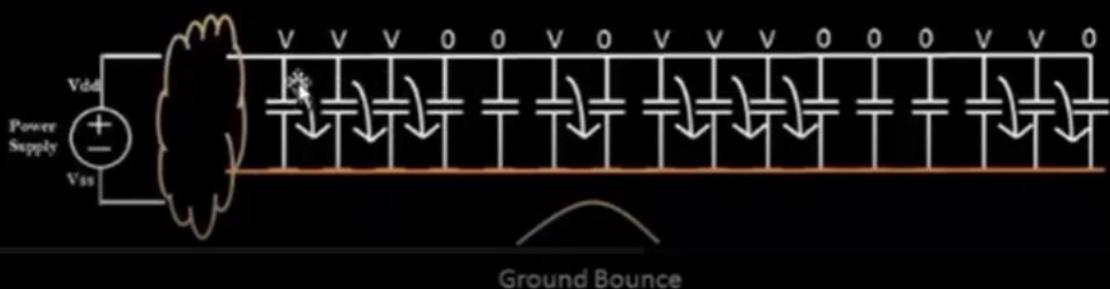


0 0 0 1 1 0 1 0 0 0 1 1 1 0 0 1

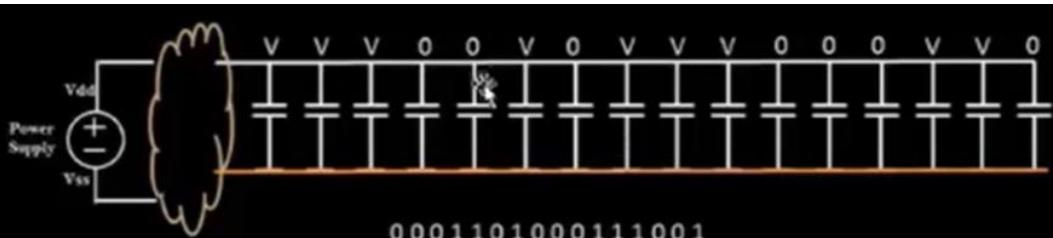


What does this mean?

This means, all capacitors which were charged to 'V' volts will have to discharge to '0' volts through single 'Ground' tap point. This will cause a bump in 'Ground' tap point.

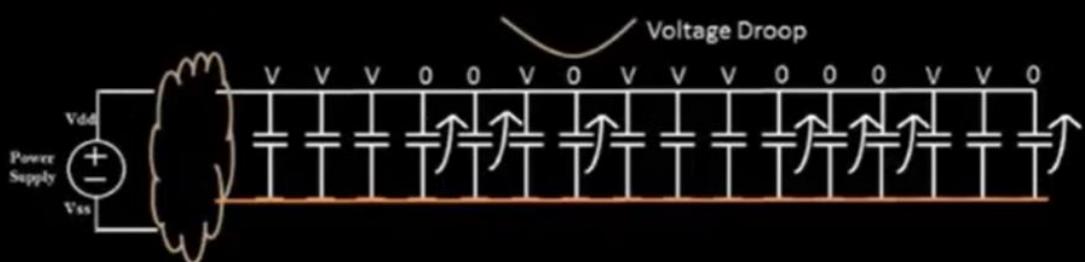


Here so since all of them discharge the energy at the same time a ground bounce will occur in the ground line



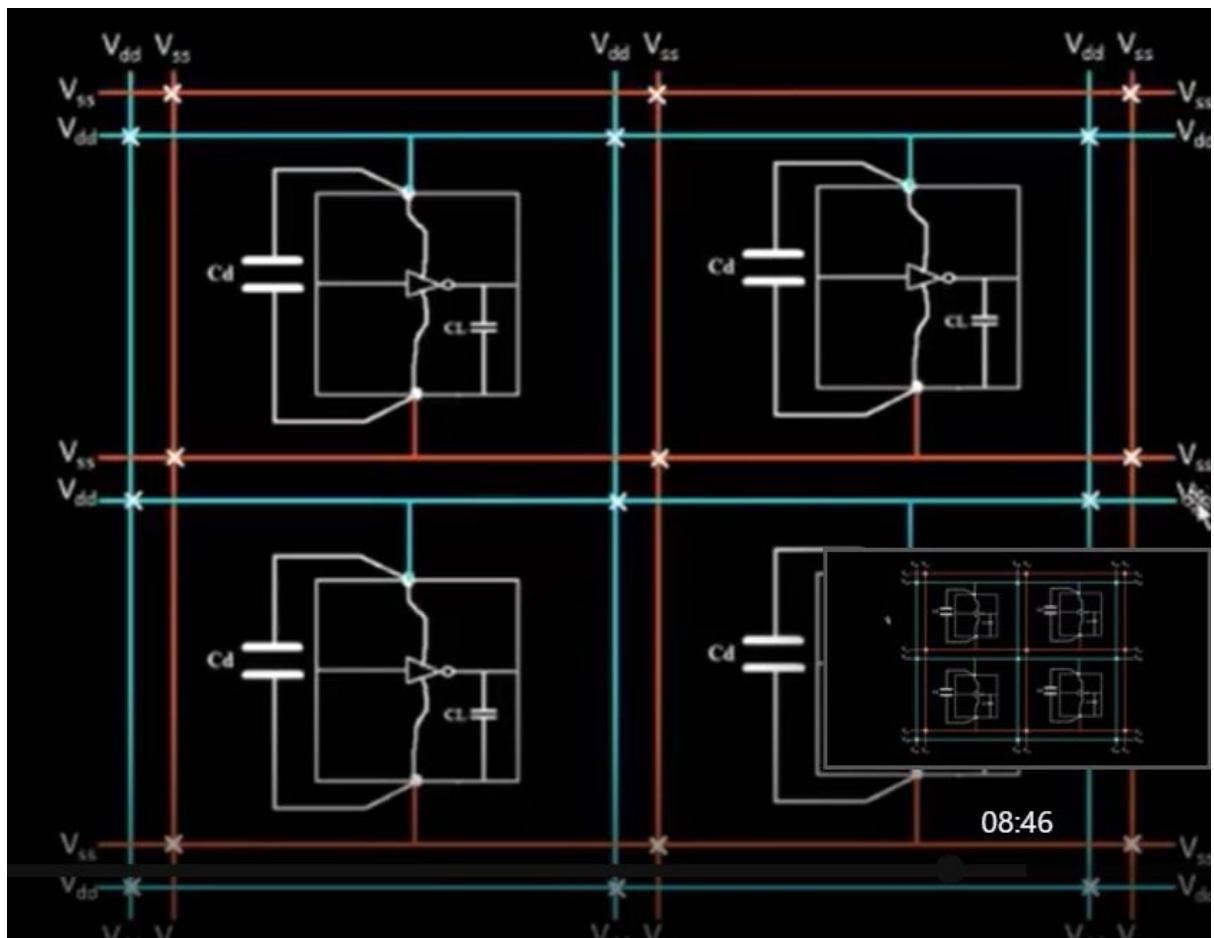
What does this mean?

Also, all capacitors which were '0' volts will have to charge to 'V' volts through single 'Vdd' tap point. This will cause lowering of voltage at 'Vdd' tap point.



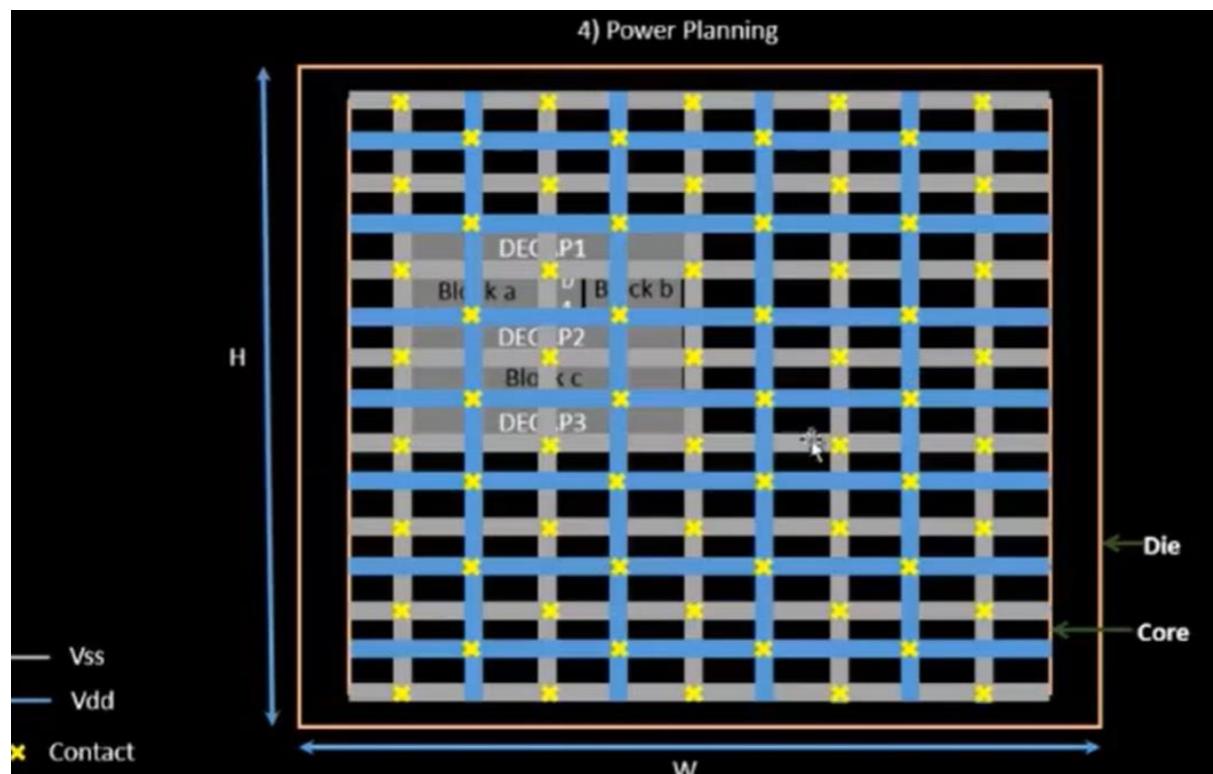
Lets take the opposite here

When all of them drop at the same time a voltage drop occurs

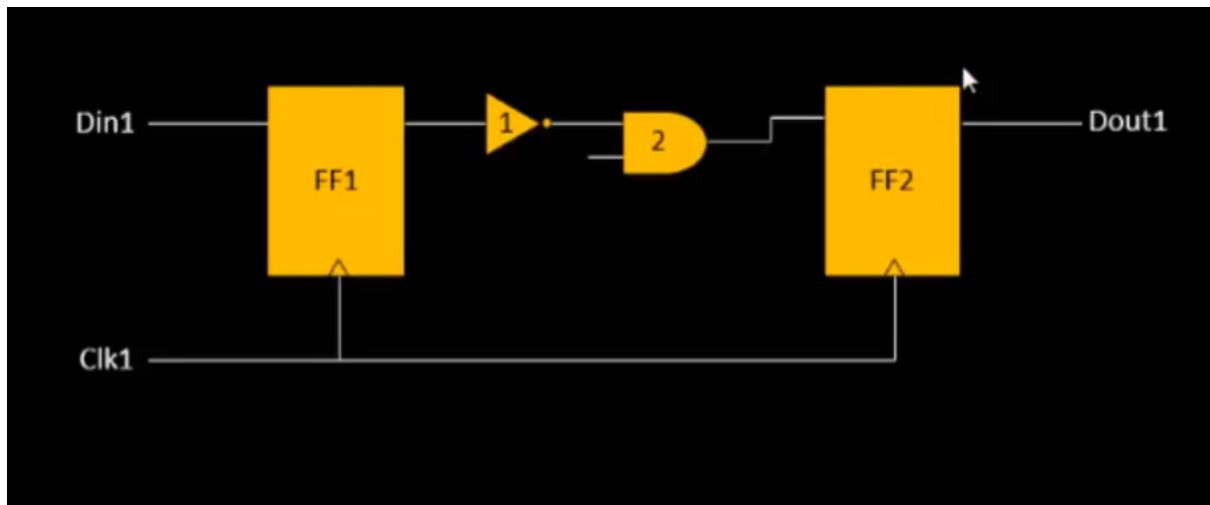


so now we have many power supplies , than the 1st one

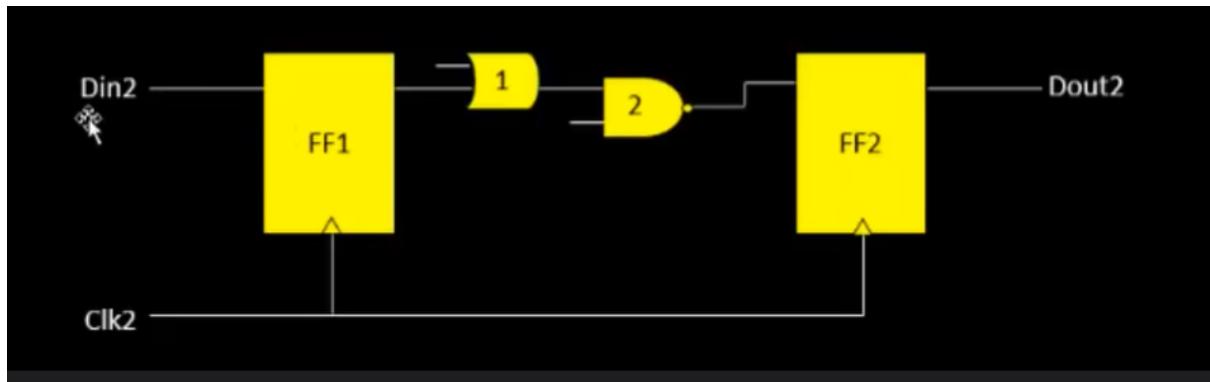
Now if we add the power planning to the die we get this



Next pin placement

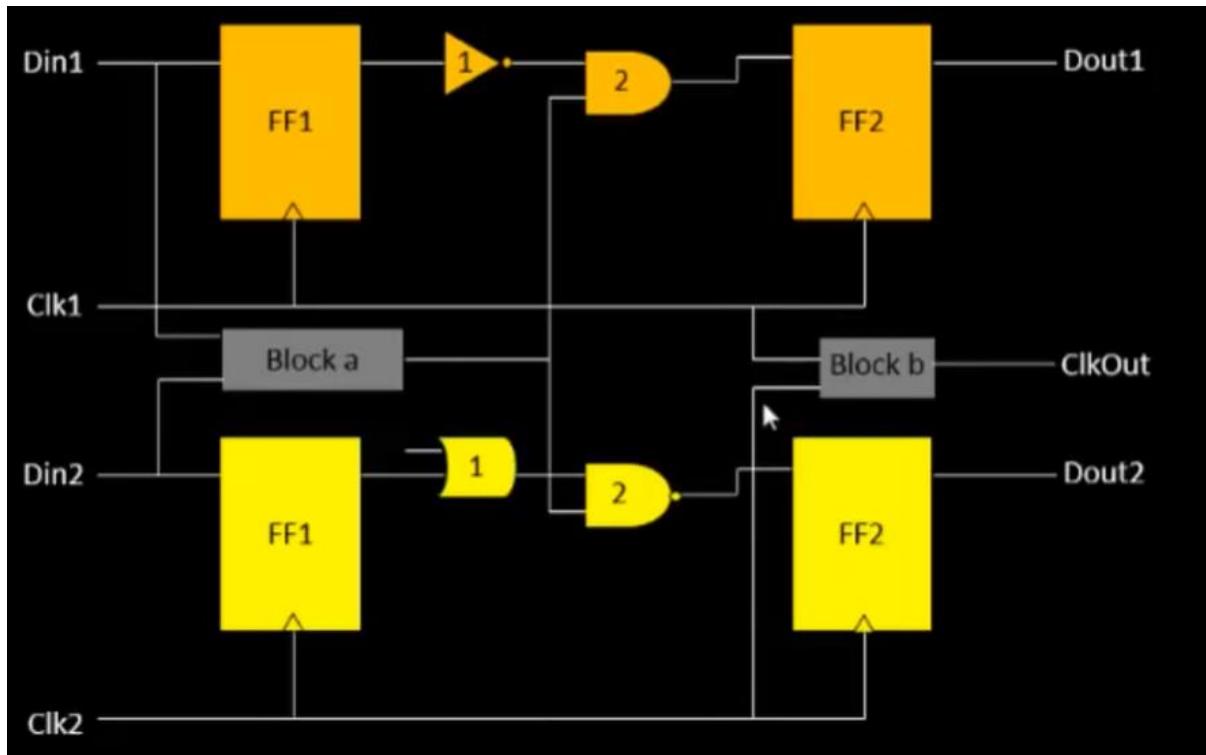


Just an example

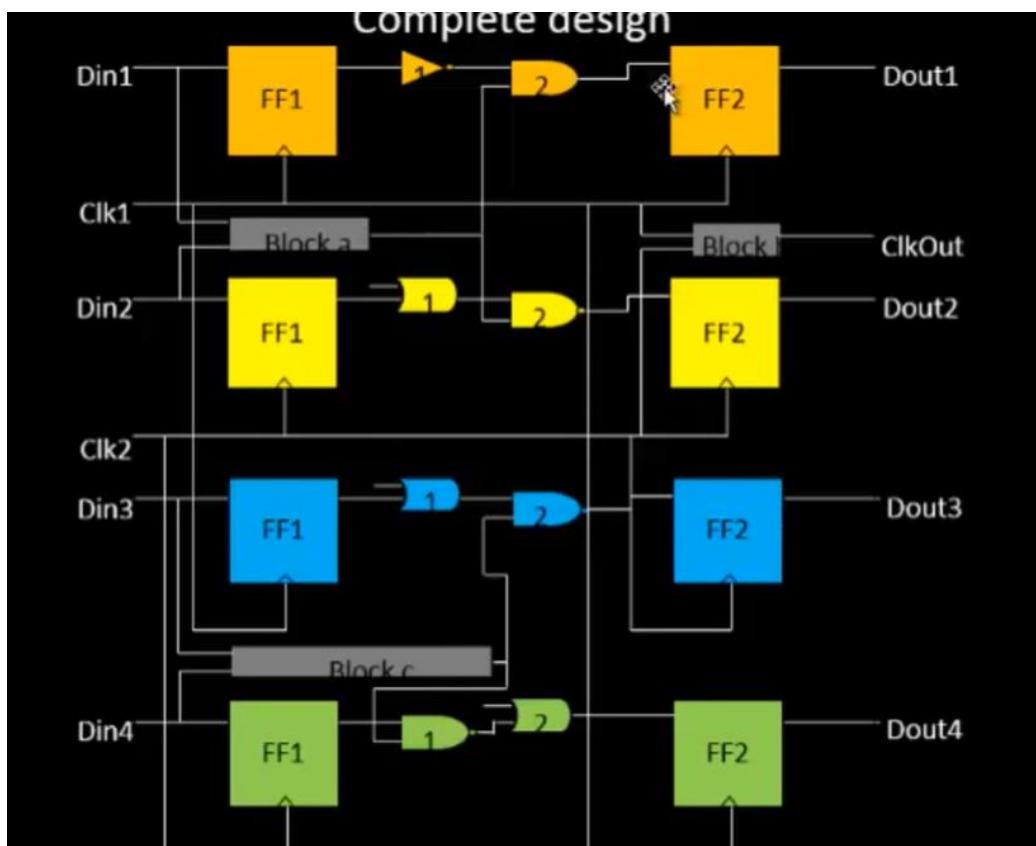


it's the same thing with a diff color

we added a block



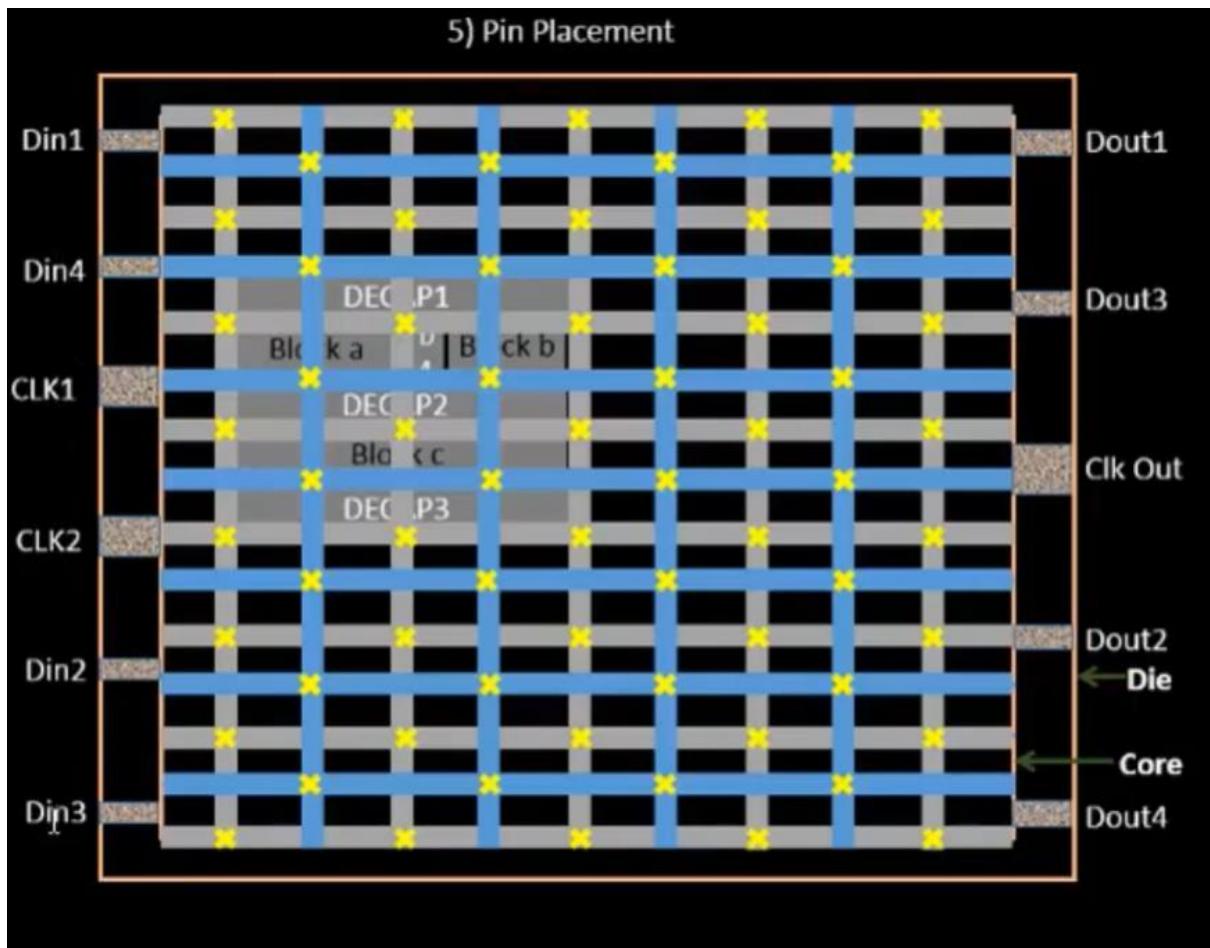
Now we add YET another 2 color circuits AND another block



This is a netlist (we learnt before)

So now lets put the pin information thingy in the die 😊

So the trend is we put the INP in the left side and the OPT in the right side



yay



we will use this for blockage

Now floor plan is ready for placement and routing step

FLOOR PLAN IN OPENLANE

Type **run_floorplan**