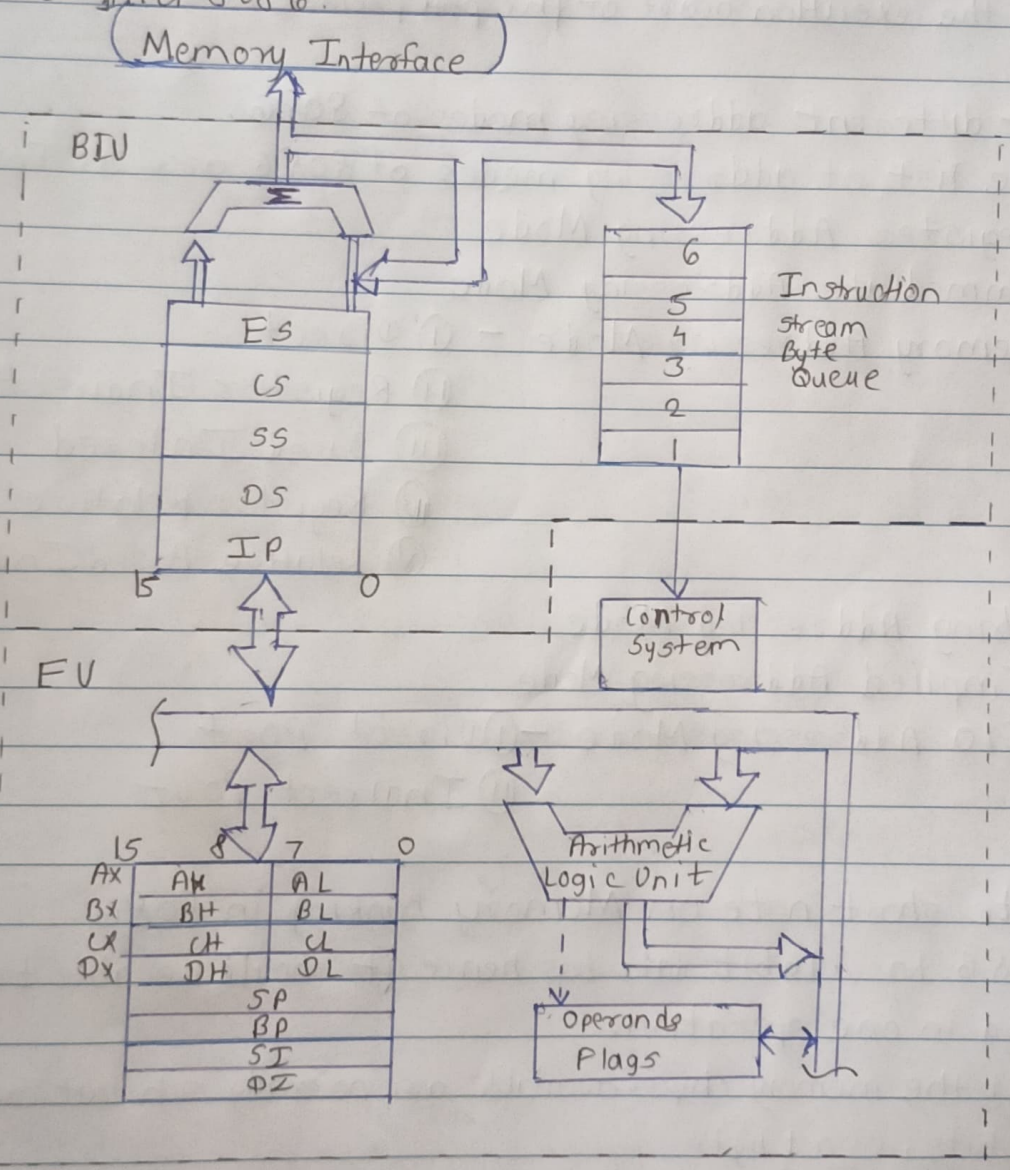
LTCE

Assignment No. 1

Q. 1 Explain Architecture of 8086 in detailed.

→ - The below dia shows the block schematic of the internal structure of Intel 8086.



- As shown in above fig, the 8086 CPU is divided into 2 parts ① The bus interfacing unit (BIU) & ⑪ The execution unit (EU)
- BIU is mainly responsible for external accesses, hence it is called the external world interface of the processor.
- EU is the main processing section of the processor. It is responsible for doing all calculations, arithmetic & logical operations.

It also controls the different operations in the processor.
- EU takes care of performing operations on the data & it is called as the execution heart of the ~~proc~~ processor.

Q. 2 List different addressing modes of 8086.

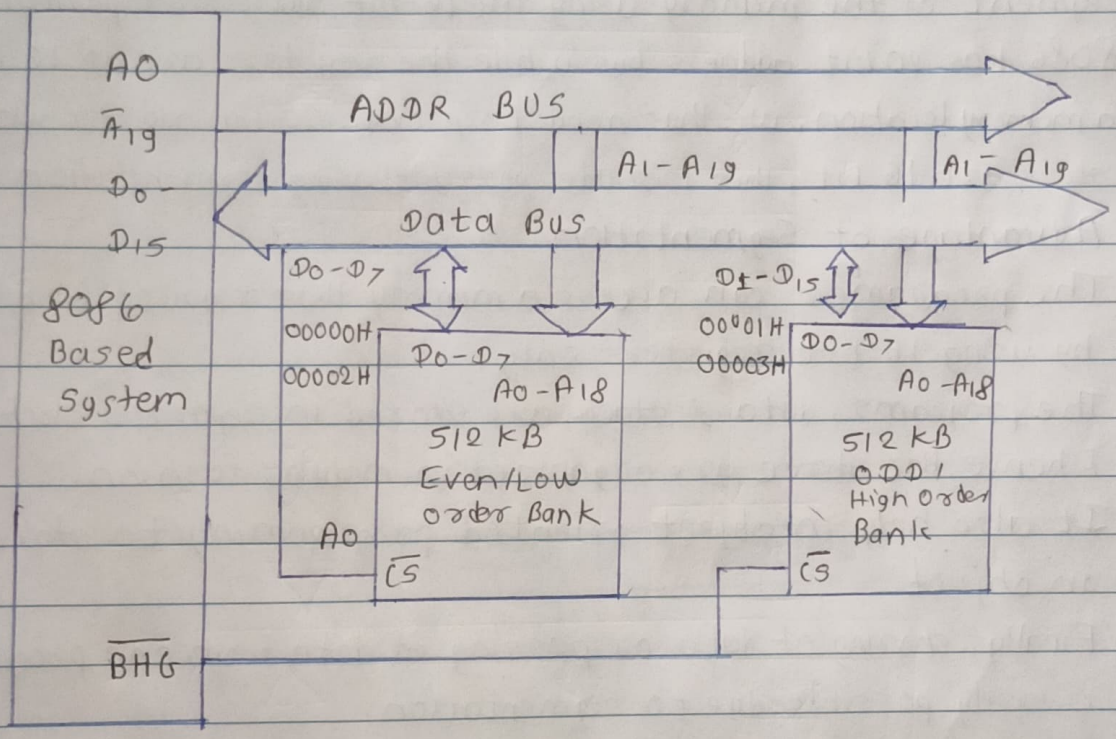
→ The list of addressing modes of 8086 are as follows:

1) Register Addressing Mode
2) Immediate Addressing Mode
3) Memory Addressing Mode – (I) Direct
   (II) Register Indirect
   (III) Based Indexed
   (IV) Register Relative
   (V) Relative Based Indexed
4) String Addressing Mode
5) Implied Addressing Mode
6) I/O Addressing Mode – (I) Direct Port
   (II) Indirect Port

Q. 3 Write short note on Memory banking in 8086.

→ - 8086 has a 16 bit data bus hence it should be able to acess 16-bit data in one operation.
- But the memory chips available are normally such that each location has 8-bits i.e. a 1 byte.
- Hence to read 16-bits it need to acess 2 memory locations.
- However, if both these memory locations are in same memory chip then the address bus will have to provide two addresses sequentially & will require double the time also 16-bits would not be accessed simultaneously
- To solve this problem, the memory of 8086 is divided into 2 banks each bank provides 8-bits.

- One bank contains all even addresses called the "Even Bank", whil the other is called "odd Bank" containing all odd addresses.
- The below fig's shows the different accesses posible for 8086. They are explained below.



Memory Location	Address	Data type	BHE	A0	Bus cycles	Data Lines Used
Even	00000	Byte	1	0	One	$D_0 - D_7$
Even	00000	Word	0	0	One	$D_0 - D_{15}$
odd	00001	Byte	0	1	One	$D_8 - D_{15}$
odd	00001	Word	0	1	First	$D_0 - D_7$
			1	0	Second	$D_8 - D_{15}$

Q.4 What is memory segmentation? State the advantage of memory segmentation.

→ - Segmentation in 8086 refers to division of the 1MB main memory into segments or blocks of 64 KB each. This is done so as to acess a segment of the memory using the 16-bit address or pointer registers.
- 8086 has 20 bit address bus while the registers are of 16-bit. To access a memory location, we thus need to provide 20-bit address while the registers are 16-bit, this is made possible using segmentation.

Advantages of Segmentation

1) The programmer can access a memory that required 20-bit address, by using 16-bit registers only.
2) The programs, data & stack are stored in separate blocks in memory & hence the three are organized in modular fashion.
3) It also help in object oriented programming to store data of an object.
4) Finally, sharing of data or passing of data from one program to another is easily possible due to segmentation.
5) Also the segmentation makes data relocatable as the program uses only offset register pointer while the segment points to the base of segment.

Q.5 Explain power ON reset circuit used in 8086 system.

Q.6 Draw the timing dia of memory read in minimum mode.

→ -The sequence of operations during the read machine cycle are as follows -
1): The 8086 will make $M/\overline{IO} = 1$ if the read is from memory & $M/\overline{IO} = 0$ if the read is from the I/O device.
2): At about the same time the ALE o/p is asserted to 1.
3): Make $\overline{BHE}$ low/high & send out the desired address on AD_0 to AD_{15} & A_{16} to A_{19} lines.

4): Pull down ALE. The address is latched into external latch.

5): Remove the address from AD_0 to AD_{15} lines & put them in the input mode.

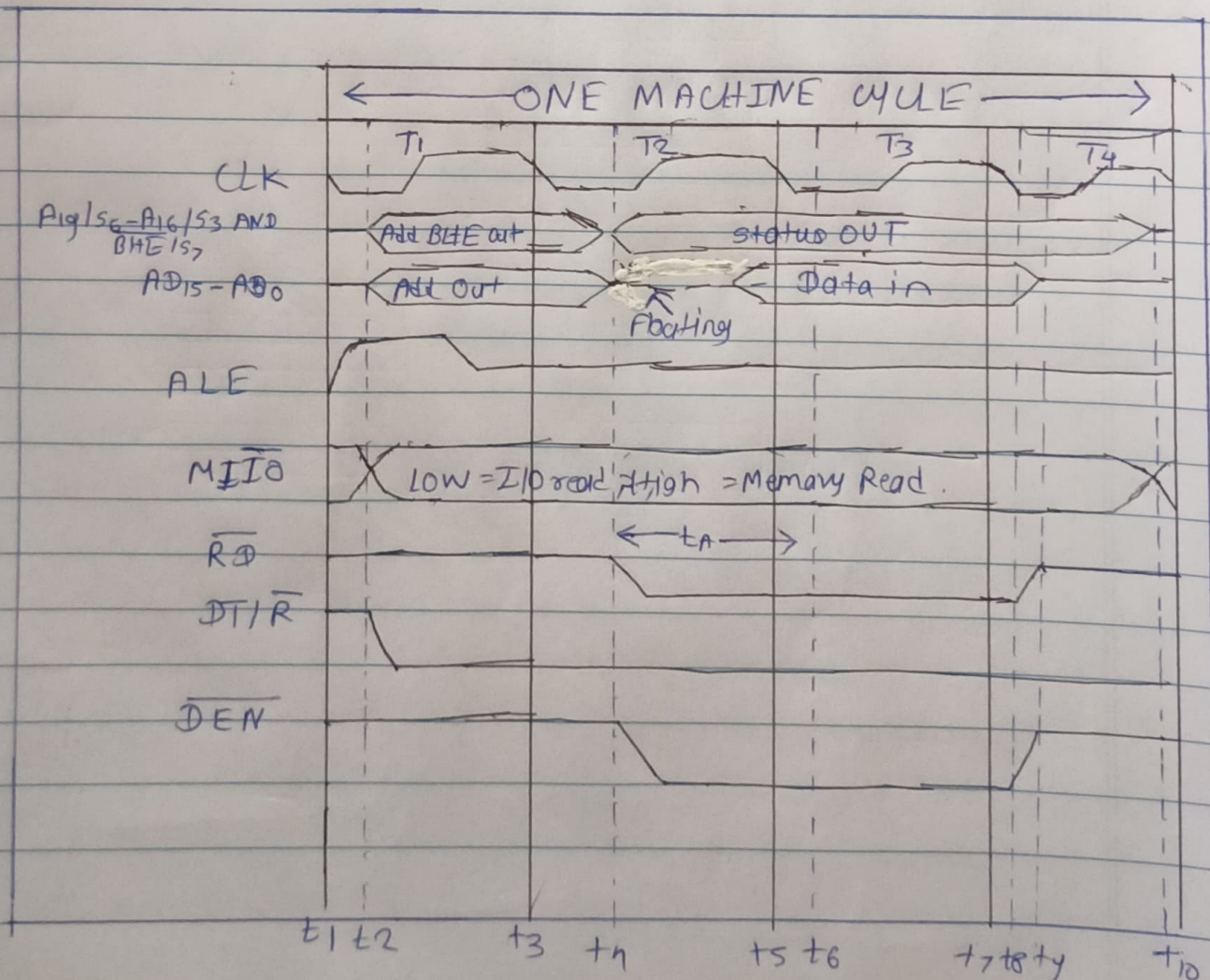
6): Assert the $\overline{RD}$ signal low. This will put the data from the addressed memory location or I/O port to the data bus.

7): Insert the "Wait" T-state if the 8086 READY input is made low before or during the T_2 state of a machine cycle.

8): As soon as ready input goes high, 8086 comes out of the wait T-states & complete the machine cycle.

9): Calculate the "READ" cycle by making the $\overline{RD}$ line high.

10): For larger systems we need to use the data buffers. Then the $DT/\overline{R}$ & $\overline{DEN}$ signals of 8086 are connected to 8086 & enabled at the appropriate time.

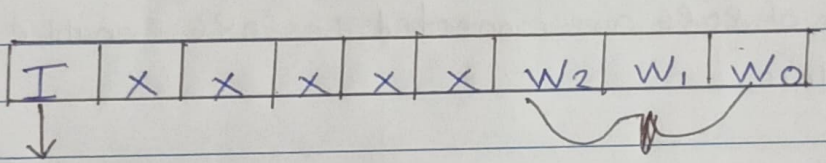


Q.7 Explain operating modes in 8259

→ 8259 has 2 operating modes viz. interrupt driven & polling mode. In interrupt driven mode, 8259 interrupts the processor with the INT pin whenever it gets an interrupt.

Polled mode -

- In this mode the INT o/p is not used. The microprocessor checks the status of the interrupt request by issuing poll command.
- The microprocessor reads contents of 8259A after issuing poll command
- During the read operation the 8259A provides polled word & sets the InSR bit of highest active interrupt request in following format.



I = One or more interrupt request is activated

Binary code of highest active priority

I = 0 No interrupt request activated interrupt request.

Q.8 Explain with block dia working of 8255 PPI

→ The architecture of 8255 can be divided into following parts.

1) Data Bus Buffer - This is an 8-bit bi-directional buffer used to interface the internal data bus of 8255 with the external data bus.
- The CPU Transfers data to & from the 8255 through this buffer.

2) Read/Write Control Logic - It accepts address & control signals from µP
- The control signals determine whether it is a read or write program & also select or reset the 8255 chip.
- The address bits (A1, A0) are used to select the ports or the control word register are as follows:

A1	A0	Selection	Sample address
0	0	Port A	80H (1000 0000)
0	1	Port B	81H (1000 0001)
1	0	Port C	82H (1000 0010)
1	1	Control Word	83H (1000 0011)

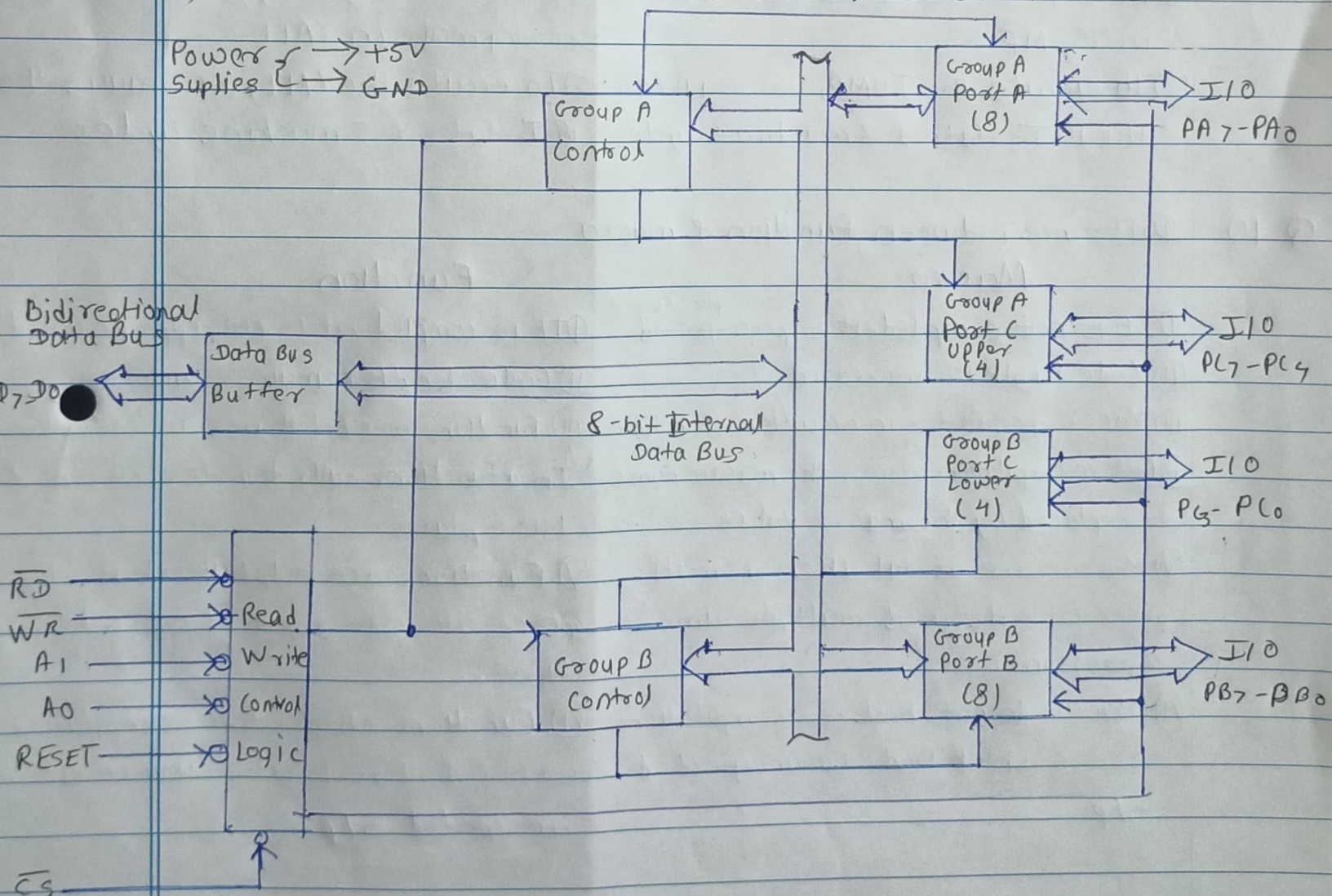
- The ports are controlled by their respective group control register.

3) Group A Control - This control block contains port A & C (i.e PC7-PC4

- It accepts control signals from the control word & forward them to respective ports.

4) Group B Control - This control block control port B & Lower, i.e. PC3-PC0

5) Port A, Port B, Port C - These are 8 bit bi-directional Ports.



Q.9 Difference between Jump & call instruction.

Jump	Call
① It is not mandatory to initialize the stack pointer in Jump instruction.	① It is mandatory to initialize the stack pointer in CALL instruction.
② In the JUMP, the value of SP does not change	② In the CALL, the value of SP is decremented by 2.
③ The JUMP is not used to transfer the value of PC into stack.	③ It is used to transfer the value of PC into a subroutine so that it can come back to main program.
④ There is an immediate addressing mode in JUMP	④ There is a register, immediate addressing mode in CALL.
⑤ To execute the JUMP, we require the 10 T-state & 3 machine cycles.	⑤ To excute the CALL, we require the 18 T-states & 5 machine cycles.

Q. 10 Difference between function & macro

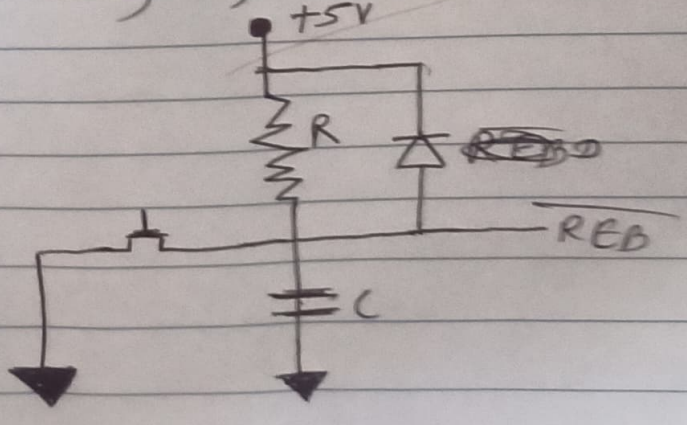
Macro	Function
(I) It is not compiled, it is pre-passed processed.	(I) It is compiled, it is not a pre-processed.
(II) Code length is increased.	(II) Code length remains same.
(III) Macros are faster in execution than function	(III) Functions are bit slower in execution.
(IV) Before compilation process the macro name is replaced by the macro value.	(IV) In a function call, transfer of control take place.
(V) Macros are useful when a small piece of code used maltiple times in a program.	(V) Functions are helpfull when a large piece of code repeated no. of times.
(VI) Macros do not check for compilation error which leads to unexpected o/p	(VI) Function checks for compilation error & there is a less chance of unexpected o/p

Q.5→ ① Pin 17, 16, 15 -
- These are the i/p lines of 8284. X1 & X2 are the i/p b/w which the crystal is actually connected.
- TNK stands for tank. These 3 i/p are interfaced to the internal oscilator of 8284.

②

Q.5→ - When power supply is switched on, there are some spikes in its o/p for some time.
- These spikes cause change in the default values of the register.
- The default value of all the registers of 8086 is 0000 H except for CS is FFFF H.
- Hence the address of the first instruction fetched by the processor is FFFF0H.
- The change in these register values alter the behaviour of the processor, espacially is CS or IP change.
- This makes it necessary to implement power on reset circuit, which should reset the processor during these spikes & maintain register to their default values.

*Operations on power on reset circuit -
- The following fig illustrates power-on-reset circuit.



- Initially the capacitor has no ~~charge~~ charge across it, when system is switched on.
- Hence it provides logic 0 on $\overline{RES}$ pin & reset is activated.
- Slowly the capacitor is charged through the resistor & makes the reset pin to logic '1'. The charging time of capacitor is such that by this time the spikes of power supply are vanished.
- This disables the reset & the processor switches on.
- The diode is connected across the resistor to discharge the capacitor rapidly when power supply is switched off.
- The switch is for manual reset to discharge the capacitor by connecting it to ground.