BOOLEAN_FUNCTION_MINIMIZATION

AIM:

To implement the given logic function verify its operation in Quartus using Verilog programming.

F1= A'B'C'D'+AC'D'+B'CD'+A'BCD+BC'D

F2=xy'z+x'y'z+w'xy+wx'y+wxy

Equipment Required:

Hardware – PCs, Cyclone II , USB flasher

Software – Quartus prime

Theory

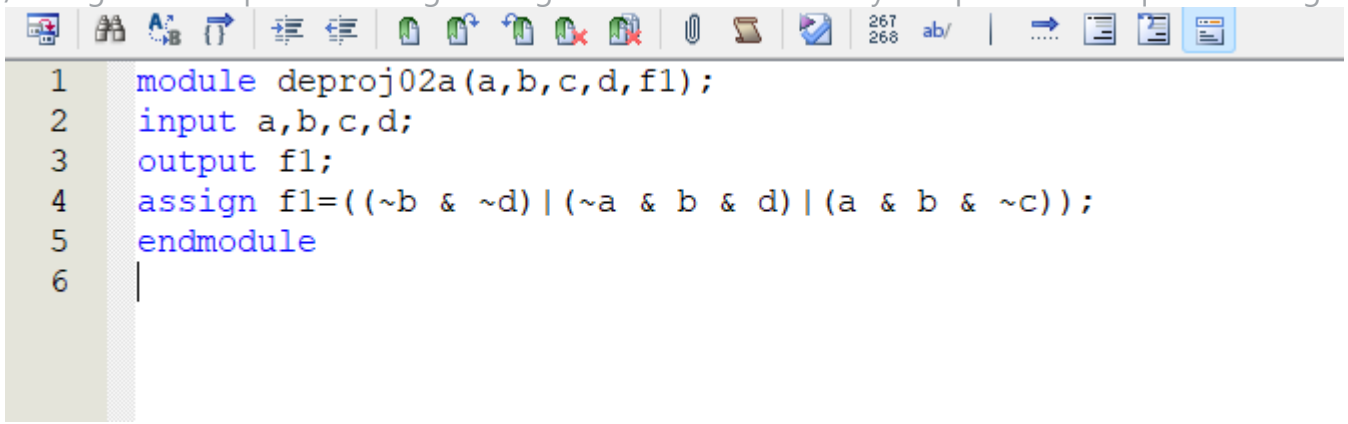
Logic Diagram

Procedure

1. Type the program in Quartus software.
2. Compile and run the program.
3. Generate the RTL schematic and save the logic diagram.
4. Create nodes for inputs and outputs to generate the timing diagram.
5. For different input combinations generate the timing diagram.

Program:

/* Program to implement the given logic function and to verify its operations in quartus using Verilog programming.



```
1  module deproj02a(a,b,c,d,f1);
2  input a,b,c,d;
3  output f1;
4  assign f1=((~b & ~d)|(~a & b & d)|(a & b & ~c));
5  endmodule
6
```

Quartus II 64-Bit - C:/altera/13.0sp2/boolean - boolean

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boolean

db/boolean.v

Compilation Report - boolean

```
1  module boolean(w,x,y,z,f2);
2  input w,x,y,z;
3  output f2;
4  assign f2=((~y&z)|(x&y)|(w&y));
5  endmodule
6
```

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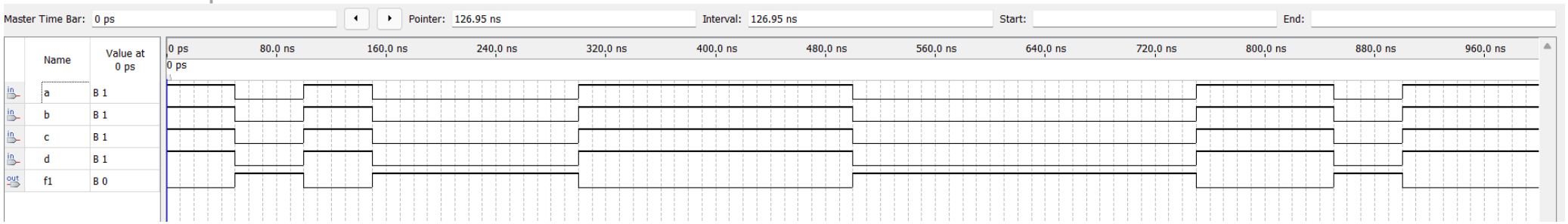
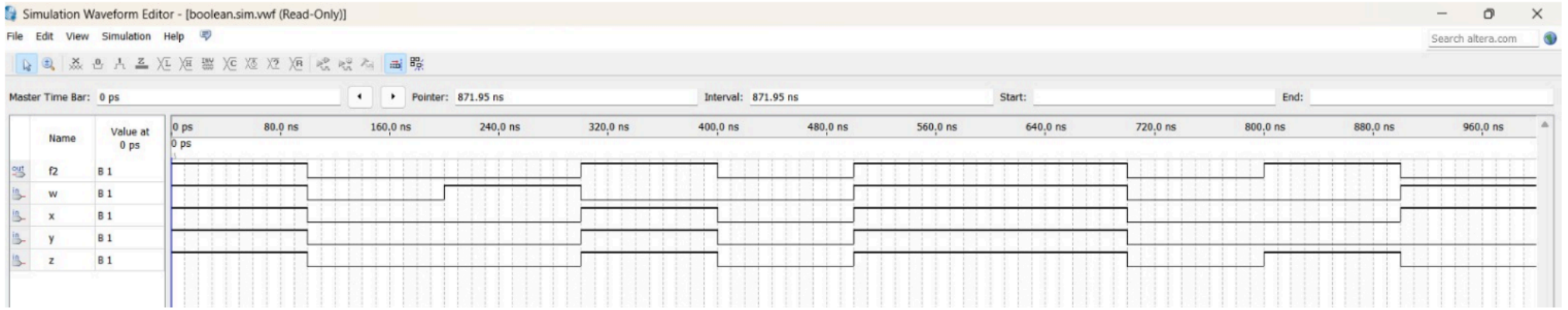
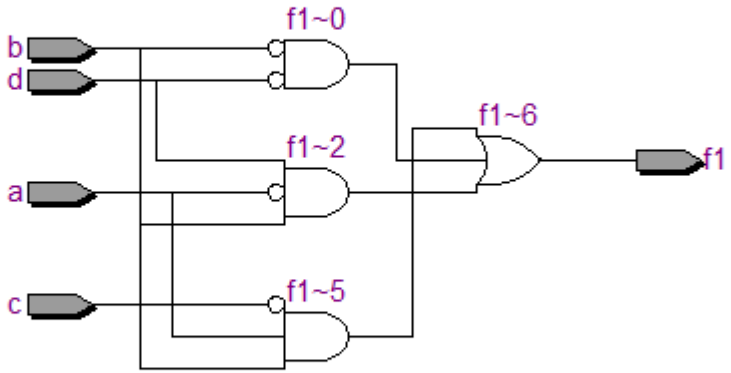
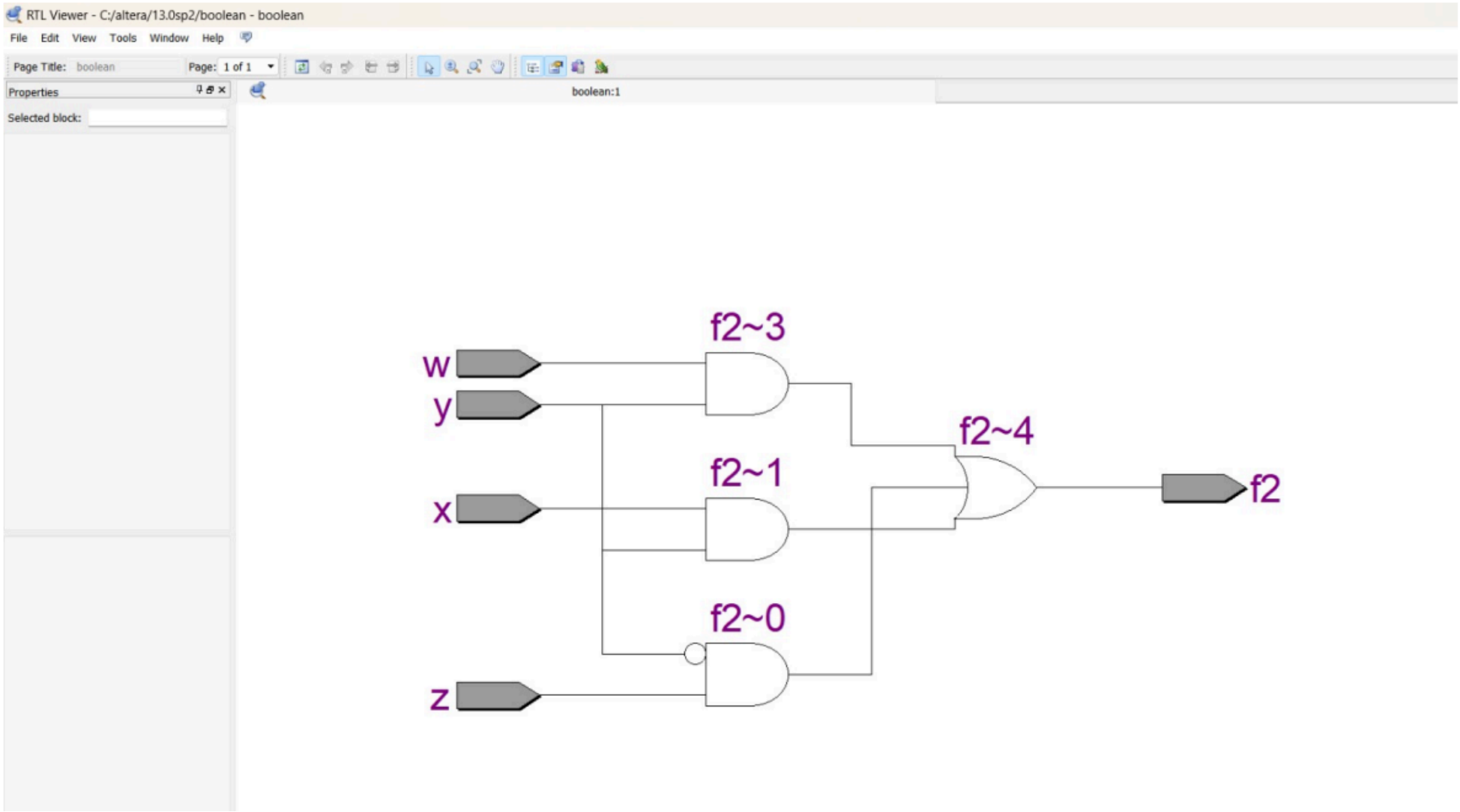
RTL realization output





RTL


f1~0
b
d
f1~6
f1~2
f1
a
c
f1~5


RTL Viewer - C:/altera/13.0sp2/boolean - boolean
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Page Title: boolean
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Properties
Selected block:
boolean:1
f2~3
w
y
f2~4
f2~1
x
f2
f2~0
z

Truth Table

A	B	C	D	A`B`C`D`	AC`D`	B`CD`	A`BCD	BC`D	F1
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	0	0	0
0	1	1	1	0	0	0	1	0	1
1	0	0	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	1
1	0	1	1	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0	1
1	1	0	1	0	0	0	0	1	1
1	1	1	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

W	X	Y	Z	XY`Z	X`Y`Z	W`XY	WX`Y	WXY	F2
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	1
0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	0	1	0	0	1
0	1	1	1	0	0	1	0	0	1
1	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	1	0	1
1	0	1	1	0	0	0	1	0	1
1	1	0	0	0	1	0	0	0	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	0	0	0	0	1	1
1	1	1	1	0	0	0	0	1	1

Result: The implement of the given logic functionand to verify its operation in Quartus using Verilog programming .
Thus the given logic functions are implemented using and their operations are verified using Verilog programm