ENCODER 8TO3 DATAFLOW Modelling

AIM:

To implement Encoder 8 To 3 in Dataflow Modelling using verilog and validating their functionality using their functional tables

SOFTWARE REQUIRED: Quartus prime

THEORY

Encoder 8 To 3

The 8 to 3 line Encoder is also known as Octal to Binary Encoder. In 8 to 3 line encoder, there is a total of eight inputs, i.e., D0, D1, D2, D3, D4, D5, D6, and D7 and three outputs, i.e., A0, A1, and A2. In 8-input lines, one input-line is set to true at a time to get the respective binary code in the output side. Below are the block diagram and the truth table of the 8 to 3 line encoder.
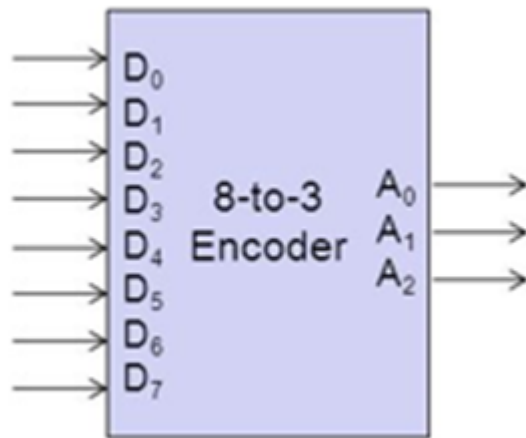

Figure 01 Block Diagram of Encoder 8 * 3

Truth Table

			inputs						outputs	
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

The logical expression of the term A0, A1, and A2 are as follows:

A0 = D1 + D3 + D5 + D7

A1 = D2 + D3 + D6 + D7

A2 = D4 + D5 + D6 + D7

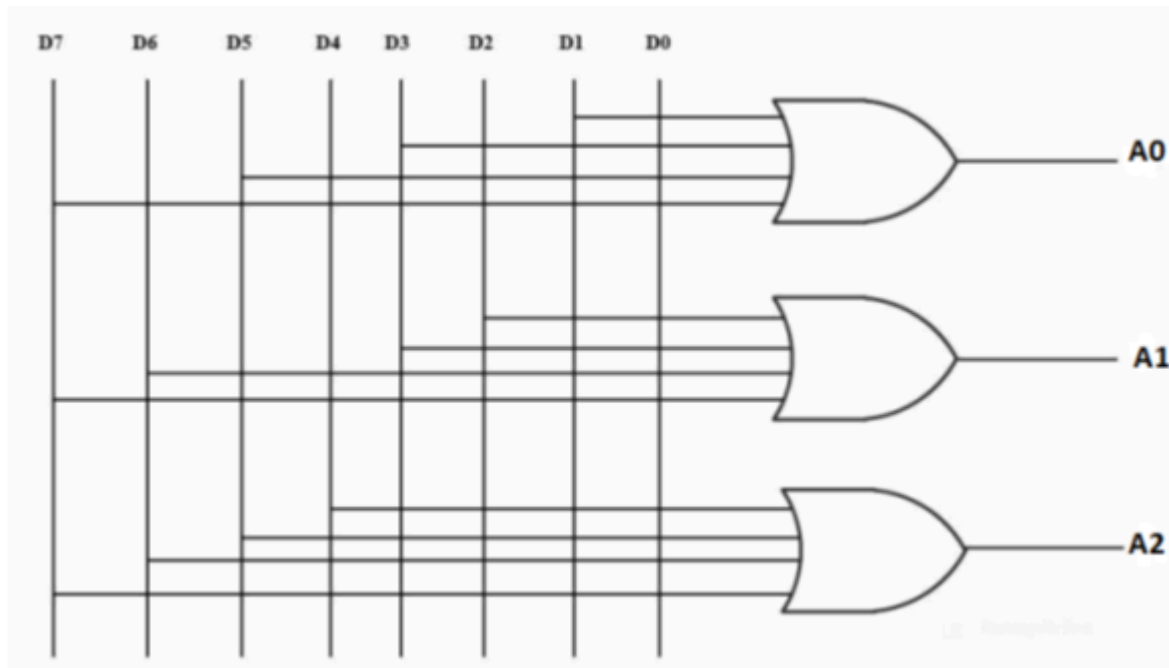Logical circuit of the above expressions is given below:

Figure 02 Encoder 8 * 3

Procedure

1. Type the program in Quartus software.

2. Compile and run the program.

3. Generate the RTL schematic and save the logic diagram.

4. Create nodes for inputs and outputs to generate the timing diagram.

5. For different input combinations generate the timing diagram.

PROGRAM

/* Program for Encoder 8 To 3 in Dataflow Modelling and verify its truth table in quartus using Verilog programming. */

```verilog
1    module digital5(a,b,c,y0,y1,y2,y3,y4,y5,y6,y7);
2    input y0,y1,y2,y3,y4,y5,y6,y7;
3    output a,b,c;
4    assign a= ( y4 | y5 | y6 | y7);
5    assign b= ( y2 | y3 | y6 | y7);
6    assign c= ( y1 | y3 | y5 | y7);
7    endmodule
8
```

Developed by: AKASH M
RegisterNumber:24900103
RTL LOGIC FOR Encoder 8 To 3 in Dataflow Modelling
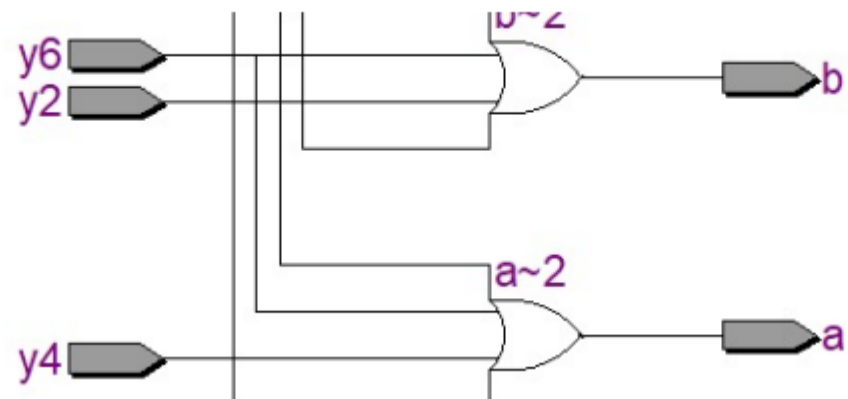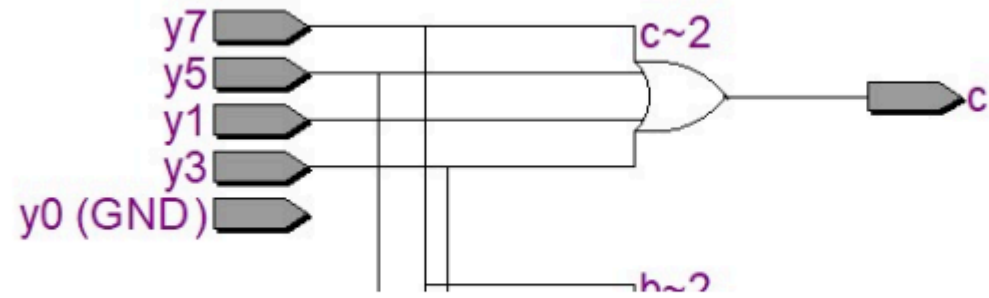
TIMING DIGRAMS FOR Encoder 8 To 3 in Dataflow Modelling
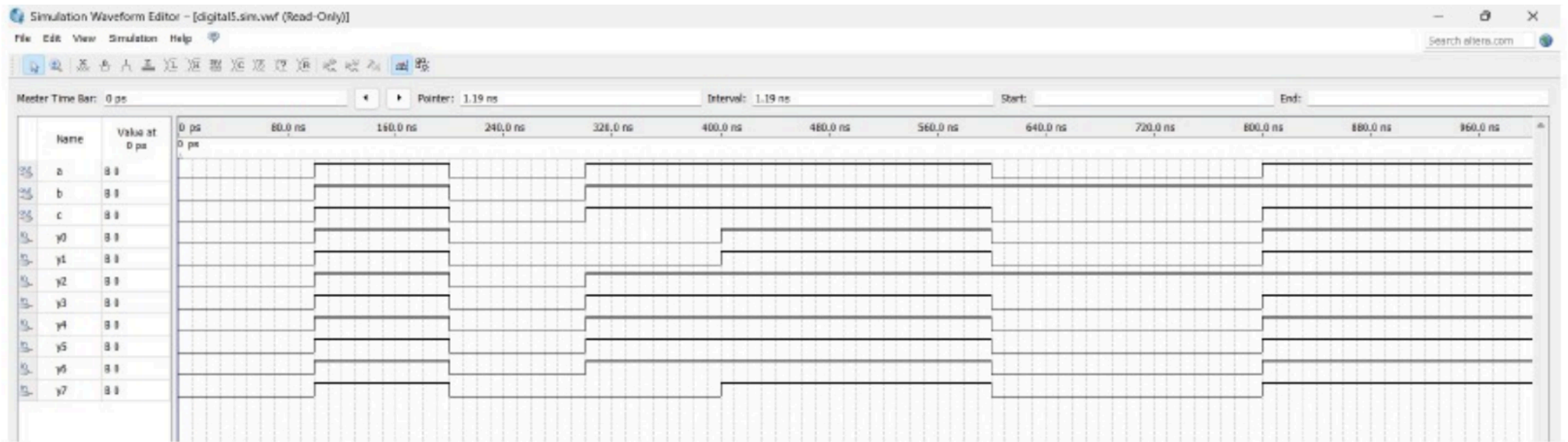
RESULTS

Thus the Encoder 8 to 3 is designed and the truthtable is verified.