# SR-FLIPFLOP-USING-CASE

AIM:

To implement SR flipflop using verilog and validating their functionality using their functional tables

SOFTWARE REQUIRED:

Quartus prime

THEORY

SR Flip-Flop SR flip-flop operates with only positive clock transitions or negative clock transitions. Whereas, SR latch operates with enable signal. The circuit diagram of SR flip-flop is shown in the following figure.
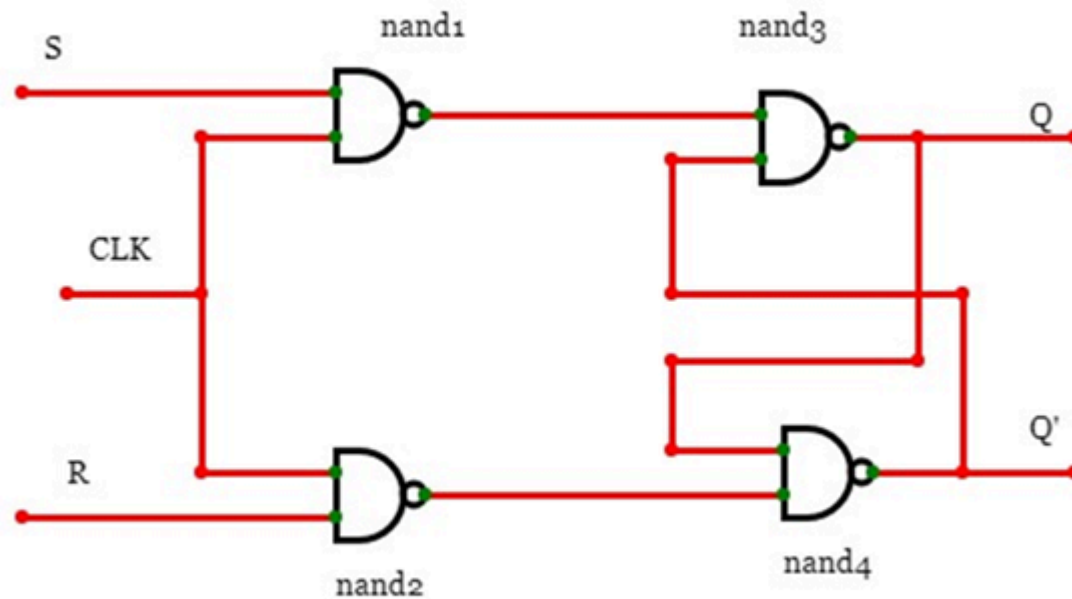
This circuit has two inputs S & R and two outputs Q_t & Q_t'. The operation of SR flipflop is similar to SR Latch. But, this flip-flop affects the outputs only when positive transition of the clock signal is applied instead of active enable. The following table shows the state table of SR flip-flop.

S	R	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	-

Here, Q_t & Q_{t+1} are present state & next state respectively. So, SR flip-flop can be used for one of these three functions such as Hold, Reset & Set based on the input conditions, when positive transition of clock signal is applied. The following table shows the characteristic table of SR flip-flop. Present Inputs Present State Next State

Present Inputs		Present State	Next State
S	R	$Q\ t$	$Q\ t+1$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

By using three variable K-Map, we can get the simplified expression for next state, $Q_{t+1}t+1$. The three variable K-Map for next state, $Q_{t+1}t+1$ is shown in the following figure.
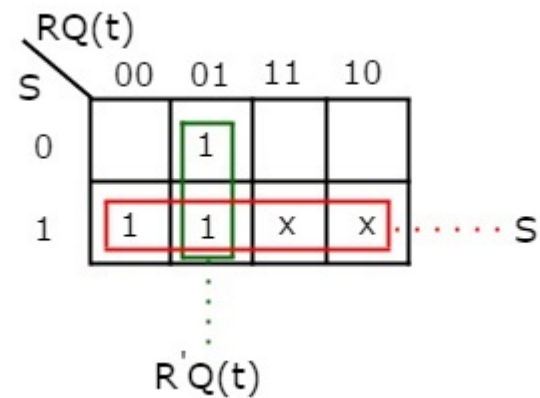
The maximum possible groupings of adjacent ones are already shown in the figure. Therefore, the simplified expression for next state Q_{t+1}^{t+1} is $Q(t+1)=S+R'Q(t)Q(t+1)=S+R'Q(t)$

Procedure

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/ 1.Type the program in Quartus software.
2.Compile and run the program.
 3.Generatethe RTL schematic and save the logic
diagram.
4.Create nodes for inputs and outputs togenerate the timing diagram.
5.For
different input combinations generatethe timing diagram.
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PROGRAM

/* Program for flipflops and verify its truth table in quartus using Verilog programming.
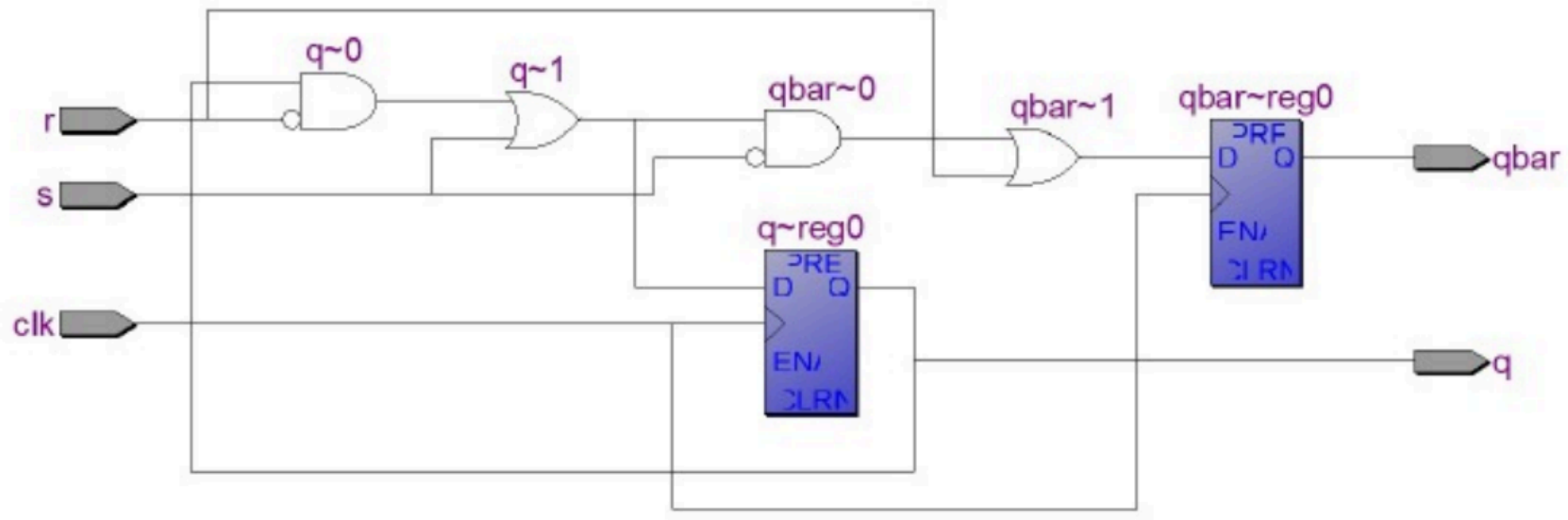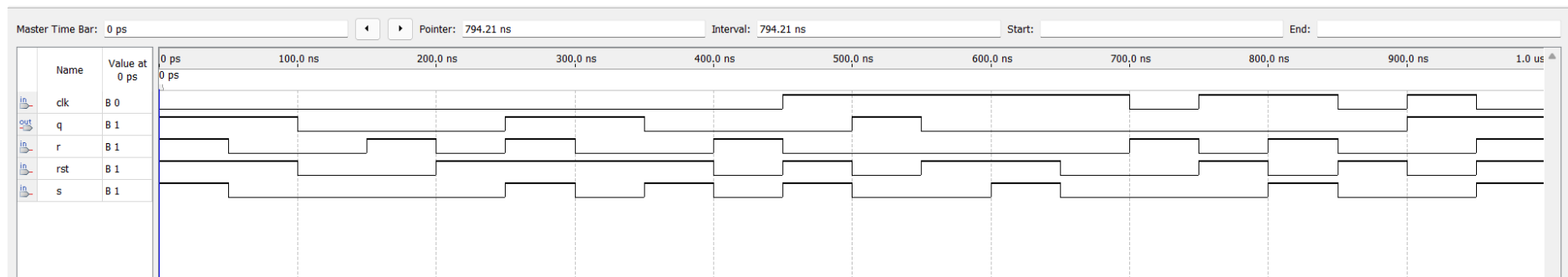
Developed by:

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24900103 */

RTL LOGIC FOR FLIPFLOPS

TIMING DIGRAMS FOR FLIP FLOPS

RESULTS

Thus, the SR Flip-Flop is designed, and its functionality is validated using the truth table and timing diagrams.