Ahsanullah University of Science & Technology

Department of Computer Science & Engineering

Experiment No : 02

Course No : CSE3110

Course Title : Digital System Design Lab

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Submitted by

Group No : 01

Section : A2

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Introduction :

Booth's multiplication algorithm is an algorithm which multiplies 2 signed or unsigned integers in 2's complement. This approach uses fewer additions and subtractions than more straight forward algorithms.

The algorithm was invented by Andrew Donald Booth in 1950. Booth's algorithm follows this old scheme by performing an addition when it encounters the first digit of a block of ones (0 1) and subtraction when it encounters the end of the block (1 0). This works for a negative multiplier as well.

Problem statement :

Design a 5×5 booth multiplier

Hardware Design:

(i) Initialization:

$u \leftarrow 0$

$v \leftarrow 0$

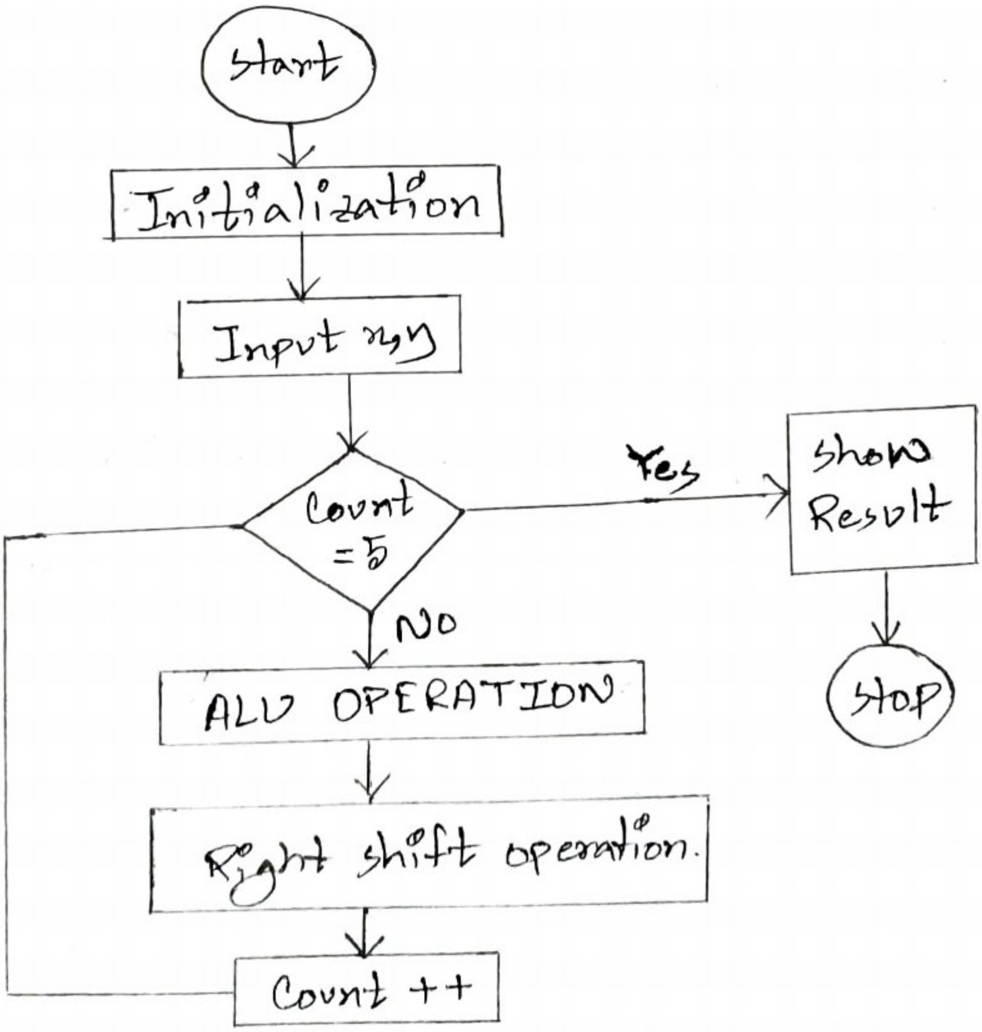
$x \leftarrow$ input

$y \leftarrow$ input

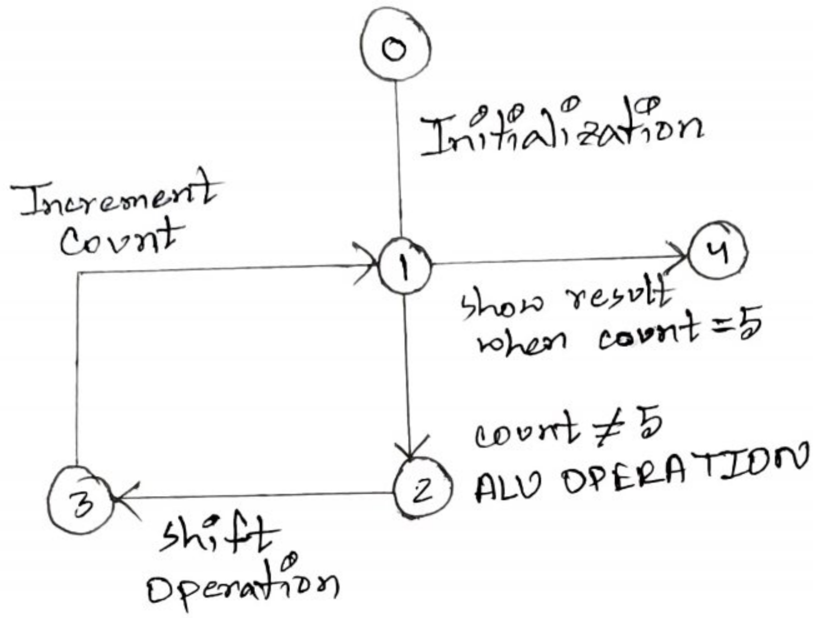
$x_{-1} \leftarrow 0$

count $\leftarrow 0$

(ii) flow chart:



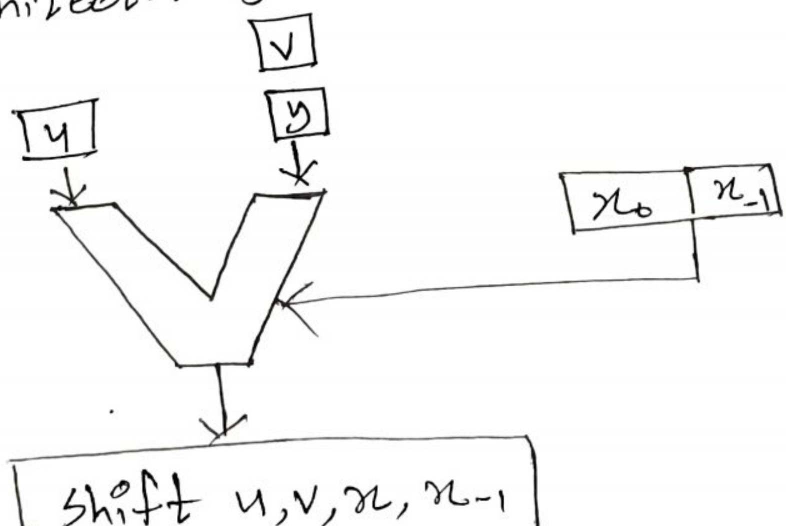
(iii) State Diagram :



ALU Operation

S_1	S_0	Operation
0	0	u+0
0	1	u+y
1	0	u−y
1	1	u+0

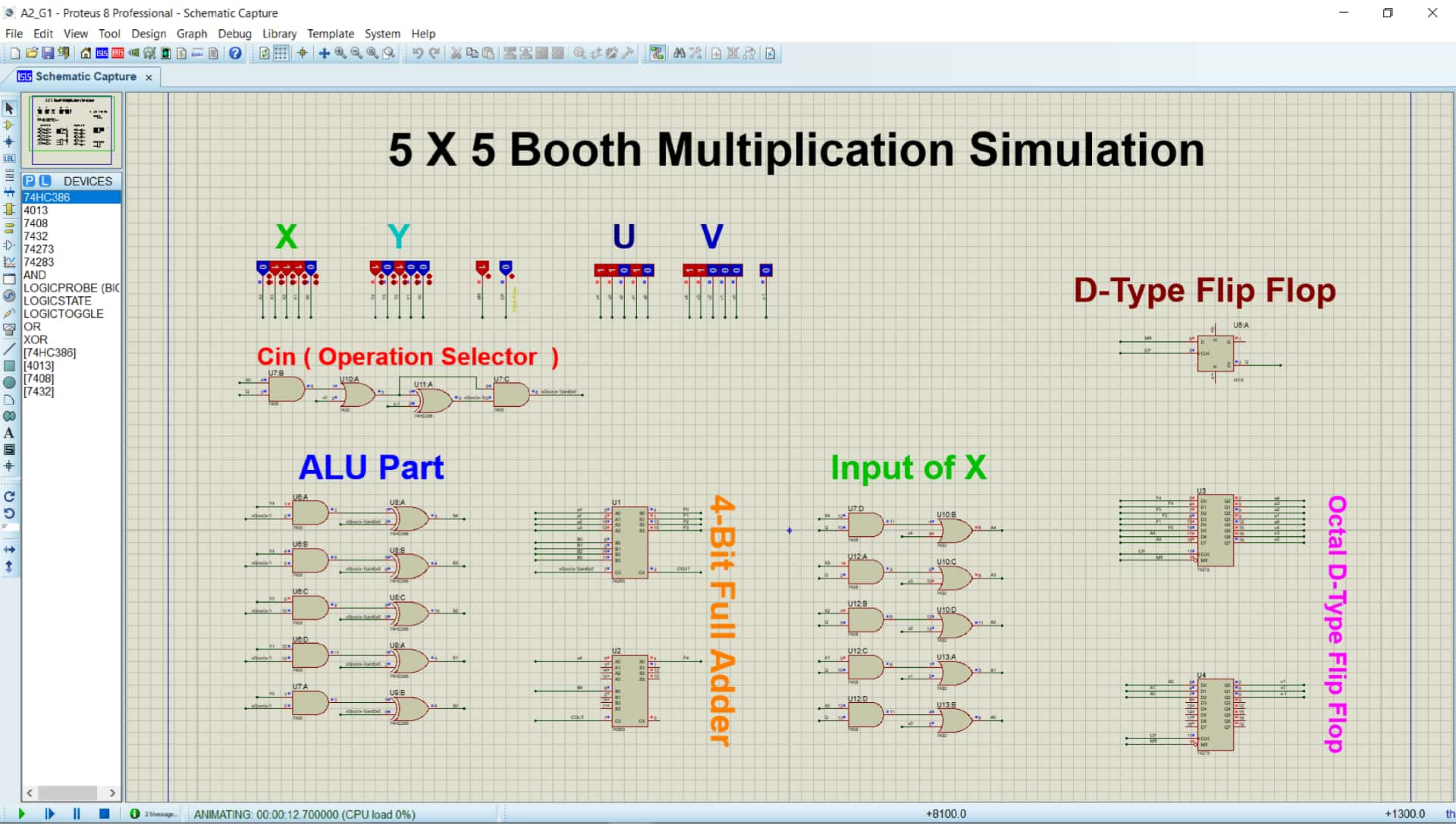
(iv) Architecture :



⊞ Equipment:

Equipments	Quantity	Unit Price	Total
Breadboard	10	65	650
Power Adapter	1	170	170
Breadboard power module	1	100	100
LED (Red 5mm)	5	·60	3
LED (Green 5mm)	5	·60	3
LED (Blue 5mm)	1	1	1
AND Gate - 7408 IC	3	13	39
OR Gate - 7432 IC	2	13	26
XOR Gate - 7486 IC	2	13	26
D-Type Flip-Flip - 4013 IC	1	40	40
Octal D-Type Flip Flop - 74283 IC	2	40	80
4 bit Full Adder - 7483 IC	2	38	76
Total			1214

Total Cost 1214 taka


A2_G1 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Schematic Capture
DEVICES
74HC386
4013
7408
7432
74273
74283
AND
LOGICPROBE (BI
LOGICSTATE
LOGICTOGGLE
OR
XOR
[74HC386]
[4013]
[7408]
[7432]
5 X 5 Booth Multiplication Simulation
X
Y
U
V
D-Type Flip Flop
Cin (Operation Selector)
ALU Part
Input of X
4-Bit Full Adder
Octal D-Type Flip Flop
ANIMATING: 00:00:12.700000 (CPU load 0%)
+8100.0
+1300.0

Result:

Here, we will do a step by step calculation that used to done by a 5x5 bit booth multiplier:

We are taking 14 as multiplicand and
-12 as multiplier

So, $x = (14)_{10} = 01110$ [Multiplicand]

$y = (-12)_{10} = 10100$ [Multiplier]

$-y = (12)_{10} = 01100$

$m = 14$, $n = -12$

Now, initially

u	v	x	x_{-1}
00000	00000	01110	0

Step-1: As the last bit of $x = 0$ and $x_{-1} = 0$, there will be a shift only

After shifting,

u	v	x	x_{-1}
00000	00000	01110	0
00000	00000	00111	0

Step-2: As the last bit of x is 1 and $x_{-1} = 0$, there will be a subtraction of y from u

which means,

$u = u - y$

$$\begin{array}{r} 00000 \\ 01100 \\ \hline 01100 \end{array}$$

$\therefore$ So, $u = 01100$

So,

u	v	x	x_{-1}
01100	00000	00111	0

Shift: 00110 00000 00011 1

Step: 3

As the last bit of x is 1 and $x_{-1} = 1$ so there will be shifting only

So,

	u	v	x	x_{-1}
	00110	00000	00011	
Shift:	00011	00000	00001	1

Step: 4

As the last bit of x is 1 and $x_{-1} = 1$

So, there will be shift only.

So,

	u	v	x	x_{-1}
	00011	00000	00001	1
Shift:	00001	10000	00000	1

5th step: As last bit of x_0 is 0 and $x_{-1} = 1$,

So, $u = u + y$

$= 10101$

$$\begin{array}{r} 00001 \\ 10100 \\ \hline 10101 \end{array}$$

So,

u	v	x	x_{-1}
10101	10000	00000	1
Shift: 11010	11000	00000	0

So,

the final Result is, $(u+v)$

$= 11010\ 11000$

$= (-168)_{10}$

Also,

$(14)_{10} \times (-12)_{10} = (-168)_{10}$

Conclusion:

In this experiment, we had to make a 5x5 Multiplier using Booth's Algorithm. Here, we can see the circuit is showing correct outputs for different combinations of Input. We used XOR, AND, OR, Adders and flip-flop and shift-Registers to build this circuit through Simulation software Proteus. During the making of this circuit on proteus we didn't face any difficulties also. We will see the final output which is (u+v) by giving 5 clock pulses.