Part 1A Paper 3: Electrical and Information Engineering,

ANALYSIS OF CIRCUITS EXAMPLES PAPER 3

Questions containing material of tripos standard are marked *.

Amplifiers

1. The circuit of a signal source, a voltage amplifier and an output load is shown in Fig. 1. The source has an internal resistance, R_S = 1 kΩ, the amplifier has an input resistance R_{in} = 1MΩ, an output resistance R_{out} = 1kΩ and a gain of A = 100. The load comprises a resistor, R_L = 9 kΩ in parallel with a capacitor, C_L = 180 pF. The output of the amplifier can be switched between DC and AC mode via a capacitor C = 10 μF.

(a) With the switch in the DC position as shown, and at a frequency where the effect of the capacitor C_L can be ignored (i.e. mid-band), what is the value of the voltage gain, v_{out}/v_{in}?

(b) When the effect of C_L cannot be ignored, find the frequency, f, at which the gain drops to 70% ($1/\sqrt{2}$ otherwise known as the -3dB point) of its mid-band value.

(c) The switch is now moved into the AC position. For the case that the frequency is far enough below f that the effect of the capacitor C_L can be ignored, find the new -3dB frequency of the circuit.

(d) Determine the mid-band power gain of the amplifier both numerically and in dB.

(e) If the amplifier is preceded by another stage whose gain is +40 dB and a variable gain control between the two amplifiers is set to -4dB (i.e. a loss, or *attenuation*), what is the overall gain in dB?

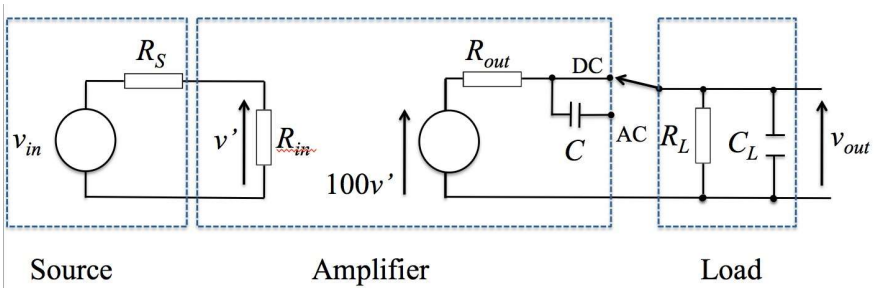

Fig. 1

2.* A strain gauge to be used on a bridge design has an output voltage of v_{in} = 1 mVpp and a series resistance of R_s = 10 kΩ. The gauge is required to send a signal to a digital processor which has an input with an impedance of 100 kΩ and requires a minimum peak voltage of 1 V. Design an amplifier for this application using a cascaded system based on single stage amplifiers that have an input impedance of R_{in} = 100 kΩ, output impedance of R_{out} = 1 kΩ and a voltage gain of 22 dB. Derive an expression for the total gain and calculate how many stages are required?

The amplifiers used require DC biasing for the transistors inside, with 3 V set at the input and 8 V set at the output. How would your cascaded amplifier be modified to prevent the DC biasing of each amplifier affecting the operation of the other stages? What value of component might be used if the minimum frequency of the sensor signal was 100Hz?

Electrical properties of materials; semiconductor diodes

3. Consider a solid slab of material as shown in Fig. 2. Calculate its electrical resistance assuming that it is made of copper, of resistivity 1.7×10^{-8} Ωm.

If we assume that a DC voltage of 1 V is applied across the ends of this slab, calculate how much current will flow, and hence how much power will be dissipated in it, assuming that it is made from copper.

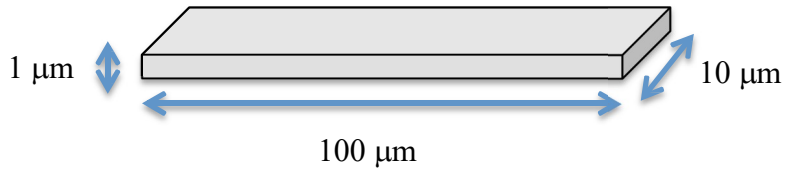

Fig. 2

4. A silicon diode with the I-V characteristics shown in Fig. 3(b) is used in the circuit shown in Fig. 3(a). The diode has non-linear characteristics, so we need to use to a graphical method to determine the operating point of the diode. Find the operating point. (The divisions in the x-axis are each 0.02 V, and in the y-axis are 0.5 mA).

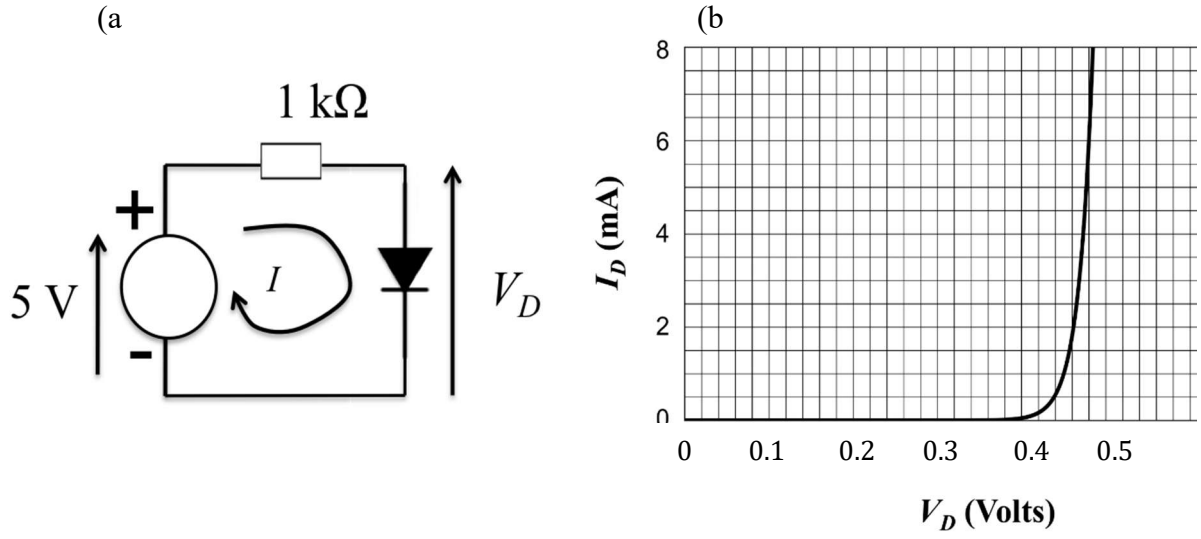

Fig. 3

FET Amplifiers

5. The characteristics and maximum ratings of a field-effect transistor (FET) are shown in Fig. 4.

(a) Is the device a p-channel or n-channel FET?
(b) Using the maximum ratings and the fact that you want to design an amplifier with as high an input resistance as possible, and with an approximately linear relationship between the input and output voltages, eliminate the forbidden regions of operation of the FET.

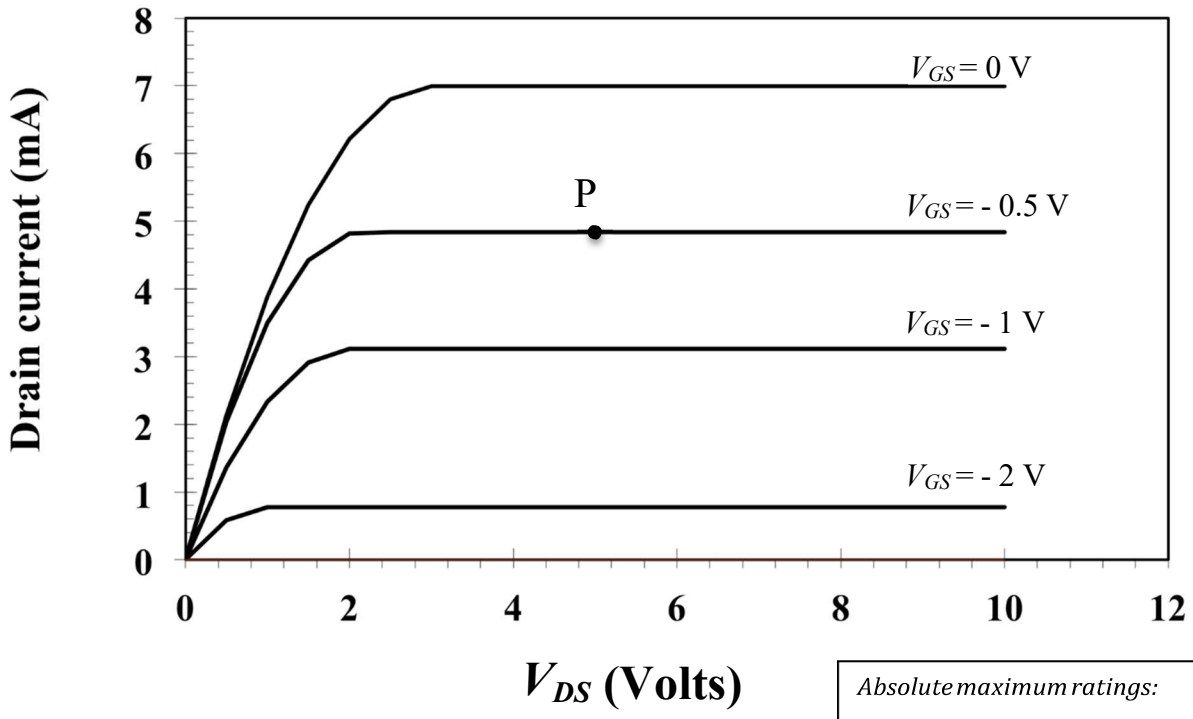

Fig. 4

Absolute maximum ratings:
V_{DS} *max* = 8 V
V_{GS} cannot be positive
Max power in FET = 32 mW

7. A common-source amplifier circuit is shown in Fig. 5. The FET has the characteristics shown in Fig. 4.

(a) Calculate an appropriate value of R and determine the bias voltage, V_G required if the FET is to operate at the operating point marked "*P*" in Fig. 4.

(b) *Graphically* estimate the voltage gain (v_2/v_1, or $\Delta V_{DS}/\Delta V_{GS}$) for the case of a 1 V peak- to peak voltage signal, v_1 applied to the gate.

Discuss with your supervisor the practicality of V_G and why it leads to the circuit of Fig 6.

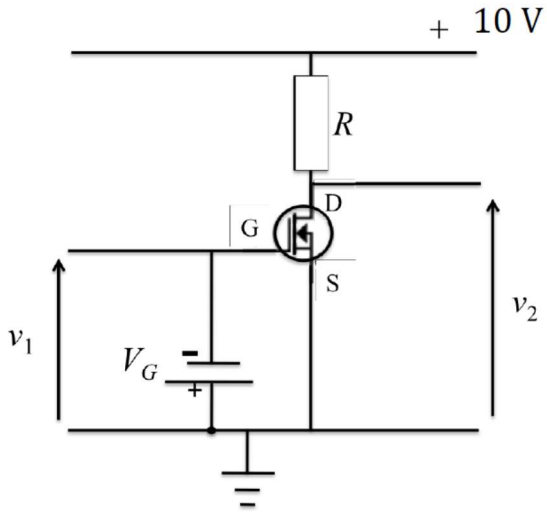

Fig. 5

8.* The self-biased common-source amplifier circuit shown in Fig. 6 uses an FET with the same characteristics as shown in Fig. 4. Determine the values of the resistors R_1 and R_2 that will enable the transistor to be at the operating point, P.

Discuss with your supervisor the advantages and disadvantages of having the resistor R_2 present.

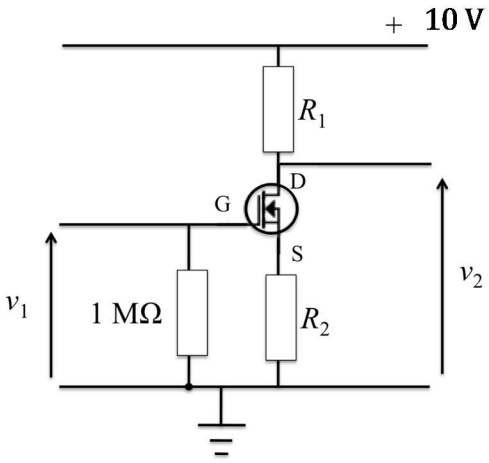

Fig. 6

Solutions:

1. a) $\frac{v_{out}}{v_{in}} = 90$, b) $f_{3dB} = \frac{R_L+R_{out}}{2\pi C_L R_L R_{out}} = 980kHz$, c) $f_{3dB} = \frac{1}{2\pi C(R_L+R_{out})} = 1.6Hz$ d) 59.5dB, e) 95.5dB
2. $G = \left(\frac{R_{in}}{R_S+R_{in}}\right)\left(\frac{AR_{in}}{R_{in}+R_{out}}\right)^{n-1}\left(\frac{AR_L}{R_L+R_{out}}\right) = 2000$, $n = 3$ will do, C = 15.8 nF
3. $R = 0.17\ \Omega$, $I = 5.88$ A, $P = 5.88$ W
4. (Approx) $I_D = 4.5$ mA, $V_D = 0.475$ V
5. (Approx) $V_0 = 1.7$ V, 6. n-channel
7. (Approx) i) $R = 1\text{k}\Omega$, ii) Gain ~ -4
8. $R_2 = 104\ \Omega$, $R_1 = 940\ \Omega$.

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