Part 1A Paper 3 : Electrical and Information Engineering

DIGITAL CIRCUITS AND INFORMATION PROCESSING

SOLUTIONS TO EXAMPLES PAPER 3

1.

State			$\overline{Q_C}$	Q_B	Q_A	$\overline{Q_A}$	Q_B	$\overline{Q_B}$	Next State		
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C	A	B	C
0	0	0	1	0	0	1	0	1	1	0	0
1	0	0	1	0	1	0	0	1	1	1	0
1	1	0	1	1	1	0	1	0	0	1	1
0	1	1	0	1	0	1	1	0	0	0	1
0	0	1	0	0	0	1	0	1	0	0	0

So this arrangement generates a sequence of length 5.

2.

Counter state			Next state			Bistable inputs					
C	B	A	C	B	A	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	×	0	×	1	×
0	0	1	0	1	0	0	×	1	×	×	1
0	1	0	0	1	1	0	×	×	0	1	×
0	1	1	1	0	0	1	×	×	1	×	1
1	0	0	1	0	1	×	0	0	×	1	×
1	0	1	0	0	0	×	1	0	×	×	1

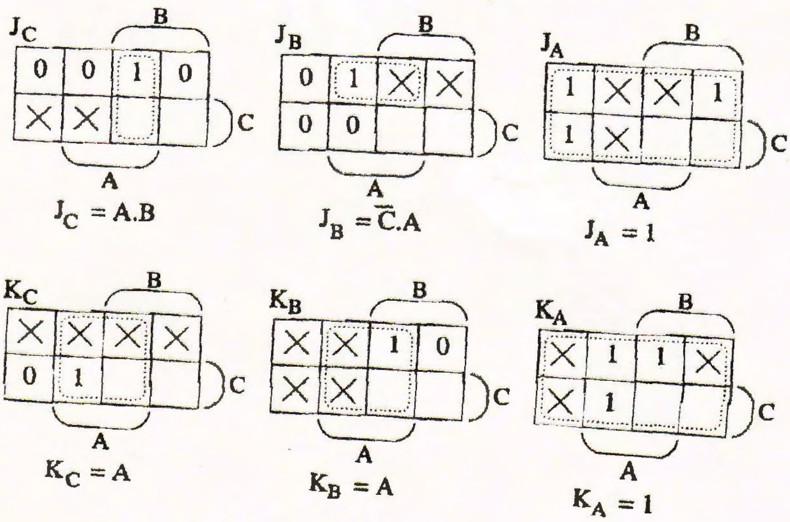


Figure 1:

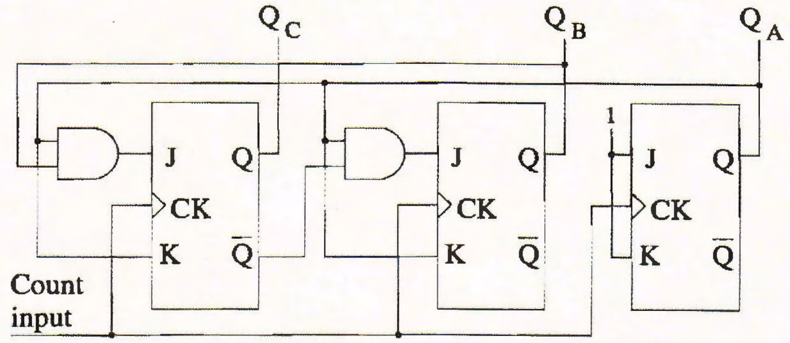


Figure 2:

3.

Counter state			Next state			Bistable inputs					
C	B	A	C	B	A	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	×	0	×	1	×
0	0	1	0	1	0	0	×	1	×	×	1
0	1	0	0	1	1	0	×	×	0	1	×
0	1	1	1	0	0	1	×	×	1	×	1
1	0	0	1	0	1	×	0	0	×	1	×
1	0	1	0	0	0	×	1	0	×	×	1
1	1	0	0	0	1	×	1	×	1	1	×
1	1	1	0	0	1	×	1	×	1	×	0

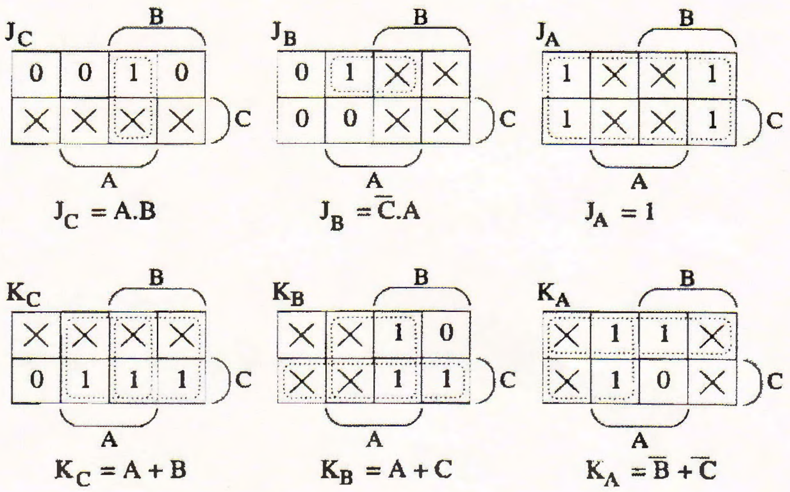


Figure 3:

4.

Input	State		Next State		Inputs needed			
Z	B	A	B	A	J_B	K_B	J_A	K_A
0	0	0	0	1	0	×	1	×
0	0	1	1	0	1	×	×	1
0	1	0	1	1	×	0	1	×
0	1	1	0	0	×	1	×	1
1	0	0	1	1	1	×	1	×
1	0	1	0	0	0	×	×	1
1	1	0	0	1	×	1	1	×
1	1	1	1	0	×	0	×	1

By inspection $J_A = K_A = 1$, so we only need Karnaugh maps for J_B and K_B. Figure 4 shows

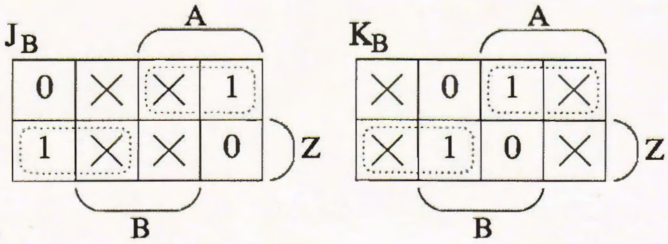


Figure 4:

that we can use a single exclusive-or gate for these remaining inputs. $J_B = K_B = A \oplus Z$. The circuit is given in Figure 5.

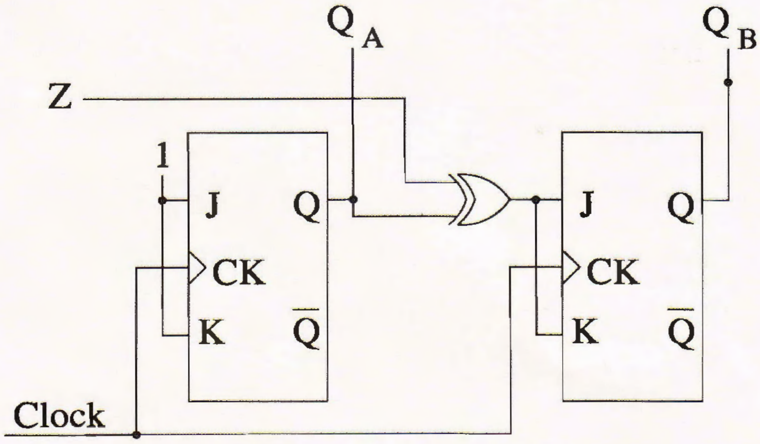


Figure 5:

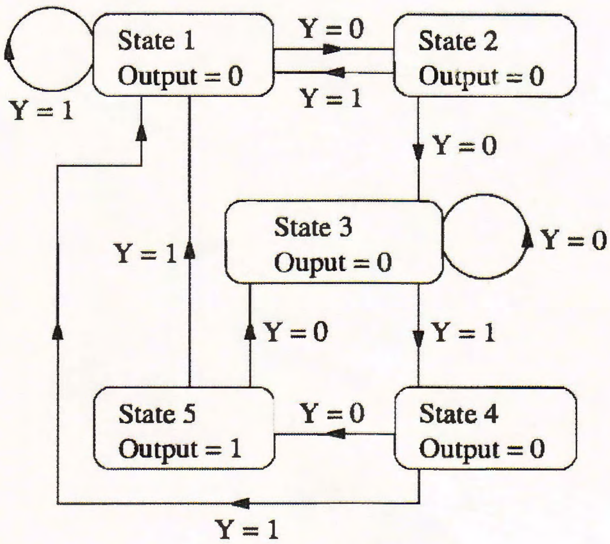
5. The characteristic (or excitation) table of the JK bistable defines what inputs are required to achieve a particular output change.

Output before → after		Required inputs	
$Q(n)$	$Q(n+1)$	Input J	Input K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Thus:

$$\begin{aligned} I_1 &\text{ is } (J = 0,\ K = \text{anything}) \\ I_2 &\text{ is } (J = 1,\ K = \text{anything}) \\ I_3 &\text{ is } (K = 0,\ J = \text{anything}) \\ I_4 &\text{ is } (K = 1,\ J = \text{anything}) \end{aligned}$$

6.



7. The state diagram is shown in Figure 6. We note that there are 4 states so only two bistables are required. We choose the bistables to represent R and Y directly, and use $G = \overline{R + Y}$ to compute the state of the green light. The state transition table is followed by the Karnaugh maps in Figure 7, and the circuit in Figure 8.

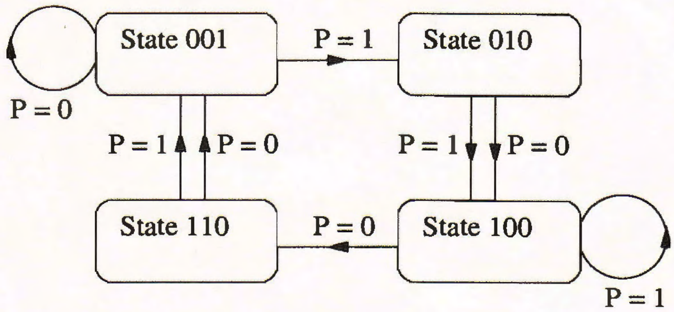


Figure 6:

Input	State		Next State		Inputs needed			
P	R	Y	R	Y	J_R	K_R	J_Y	K_Y
0	0	0	0	0	0	×	0	×
1	0	0	0	1	0	×	1	×
×	0	1	1	0	1	×	×	1
0	1	0	1	1	×	0	1	×
1	1	0	1	0	×	0	0	×
×	1	1	0	0	×	1	×	1

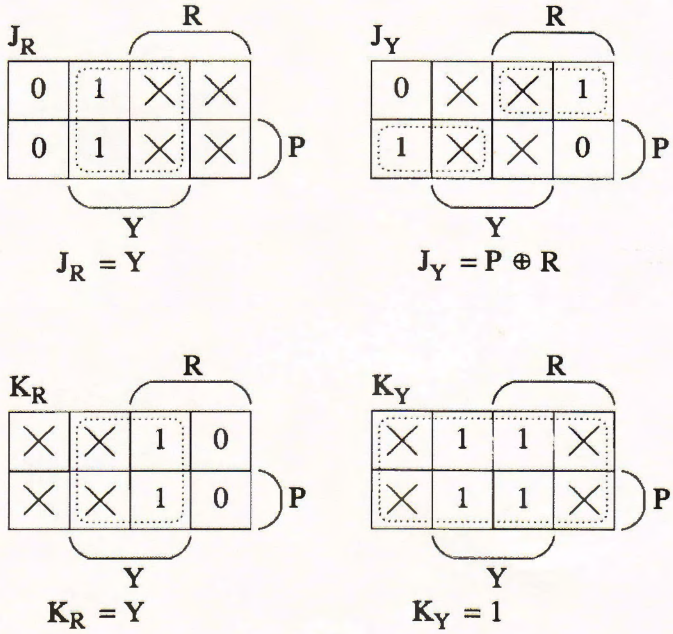


Figure 7:

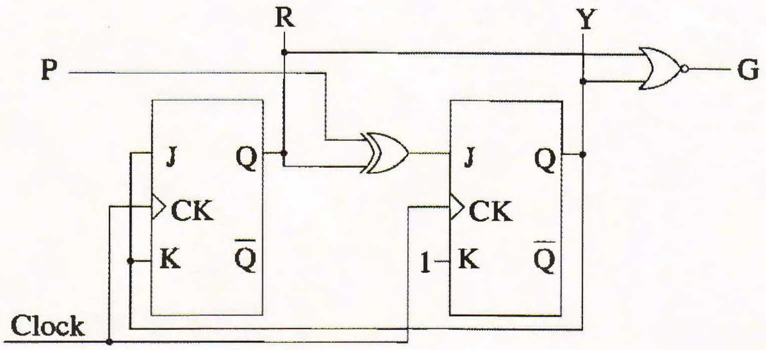
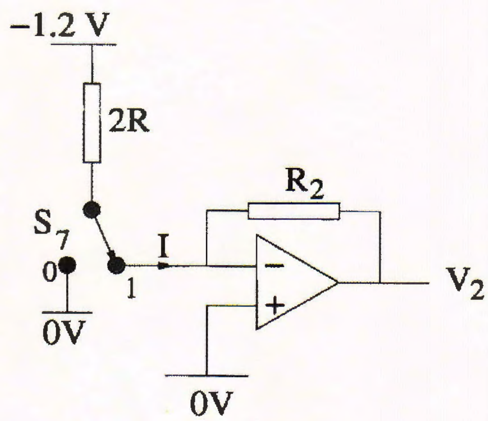


Figure 8:

8. When 10000000 is set on the switches, the circuit reduces to that shown on the right. Using the usual expression for the gain of an ideal inverting op-amp we have.



$$V_2 = \frac{-R_2}{2R} \times (-1.2)$$
$$\Rightarrow R_2 = \frac{-V_2.2R}{-1.2} = 8.33R$$

To work out the output voltages for other switch settings we first note that the inverting input to the op-amp is a *virtual earth*. Therefore the currents through the various switches are independent of the switch settings. Because of the symmetry of the circuit, the current through S_1 is twice the current through S_0, and the current through S_2 is twice the current through S_1. This pattern continues right up to S_7. The current I is therefore proportional to the value of the binary number set on the switches. As the op-amp is ideal, the output V_2 is, in turn, proportional to I. Thus we can say:

Switches	Decimal Value	V_2 / Volts
10000000	128	5.000
01010101	85	3.320
01100100	100	3.906
10100001	161	6.289

9.

(a) For $A = 00110_2$ and $B = 00010_2$

Before clock pulse	A	B	Q	C_o	Sum
1	00110	00010	0	0	0
2	00011	00001	0	1	0
3	00001	00000	1	1	0
4	00000	00000	1	0	1
5	00000	10000	0	0	0
6	00000	01000	0	0	0

The answer is left in B and is thus 01000_2. We have worked out $6 + 2 = 8$.

B_4 is the most significant bit of the answer and B_0 is the least significant bit of the answer.

If both A_4 and B_4 were 1 at the start of the addition, the B register would need to be one bit longer to avoid overflow and an extra clock pulse would be required for the calculation to complete.

(b) The configuration described in the question results in taking the complement of the number in A and adding 1 (from C_i) to the solution. This is the strategy for finding the negative of a 2's complement binary number. The result is therefore to work out $(B - A)$ using 2's complement representations.

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