Engineering **FIRST YEAR**

Part 1A Paper 3 : Electrical and Information Engineering

DIGITAL CIRCUITS AND INFORMATION PROCESSING

SOLUTIONS TO EXAMPLES PAPER 1

1.

Inputs		Table for Figure 1				
A	B	$\overline{A}$	$\overline{\overline{A}.B}$	$\overline{B}$	$\overline{A.\overline{B}}$	X
0	0	1	1	1	1	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	1	0	1	0	1	0

Inputs		Table for Figure 2				
A	B	$\overline{A}$	$\overline{\overline{A}+B}$	$\overline{B}$	$\overline{A+\overline{B}}$	Y
0	0	1	0	1	0	1
0	1	1	0	0	1	0
1	0	0	1	1	0	0
1	1	0	0	0	0	1

2.

A	B	C	$\overline{A+B}$	$\overline{B+\overline{C}}$	Z
0	0	0	1	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	0	0	0
1	1	1	0	0	0

So $Z = 1$ for ABC in the states 000, 001 and 101.

3.

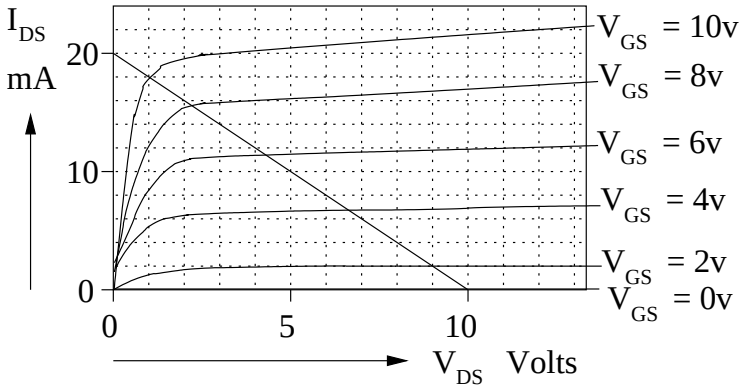


Figure 1:

(a) The load line intersects $V_{DS} = 10$V. As it is the characteristic of the resistor R, drawn backwards, it intersects the $V_{DS} = 0$ axis at $I_D = 20$mA. See Figure 1.

$V_i = 0\text{V} \quad \Rightarrow V_o = 10\text{V}$
$V_i = 10\text{V} \Rightarrow V_o = 1\text{V}$

(b) $V_i = 0\text{V} \quad \Rightarrow I_{DS} = 0$ so power in resistor and transistor is zero.
$V_i = 10\text{V} \Rightarrow I_{DS} = 18$mA so:
power in resistor $= (10 - V_{DS}) \times I_{DS} = 162$mW.
power in transistor $= V_{DS} \times I_{DS} = 18$mW.

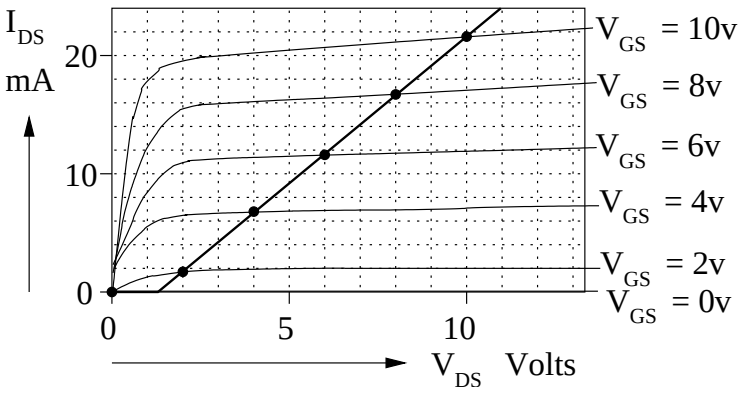
(c) Initially, $V_o = 1$V. When the transistor switches off the current through the resistor equals the current through the capacitor.

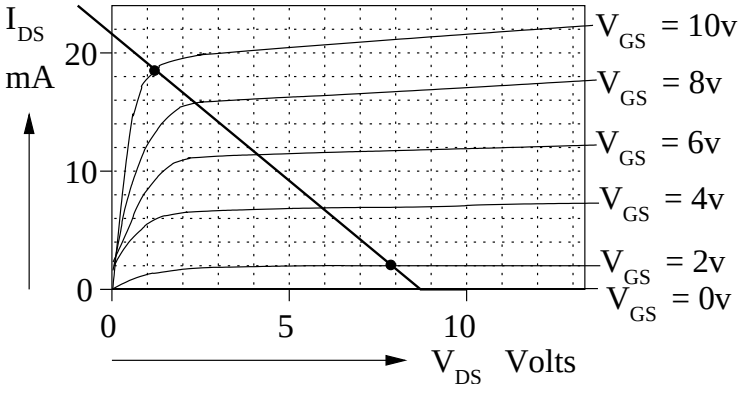
$$\begin{aligned} \frac{10 - V_o}{R} &= C\frac{dV_o}{dt} \\ \Rightarrow RC\frac{dV_o}{dt} + V_o &= 10 \\ \Rightarrow \text{ general solution } V_o &= A\exp\left(\frac{-t}{RC}\right) + 10 \\ V_o = 1 \text{ when } t = 0 \Rightarrow A &= -9 \\ \Rightarrow V_o &= 10 - 9\exp\left(\frac{-t}{RC}\right) \end{aligned}$$

To find the time when $V_o = 8$ we set $8 = 10 - 9\exp(-t/RC)$, giving the answer $t = 30.1$ns.

4. Plot the points where $V_{DS} = V_{GS}$ for the six V_{GS} curves provided. Join the 2, 4, 6, 8, and 10V points to form a line with gradient 395Ω, intersecting the $I_{DS} = 0$ line at 1.5V. T_1 is thus equivalent to a voltage drop $V_1 = 1.5$V in series with a resistor $R_1 = 395\Omega$.

The bent line constructed above is the characteristic (graph of current against voltage) of the transistor T_1, with its gate connected to its drain. To discover the operation of the circuit, we use this bent line as a 'load line,' and draw it backwards, starting at the supply voltage. The output of the circuit can now be found for any input voltage by looking for the intersection of the this bent load line with the appropriate T_2 characteristic curve.





A	T_2	X
0	OFF	1
1	ON	0

$V_A = 2$V $\Rightarrow V_X = 8$V
$V_A = 10$V $\Rightarrow V_X = 1.2$V

5.

(a) When either A or B is low, one of T_2 or T_3 will be off, so the output, X, will be high.

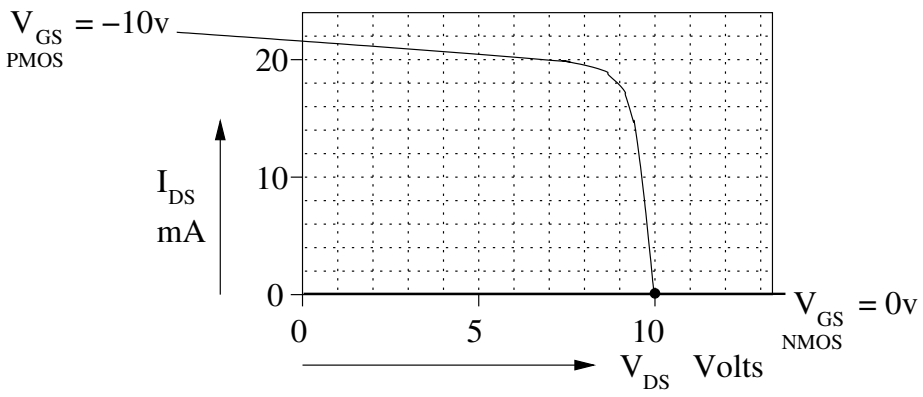
(b) When both A and B are low, both of T_4 and T_5 will be off, so the output, Y, will be high.

Inputs		Table for (a)		
A	B	T_2	T_3	X
0	0	OFF	OFF	1
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	0

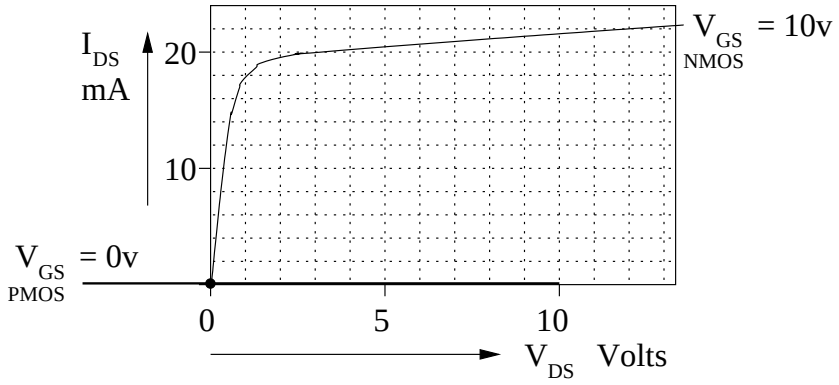
Inputs		Table for (b)		
A	B	T_4	T_5	Y
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0

So (a) is a NAND gate and (b) is a NOR gate.

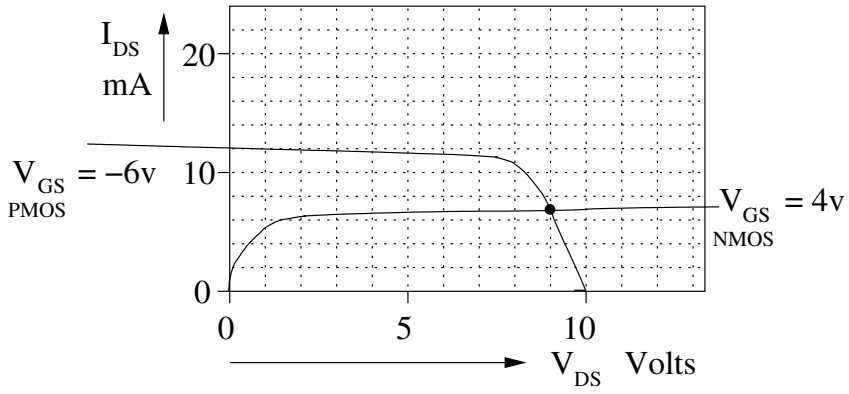
6.



(a) $V_i = 0$V



(b) $V_i = 10$V



(c) $V_i = 4$V

Figure 2:

(a) When $V_i = 0$V we take the $V_{GS} = 0$ curve for the NMOS and draw the PMOS curve for $V_{GS} = -10$ backwards from the supply voltage. The intersection of these curves gives $V_o = 10$V. See Figure 2(a).

When $V_i = 10$V we take the $V_{GS} = 10$ curve for the NMOS and draw the PMOS curve for $V_{GS} = 0$ backwards from the supply voltage. The intersection of these curves gives $V_o = 0$V. See Figure 2(b).

(b) In both Figure 2(a) and Figure 2(b) the current passing through the circuit is zero thus no power is dissipated.

(c) When $V_i = 4$V we take the $V_{GS} = 4$ curve for the NMOS and draw the PMOS curve for $V_{GS} = -6$ backwards from the supply voltage. The intersection of these curves gives $V_o =$ approx 9V. See Figure 2(c).

From Figure 2(c), the current in the circuit is approximately 7mA. The power dissipated in the NMOS transistor is thus 63mW, and in the PMOS 7mW. The power drawn from the supply is 70mW.

7.

(a) $A.B.C + A.B.\overline{C} = A.B.(C + \overline{C}) = A.B$

(b) $A.(\overline{A} + B) = A.\overline{A} + A.B = A.B$

(c)

$$\begin{aligned}(A + C).(\overline{A} + B) &= A.\overline{A} + A.B + C.\overline{A} + C.B \\ &= A.B + \overline{A}.C + B.C \\ &= (A.B.C + A.B.\overline{C}) + (\overline{A}.C.B + \overline{A}.C.\overline{B}) + (B.C.A + B.C.\overline{A}) \\ &= (A.B.C + A.B.\overline{C}) + (\overline{A}.C.B + \overline{A}.C.\overline{B}) \\ &= A.B + \overline{A}.C\end{aligned}$$

(d)

$$\begin{aligned}(A + C).(A + D).(B + C).(B + D) &= (A + A.D + C.A + C.D).(B + B.D + C.B + C.D) \\ &= (A + C.D).(B + C.D) \\ &= A.B + A.C.D + C.D.B + C.D \\ &= A.B + C.D\end{aligned}$$

8.

$$\begin{aligned}\overline{(A.B.C + \overline{A})} + B &= \overline{(A.B.C + \overline{A}).\overline{B}} \\ &= \overline{A.B.C.\overline{B} + \overline{A}.\overline{B}} \\ &= \overline{\overline{A}.\overline{B}} \\ &= A + B\end{aligned}$$

9.

$$V = A.B.C.D + \overline{A}.B.C.D + A.\overline{B}.C.D + A.B.\overline{C}.D + A.B.C.\overline{D}$$

Take the $A.B.C.D$ term with each other term to give

$$V = A.B.C + A.B.D + A.C.D + B.C.D$$

which can be implemented from 3-input AND gates and one 4-input OR gate.

10.

(a) Use de Morgan's theorem on the answer to Q9.

$$\begin{aligned} V &= A.B.C + A.B.D + A.C.D + B.C.D \\ &= \overline{\overline{(A.B.C)}.\overline{(A.B.D)}.\overline{(A.C.D)}.\overline{(B.C.D)}} \end{aligned}$$

(b) Write down a new expression for $\overline{V}$.

$$\begin{aligned} \overline{V} &= \overline{A}.\overline{B} + \overline{A}.\overline{C} + \overline{A}.\overline{D} + \overline{B}.\overline{C} + \overline{B}.\overline{D} + \overline{C}.\overline{D} \\ \Rightarrow V &= \overline{\overline{(A+B)} + \overline{(A+C)} + \overline{(A+D)} + \overline{(B+C)} + \overline{(B+D)} + \overline{(C+D)}} \end{aligned}$$

11.

To define an OR gate.

```
entity OR2 is
  port(A, B :  in BIT;
       Y    :  out BIT);
end OR2;

architecture GOR2 of OR2 is
begin
  Y <= (A or B);
end GOR2;
```

To implement
$Z = \overline{\overline{(A+B)} + \overline{(B+\overline{C})}}$.

```
entity ZVAL is
  port(A, B, C :  in BIT;
       Z       :  out BIT);
end ZVAL;

architecture FIG3 of ZVAL is
  signal P, Q, R : BIT;
begin
  N1:entity NOR2(NO2M) port map(A,B,P);
  I1:entity INV(IMOD) port map(C,R);
  N2:entity NOR2(NO2M) port map(B,R,Q);
  O1:entity OR2(GOR2) port map(P,Q,Z);
end FIG3;
```