Engineering **FIRST YEAR**

Part 1A Paper 3 : Electrical and Information Engineering

DIGITAL CIRCUITS AND INFORMATION PROCESSING

EXAMPLES PAPER 1

∗ Harder questions. † Straightforward questions.

† 1. Complete the truth tables for the logic circuits in Figures 1 and 2.

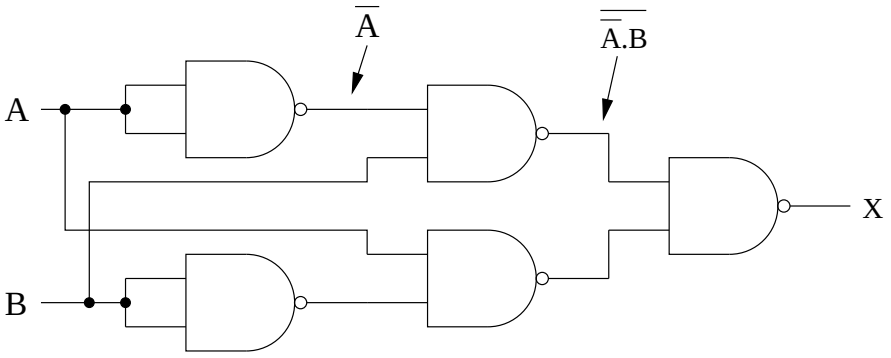


Figure 1:

Inputs		Table for Figure 1				
A	B	$\overline{A}$	$\overline{\overline{A}.B}$			X
0	0					
0	1					
1	0					
1	1					

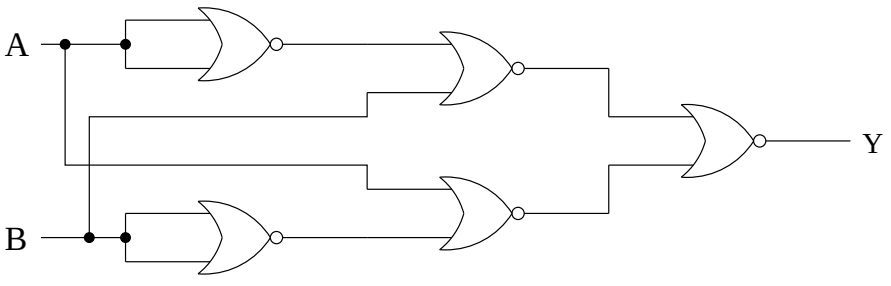


Figure 2:

Inputs		Table for Figure 2				
A	B	$\overline{A}$	$\overline{\overline{A}+B}$			Y
0	0					
0	1					
1	0					
1	1					

† 2. Find the state of inputs A, B and C for which the circuit of Figure 3 has output Z at logic 1.

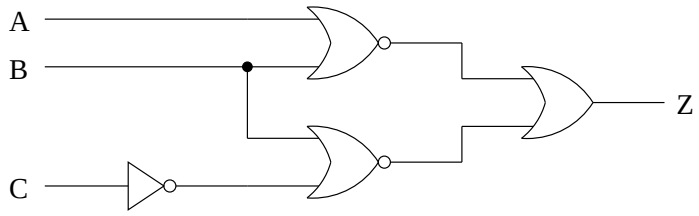
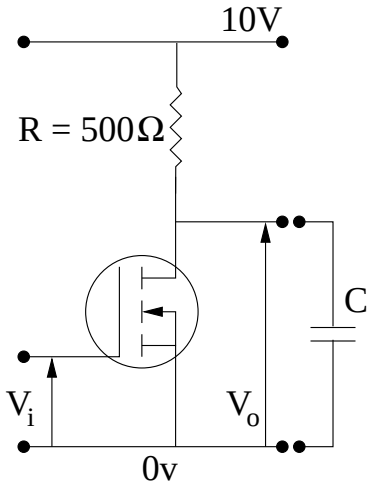
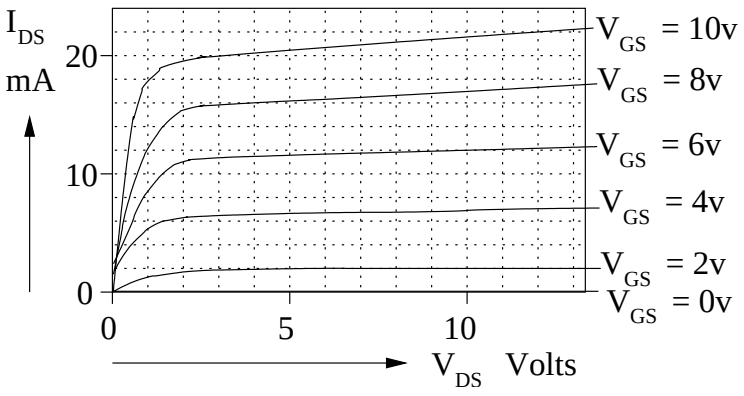


Figure 3:

3. The NMOS field-effect transistor with characteristics shown in Figure 4(b) is connected into the inverter circuit shown in Figure 4(a).



(a)



(b) NMOS Characteristics

Figure 4:

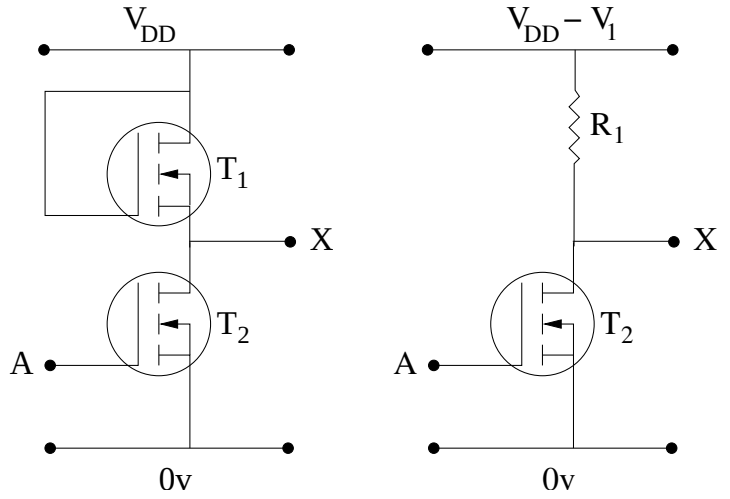
(a) Draw a load line on Figure 4(b) and determine the output voltage V_o corresponding to input voltages of 0V and +10V.

(b) Calculate the power dissipated in the 500Ω resistor and the transistor for each input voltage.

(c) The capacitor C is now connected to the output of the circuit, as shown in the figure. V_i is initially 10V. At time $t = 0$, V_i falls to 0V, switching the transistor off. Show that V_o as a function of time is $10 - 9\exp(-t/(CR))$. If $C = 40$pF, find the time for V_o to rise from 1V to 8V.

4. Figure 5(a) shows a NMOS gate where a second transistor T_1 replaces the load resistor. The characteristics of T_1 are identical to that shown in Figure 4(b). Using the fact that $V_{DS} = V_{GS}$ for this transistor, construct a graph showing the relationship between V_{DS} and I_{DS} for T_1.

Show that T_1 is equivalent to a voltage drop V_1 in series with a resistor R_1, so that the circuits of Figures 5(a) and 5(b) are identical. Find V_1 and R_1.



(a) (b)

A	T_2	X
0	OFF	1
1		

(c)

Figure 5:

Draw a new load line on Figure 4(b) to represent the possible working points of T_2. Assume $V_{DD} = 10$V, and hence find the output voltage X corresponding to input voltages of 2V and 10V.

The table shown in Figure 5(c) summarises the operation of the circuit; complete the second line.

† 5. Figures 6(a) and 6(b) show simple extensions of the inverter circuit of Figure 5(a). By completing the tables,

Inputs		Table for (a)		
A	B	T_2	T_3	X
0	0			
0	1			
1	0			
1	1			

Inputs		Table for (b)		
A	B	T_4	T_5	Y
0	0			
0	1			
1	0			
1	1			

determine what function the outputs X and Y are of the inputs A and B.

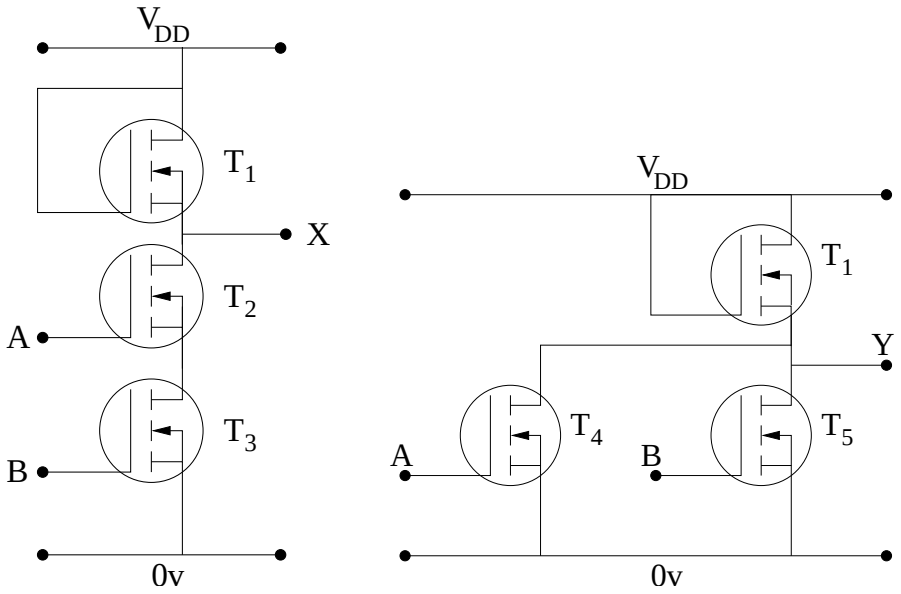


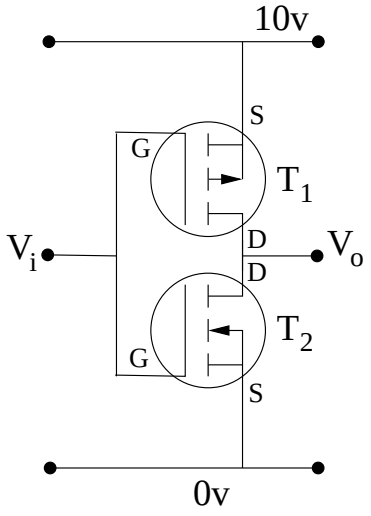
Figure 6:

∗ 6. A CMOS (Complementary MOS) inverter circuit is shown in Figure 7(a) in which the 500Ω resistor of Figure 4(a) has been replaced by a PMOS transistor T_1 with characteristics shown in Figure 7(b). The characteristic of the NMOS transistor is repeated as Figure 7(c).

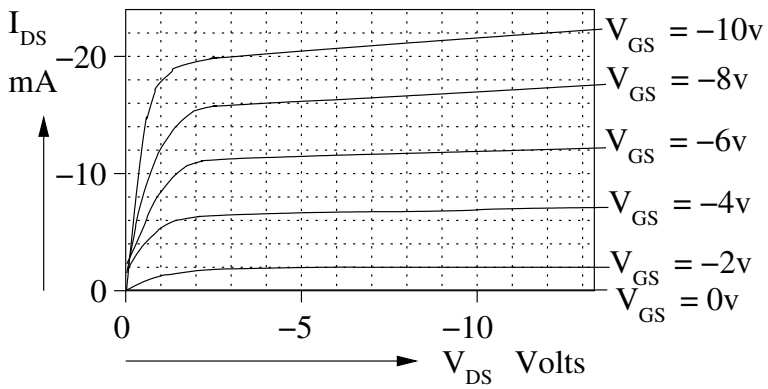
(a) Determine the output voltages V_o corresponding to input voltages V_i of 0V and 10V (Low and High inputs).

(b) Check that the power dissipated in each transistor for high and low inputs is negligible.

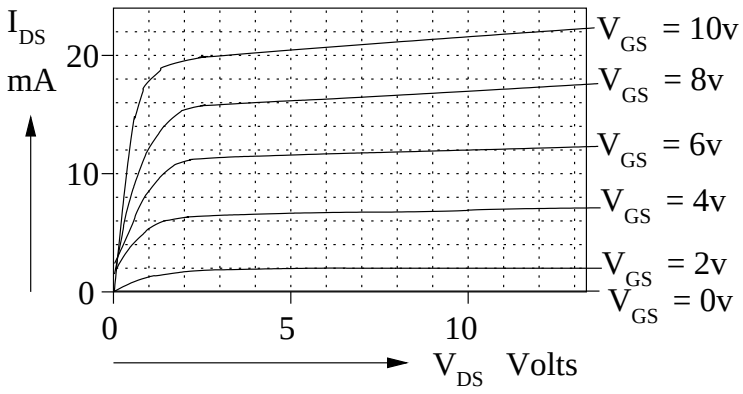
(c) If, due to a faulty lead, the input is floating and becomes +4V, determine V_o, the power dissipated in each transistor, and the power taken from the supply.



(a)



(b) PMOS Characteristics



(c) NMOS Characteristics

Figure 7:

7. Use Boolean algebra to prove the following identities:

$$\begin{aligned} A.B.C + A.B.\overline{C} &= A.B \\ A.(\overline{A} + B) &= A.B \\ A.B + \overline{A}.C &= (A + C).(\overline{A} + B) \\ (A + C).(A + D).(B + C).(B + D) &= A.B + C.D \end{aligned}$$

† 8. The circuit of Figure 8 does not make efficient use of logic gates. Write a Boolean expression for Z and hence show how Z can be realised more simply.

9. A logic 'voter' circuit has four inputs A, B, C, D and one output V. The output is to be logic 1 if any three or all four inputs are at logic 1. Design a circuit using AND and OR gates to satisfy this requirement.

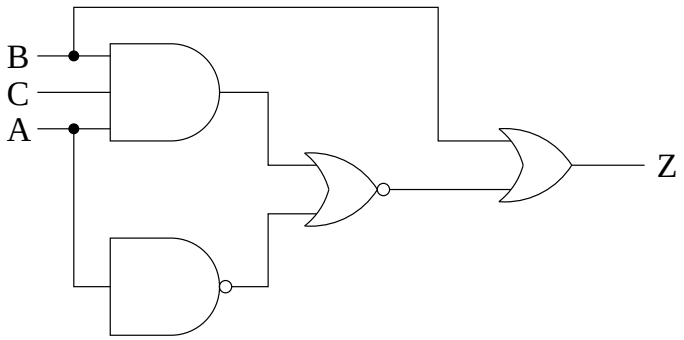


Figure 8:

∗ 10. Devise circuits to solve question 9 if

(a) NAND gates only;

(b) NOR gates only are to be used.

HINT for part (b): consider when no output is wanted from the circuit and write a new Boolean expression. Then use de Morgan's theorem.

11. Following the examples on pages 67 and 68 of handout 1, write a VHDL definition of an OR gate.

Using this definition, and the gates defined in the handout, produce a VHDL description of the circuit shown in Figure 3.

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Lent 2019

Revision tripos questions: 2012 Paper 3 Question 6
2014 Paper 3 Question 6
2016 Paper 3 Question 6
2017 Paper 3 Question 6 .

ANSWERS

1.

Inputs		Outputs	
A	B	X	Y
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

2. $Z = 1$ for ABC in the states 000, 001 and 101.

3. 10V, 1V, 0mW, 0mW, 162mW, 18mW, 30.1ns.

4. 1.5V, 395Ω, 8V, 1.2V, 1 ON 0.

5. NAND, NOR.

6. 10V, 0V, approx 9V, 63mW, 7mW, 70mW.

8. $Z = A + B$

9. $V = A.B.C + A.B.D + A.C.D + B.C.D$

10.

$$V = \overline{\overline{(A.B.C)}.\overline{(A.B.D)}.\overline{(A.C.D)}.\overline{(B.C.D)}}$$

$$V = \overline{\overline{(A+B)} + \overline{(A+C)} + \overline{(A+D)} + \overline{(B+C)} + \overline{(B+D)} + \overline{(C+D)}}$$