1A Analyzer of cets +der Ex #3 CRIBO Q1 a) DC -> NO C + Cc = open cct =) upt Vn => put duider Rin

Ro+Rin

Ro = Un ar Rn = (MN)/kn

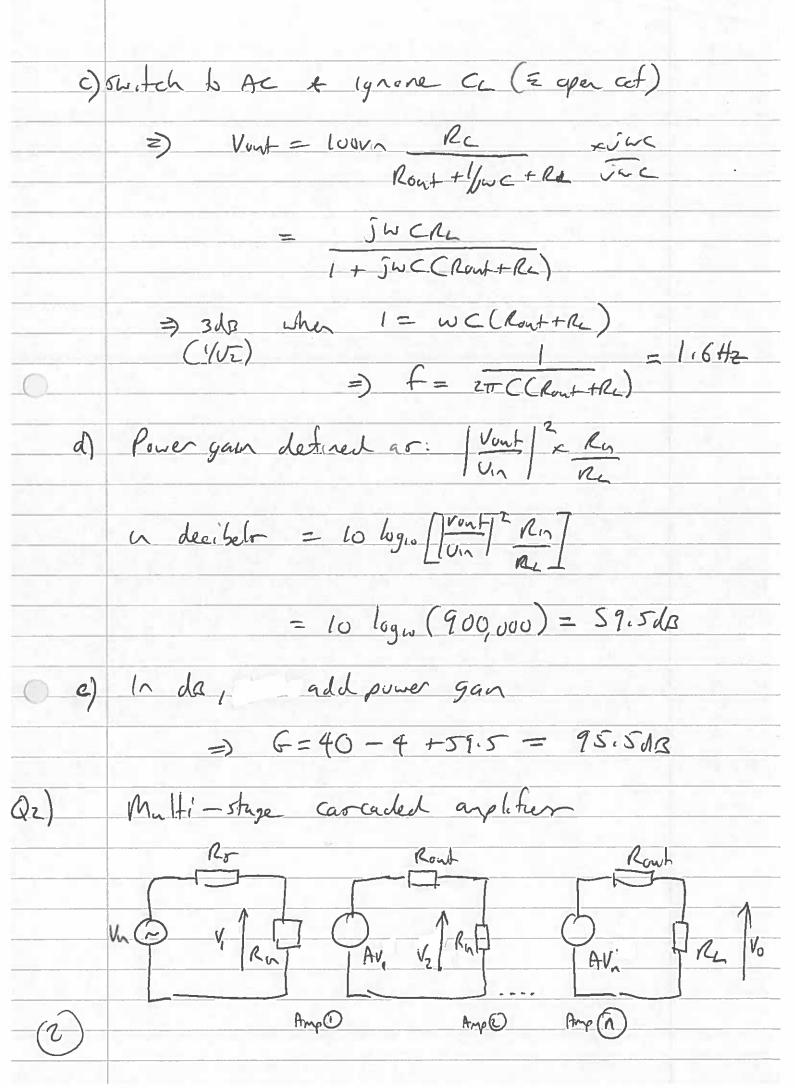
=) V'= Vin Ro+Rin b) Include CI/Re = Re/jwa jwa = Re

Re+/jwa jwa 1+jwar From Midband (a) Vont = 100 vn Rout + Re Replate Re with Rell Re => Un = 100 Re/1/10 CRC x1+j'10 CLRC

Vont

Rout + Re/ 1+jw CcRc

(1+jw CcRc) = LOURL (AtiB) De=D Re+(ItjwcaRe) Rout (CtjD) at3/b. => Re+Rout = WCLReRunt => f= Re+Rout =980htz



At input V' = Rin Vin 1st amp cutput to 2nd amp uput V2 = Av. Rin
Rn+Ront Thir then repeats no timer till the last Vo = Rc AVA
Rout + Re = Total gain of the carcade G= Vo = (Rn / Rn+Rout) ARL

Rout + RL the Input voltage Vn = InVp-p = 0.5 mVp Vo required = 1 Vp 22d3 -> A= 12.59 per stage

=> Gan = /0.5x10-3 = 2000 =) 2000 = (100 K) (100 K 12.59) N-1 (12.59 x 100 h)

10 K+100 K) (100 K+1 /2) (12.59 x 100 h) =0.91 × (12.47) (12.47) (12,47) = 2000 = 2198 =) N = 3,05 can add a but of cooks gain to I stage.

(3)

Qz Each stage has to own DC basing an we do not want DC convento between oftager, have tra we add a capacifor between each stage to block to DC and allow AC signal to poor between otager VN @ VI PM AVI This is in fact the same situation as in Or part (c) where C is acting as a & decoupling capacitor between each stage, but R=Ris from =) f = 2TC(Rout +Rin) f= 100Hz => (= 2T x 100 x (100 x 12 + 1x 103) = 1.58 x10 -8 F (15,8 NF) frequency lear than courte to reduce the effect of the USZ attenuation at the 3ds freq. (4) ~ 70 Hz

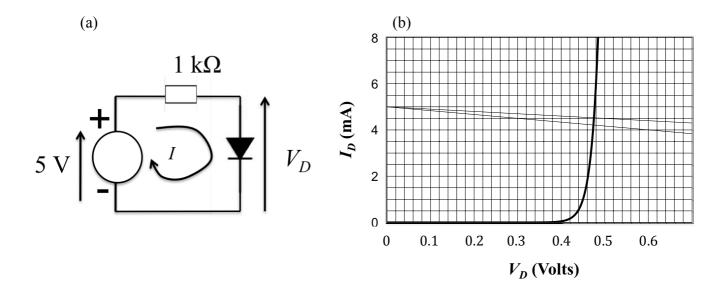
3. Use 
$$R = \frac{\rho l}{A}$$
,  $= R = \frac{\rho \times 100 \times 10^{-6}}{10 \times 10^{-6} \times 1 \times 10^{-6}} = 10^7 \rho$ 

Copper,  $\rho = 1.7 \times 10^{-8} \Omega m => R = 0.17 \Omega$ 

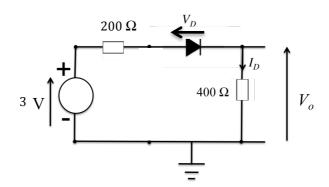
Current, 
$$I = V/R = \frac{1 \text{ V}}{0.17 \Omega} = 5.88 \text{ A}$$

Power, P = VI = 5.88 W.

4. Draw the load-line, using the relationship  $V_D = 5\text{-}1000I_D$ . =>  $I_D = 5\text{x}10^{-3} - V_D/1000$ , or  $I_D$  (mA) =  $5\text{-}V_D$  (mV) [this is the upper line shown below]. This intercepts the diode curve at  $I_D = 4.5$  mA,  $V_D = 0.475$  V.



5. Replace the battery and the 600  $\Omega$  and 300  $\Omega$  resistors with their Thevenin equivalent to simplify the circuit:



$$V_0 = 400I_D$$

Applying Kirchoff's voltage law around the loop, we obtain:

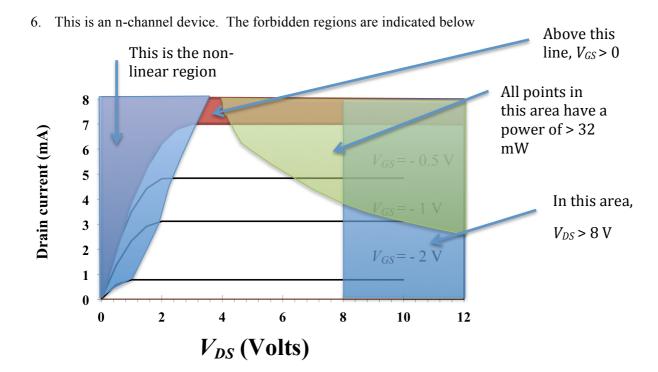
$$3 - 200I_D - V_D - 400I_D = 0$$
 .....there will be a voltage *drop* across the diode.

$$=> I_D = \frac{3}{600} - \frac{V_D}{600}$$

From which we find that  $I_D$  (mA) = 5 – 1.66 $V_D$  (mV)

This is the lower line on the diode curve, from which we find that at  $I_D = 4.25$  mA,  $V_D = 0.4$  V. The output voltage,  $V_0 = 400I_D = 1.7$  V.

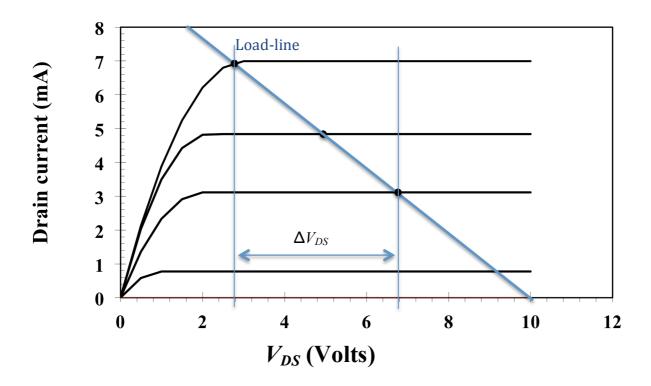
## **FET Amplifiers**



7. The operating point is P, where VDS = 5 V,  $V_{GS}$  = - 0.5 V,  $I_D$  = 4.8 mA.

(i) The voltage across  $R = 10 \text{ V} - V_{DS} = 5 \text{ V}$ .

 $=> R = 5V/4.8 \text{ mA} = 1.042 \text{ k}\Omega.$ 



- (ii) From the load-line, when  $V_{GS}$  changes between 0 & 1 V, the load-line intercepts move to  $V_{DS} = \sim 2.8$  V and 6.8 V. Therefore, the change in  $V_{DS}$  is 4 V. The gain is (change in  $V_{DS}$ )/(change in  $V_{GS}$ ) = 4.
- 7 8. The operating point is the same as before, so the voltage across  $R_2$  is 0.5 V ( $V_{GS}$ ).
- $\Rightarrow$  R<sub>2</sub> = 0.5 V/4.8 mA = 104.2 Ω.

The voltage across  $R_1$  is 10 V - 5 V - 0.5 V = 4.5 V, =>  $R_1 = 4.5 \text{ V}/4.8 \text{ mA} = 937.5 \Omega$ .