Part 1A Paper 3 : Electrical and Information Engineering

DIGITAL CIRCUITS AND INFORMATION PROCESSING

EXAMPLES PAPER 2

* Harder questions.   † Straightforward questions.

† 1.   Using a Karnaugh map, write simple sum of products expressions for F and $\overline{F}$ where,

$$F = \overline{A}.\overline{D} + \overline{B}.\overline{C} + \overline{A}.B.\overline{C}.D$$

and $A.\overline{B}.C.\overline{D}$ is a don't care state.

† 2.   A three variable function is given by:

$$F = A.\overline{B}.\overline{C} + A.\overline{B}.C + A.B.C$$

Find the simplest sum of products form for F using a Karnaugh map. Express F using:

(a) NAND gates only;

(b) NOR gates only. (Hint: try mapping $\overline{F}$ for fewest gates.)

† 3.   The function F in question 2 can be written in the form:

$$F = 100 + 101 + 111 = \Sigma(4, 5, 7)$$

Find the simplified sum of products and product of sums forms for the four variable function G where:

$$G = \Sigma(5, 6, 7, 8)$$

and terms 10 to 15 inclusive are don't care states. Take $ABCD$ to be the four variables, with A most significant.

4.   The months of the year are coded in binary with January represented by A_3, A_2, A_1, $A_0 = (0001)$ and December by (1100). Find a simple sum of products expression in terms of A_3, A_2, A_1 and A_0 for the months without an R in their name.

Show that a simpler expression is obtained by changing the coding so January is represented by (0000) and December by (1011). What is the expression then?

5.

(a) Each gate in the circuit of Figure 1 has a propagation delay of τ. Draw a timing diagram showing the output of each gate for $A = B = 0$; and C initially 0, switching to 1 for a time t $(t \gg \tau)$, and then returning to 0. Hence show that a static hazard exists. Is it a static 1-hazard or a static 0-hazard?
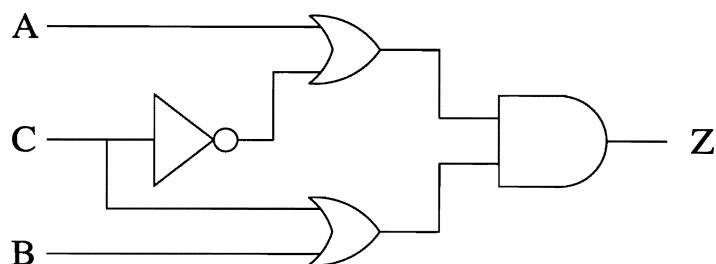
Figure 1:

(b) Write down a product-of-sums expression for Z from the circuit and use de Morgan's theorem to obtain a sum-of-products expression for $\overline{Z}$.

(c) Draw a Karnaugh map of $\overline{Z}$ and thus show how the hazard can be removed by adding one more OR gate to the circuit.

† 6.

(a) Calculate the 2's-complement 8-bit signed binary representation of the decimal numbers -38 and $+100$.

Show that the bit pattern for -38 may be added to that for $+100$ effectively forming $(100 - 38)$, and the 'right' answer interpreted if we ignore the extra 9th bit. Use your calculator to convert the 8-bit binary answer to decimal and hexadecimal.

(b) Write out the following hexadecimal sequence in binary.

2, 6, 7, 5, 4, C, D, F, E, A

Observe that only one bit changes in each step along the sequence. Show how this unit-distance sequence can be represented as a path around a 4 × 4 Karnaugh map.

* 7. A logic circuit has four inputs and four outputs. The four inputs A_1, A_0 and B_1, B_0 represent two 2-bit unsigned binary numbers. The outputs are the four bits of the product of the input numbers.

Express the logic function for each term P_3, P_2, P_1, P_0 in the product on a Karnaugh map of the four input variables.

Hence design a multiplier circuit using 4-input NAND and inverter gates only.

† 8. A three-bit ripple counter is shown in Figure 2. The counter input is a square wave of period T. Each J-K master-slave flip-flop changes state a finite time after the falling edge of the signal applied to its clock input. Assuming this delay is finite but much smaller than T, find all the possible states of the counter by drawing a timing diagram showing the outputs of the three flip-flops. Start with $Q_0 = Q_1 = Q_2 = 0$.
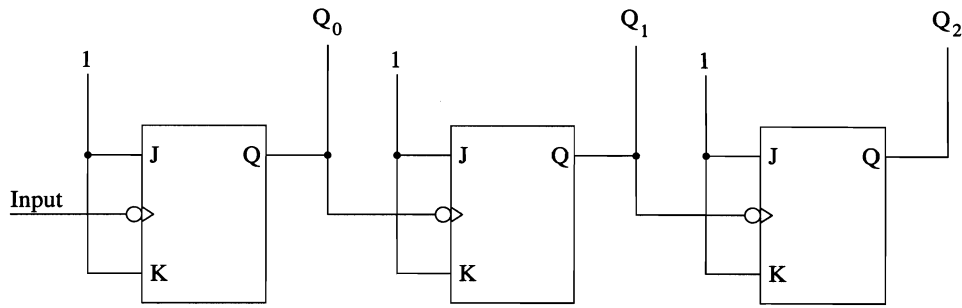
Figure 2:

9.   The input to the first stage of a five-stage register is obtained from the exclusive-or function of the outputs of the 3rd and 5th stages. Consider at the start that all 5 stages have a 1 output which shifts right on each clock pulse. What is the output sequence expressed as a decimal number, taking the right (5th) stage as the least significant bit? After how many clock pulses does it repeat?

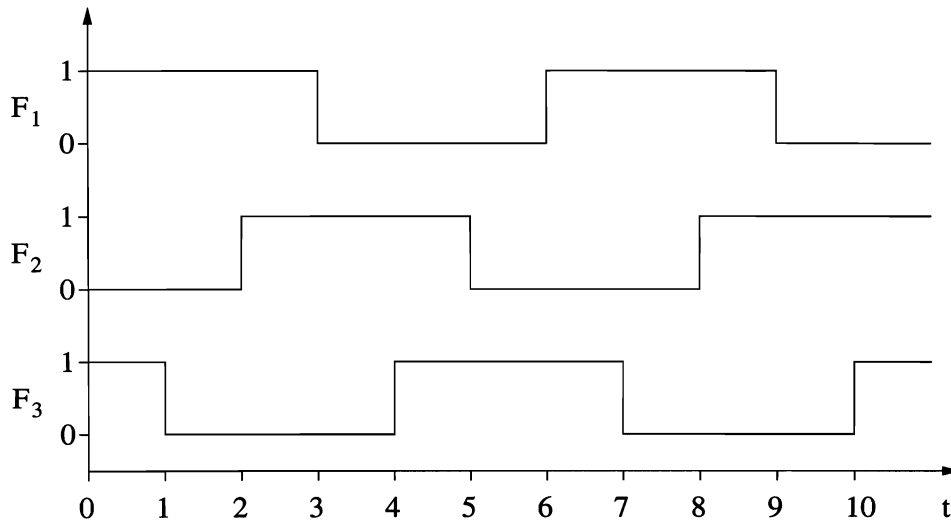What happens if all 5 stages have 0 set on them at the start?

Figure 3:

* 10.   A shift register has the output of the last stage connected as input to the first. The output of the first stage and two other stages are to be waveforms shown in Figure 3. How many stages are required? What should the register contents be for $0 < t < 1$? Which stage outputs form F_2 and F_3?

* 11.   A Johnson counter is formed by connecting the complement of the output of the last stage of a 4-stage shift register to its input. Show that two output sequences are possible.
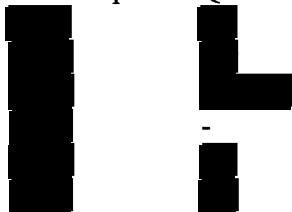
A 5-stage Johnson counter is to be used as a decimal counter. What initial states of the five

3

stages will not produce a ten state count.

A decimal Johnson counter uses (ABCDE)=(00000) to represent zero, 10000 to represent 1 etc. A combinational logic circuit is required which has the counter stage states as inputs and forms one output for each of the numbers 0–9. Show that the logic function for 1 can be reduced to $A.\overline{B}$ and find the function for 5 and 9.

ANSWERS

1.

$$F = \overline{A}.\overline{C} + \overline{B}.\overline{C} + \overline{A}.\overline{D}$$
$$\overline{F} = A.B + C.D$$

2.

$$F = \overline{\overline{(A.\overline{B})}.\overline{(A.C)}} = \overline{A} + \overline{(\overline{B} + C)}$$

3.

$$G = A.\overline{D} + B.C + B.D \text{ or } (A + B).(A + C + D).(\overline{A} + \overline{D})$$

4.

$$F_{\text{first code}} = A_1.A_2 + A_0.A_2 + \overline{A_0}.\overline{A_1}.\overline{A_2}$$
$$F_{\text{second code}} = A_2$$

5.

$$Z = (A + \overline{C}).(B + C).(A + B)$$

6.   11011010   01100100   00111110

7.

$$P_0 = \overline{A_0.B_0}$$

$$P_1 = \overline{(\overline{A_0}.A_1.B_0).(A_0.\overline{A_1}.B_1).(A_0.\overline{B_0}.B_1).(A_1.B_0.\overline{B_1})}$$

$$P_2 = \overline{(\overline{A_0}.A_1.B_1).(A_1.\overline{B_0}.B_1)}$$

$$P_3 = \overline{A_0.A_1.B_0.B_1}$$

8.   <u>000</u>, <u>001</u>, 000, <u>010</u>, <u>011</u>, 010, 000, <u>100</u>, <u>101</u>, 100, <u>110</u>, <u>111</u>, 110, 100

9. $31, 15, 7, 3, 17, 24, 12, \ldots, 25, 28, 30$ 00000 remains at 00000.

10.   6 stages, outputs from the first, third and fifth.

11.   10101, 01010 $A.E, \overline{D}.E$