

1 A P3/4 Examples Cmos

i) $g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS}}$ from graph $\approx 4.6 \text{ mS}$

$r_d = \left. \frac{1}{\frac{\partial I_D}{\partial V_{DS}}} \right|_{V_{GS}} \approx 40 \text{ k}\Omega$

Depletion mode as V_{GS} is -ve (could also be a JFET)

ii) Operating point P $V_{GS} = -1 \text{ V}$

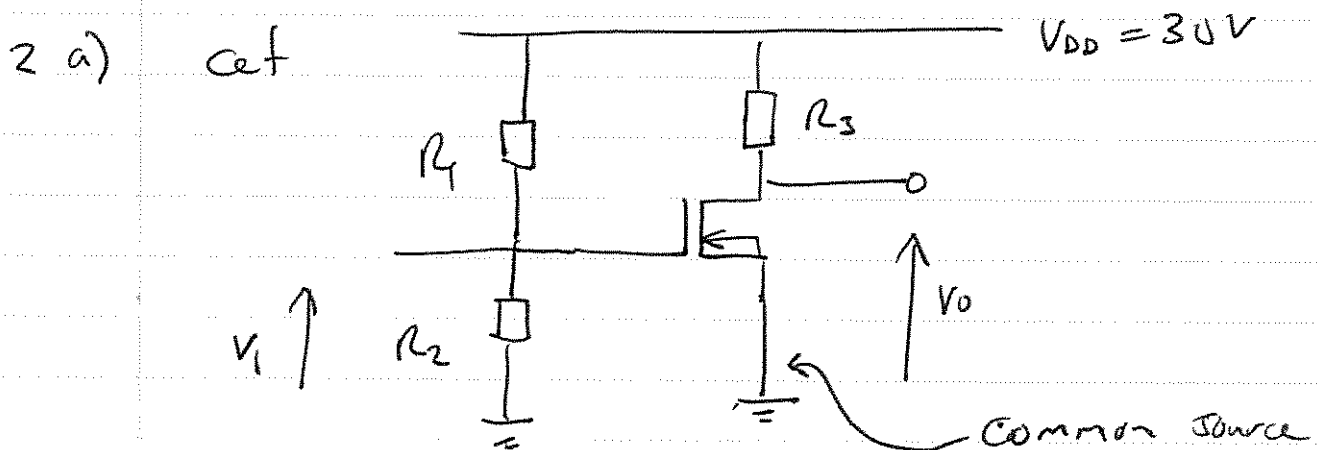
$\Rightarrow V_G = -1 \text{ V}$

$R_1 = 1 \text{ M}\Omega$ (or suitably large R to set R_{in} of the amplifier)

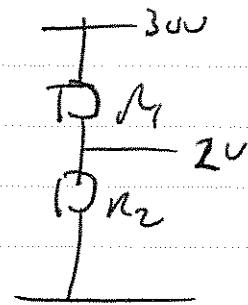
$I_{D0} = 4 \text{ mA}$ $V_{DS} = 10 \text{ V}$

$\Rightarrow R_D = \frac{20 - 10}{4 \times 10^{-3}} = 2.5 \text{ k}\Omega$

From the 55m $R_c = R_d$ $R_3 = R_D$
 $R_2 = r_d$



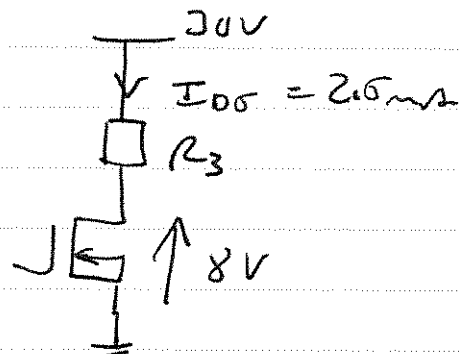
b) P.D. at input to gate



$$\Rightarrow \frac{R_2 \times 30}{R_1 + R_2} = 2$$

$$\Rightarrow \frac{R_1}{R_2} = 14$$

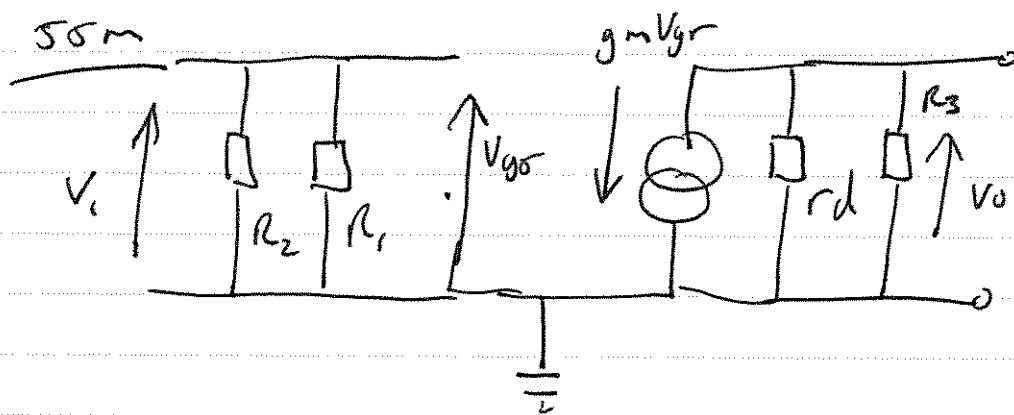
Drain resistor R_3



$$\Rightarrow \frac{30 - 8}{R_3} = 2.5 \times 10^{-3}$$

$$R_3 = 8.8 \text{ k}\Omega \quad (8.2 \text{ k}\Omega \text{ std val})$$

c)



$$G_{A_{un}} = \frac{V_o}{V_i} \quad \text{At input } V_i = V_{gs}$$

$$\text{at output } \frac{0 - V_o}{r_d \parallel R_3} = g_m V_{gs}$$

$$\Rightarrow V_o = -g_m V_{gs} R_{o \parallel r_d} \Rightarrow \frac{V_o}{V_i} = -g_m R_3 \parallel r_d$$

$$= 4 \times 10^{-3} \times \frac{8.8 \text{ k}\Omega \times 10 \text{ k}\Omega}{8.8 \text{ k}\Omega + 10 \text{ k}\Omega}$$

$$= -18.7$$

d) From 50m $R_{in} = \frac{V_1}{I_1} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$

If $R_{in} = 100k\Omega$ & $R_1/R_2 = 14$

$\Rightarrow R_2 = 107k\Omega$ $R_1 = 1.5M\Omega$

nb R_2 is not a standard value. If we choose $R_1 = 100k\Omega$ then $R_1 \parallel R_2 < 100k\Omega$ which does not fit the brief. If we choose $R_2 = 120k\Omega$ (std value) then $R_1 = 1.7M\Omega$ ($1.8M\Omega$ std value)

This would give $V_{DS} = 1.875V$ (should be ok)

$R_{in} = 112.5k\Omega$ (meets spec)

3) This is a self biasing FET circuit. By setting the DC value of V_S to be 3V higher than V_G we can set $V_{GS} = -3V$

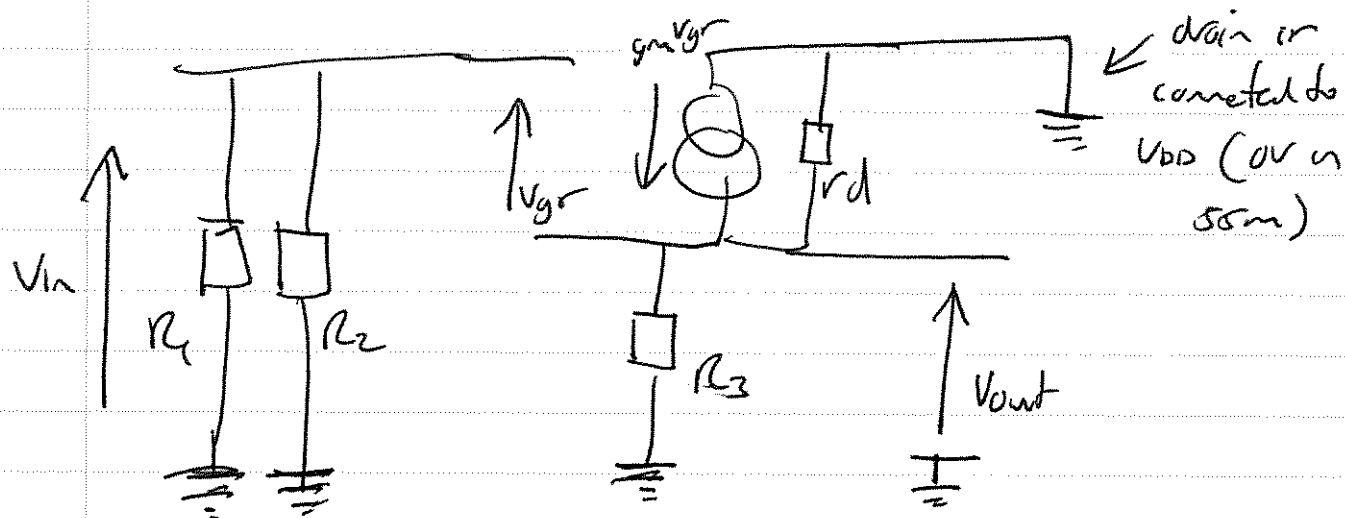
\Rightarrow at source $V_S = 20 - V_{DS} = 13V$

$I_{DS} = \frac{V_S - 0}{R_S} \Rightarrow R_S = \frac{13}{2.6 \times 10^{-3}} = 5k\Omega$

We want $V_{GS} = -3V \Rightarrow V_G = 10V$

P.D. at gate $V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} \Rightarrow R_2 = 2M\Omega$

- b) ssm — draw it as it appears in the ckt starting with the FET



- c) at input we can see that

$$V_{in} = V_{gs} + V_{out}$$

At output we see that r_d is in parallel with R_3 hence the current source is pushing the current through $r_d \parallel R_3$

$$\Rightarrow V_{out} = g_m V_{gs} R_3 \parallel r_d$$

Combine to get

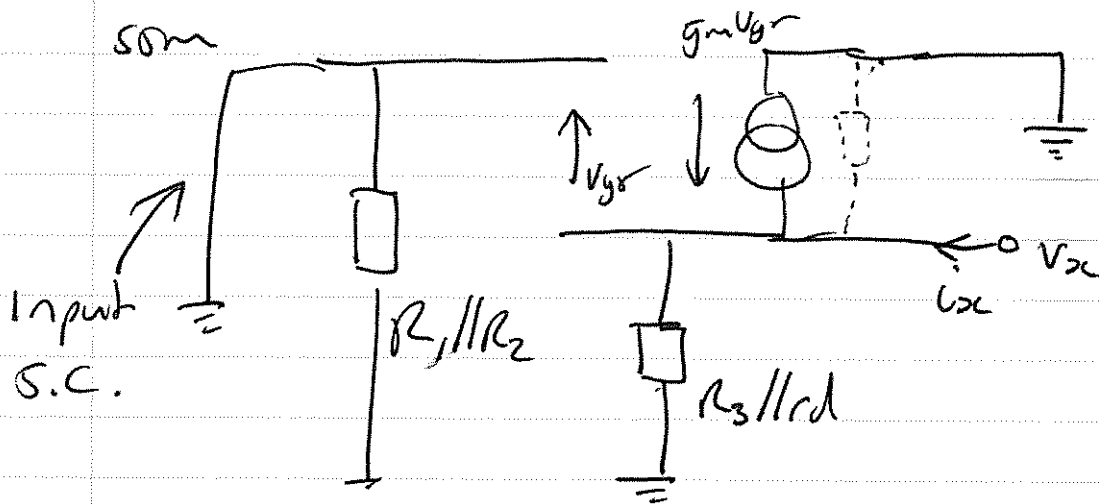
$$\frac{V_{out}}{V_{in}} = \frac{g_m R_3 \parallel r_d}{1 + g_m R_3 \parallel r_d} = 0.958 \approx 1$$

$$R_{in} = \frac{V_i}{I_i} = R_1 \parallel R_2 \approx 1 \text{ M}\Omega$$

3c (cont) When calculating R_{out} be careful as $R_{out} \neq r_d \parallel R_3$

To find R_{out} we apply a test voltage V_x at the output & measure the current i_x with the input short ~~at~~ circuited.

$$R_{out} = \frac{V_x}{i_x} \bigg|_{i/p \text{ sc}}$$



At the input we see that $V_{gs} = -V_x$

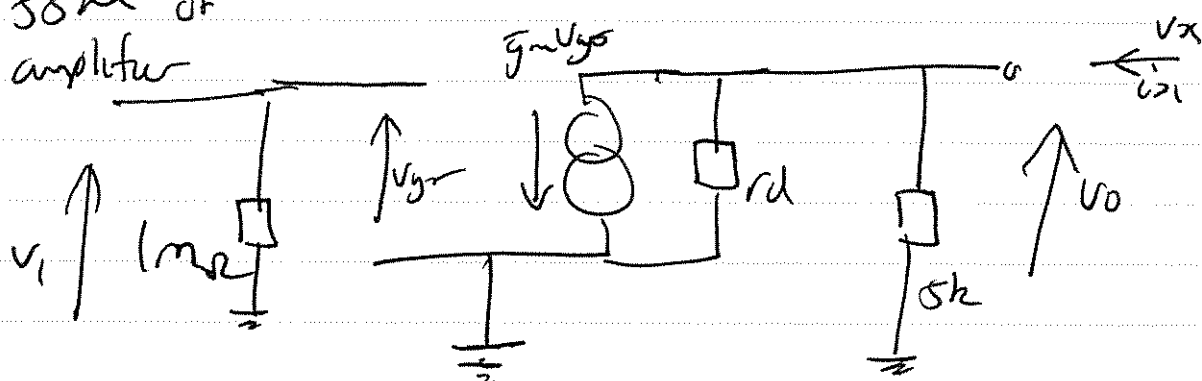
Sum currents at output

$$i_x + g_m V_{gs} = \frac{V_x - 0}{R_3 \parallel r_d} \quad \leftarrow \text{out}$$

$$\Rightarrow \frac{V_x}{i_x} = \frac{R_3 \parallel r_d}{1 + g_m R_3 \parallel r_d} = 192 \Omega$$

4)

50mV at
amplifier



Need to calculate R_{out} for amplifier

$$\Rightarrow R_{out} = \frac{v_x}{\frac{v_x}{i_x}} \parallel 5k\Omega$$

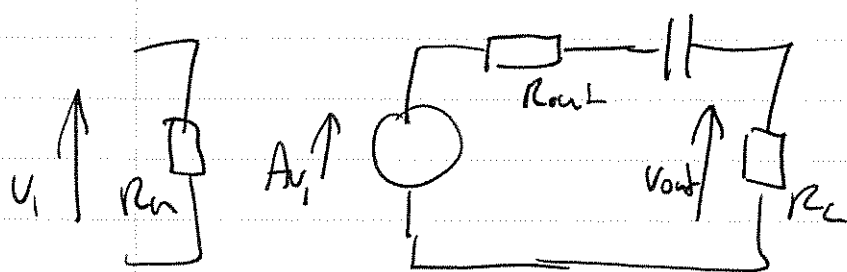
if $v_i = 0$ ($1/p\Omega$) then $v_{gs} = 0$

$$\Rightarrow v_{gs} g_m = 0$$

$$\Rightarrow \frac{v_x}{i_x} = r_d \parallel 5k\Omega$$

$$\Rightarrow R_{out} = 3.33k\Omega$$

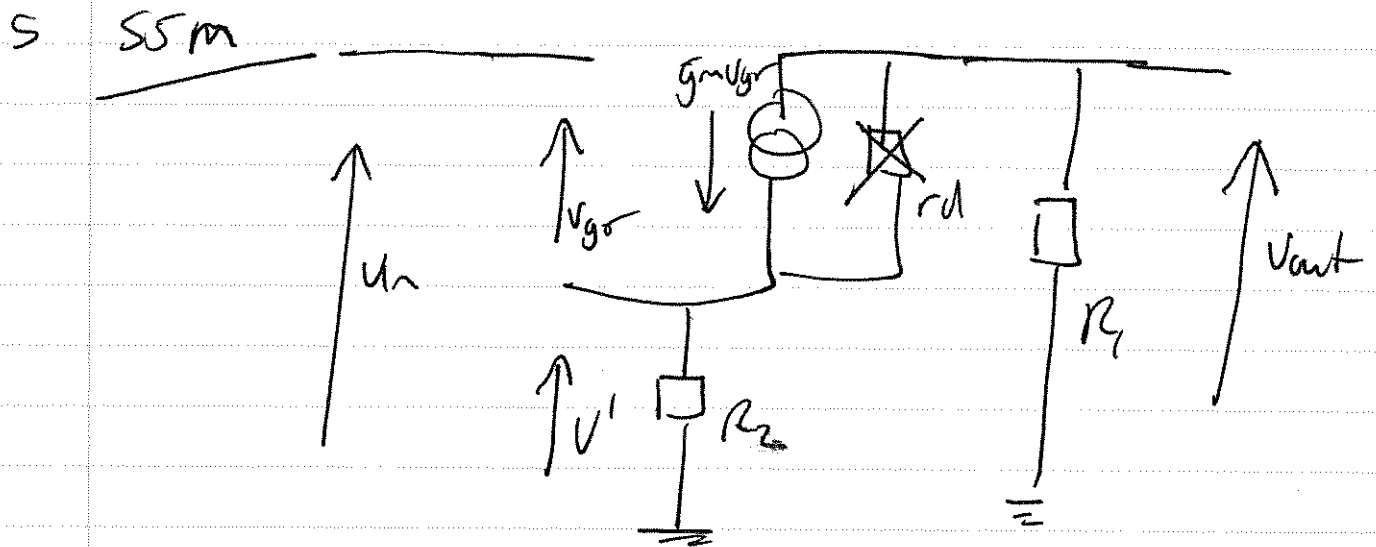
We can now use the amplifier model:



From data book & earlier lecture we can find the $1/\Omega$ or 3dB frequency

$$f = \frac{1}{2\pi C(R_L + R_{out})}$$

$$\Rightarrow C = 2.08\mu F \quad (3dB \text{ point})$$



Remove $r_d (\infty)$

at input $V_{in} = V_{gs} + V'$ (1)

at output $\frac{0 - V_{out}}{R_L} = g_m V_{gs}$ (2)

at source $V' = g_m V_{gs} R_S$ (3)

Combine (1) (2) & (3) to get the gain

$$\frac{V_{out}}{V_{in}} = \frac{-g_m R_L}{1 + g_m R_S} \leftarrow R_S \text{ reduces gain}$$

If we include capacitor C then replace R_S with Z , where:

$$Z = R_S // C = \frac{R_S}{1 + j\omega C R_S}$$

Substitute into above equation for the gain

$$\frac{V_{out}}{V_{in}} = \frac{-g_m R_1}{1 + \frac{R_1}{1+j\omega C R_2}} \times \frac{(1+j\omega C R_2)}{(1+j\omega C R_2)}$$

$$= \frac{-g_m R_1 (1+j\omega C R_2)}{1 + g_m R_1 + j\omega C R_1 R_2}$$

R_2 is required for the biasing to define the operating point (as in Q3) but it reduces the overall gain. The solution is to bypass R_2 with a suitable capacitor C to remove R_2 from the sum at suitable frequencies

$$\Rightarrow \frac{V_{out}}{V_{in}} = -g_m R_1 \quad (R_2 \text{ bypassed})$$

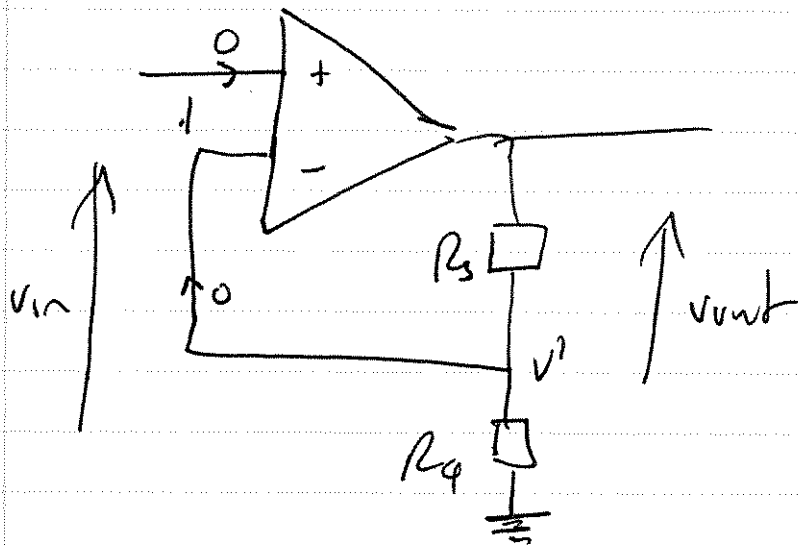
$$\text{At } f = 1.59 \text{ Hz} \quad \text{Gain} = -9$$

$$f = 159 \text{ Hz} \quad \text{Gain} = -53$$

$$f = 15.9 \text{ kHz} \quad \text{Gain} = -80$$

No the ckt is not complete. The gate voltage is not defined at DC as ~~the~~ the FET has ∞ input resistance. We need to add a resistor or potential ~~divider~~ divider at the gate to provide a suitable DC bias to set V_{GS} .

6



Op-Amp ideal

$$\Rightarrow A = \infty$$

$$V_+ = V_-$$

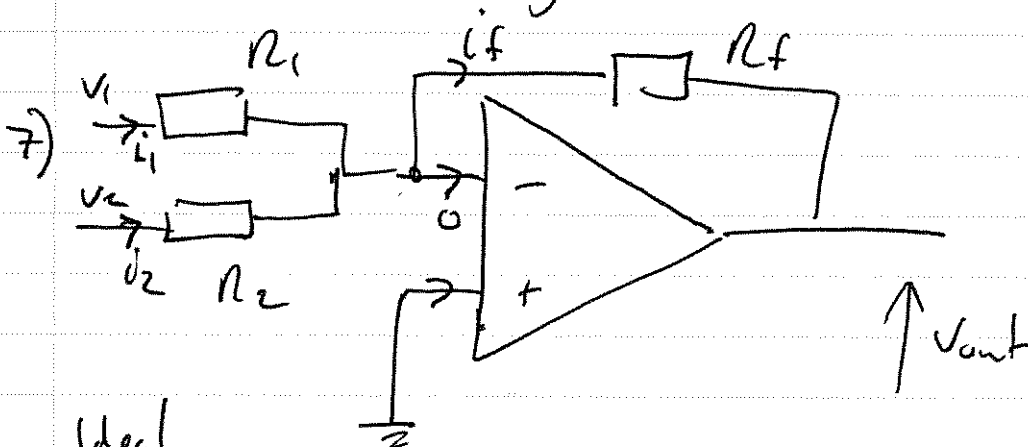
no input current
due to $R_{in} = \infty$

$$V_+ - V_- = 0 \Rightarrow V' = V_{in}$$

R_3 & R_4 form a potential divider

$$V_{out} = V_{in} \frac{R_4}{R_3 + R_4} \Rightarrow \frac{V_{out}}{V_{in}} = \frac{R_3 + R_4}{R_4}$$

\Rightarrow Non-inverting amplifier.



Ideal

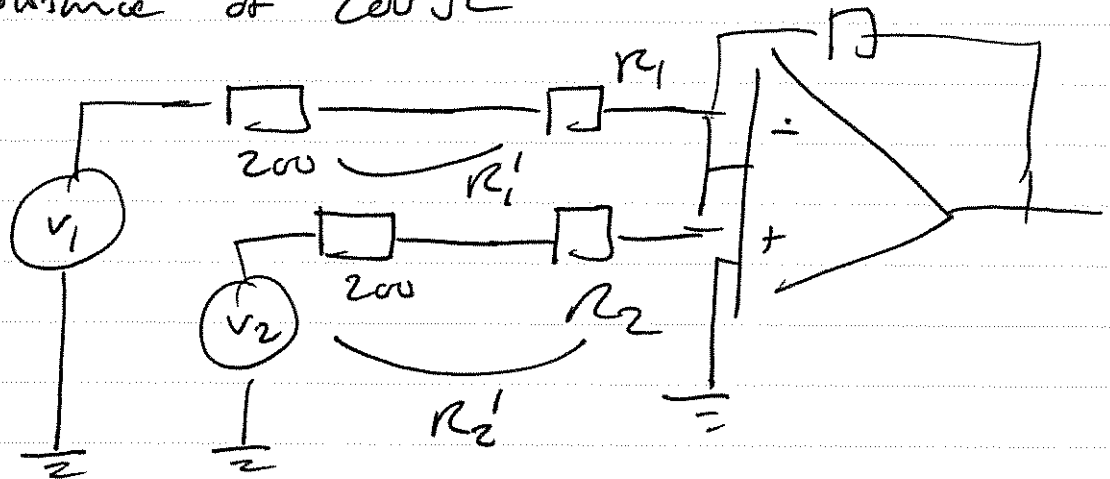
$$\Rightarrow V_+ = V_- = 0 \quad \text{no current into inputs}$$

$$\Rightarrow i_f = i_1 + i_2$$

$$\frac{0 - V_{out}}{R_f} = \frac{V_1 - 0}{R_1} + \frac{V_2 - 0}{R_2} \Rightarrow V_{out} = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2\right)$$

7 a) $R_f = 100k \Rightarrow \frac{R_f}{R_1} = 200 \quad \frac{R_f}{R_2} = 40$

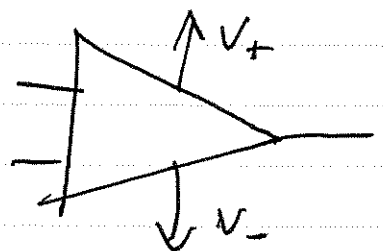
Both input sources have an internal resistance of 200Ω



$\Rightarrow \frac{R_f}{200 + R_1} = 200 \quad R_1 = 300\Omega$

$\frac{R_f}{200 + R_2} = 40 \quad R_2 = 2300\Omega$

b) Op-amp has bipolar supply



Output voltage should not exceed either $\pm V$ to avoid clipping of the output signal.

Max output voltage will occur when both v_1 and v_2 are at max (or peak) values

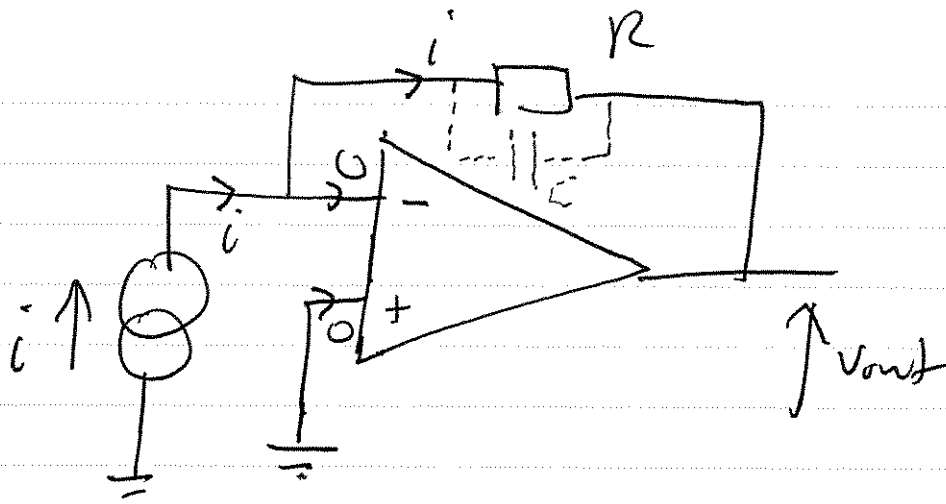
$v_1 = 10mV$

$v_2 = 50mV$

$V_{out} = 200 \times 10 \times 10^{-3} + 40 \times 50 \times 10^{-3}$
 $= 4V \quad (\text{max output})$

$\Rightarrow +V$ & $-V$ should be larger than $+4V$ & $-4V$

8)



No current at inputs

Op-amp ideal $\Rightarrow v_+ = v_- = 0V$

$\Rightarrow i'$ must travel through R

$$\Rightarrow \frac{0 - V_{out}}{R} = i'$$

$$\frac{V_{out}}{i'} = -R$$

b) Replace R with $Z = R \parallel C$

$$Z = \frac{R}{1 + j\omega CR}$$

$$\Rightarrow \frac{V_{out}}{i'} = \frac{-R}{1 + j\omega CR}$$

3dB frequency ($1/\sqrt{2}$, 70% etc) $1 = \omega CR$

$$f_z = \frac{1}{2\pi RC} = 8 \text{ kHz}$$