Part 1A Paper 3 : Electrical and Information Engineering

DIGITAL CIRCUITS AND INFORMATION PROCESSING

EXAMPLES PAPER 3

* Harder questions. † Straightforward questions.

† 1. For the arrangement of three J-K bistables shown in Figure 1, starting with $Q_A Q_B Q_C = 000$, determine how many clock pulses are needed before the circuit returns to the same state.

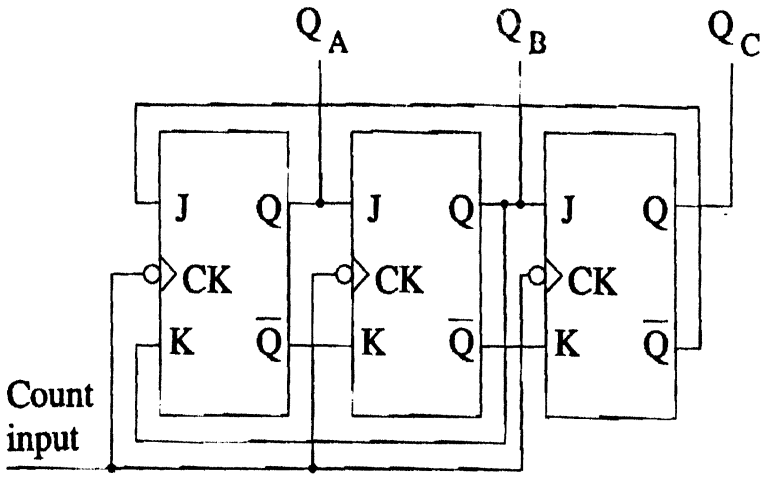


Figure 1:

2. The six states of a divide-by-six counter using three J-K bistables are shown in the left-hand column of the table below, and uses the normal binary count.

Counter state			Next state			Bistable inputs					
C	B	A	C	B	A	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	×	0	×	1	×
0	0	1									
0	1	0									
0	1	1									
1	0	0									
1	0	1	0	0	0						

The top line of the table has been completed where × denotes a 'don't care' state. Complete the table, draw Karnaugh maps for the six bistable inputs in terms of C, B and A to determine the simplest expressions for them. Hence show that the counter can be made with only two AND gates added to the bistables, provided $\overline{C}$ is available.

3. Amend the design of the divide-by-six counter in question 2 so that if the three bistables switch on with $CBA = 110$ or 111, the unused states, then in both cases they become 001 on the first clock pulse. Obtain expressions for the bistable inputs now required.

* 4. Design a divide-by-four synchronous counter which will count up when an input $Z = 0$

Bistable allocation

State	B	A
S1	0	0
S2	0	1
S3	1	0
S4	1	1

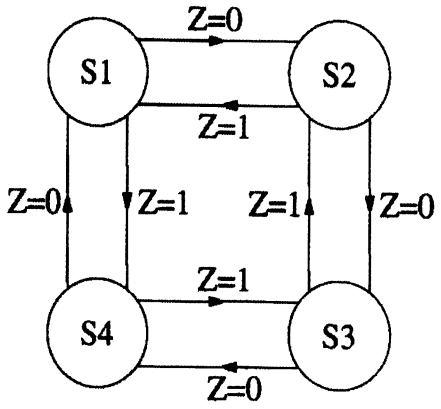
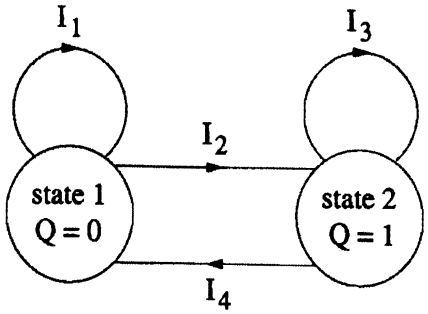


Figure 2:

and which will count down when $Z = 1$. Use the state allocation table and state diagram shown in Figure 2, and design it to use J-K bistables.

5. The figure on the right shows the state diagram for a J-K bistable. Write down the inputs I_1 to I_4 needed to complete the diagram in terms of conditions on J and K.



6. Draw the state diagram only for a system with a single input, Y, connected to a line carrying serial digital data on which it is desired to detect a sequence $Y = 0010$. The sequence 0010010 should give output twice, at the times underlined.

* 7. A sequencer is made of J-K bistables to drive the lights on a road at a pedestrian crossing in the following sequence: $RYG = 001, 010, 100, 110, 001$. A signal P, derived from a push button, controls the sequence. While $P = 0$ the lights stay in the state RYG= 001 allowing free use of the road. The sequence is driven by a special slow clock connected to the clock inputs of all the bistables. If $P = 1$ as the clock waveform rises, the sequence begins. From then on, the value of P does not matter, except that if $P = 1$ when the clock rises in the state RYG= 100, the bistables will stay in that state.

Draw the state diagram and hence decide on an appropriate number of bistables for the circuit. Draw the state table and the complete circuit diagram.

* 8. A converter to change an 8-bit code into an analogue signal is shown in Figure 3, the

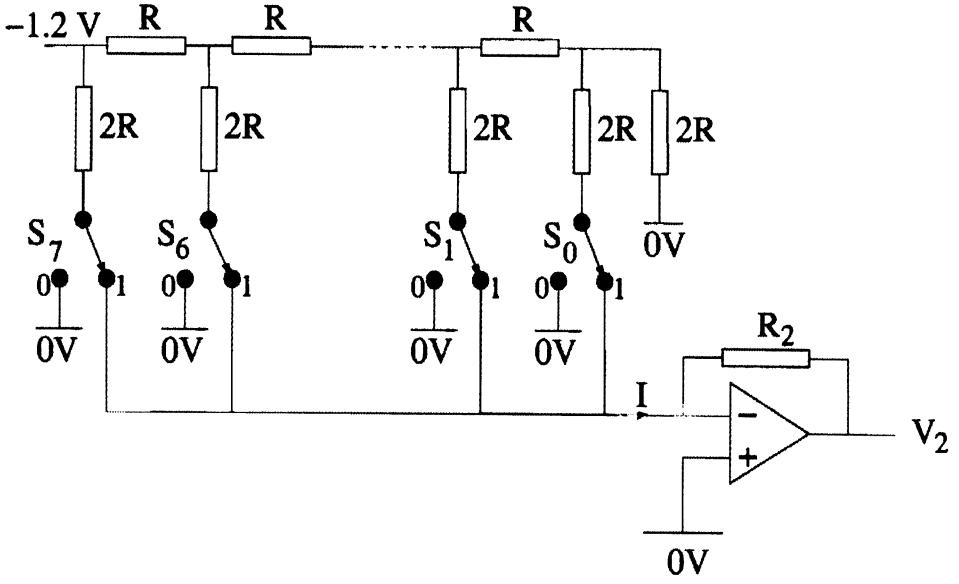


Figure 3:

amplifier has high gain and high input resistance. What value should R_2 be (in terms of R), so that a 10000000 binary code ($= 80_{16}$ or 128_{10}), set up on switches S_7 to S_0, gives an output V_2 of +5V? What outputs will then be given by 01010101_2, 100_{10}, and $A1_{16}$?

9.

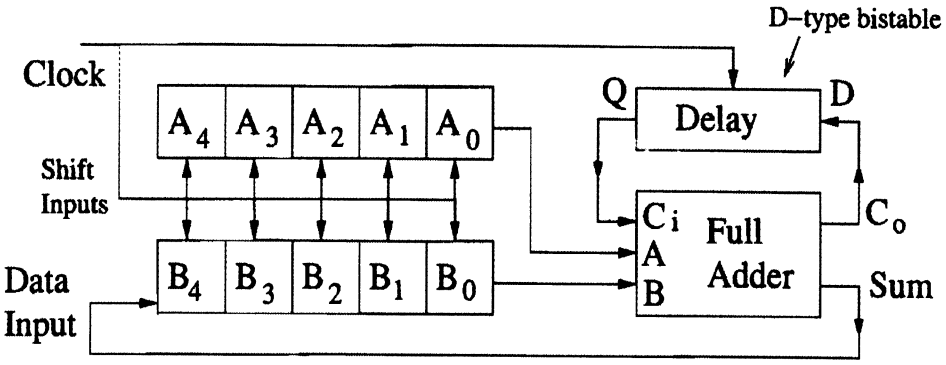


Figure 4:

(a) A serial binary adder is shown in Figure 4, having two 5-bit shift registers A and B connected to a single full adder. The two 5-bit numbers $A_4 \ldots A_0$ and $B_4 \ldots B_0$ are to be added.

Explain how the adder works if $A = 00110_2$ and $B = 00010_2$. Is B_0 or B_4 more significant? If A_4 and B_4 were both 1 at the start of the addition, what modifications would be needed to the arrangement to give a correct sum and not overflow?

(b) In Figure 4, if the A register has $\overline{A_0}$ available and that was connected to the adder input A (in place of A_0), and if Q (and hence C_i), is set to 1 at the start of "addition", what

function of A and B will result from the operation of the circuit?

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Revision Tripos Questions
2009 Paper 3 Q6, Q8

[redacted]

2013 Q9
2014 Q9
2015 Q9b
2016 Q9
2017 Q7, 9
2018 Q7, 9

ANSWERS

1. 5

2. $J_A = K_A = 1,\ J_B = \overline{C}.A,\ K_B = A,\ J_C = A.B,\ K_C = A$

3. $J_A = 1,\ K_A = \overline{B} + \overline{C},\ J_B = \overline{C}.A,\ K_B = A + C,\ J_C = A.B,\ K_C = A + B$

4. $J_A = K_A = 1,\ J_B = K_B = A \oplus Z$

5. I_1 is ($J = 0$, $K =$ anything); I_2 is ($J = 1$, $K =$ anything); I_3 is ($K = 0$, $J =$ anything); I_4 is ($K = 1$, $J =$ anything).

7. Use two bistables R and Y, and $G = \overline{R+Y}$ to get green. $J_R = K_R = Y,\ J_Y = P \oplus R,\ K_Y = 1$

8. $8.33R$, 3.320V, 3.906V, 6.289V.

9. B set to 01000 after 5 clock pulses; B_4; B_5 added and 6 pulses needed. Calculates $(B - A)$.