(c) Stack pointer : The 8086 allows us to set 64KB of memory as stack. The 16-bit starting address of stack is stored in stack pointer.

Q. 3 Explain any two microprocessors in X-86 family in brief.

OR

Explain the following microprocessors in Intel's X-86 family.

Ans. : I) 8086 :

1) 8086 is a **16-bit** microprocessor, introduced by INTEL in 1978.
2) It was designed to be used as C.P.U. in microcomputer system. It's A.L.U., internal registers can work with 16 binary bits at a time.
3) 8086 has 16-bit data bus and 20-bit address bus, so that it can address a physical memory of $2^{20} = 1048576 = 1$ M Byte memory locations.
4) The least significant 8 bits of address bus are passed on same eight lines as that of data bus. This bus is known as multiplexed bus.
5) In 8086, words are stored in two consecutive bytes. If first byte of word has even address, then 8086 can read it in single operation. Else, it requires two operations.
6) This processor support multiplication and division operation.
7) The 80186 is an improved version of 8086. In addition to 16-bit C.P.U., it has programmable peripheral (I/O) devices integrated in same package. Instruction set of 80186 is superset of instruction set of 8086.

II) 80286 :

1) 80286 is a **16-bit** microprocessor, introduced in 1982. This advanced version of 8086 is specially designed to be used as a C.P.U. in multiuser/multitasking operating systems.
2) 80286 has 16-bit data bus and 24-bit address bus.
3) In 1984, IBM introduced PC/AT (Personal Computer/Advanced Technology) version of its PC using 80286.

4) 286 was having real and protected modes of operation. In real mode, the processor can address only 1 M byte of memory, where as in protected mode it can address 16 M bytes of memory.
5) Another new feature was the ability to work upto 1 G byte of virtual memory and yet another feature was added hardware multitasking.
6) The program written for 8086 can run on 80286, operating in its real address mode.

III) 80386 :

1) The INTEL's 80386 is a 32-bit microprocessor introduced in 1985.
2) 80386 is a logical extension of 80286. It is more highly pipelined.
3) The instruction set of 80386 is a superset of other members of 8086 family.
4) It has 32-bit data bus and 32-bit nonmultiplexed address bus. It can address a physical memory of 2^{32} i.e. 4 G bytes. The 80386 memory management allows it to address 2^{46} or 64 T bytes.
5) The 386 can be operated in one of the following memory management mode :
   i) Paged mode
   ii) Non-paged mode.
6) When operated in paged mode, the 386 switches the paging unit then after the segment unit. The paging unit allows memory pages of 4 KB each to be swapped in and out from disk. In non-paged mode, memory management unit operates very similar to the 286.
7) Virtual addresses are represented with selected components and an offset component as they are with 80286.

IV) 80486 :

1) Intel's 80486 is a 32-bit microprocessor. It was introduced in 1989.
2) It has 32-bit address bus and 32-bit data bus.
3) The 486 is basically a large integral circuit which contains a fast built-in, a math coprocessor, a memory management unit (M.M.U.), and an 8 kbyte cache memory.

4) 80486 has DX and SX versions.

5) All 486 processors have 32-bit data bus. SX version, does not have on chip-numeric co-processor.

6) The 486 achievs its high speed operation from its faster clock speeds, internal pipe lined architecture and the use of reduced instruction set computing (RISC) to speed up the internal microcode.

7) 486 also has 486 DX2 and 486 DX4 versions, with double and triple clock speed.

V) Pentium or 80586 : OR

Explain the main features of a pentium processor. (March 2003)

1) Pentium is a 64 bit microprocessor, introduced in 1993.

2) It has 64 bit data bus and 32-bit address bus. The use of super scalar architecture incorporates a dual-pipe lined processor, which lets the pentium process more than one instruction per clock cycle.

3) The addition both of data and code caches on chip is also a feature designed to improve processing speed.

4) A new advanced computing technique used in pentium is called the branch prediction, the pentium makes an educated guess where the next instruction following a conditional instruction will be. This prevents instruction cache from running dry during conditional instructions.

5) The pentium has 64-bit data bus. This means that it can perform data transfers with an external device twice as fast as a processor with a 32 data bus.

Q. 4 Explain the advantages of the pentium processor with respect to the following features :

1) Dual pipelining 2) On-chip caches

3) Branch prediction 4) 64-bit data bus

Ans. : 1) Dual pipelining :

The use of super scalar architecture incorporates a dual-pipelining in pentium processor, which lets pentium to process more than one instruction per clock cycle.

2) On-chip caches :

The data and code on-chip caches improves the processing speed of the pentium processor.

3) Branch prediction :

i) The advantage of branch prediction is that, using it, the pentium makes an educated guess where the next instruction following a conditional instruction will be.

ii) This prevents the instruction cache from running dry during conditional instruction.

4) 64-bit data bus :

i) Pentium has 64 bit data bus which allows higher speed of data transfer to it.

ii) The data transfer speed of pentium is twice as fast as a process or with 32-bit data bus.

Programming model of X-86 family

Q. 5 Explain the programming model for 32-bit version of X-86 family with suitable diagram. (March 2002)

Ans. :

1) The 8088 and 8086 defines the base programming model for the entire X-86 family of advanced microprocessors.

2) The newer members of X-86 family have greater computing power because they are faster, they use 32-bit registers instead of 16-bit registers and they have advanced addressing techniques.

3) Following figure shows programming model for 32-bit version of X-86 family :

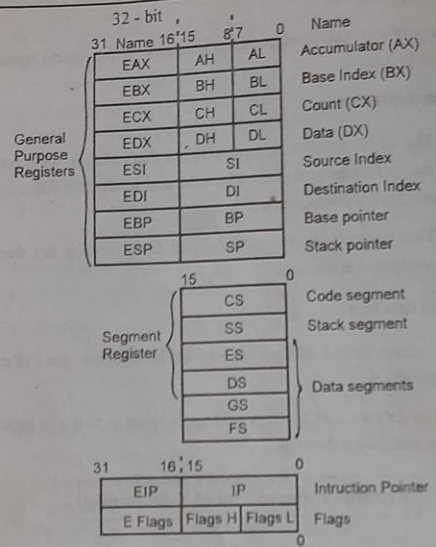


Fig. 7.2

4) The programming model of 32-bit version of X-86 family consists of 3 register groups.

5) The first group contains eight general purpose registers called EAX, EBX, ECX, EDX, ESI, EDI, ESP and EBP registers. Where E tells us that these registers have extented length. Each register can be addressed in 1, 8, 16 or 32-bit models. These registers are used to store data during computations.

6) The second group of registers is the segment group. This group consists of code segment, stack segment and four data segment registers. The data segment registers are DS, ES, FS and GS. These are 16-bit registers. These registers manage operation with external memory. Address computations and data movements are performed here.

7) The third set of registers consists of Instruction Pointer (I.P.) and flag register.

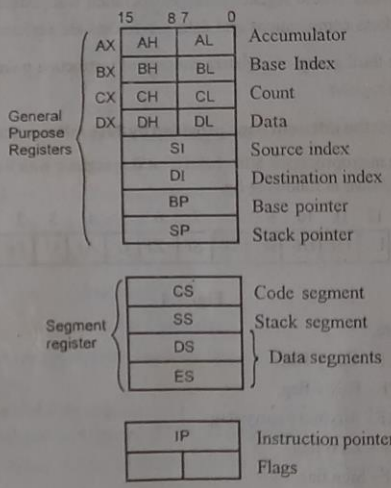
Q. 6 Draw neat labelled diagram and explain the programming model of 16-bit version of X-86 family with register set. (Oct. 2002)

Ans. :

1) The 8088 and 8086 defines basic programming model for X-86 family.

2) The 16-bit version for programming model is used in 16-bit microprocessors of X-86 family i.e. in 8086, 80286 and 80386.

3) The 16-bit version of programming model of X-86 family is shown in the following figure.



Programming model of 16-bit version of X-86 family

Fig. 7.3

4) As shown in above figure the programming model of 16-bit version of X-86 family consists of three register groups.

5) The first group contains 8-general purpose registers called A, B, C, D, SI, DI, SP and BP registers. AL, BL, ... indicates lower bytes and AH, BH, ... indicates higher bytes. The full 16-bit registers are referred as AX, BX, CX and DX, where X stands for extended SI, DI, BP, SP registers are always treated as 16-bit registers. These are pointer registers because they are used to point locations within a segment.

6) The second group of registers is the segment group of registers. This group consists of code segment, stack segment and two data segment registers. These register manages operation with external memory. Address computations and data movements are performed here.

7) The third group of registers consists of instruction pointer (IP) and flag register.

Q. 7 Enlist the different flags provided by 8086 microprocessor.

Ans. : The microprocessor 8086 has 16-bit flag register with 9 active flags, which are shown in following fig.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	OF	DF	IF	TF	SF	ZF	U	AF	U	PF	U	CF

(U empty)

Fig. 7.4

Where,

CF - Carry flag,
PF - Parity flag,
AF - Auxiliary carry flag,
ZF - Zero flag,
SF - Sign flag,
TF - Single step trap,
IF - Interrupt flag,
DF - String direction,
OF - Over flow.

Q. 8 Draw a neat labelled diagram of flag register of X86 family.
(March 2003)

Ans. : Flag register is used to store special results from data operations. The flag register of X86 family is shown in following figure.

31.....18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	A_C	V_M	R_F	O	N_T	IO	PL	O	D	I	T	S	Z	–	A	–	P	–	C

where -

C → Carry flag (CF)
P → Parity flag (PF)
A → Auxilliary carry flag (AF)
Z → Zero flag (ZF)
S → sign flag (SF)
T → Trap flag (TF)
I → Interrupt flag (IF)
D → String Direction flag (DF)
O → Overflow flag (OF)
IOPL → I/O Privileage level
N_T → Nested task flag
R_F → Resume flag
V_M → Virtual mode flag
A_C → Alingment Check flag

a) 8085 microprocessor has 8-bit flag register (0 - 7) with 5 flags are active.

b) 8086/8088 microprocessor has 16-bit flag register 8 to 11 bits are introduced and remaining bits are underfined.

c) 80286 has also 16-bit flag register but 12 to 14 bits are added.

d) 80386 microprocessor has 32 bit flag register with 16 and 17^{th} bits were introduced.

e) 80486 has 32 bit flag register with new 18^{th} bit.

Remaining all positions in flag register are reserved.