

# LAB REPORT:2

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Group No.: 9

## Experiment 1

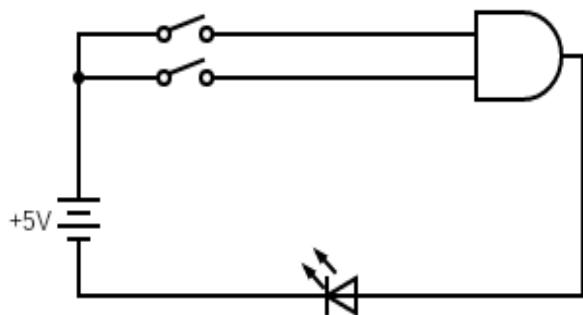
**Objective:** Identification of Logic Gate

**Electronic Component Used:**

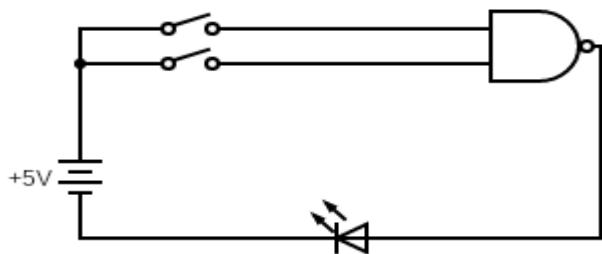
AND Gate, OR Gate, XOR Gate, NOR Gate, NAND Gate,  
Inverter ICs, Digital Testing Kit, Wires.

**The Reference Circuit:**

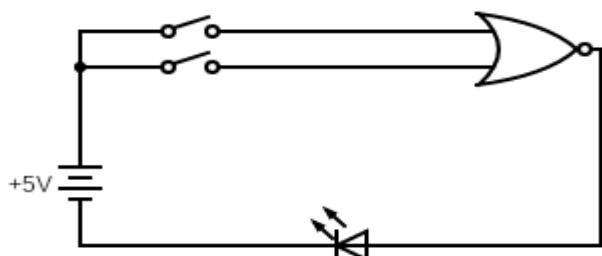
**AND GATE:**



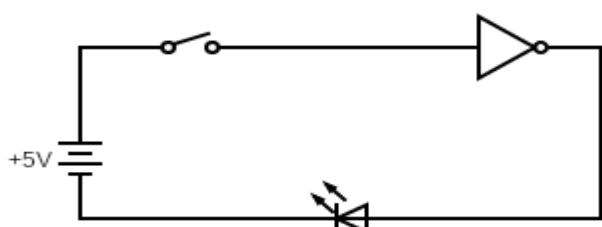
NAND GATE:



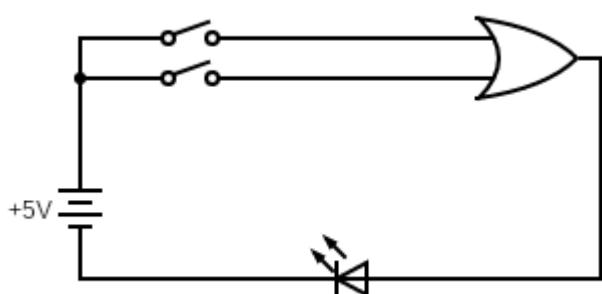
NOR GATE:



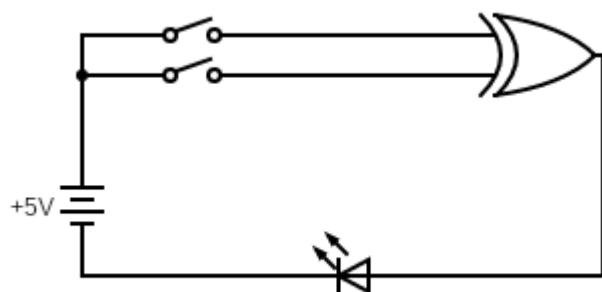
NOT GATE:



OR GATE:



## XOR GATE:



## Procedure:

1. Connect VCC and GND with BreadBoard.
2. Connect IC with VCC and ground.
3. Connect Input(Switch) to Input of IC.
4. Connect Output of IC to Output(Bulb).
5. Observe the Bulb, while changing Input Voltage(ON/OFF).  
(RED High Output, GREEN low Voltage Output)

## Observation:

From the experiment, we observed the following;

### For TTL 74LS04nh

INPUT	OUTPUT
0	1
1	0

**For TTL 74LS08nh**

A	B	OUTPUT
0	0	0
0	1	0
1	0	0
1	1	1

**For TTL 74LS32nh**

A	B	OUTPUT
0	0	0
0	1	1
1	0	1
1	1	1

**For CD4001**

A	B	OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0

**For TTL 74LS86nh**

A	B	OUTPUT
0	0	0
0	1	1
1	0	1
1	1	0

**For CMOS CD4001**

A	B	OUTPUT
0	0	1
0	1	0
1	0	0
1	1	0

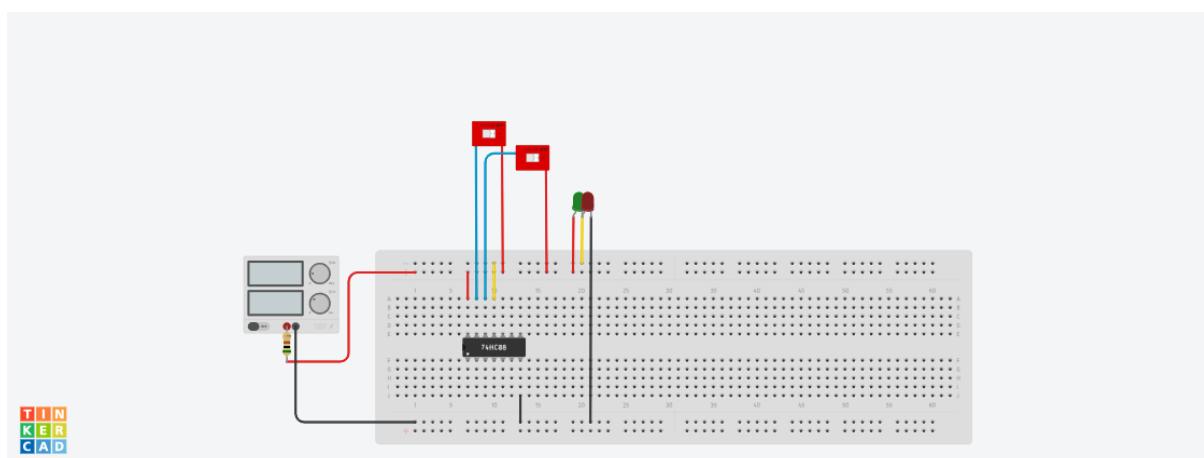
## Conclusion:

From the experiment we can identify gate as following:

GATE Series	GATE Name
TTL 74LS04nh	NOT
TTL 74LS08nh	AND
TTL 74LS32nh	OR
CMOS CD 4011	NAND
TTL 74LS86nh	XOR
CMOS CD4001	NOR

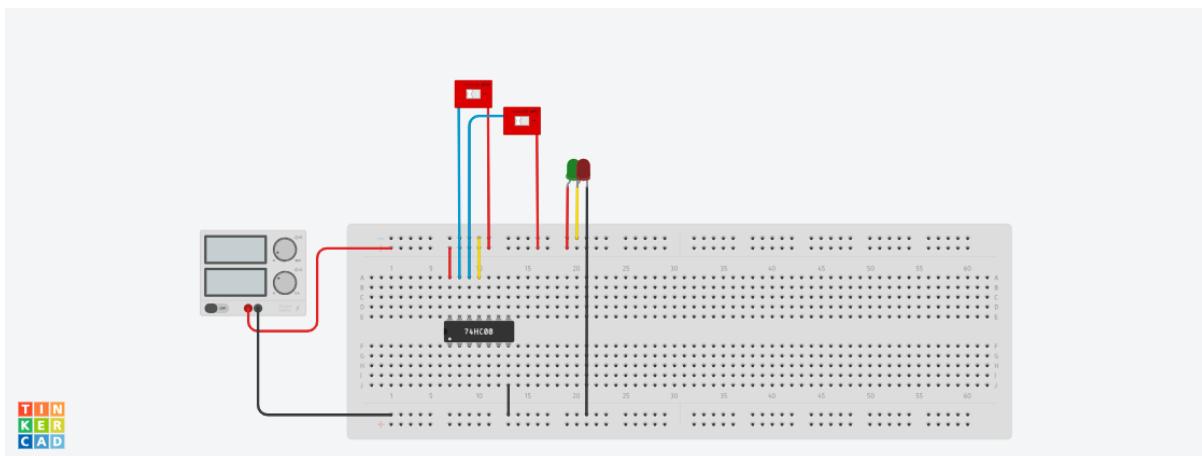
## TinkerCad:

AND:



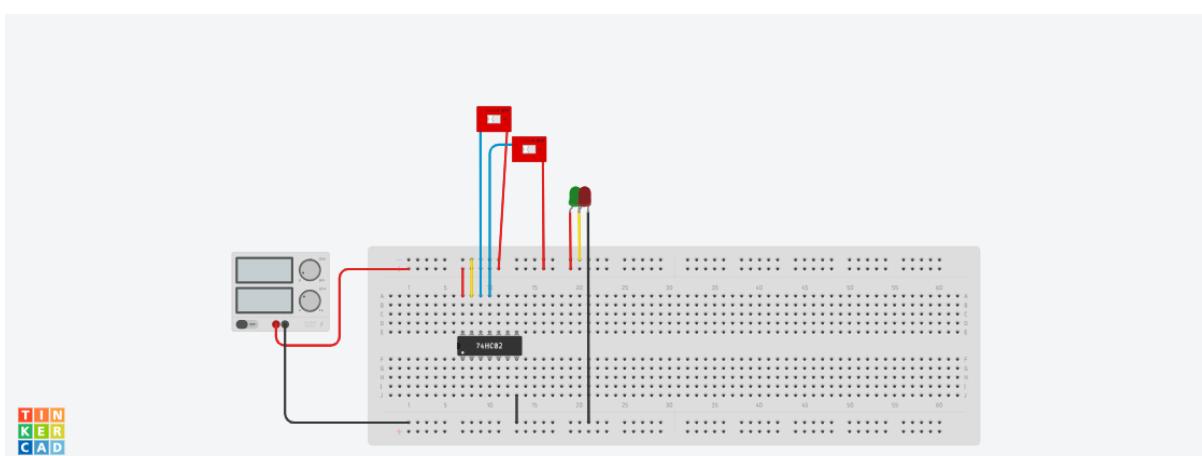
<https://www.tinkercad.com/things/hFa5fO1XIYT-21-and>

NAND:



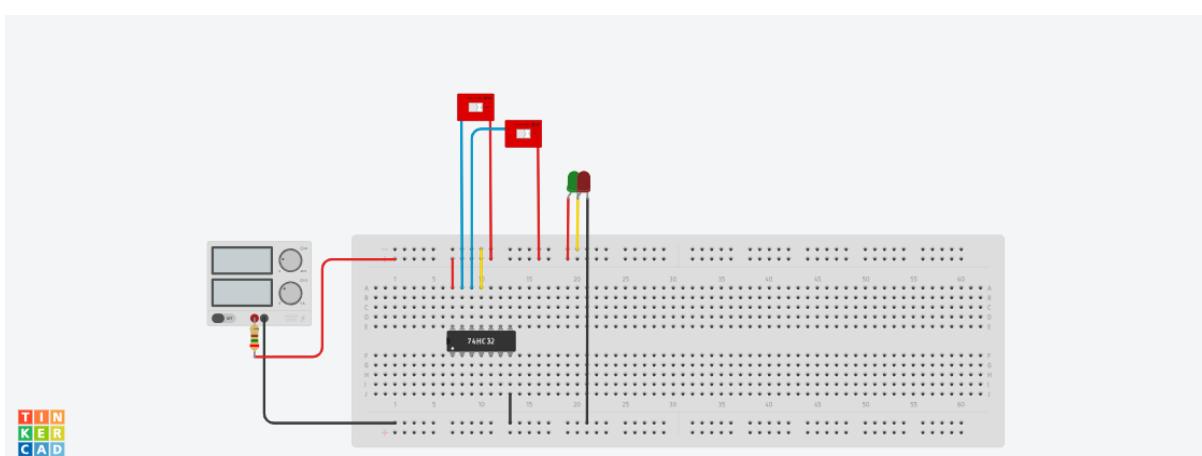
<https://www.tinkercad.com/things/8sak4wBONcz-21-nand>

NOR:



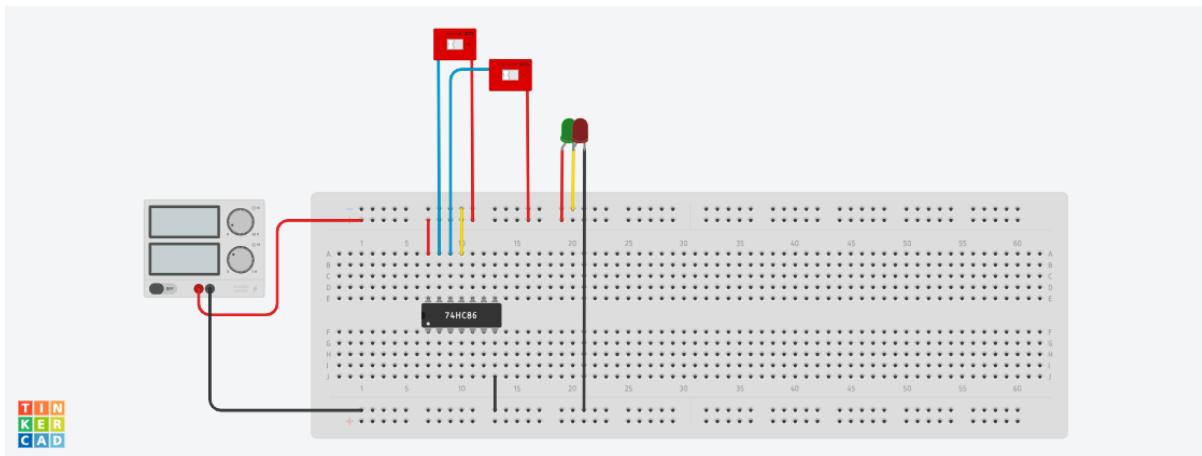
<https://www.tinkercad.com/things/0KgaTTdTh7s-21-nor>

OR:



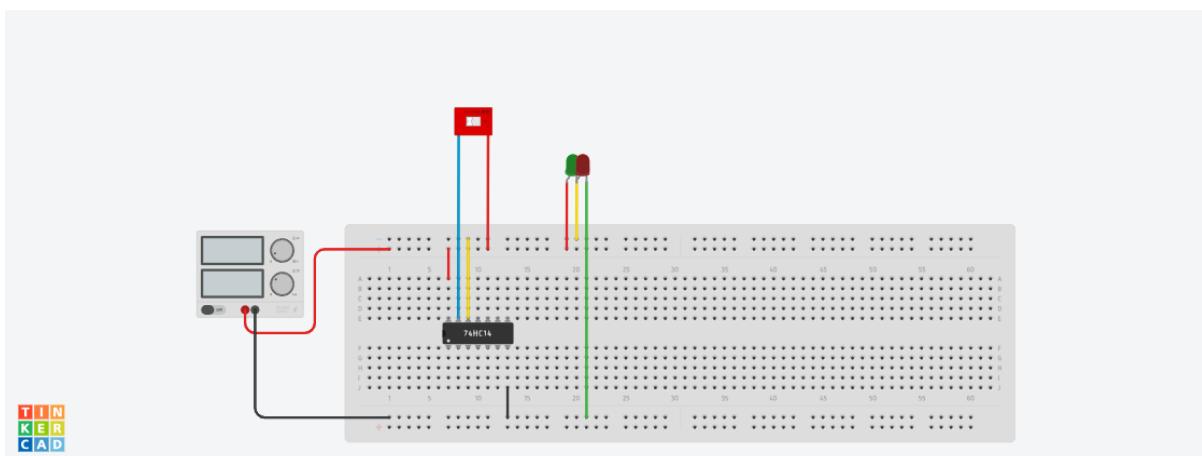
<https://www.tinkercad.com/things/kzmEFFGbfpJ-21-or>

XOR:



<https://www.tinkercad.com/things/2NLKjqGYSdH-fantabulous-gaaris-lahdi>

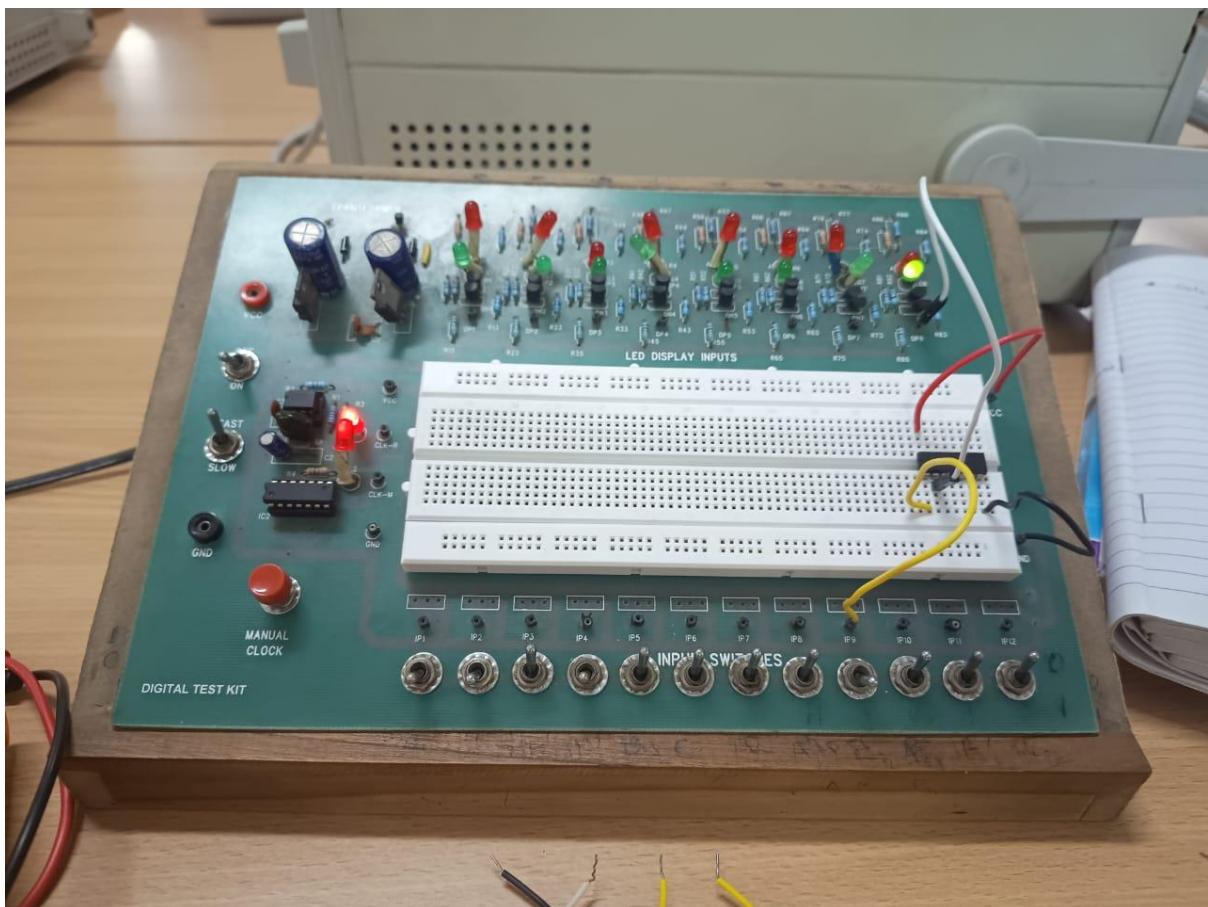
NOT:



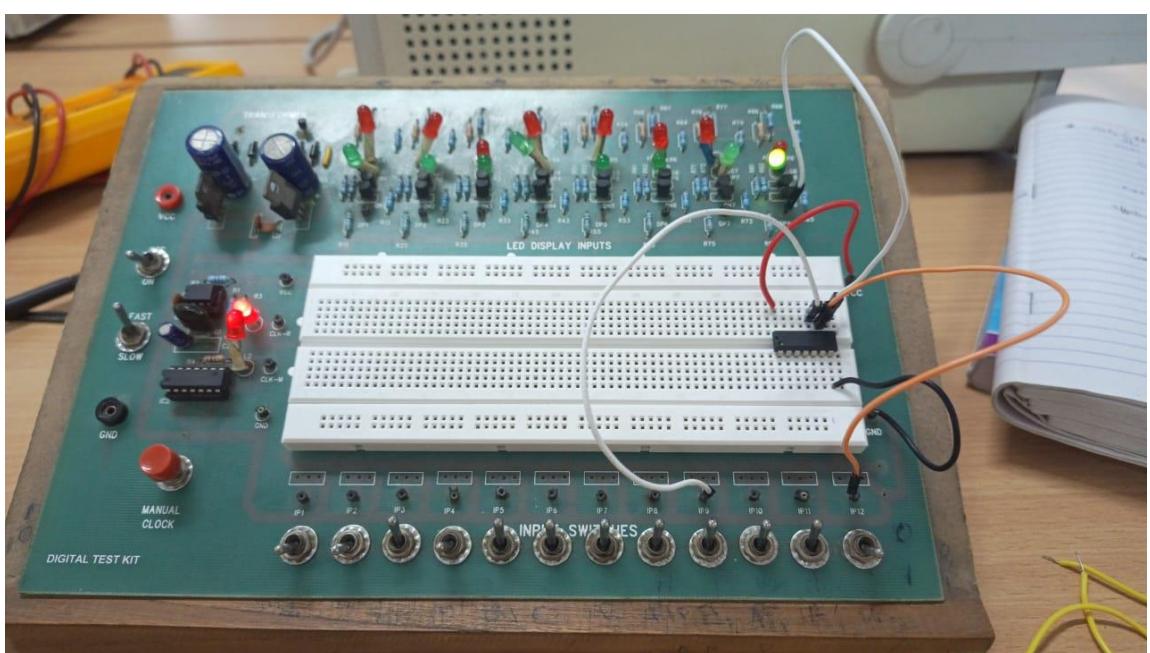
<https://www.tinkercad.com/things/eYusek0af0a-exp11>

LAB:

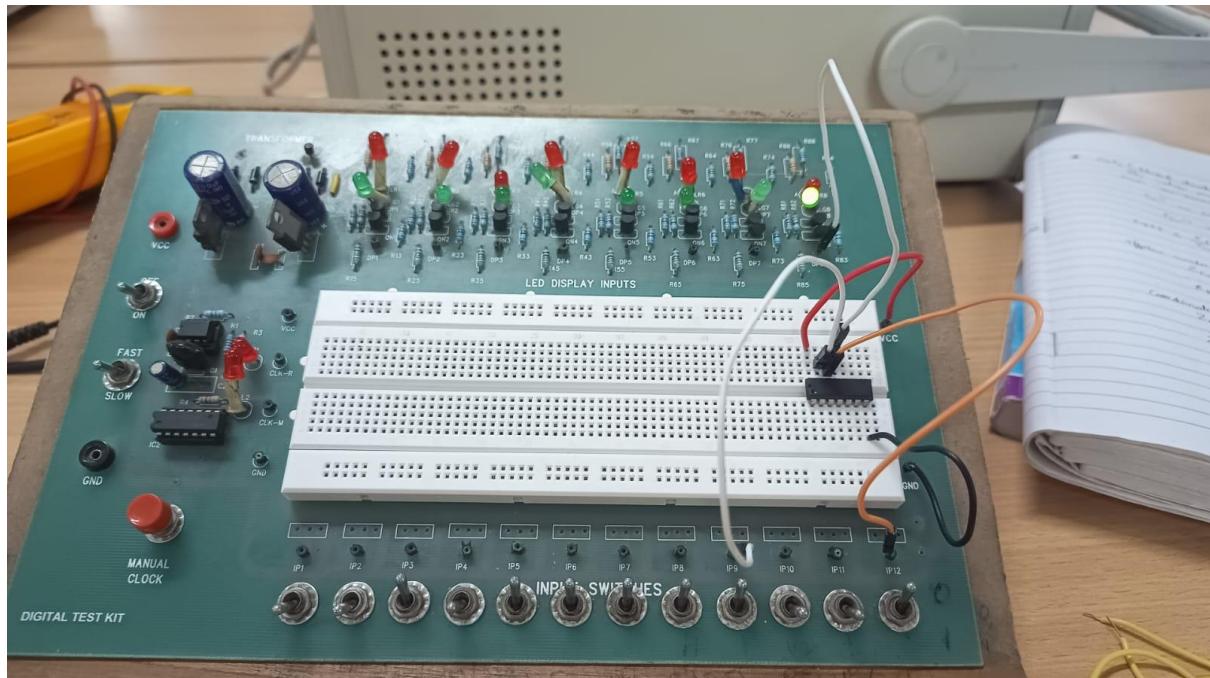
NOT GATE:



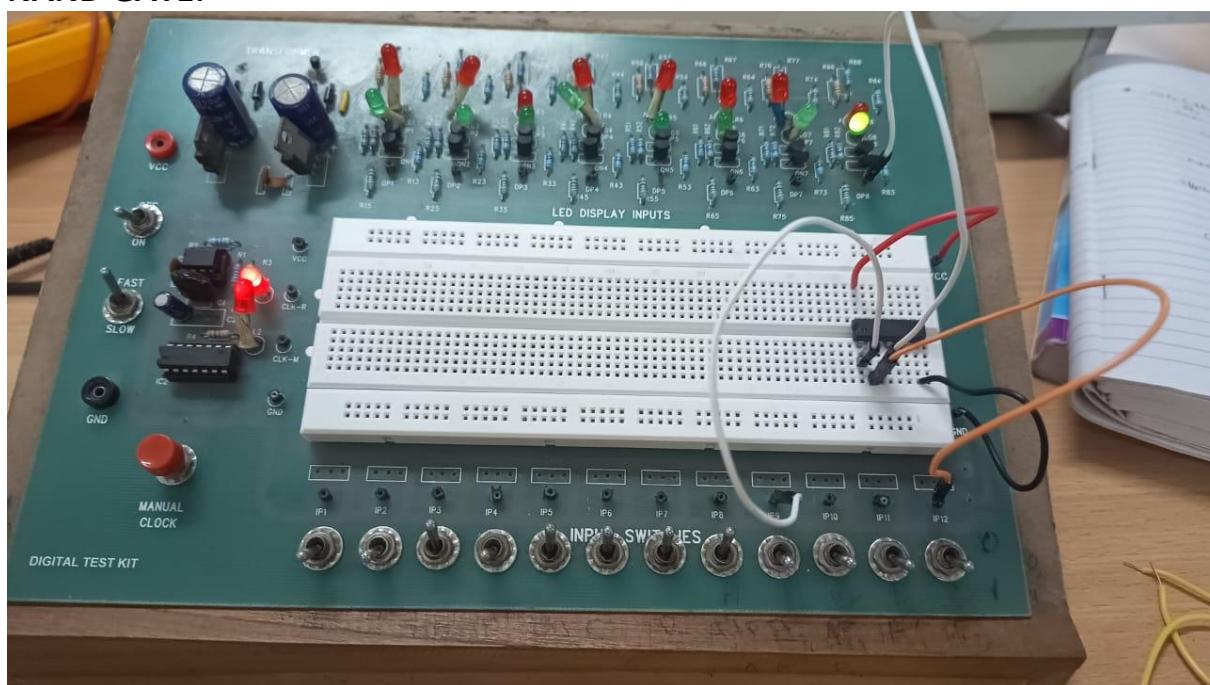
## AND GATE:



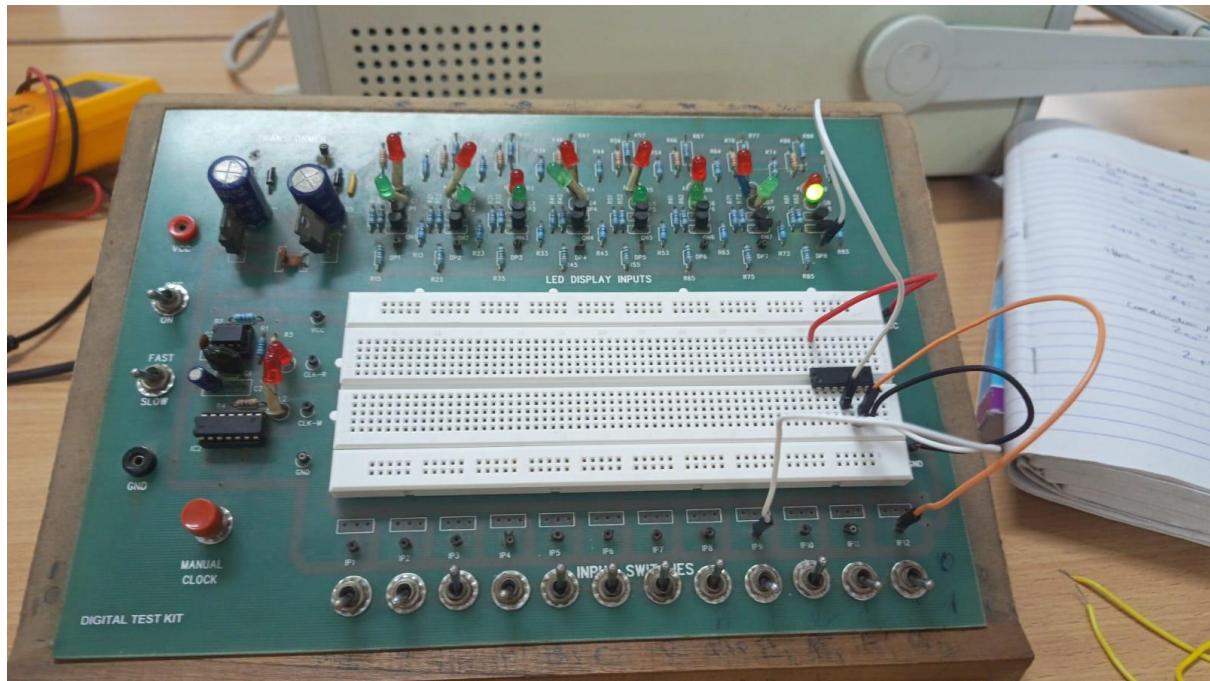
## OR GATE:



## NAND GATE:



## NOR GATE :



## XOR GATE:



# Experiment 2:

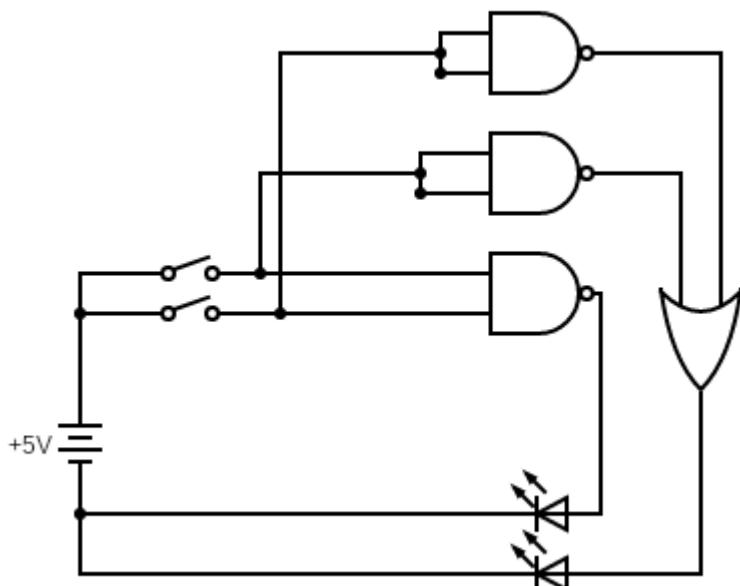
**Objective:** Checking De Morgan's theorem using logic GATES

**Electronic Component Used:**

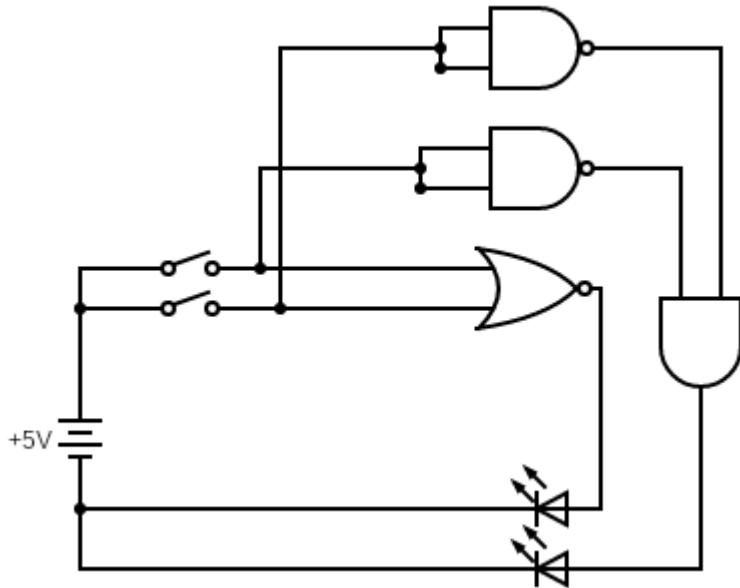
- Battery
- Logic GATES (AND, NAND, OR, NOR)
- LED bulbs
- Switches
- Wires

**The Reference Circuit:**

$$(A \bullet B)' = A' + B'$$



$$(A + B)' = A' \cdot B'$$



## Procedure:

For  $(A \cdot B)' = A' + B'$

1. We connected the VCC and GND of Logic GATES and two switches parallel to each other with battery.
2. We connected the other end of two switches with two input pins of NAND Gate and the output pin with a LED bulb.
3. We then connected parallelly from both the switches and connected to different inner circuit of NAND Gate such that in both the INPUT pin input come from same switch.
4. Then, we will connect both output pins of NAND Gate with input pin of OR Gate.
5. Then, we will connect it with LED bulb and then to ground.

**For  $(A + B)' = A' \bullet B'$**

1. We connected the vcc and ground of Logic GATES and two switches parallel to each other with battery.
2. We connected the other end of two switches with two input pins of NOR Gate and the output pin with a LED bulb.
3. We then connected parallelly from both the switches and connected to different inner circuit of NAND Gate such that in both the INPUT pin input come from same switch.
4. Then, we will connect both output pins of NAND Gate with input pin of AND Gate.
5. Then, we will connect it with LED bulb and then to ground.

### Observation:

We observed that both the LED bulbs glow in following ways:

**For  $(A \bullet B)' = A' + B'$**

A	B	$(A \bullet B)'$	$A' + B'$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

**For  $(A + B)' = A' \bullet B'$**

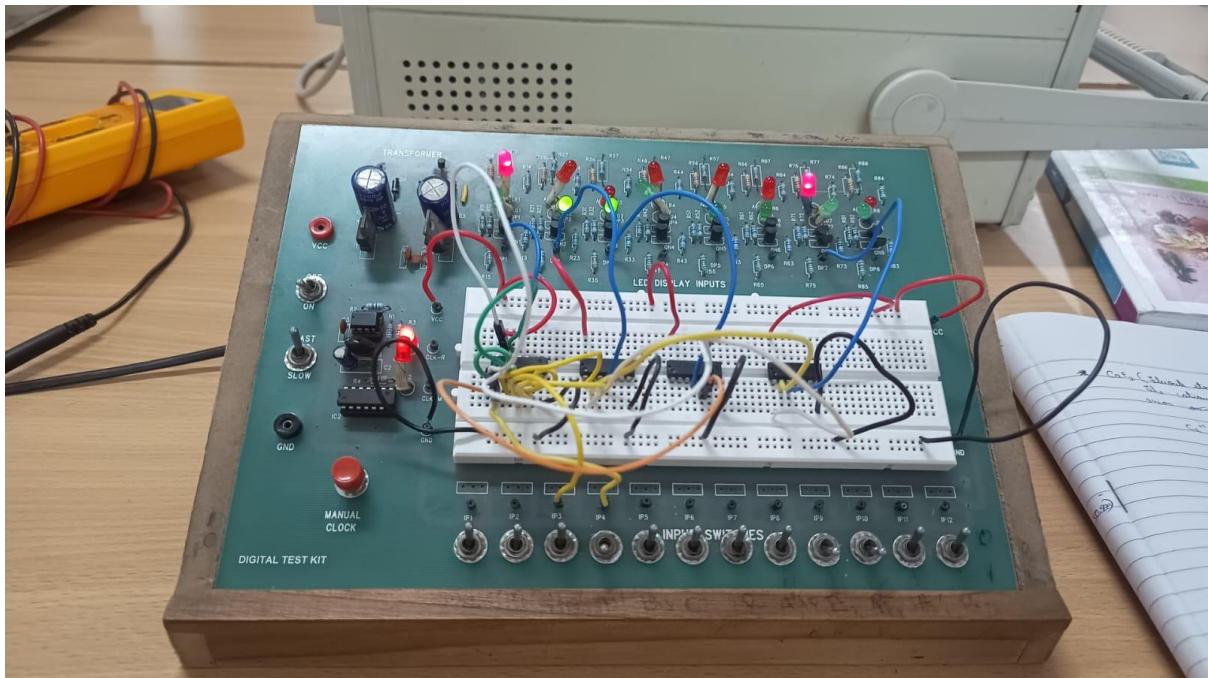
A	B	$(A + B)'$	$A' \bullet B'$
0	0	1	1
0	1	0	0

1	0	0	0
1	1	0	0

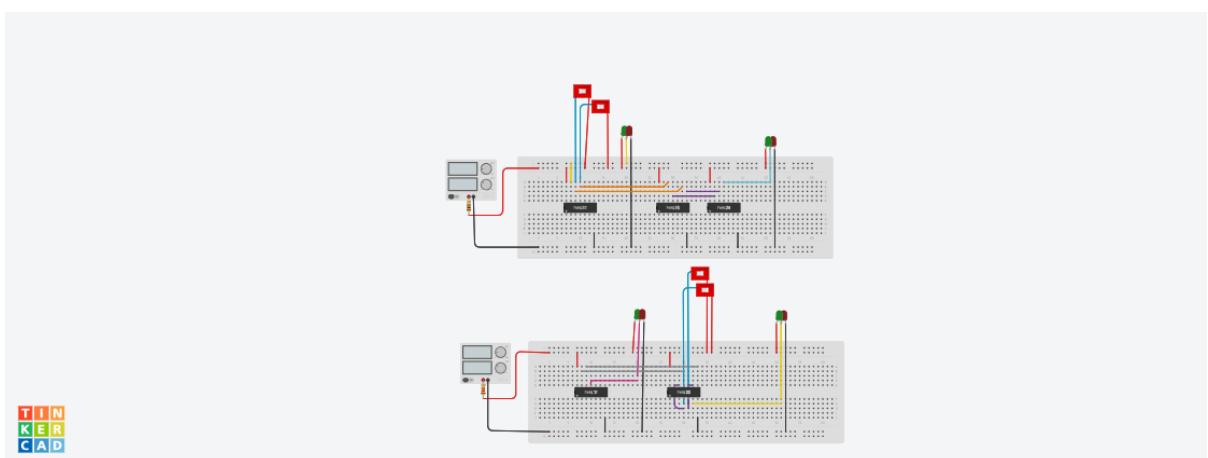
## Conclusion:

As both the LED bulbs glow together, we can conclude that De Morgan's Law is true.

## Tinkercad simulation and Lab photo:



In the above photo D1 and d7 are together



Link:

<https://www.tinkercad.com/things/73cIrOKjYtM-22-demorgan>

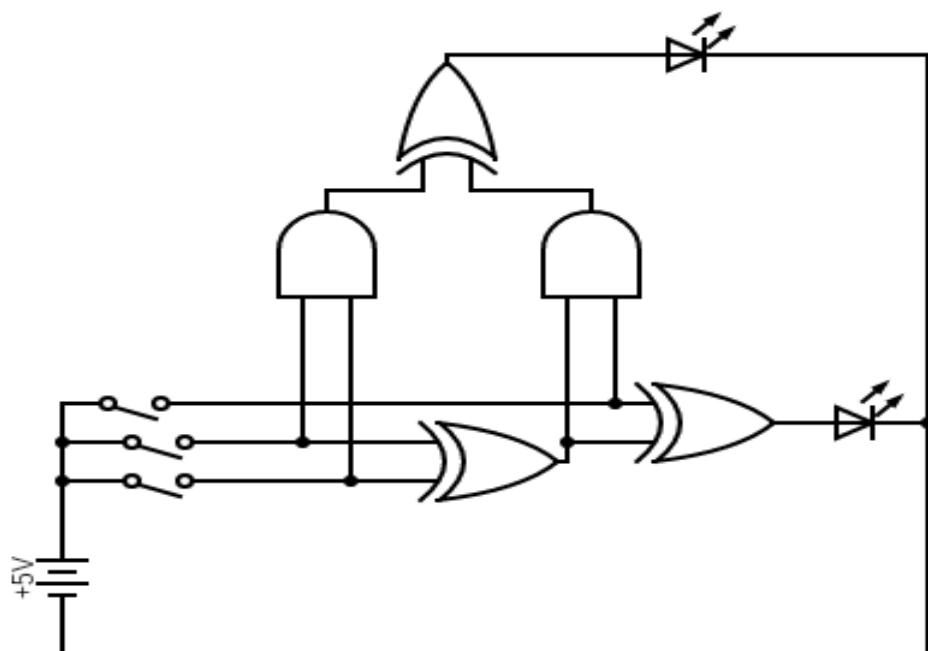
## Experiment 3:

**Objective:** Make a binary full adder using logic GATES

**Electronic Component Used:**

- Battery
- Logic GATES (AND and XOR)
- Wire
- Switches
- LED bulbs

**The Reference Circuit:**



## Procedure:

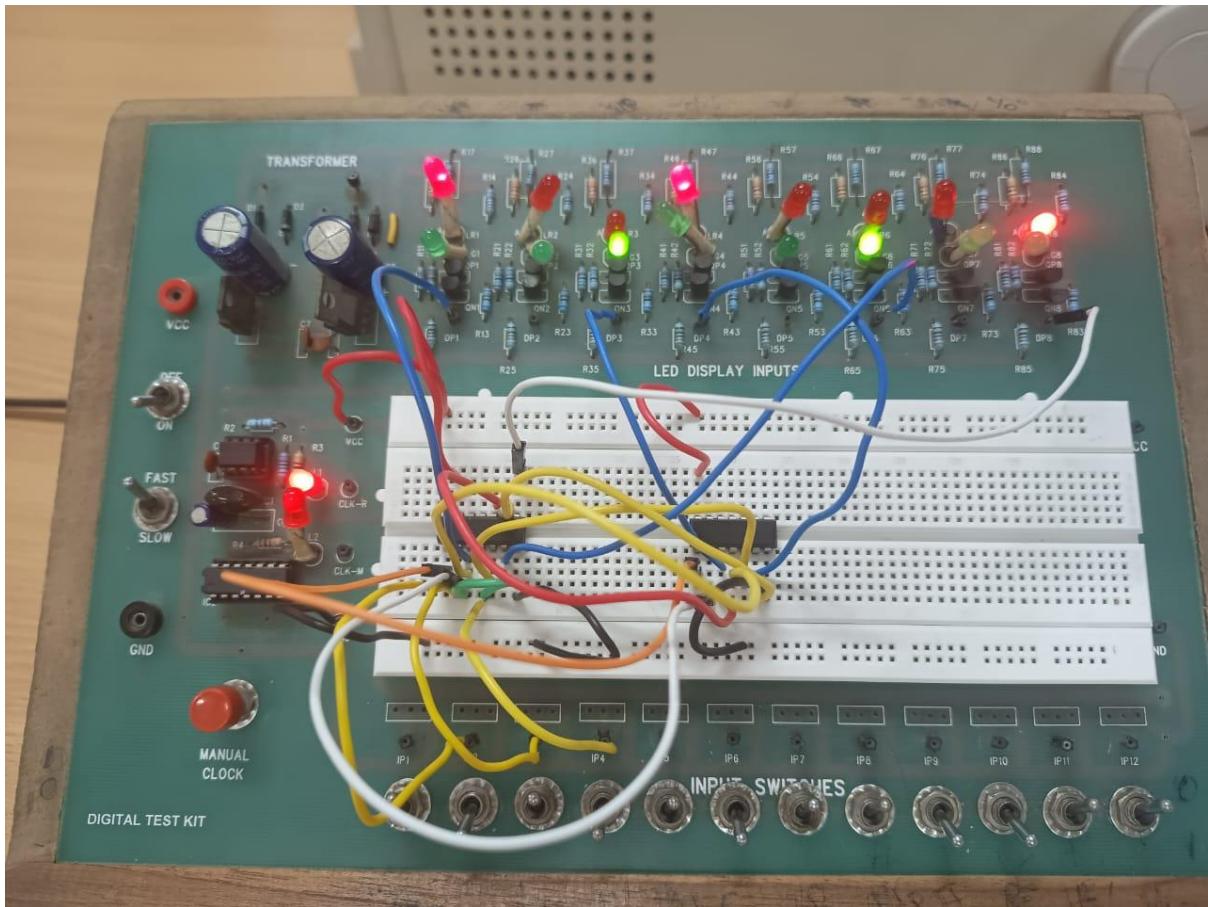
1. We connected three switches parallel to each other from the battery.
2. We connected the first two switches with input pins of XOR Gate and its output with another input pin of XOR Gate and the other input pin with third switch.
3. We connected the output pin of second XOR Gate with bulb indicating **SUM**.
4. We connected the first two switches parallelly with input pins of AND Gate.
5. We connected the third switch and output pin of first XOR Gate with another AND Gate.
6. Then, we connected the output pin of both the AND Gate as input of another XOR Gate and then to LED bulb to ground and this bulb will indicate **CARRY**.

## Observation:

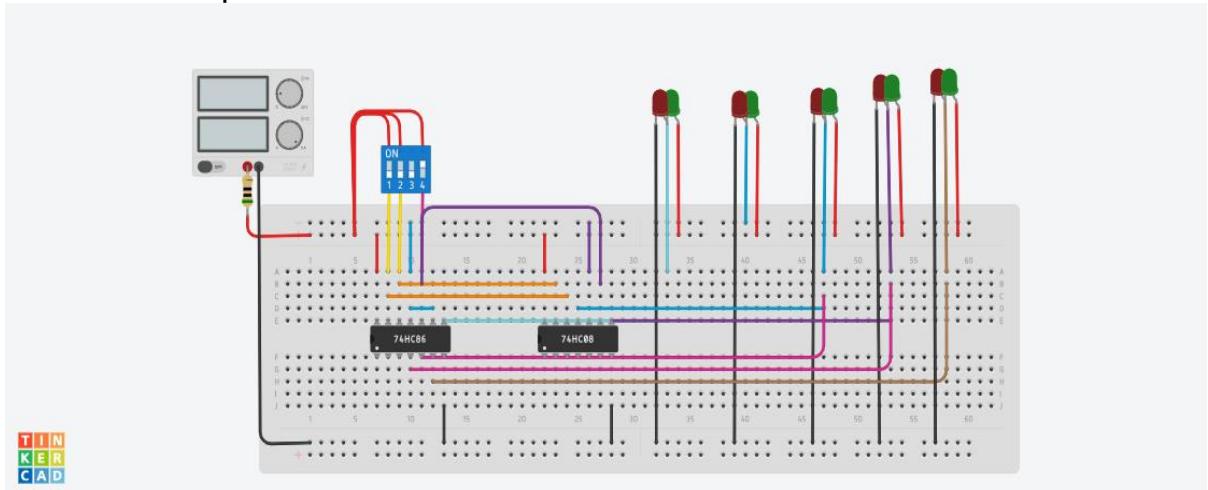
We observed the SUM and CARRY in following ways:

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

## Tinkercad simulation and Lab photo:



In the above photo D6 is SUM and D8 is CARRY.



Link:

<https://www.tinkercad.com/things/g2QHngu3fNL-25-full-adder>

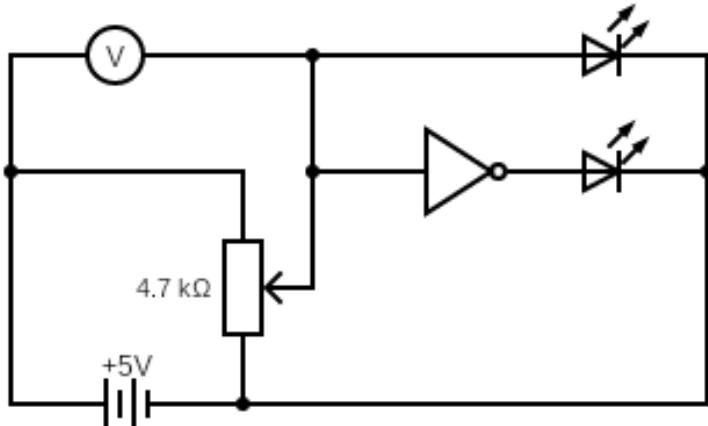
## **Experiment 4**

**Objective:** Identification of logic levels with potentiometer

**Electronic Component Used:**

- Battery
- Hex Invertor (NOT gate)
- Multimeter
- Potentiometer
- Red and Green LED bulbs
- Wire

**The Reference Circuit:**



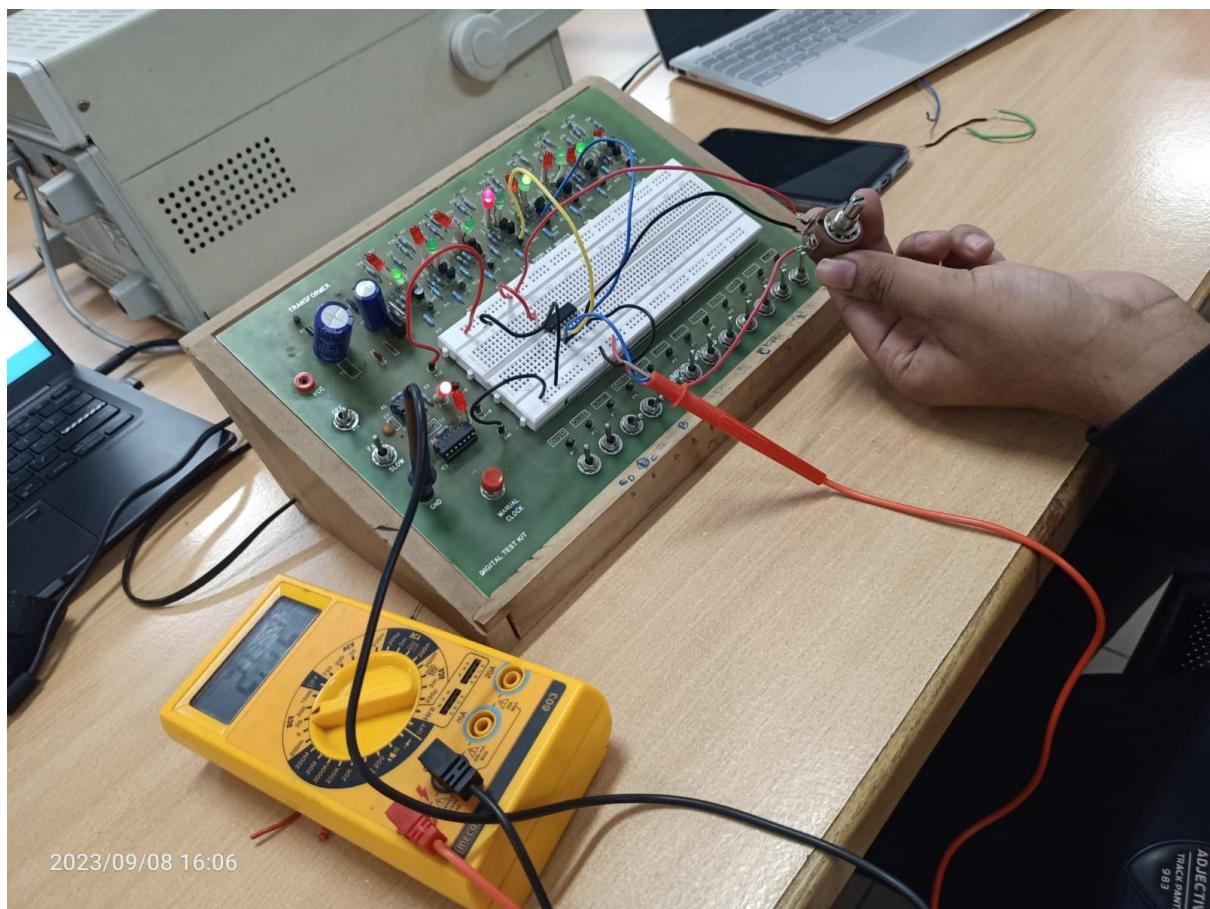
**Procedure:**

6. First of all, we connected the vcc and ground of potentiometer.
7. Then, we connected the multimeter with vcc and its other end with a LED bulb to ground, NOT GATE (Hex Invertor) and with the potentiometer parallel to each other.
8. At last, we connected the other end of NOT GATE with another LED bulb which was later connected to ground.

## Observation:

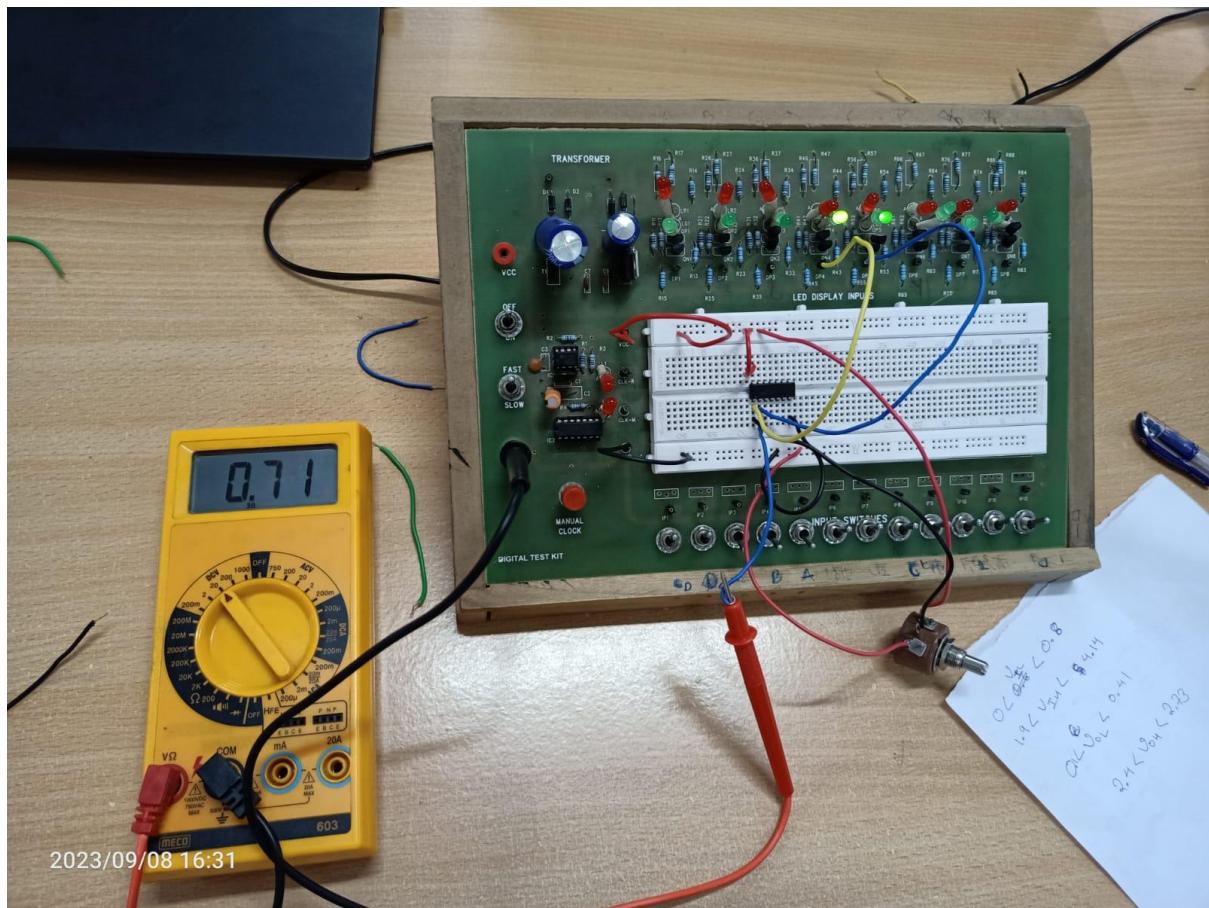
When the input voltage is low ( $0 \leq V_{IL} \leq 0.8$ ), the output voltage is max=2.73V ( $2.4 \leq V_{OH} \leq 2.73$ ). And when input voltage is high, ( $1.9 \leq V_{IH} \leq 4.14$ ), the output voltage is low ( $0 \leq V_{OL} \leq 0.4$ ).

## Low INPUT:

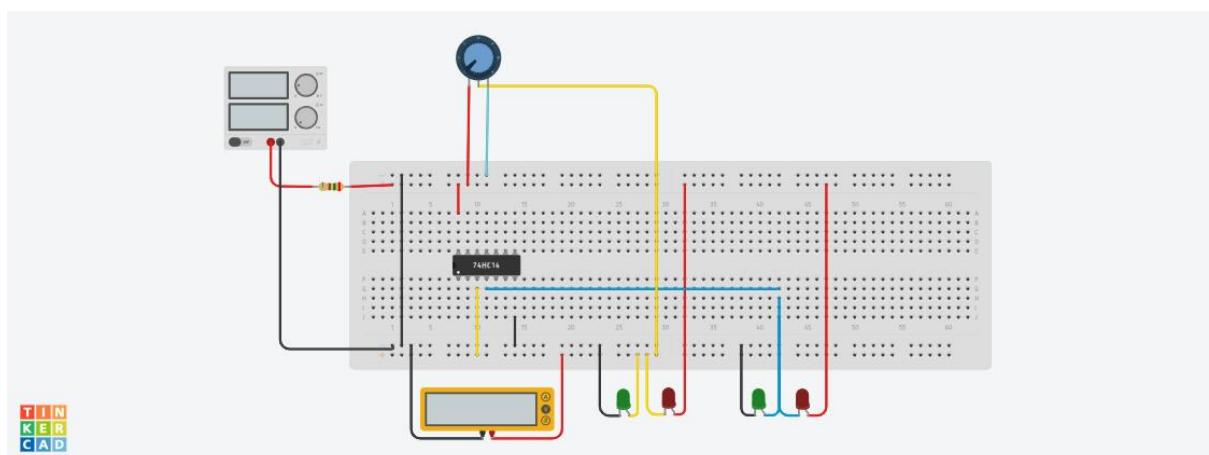


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## High INPUT:



Link for the Tinkercad simulation:



Link :

<https://www.tinkercad.com/things/8DjSzIYiDVG-exp21>