# LAB REPORT 4

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**OBJECTIVE** – Designing ALU using 8:1 Multiplexer.

**ELCTRONIC COMPONENTS REQUIRED -**

1. Digital test kit.          .
2. 8 input multiplexers(74LS151).
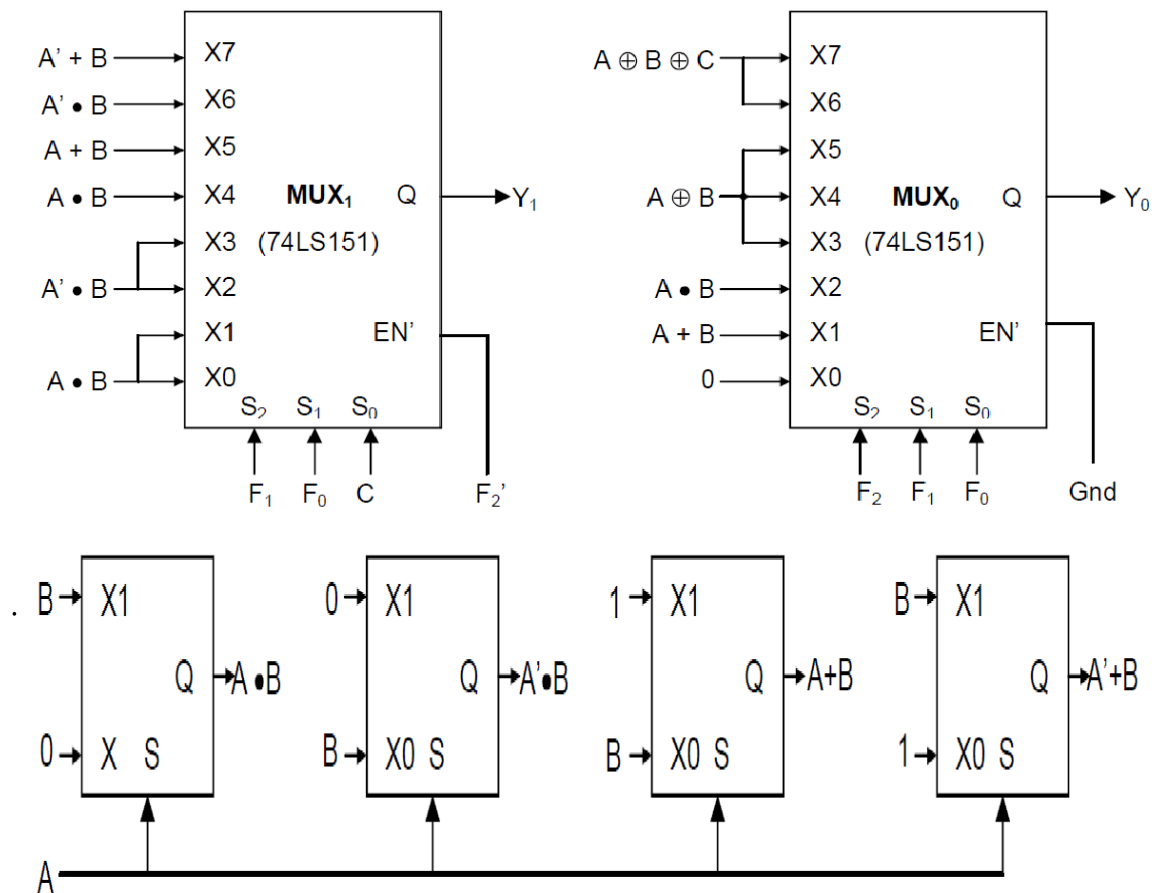3. 2 input multiplexer (74LS157).
4. Quad two input exor gate(74LS86).

**PROCEDURE:**

1. Test the ICs, LED Lights and Switches.
2. Connect ICs with GND, Power and Enable (Enable was 0).
3. Connect the *2 Input* mux gate as mentioned in the reference circuit.
4. Connect inputs to EXOR Gate as given in circuit.
5. Connect all Output from Gates to input of two 8:1 Multiplexer.
6. Connect Select line to Multiplexer.
7. Check the Output while toggling different combination of Switches.

# Truth Table:

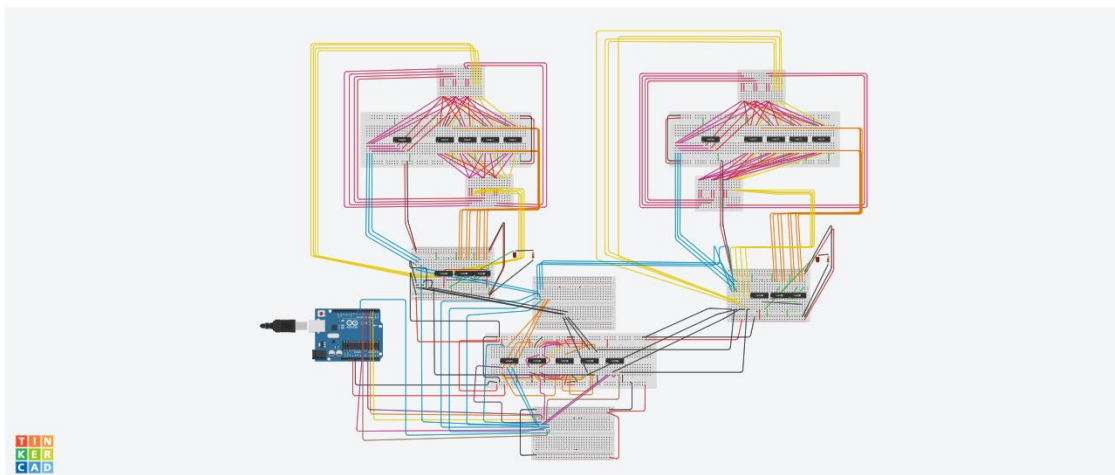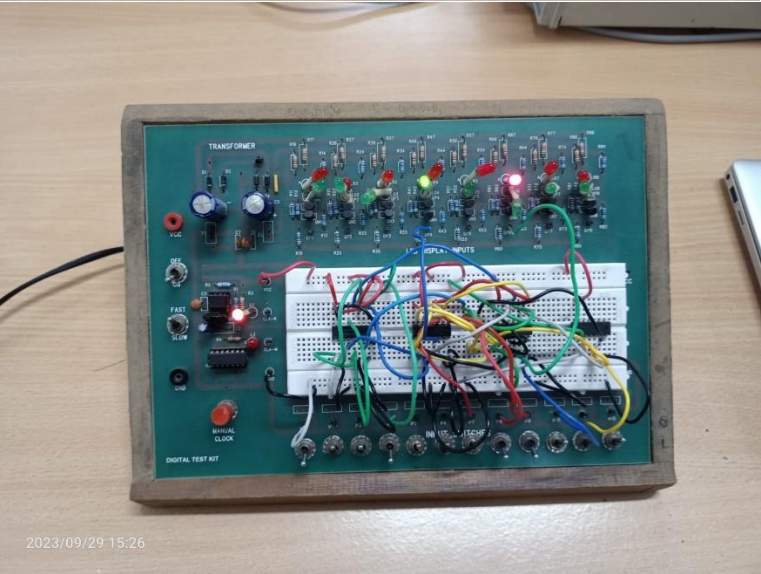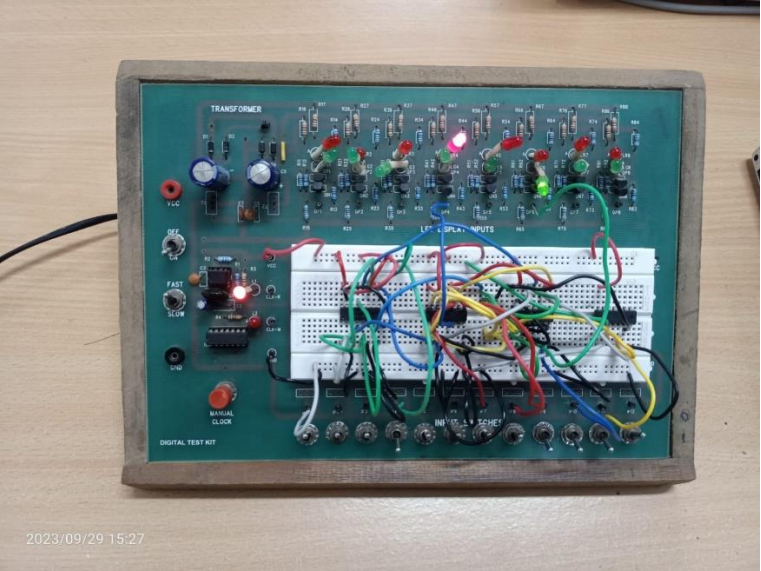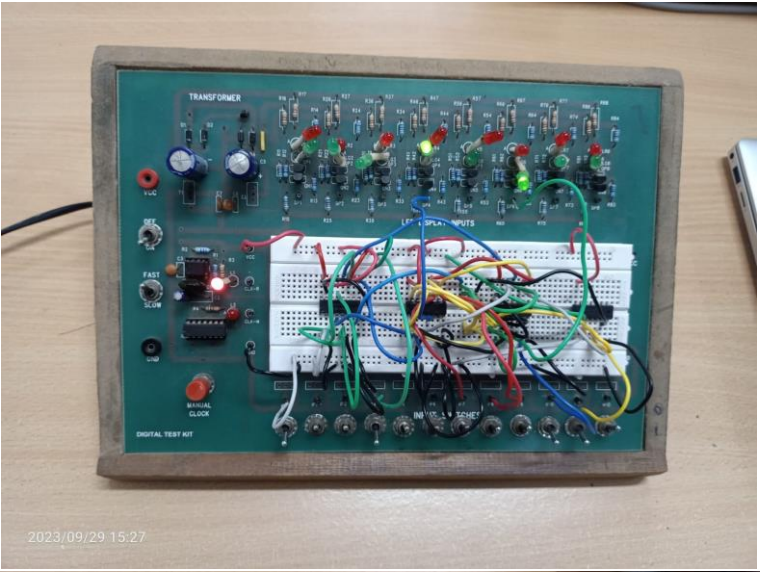| F2 F1 F0 | ALU FUNCTION | Y1 | Y2 |
|---|---|---|---|
| 000 | 0 | - | 0 |
| 001 | A+B | - | A+B |
| 010 | A.B | - | A.B |
| 011 | A EXOR B | - | A exor B |
| 100 | A PLUS B | CARRY | SUM |
| 101 | A MINUS B | BORROW | DIFF |
| 110 | A PLUS B PLUS C | CARRY | SUM |
| 111 | A MINUS B MINUS C | BORROW | DIFF |

# REFERENCE CIRCUIT:



## LINK FOR TINKERCAD SIMULATION :

https://www.tinkercad.com/things/erhuHdWMkWC-shiny-allis-elzing/editel?sharecode=SnIbyrEy4qZKIaBpDDDHOy7Ls366MLz1s9kG3AjSlIQ
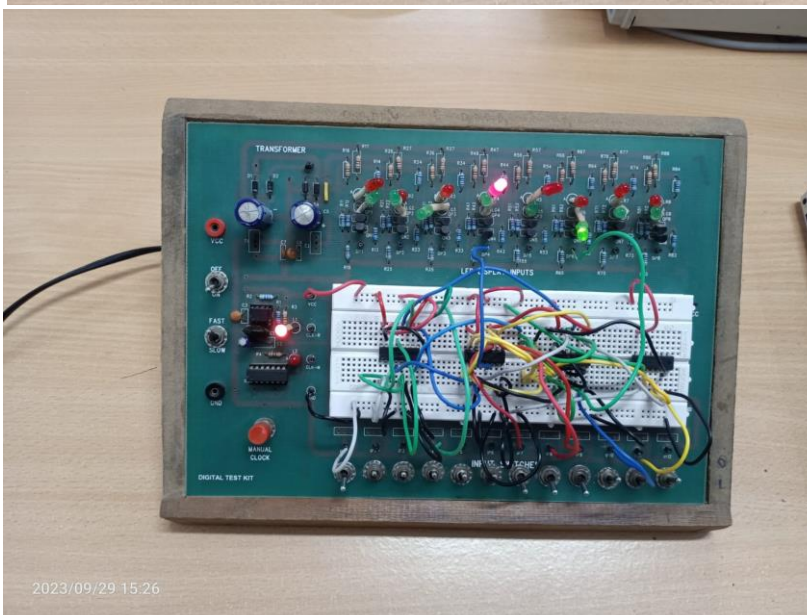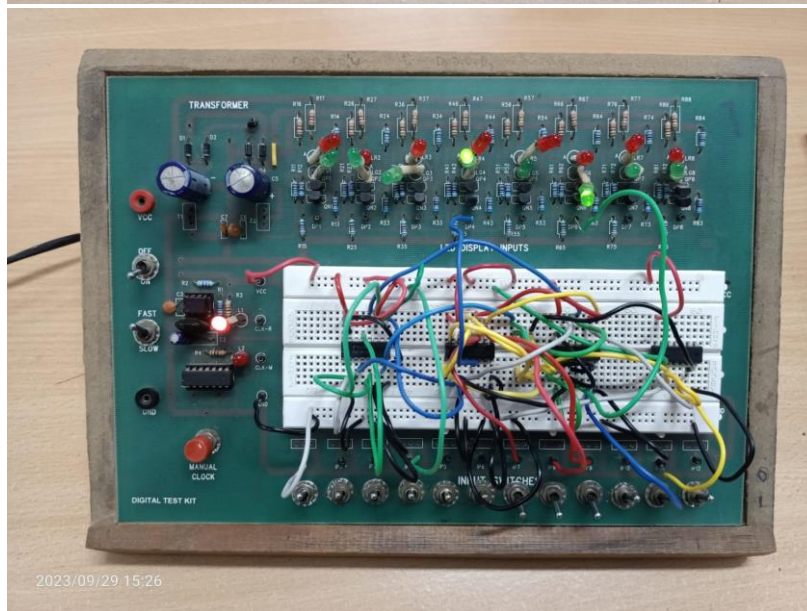
## OBSERVATION IN TINKERCARD :

2023/09/29 15:26



2023/09/29 15:26



2023/09/29 15:26

1) 0

| F2 | F1 | F0 | A | B | C | Y1 | Y0 |
|----|----|----|---|---|---|----|----|
| 0 | 0 | 0 | X | X | X | 0 | 0 |

2) A OR B

| F2 | F1 | F0 | A | B | C | Y1 | Y0 |
|----|----|----|---|---|---|----|----|
| 0 | 0 | 1 | 0 | 0 | X | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | X | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | X | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | X | 0 | 1 |

3) A AND B

| F2 | F1 | F0 | A | B | C | Y1 | Y0 |
|----|----|----|---|---|---|----|----|
| 0 | 1 | 0 | 0 | 0 | X | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | X | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | X | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | X | 0 | 1 |

4) **A XOR B**

| F2 | F1 | F0 | A | B | C | Y1 | Y0 |
|----|----|----|---|---|---|----|----|
| 0 | 1 | 1 | 0 | 0 | X | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | X | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | X | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | X | 0 | 0 |

5) **A+B**

| F2 | F1 | F0 | A | B | C | Y1 | Y0 |
|----|----|----|---|---|---|----|----|
| 1 | 0 | 0 | 0 | 0 | X | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | X | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | X | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | X | 1 | 0 |

6) **A-B**

| F2 | F1 | F0 | A | B | C | Y1 | Y0 |
|----|----|----|---|---|---|----|----|
| 1 | 0 | 1 | 0 | 0 | X | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | X | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | X | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | X | 0 | 0 |

7) **A+B+C**

| F2 | F1 | F0 | A | B | C | Y1 | Y0 |
|----|----|----|---|---|---|----|----|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |

8) **A-B-C**

| F2 | F1 | F0 | A | B | C | Y1 | Y0 |
|----|----|----|---|---|---|----|----|
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## CONCLUSION:

An ALU was designed and tested that could perform 8 arithmetic/ logical operations.