Lab Report:2

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Group No.: 8

Table No.:35

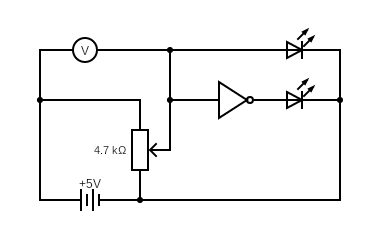
**Experiment 1**

Objective: Identification of logic levels with potentiometer

Electronic Component Used:

* Battery
* Hex Invertor (NOT gate)
* Multimeter
* Potentiometer
* Red and Green LED bulbs
* Wire

The Reference Circuit:



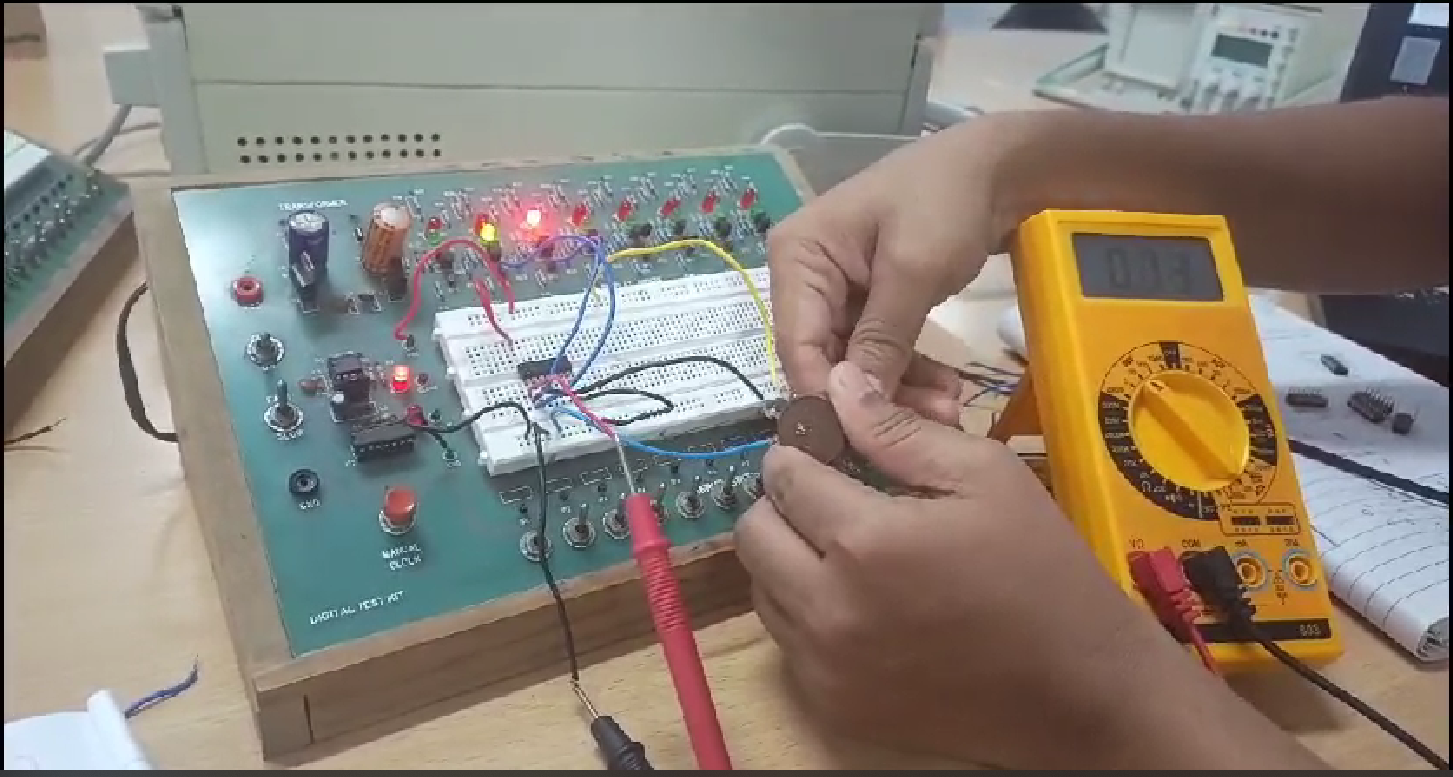
Procedure:

1. First of all, we connected the vcc and ground of potentiometer.
2. Then, we connected the multimeter with vcc and its other end with a LED bulb to ground, NOT GATE (Hex Invertor) and with the potentiometer parallel to each other.
3. At last, we connected the other end of NOT GATE with another LED bulb which was later connected to ground.

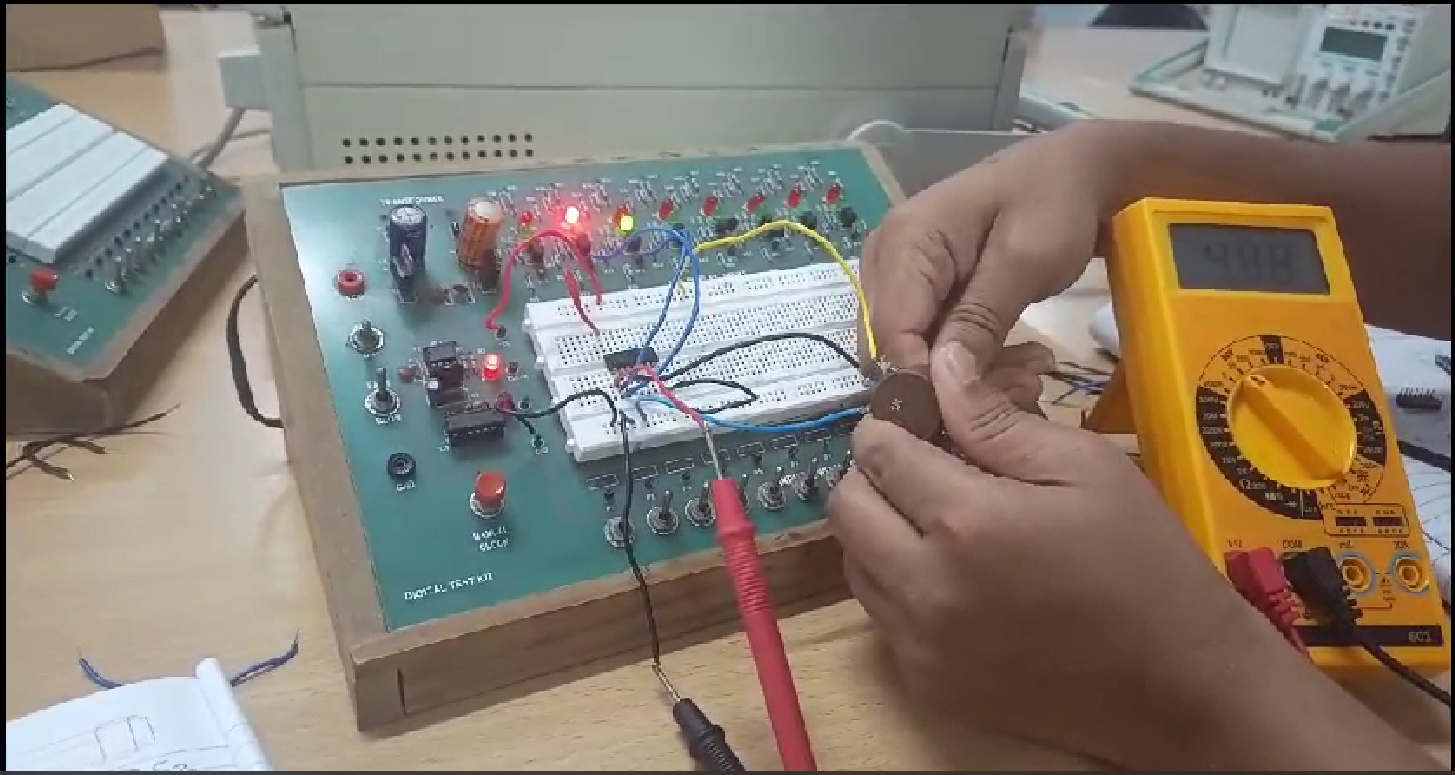
Observation:

When the input voltage is low (0 ≤ VIL≤ 0.8), the output voltage is max=4.99V (2.4 ≤ VOH ≤ 5.0). And when input voltage is high, (2.0 ≤ VIH ≤ 5.0), the output voltage is low (0 ≤ VOL ≤ 0.4).

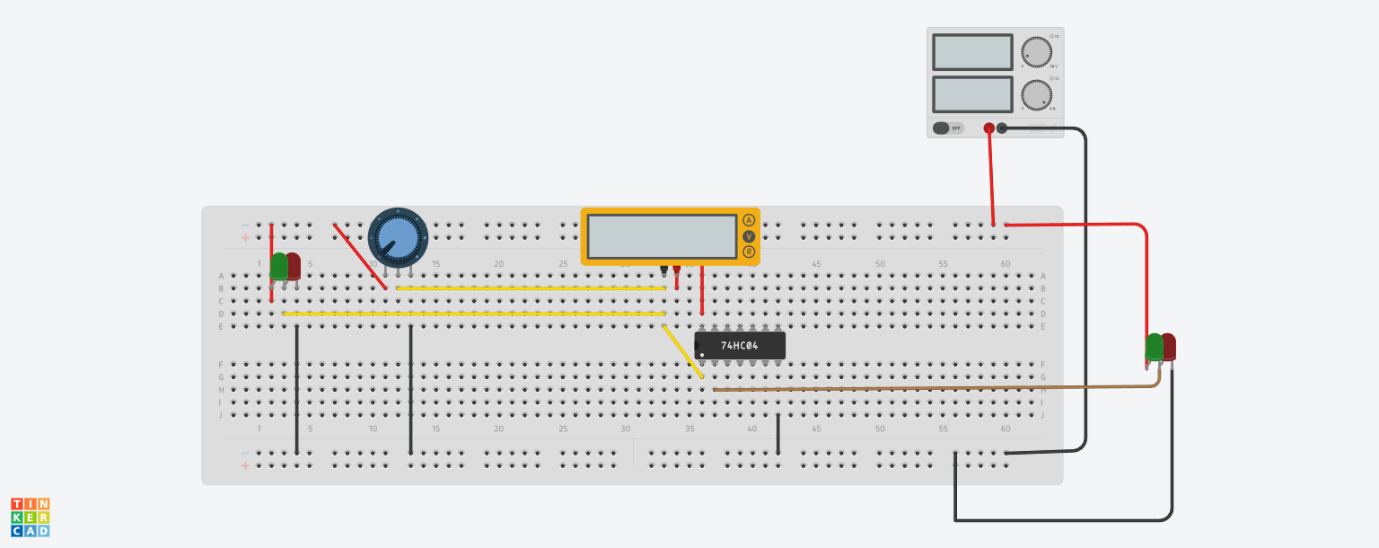
**Low INPUT:**



**High INPUT:**

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Link for the Tinkercad simulation:



 Link :

<https://www.tinkercad.com/things/0Z6gTuCyIPJ-lab2exp1/editel?sharecode=mPulkGzfiz5qX4b-ZovOYdEndbLsllKsnBfeKPCwjCs>

**Experiment 2**

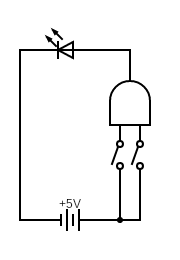
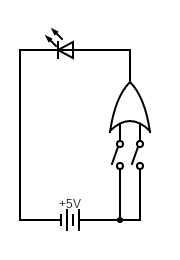
Objective: Identification of various GATE

Electronic Component Used:

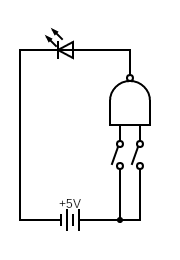
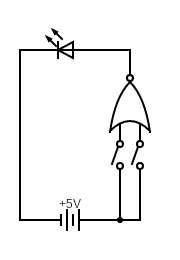
* Logic GATES (AND, OR, NAND, NOR, XOR, NOT)
* Battery
* LED bulb
* Wire
* Switches

The Reference Circuit:

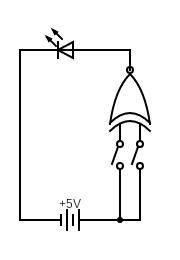
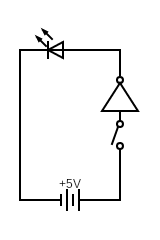
**AND OR**

** **

**NAND NOR**

** **

**XNOR NOT**

** **

Procedure:

**For TTL 74LSxx**(except NOT GATE) **ICs**

1. First of all, we connected the vcc and ground of LOGIC GATE.
2. Then, we connected two switches parallel to each other.
3. Then, we connected the other two ends of switches with the LOGIC GATE input pin 1 and 2.
4. From the output of LOGIC GATE pin 3, we connected the LED bulb and then to the ground.

**For CMOS CD40xx ICs**

1. We did the same steps as for **TTL 74LSxx** ICs but instead for connecting the switches to pin 5 and 6.
2. For the output we will collect it from pin 4.

Observation:

From the experiment, we observed the following;

**For TTL 74LS04**

|  |  |
| --- | --- |
| **INPUT** | **OUTPUT** |
| 0 | 1 |
| 1 | 0 |

**For TTL 74LS08**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **OUTPUT** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**For TTL 74LS32**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **OUTPUT** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**For TTL 74LS00**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **OUTPUT** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**For TTL 74LS86**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **OUTPUT** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**For CMOS CD4001**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **OUTPUT** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

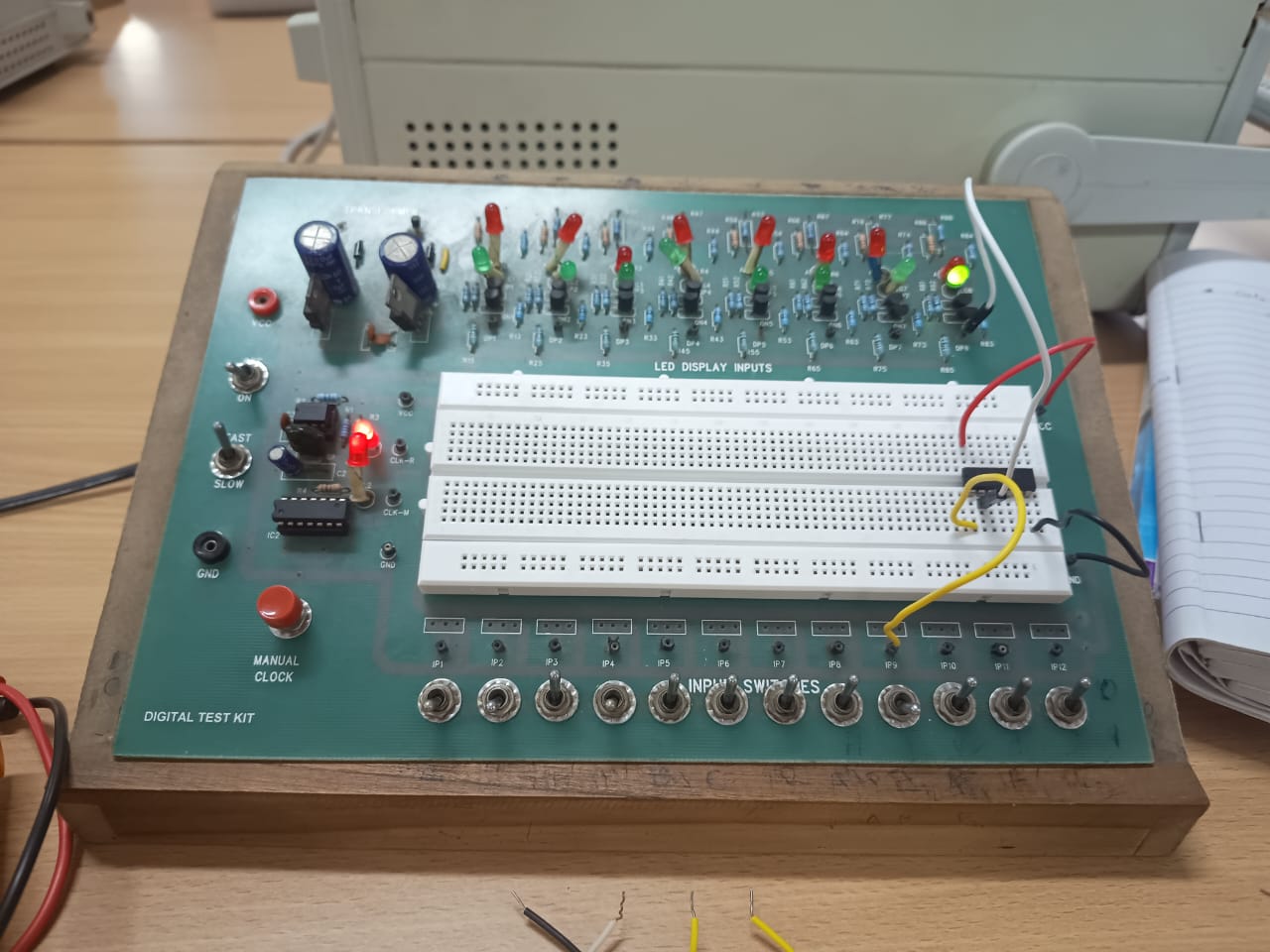
Conclusion:

From the experiment we can identify gate as following:

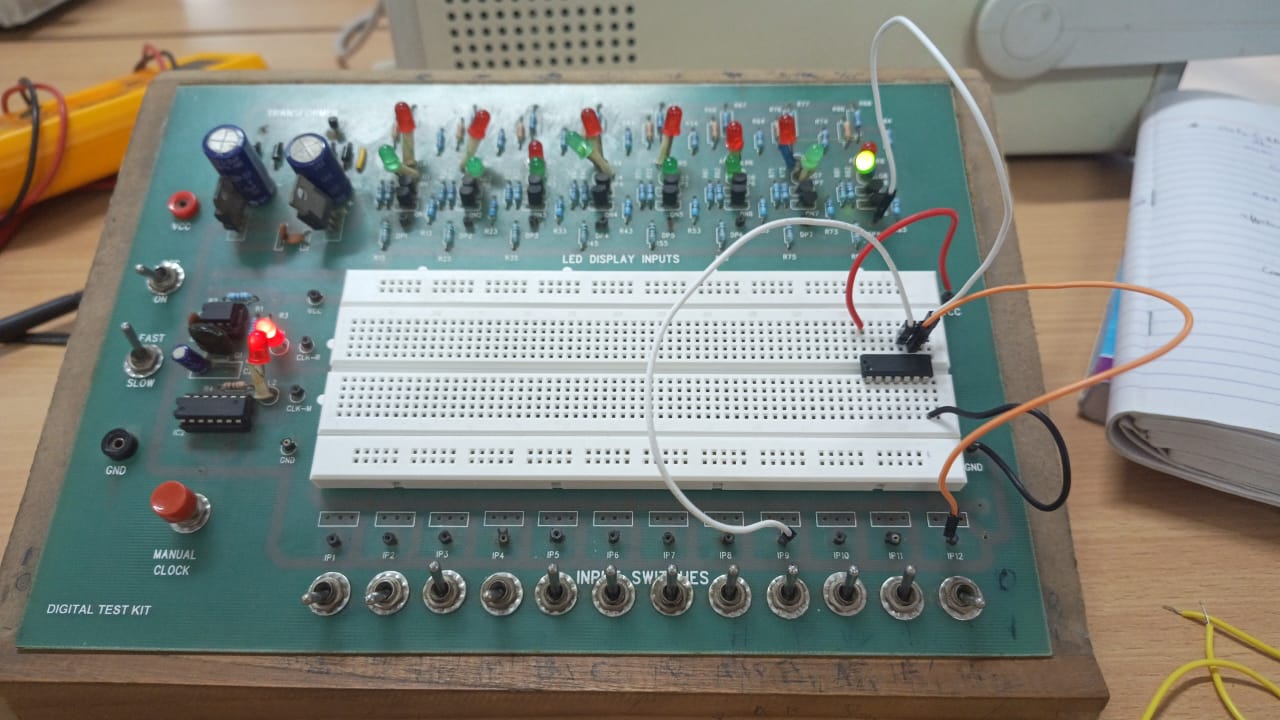
|  |  |
| --- | --- |
| **GATE Series** | **GATE Name** |
| TTL 74LS04 | NOT |
| TTL 74LS08 | AND |
| TTL 74LS32 | OR |
| TTL 74LS00 | NAND |
| TTL 74LS86 | XOR |
| CMOS CD4001 | NOR |

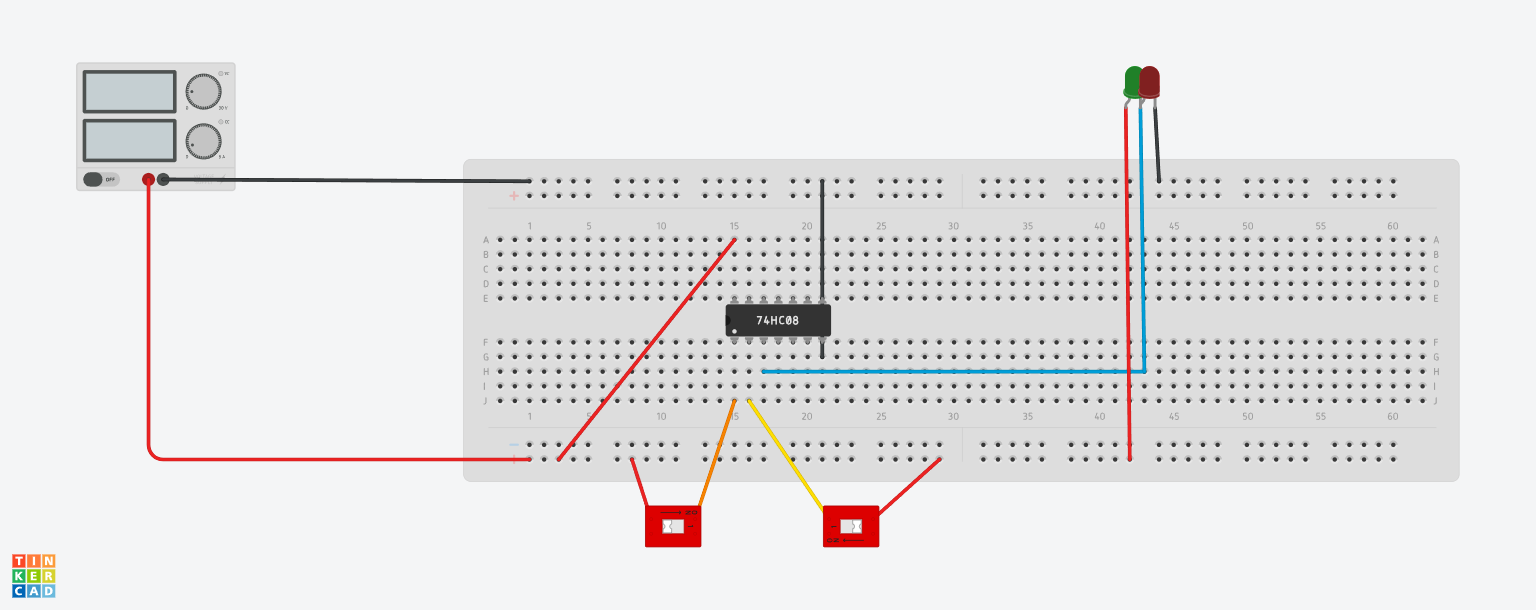
Tinkercad simulation Link and Lab Photo:

NOT GATE:



**AND GATE:**

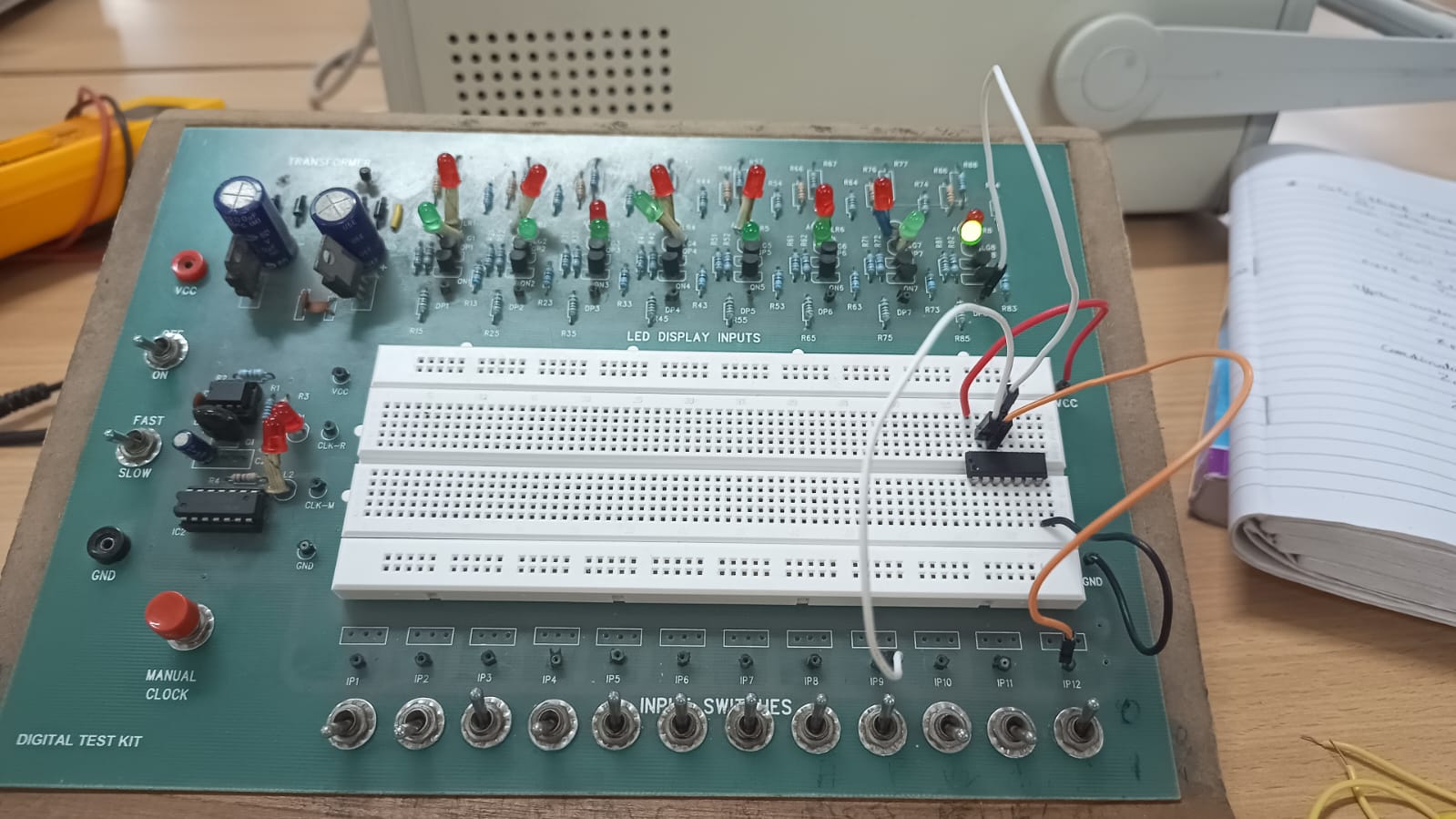


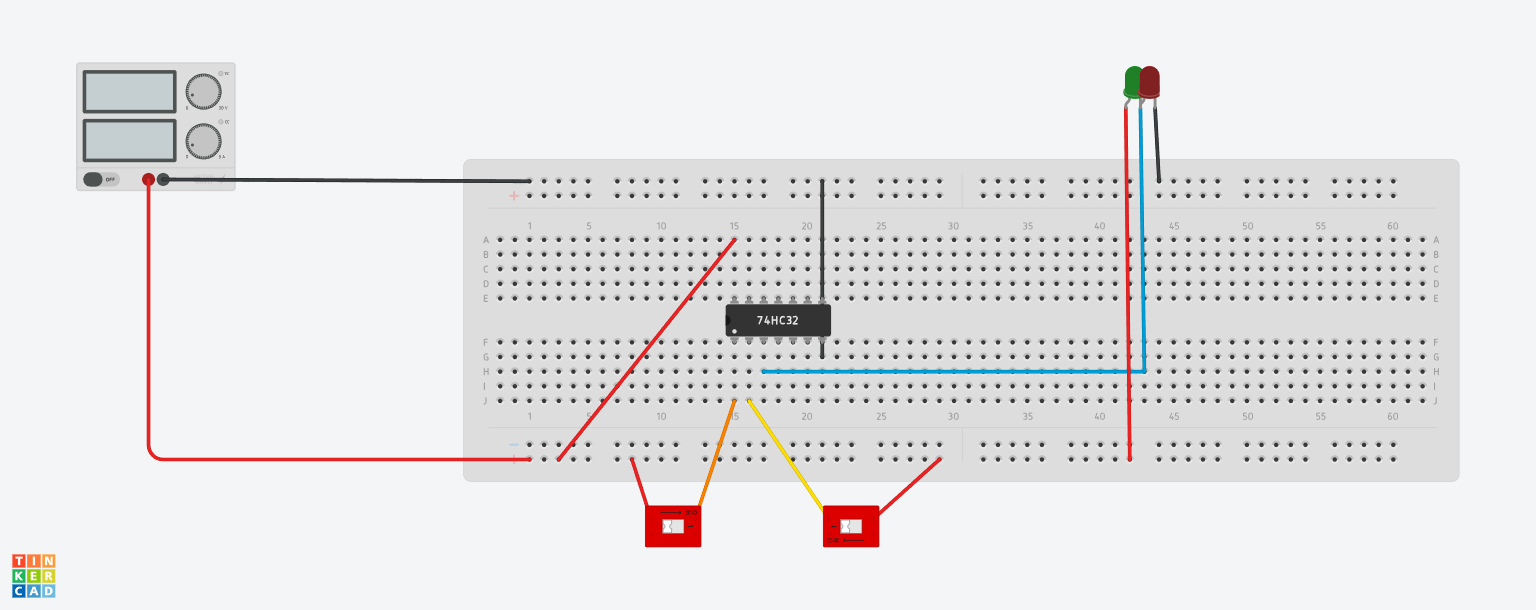


Link:

<https://www.tinkercad.com/things/97iw2p5Emmt-l2e2and/editel?sharecode=4gcg6CMp5Fp7yyIkI5qHXv4Q9Cg1iMBXUctpoITT-iA>

**OR GATE:**

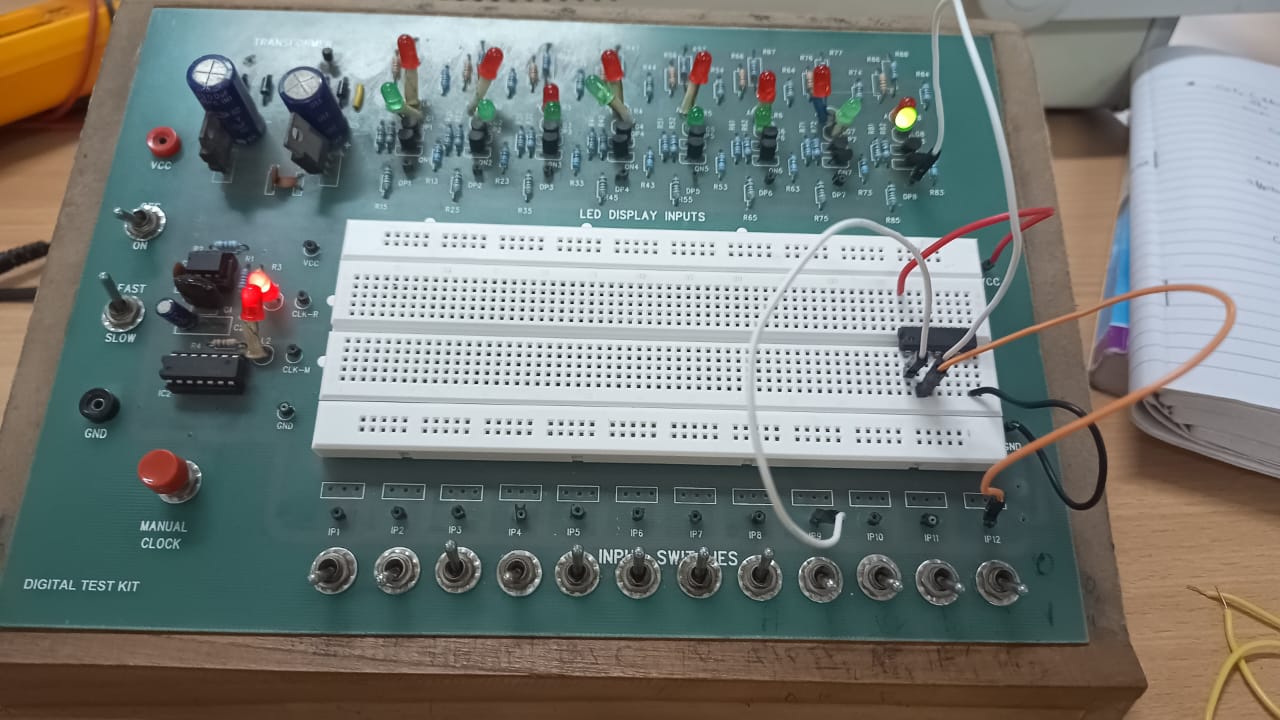
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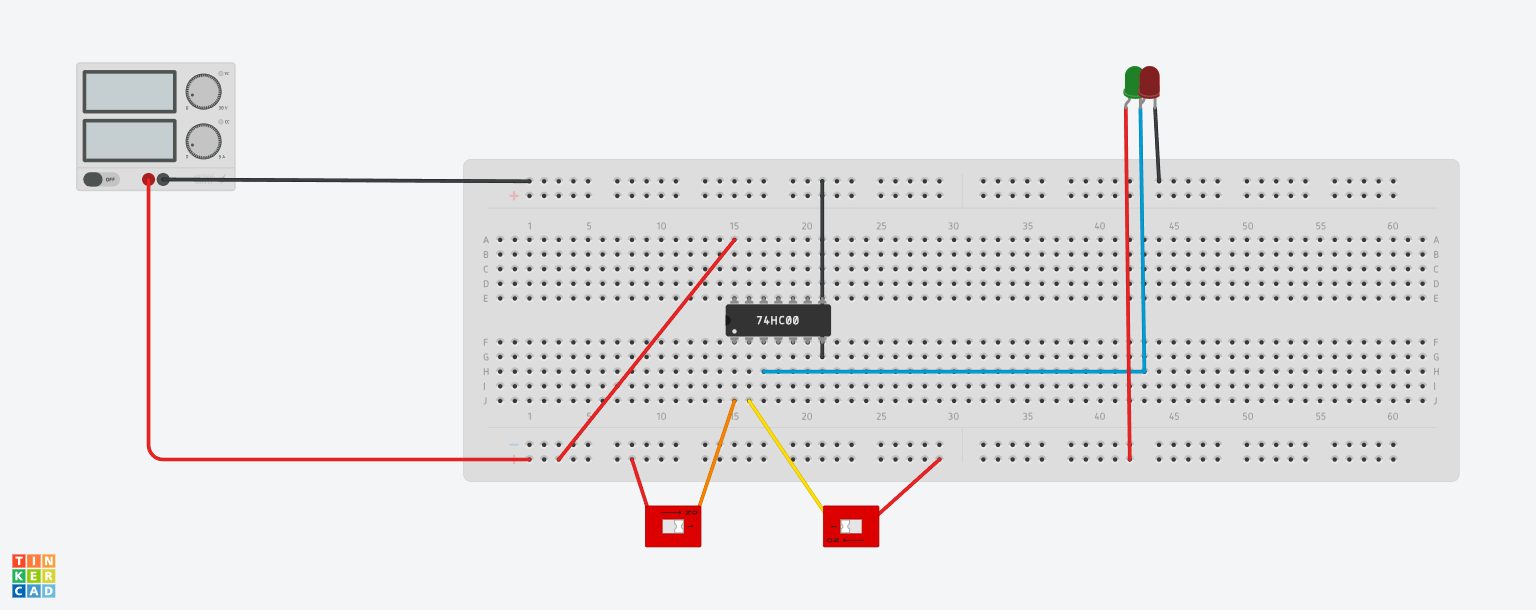


Link:

<https://www.tinkercad.com/things/bcgf2PVsML2-l2e2or/editel?sharecode=60AbXFOJ_DW5FvFYTXsi2Nk7MGcInscr1Cc9-UvEysU>

**NAND GATE:**

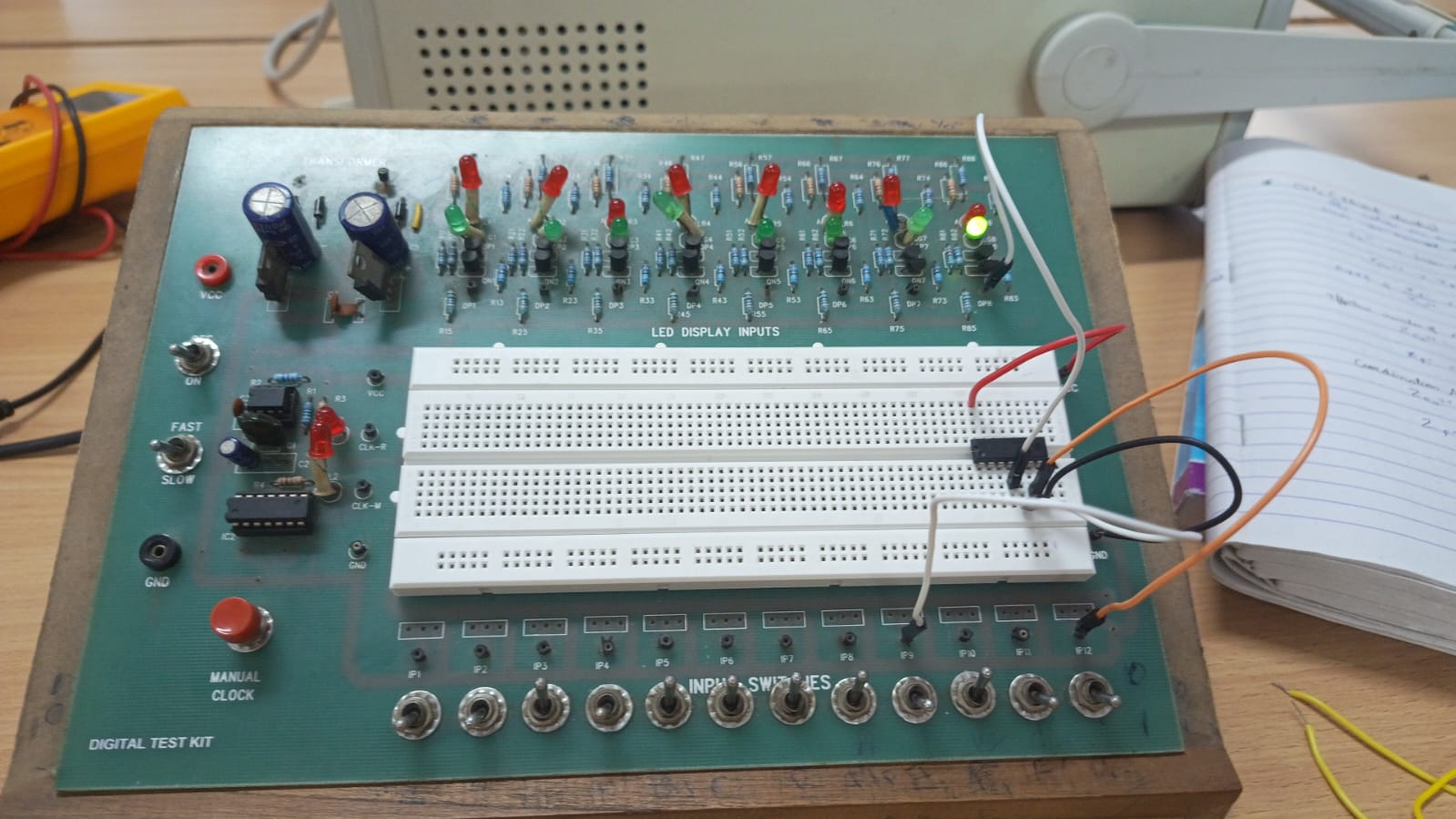
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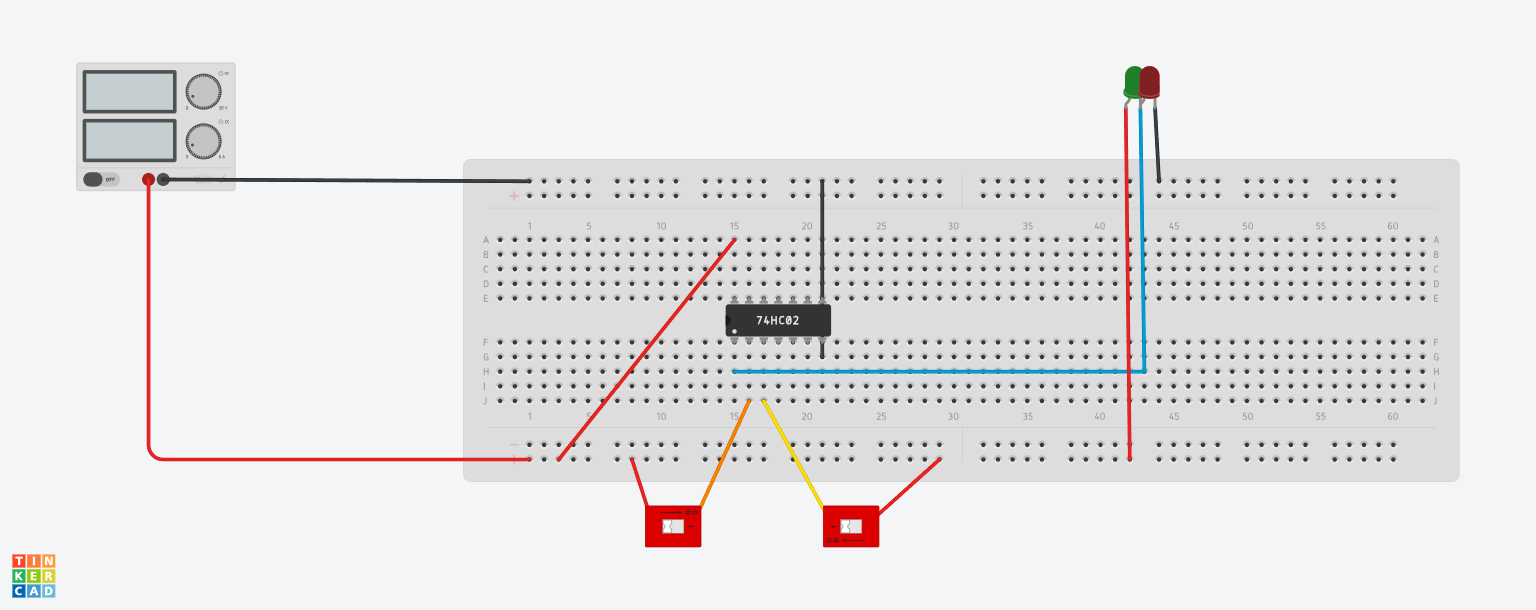


Link:

<https://www.tinkercad.com/things/2qrDHRFmEOj-l2e2nand/editel?sharecode=1j6n_lDFXmYnER46zOWsKR-L_q2pynbId5BDLyq7zZ8>

**NOR GATE :**

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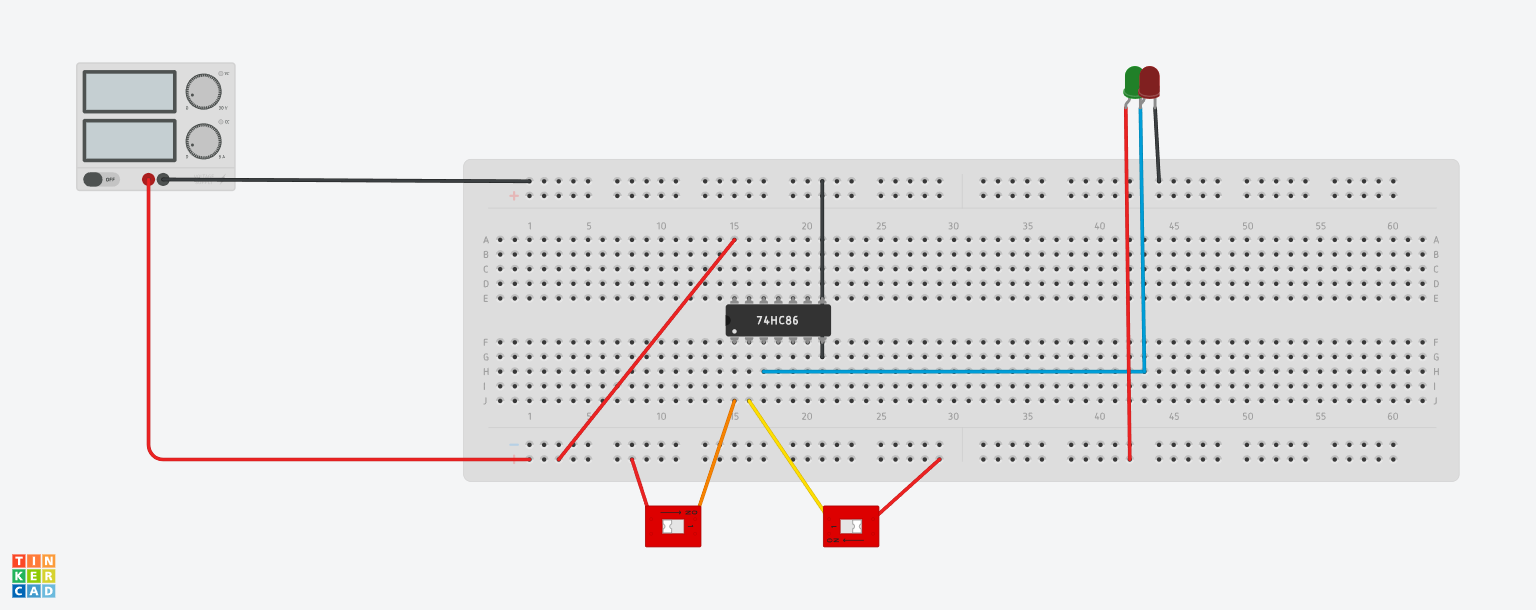
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Link:

<https://www.tinkercad.com/things/9YGtbPu5TPk-l2e2nor/editel?sharecode=huLQm_PkUrbm2utRIPvFdOh6zoMjvyLJkM7r533tINM>

**XOR GATE:**

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<https://www.tinkercad.com/things/clzFd7BUbdY-l2e2xor/editel?sharecode=7G-o6CSkX0u5CkZX0SApS7OU00nLOikrwkVr5g7Yk-c>

**Experiment 3:**

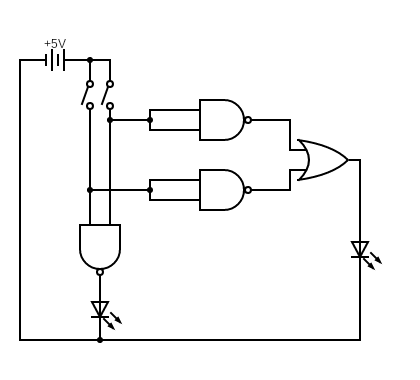
Objective: Checking De Morgan’s theorem using logic GATES

Electronic Component Used:

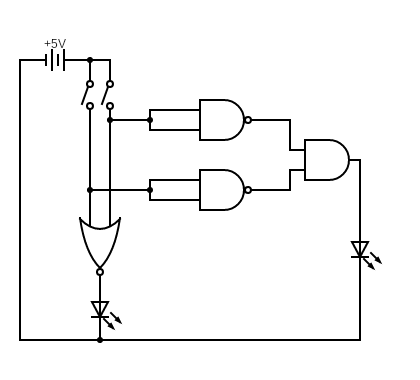
* Battery
* Logic GATES (AND, NAND, OR, NOR)
* LED bulbs
* Switches
* Wires

The Reference Circuit:

**(A • B)’ = A’ + B’**



**(A + B)’ = A’ • B’**



Procedure:

**For (A • B)’ = A’ + B’**

1. First of all, we connected the vcc and ground of Logic GATES and two switches parallel to each other with battery.
2. We connected the other end of two switches with two input pins of NAND Gate and the output pin with a LED bulb.
3. We then connected parallelly from both the switches and connected to different inner circuit of NAND Gate such that in both the INPUT pin input come from same switch.
4. Then, we will connect both output pins of NAND Gate with input pin of OR Gate.
5. Then, we will connect it with LED bulb and then to ground.

**For (A + B)’ = A’ • B’**

1. First of all, we connected the vcc and ground of Logic GATES and two switches parallel to each other with battery.
2. We connected the other end of two switches with two input pins of NOR Gate and the output pin with a LED bulb.
3. We then connected parallelly from both the switches and connected to different inner circuit of NAND Gate such that in both the INPUT pin input come from same switch.
4. Then, we will connect both output pins of NAND Gate with input pin of AND Gate.
5. Then, we will connect it with LED bulb and then to ground.

Observation:

We observed that both the LED bulbs glow in following ways:

**For (A • B)’ = A’ + B’**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **(A • B)’** | **A’ + B’** |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

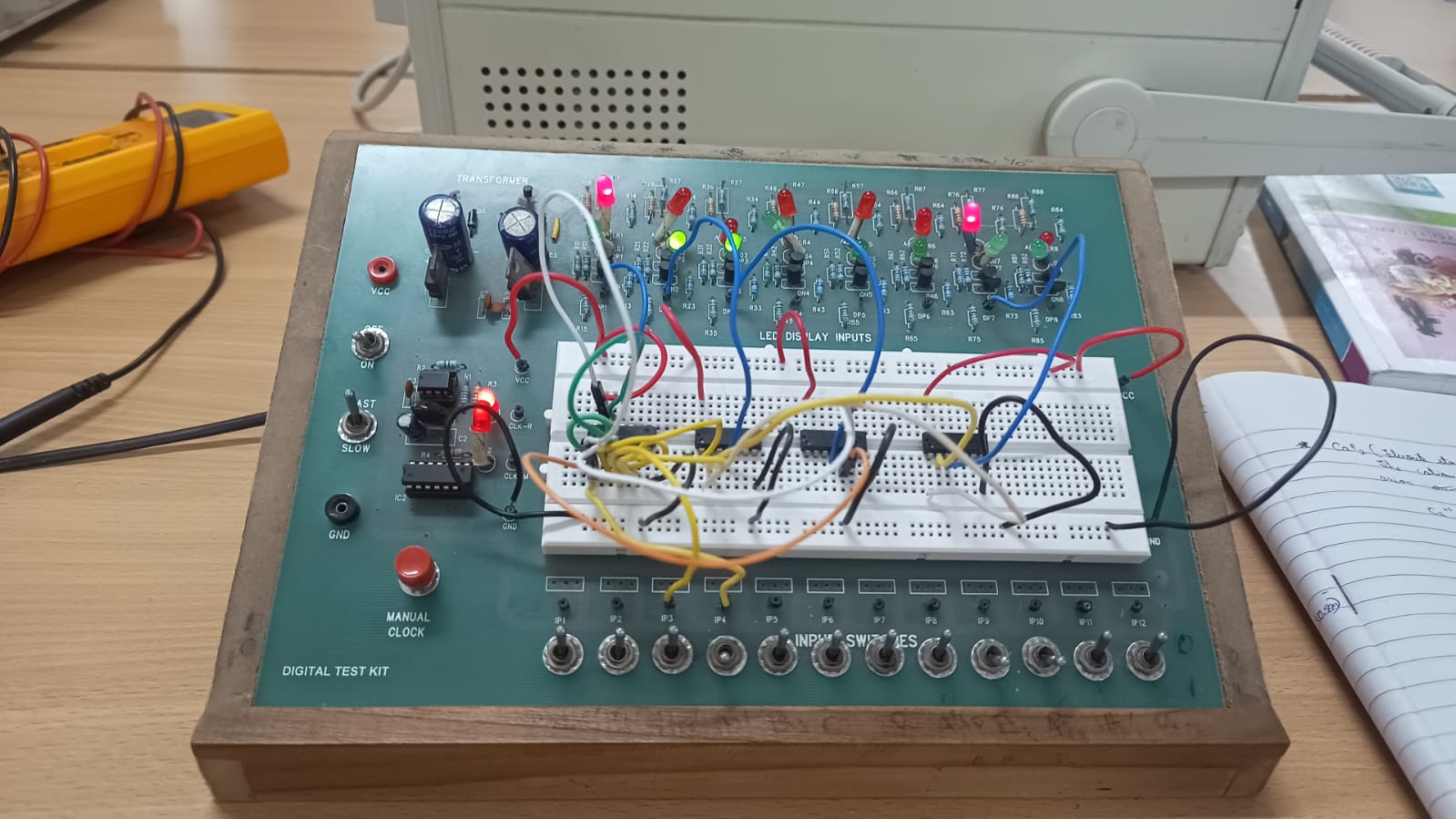
**For (A + B)’ = A’ • B’**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **(A + B)’** | **A’ • B’** |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |

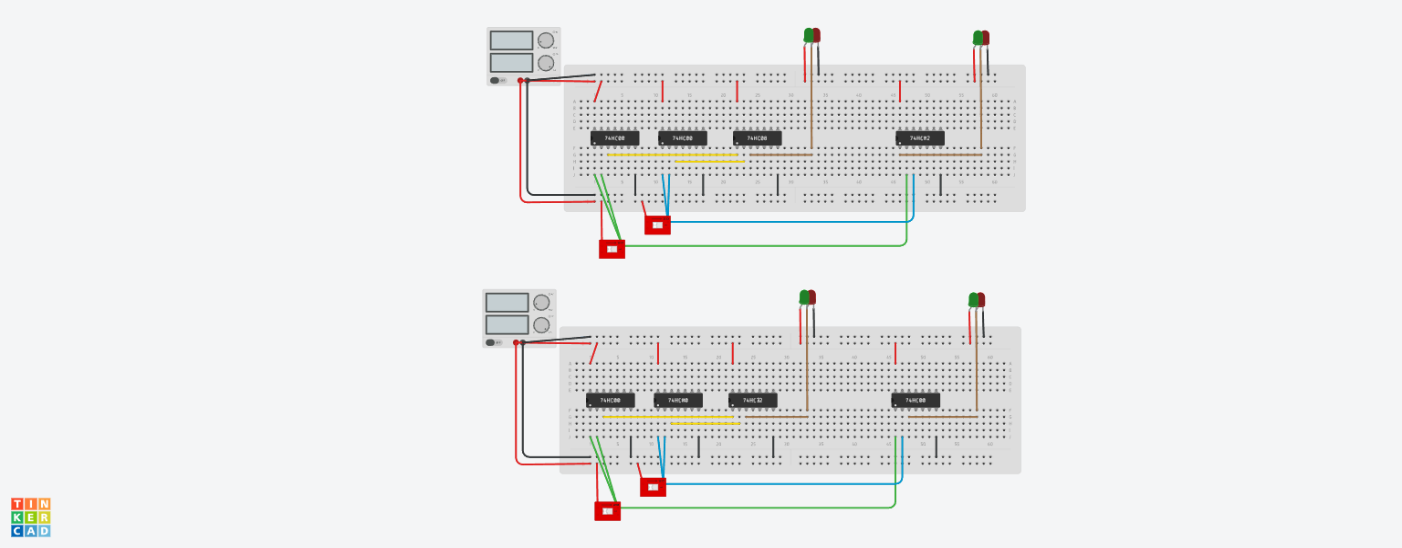
Conclusion:

As both the LED bulbs glow together, we can conclude that De Morgan’s Law is true.

Tinkercad simulation and Lab photo:



In the above photo D1 and d7 are together



Link:

<https://www.tinkercad.com/things/g0IvE3C3B3i-l2e3/editel?sharecode=jRRSpY2BdazUjpH0XwMYnXg1c5tlDTCjyBb_I9NP-R8>

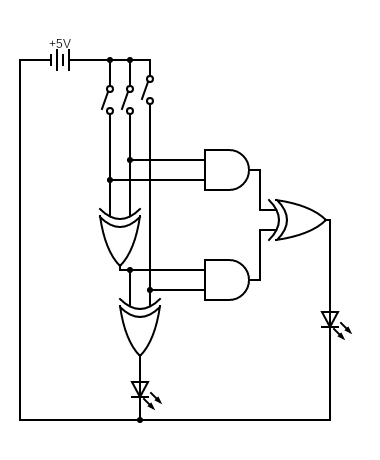
**Experiment 4:**

Objective: Make a binary full adder using logic GATES

Electronic Component Used:

* Battery
* Logic GATES (AND and XOR)
* Wire
* Switches
* LED bulbs

The Reference Circuit:



Procedure:

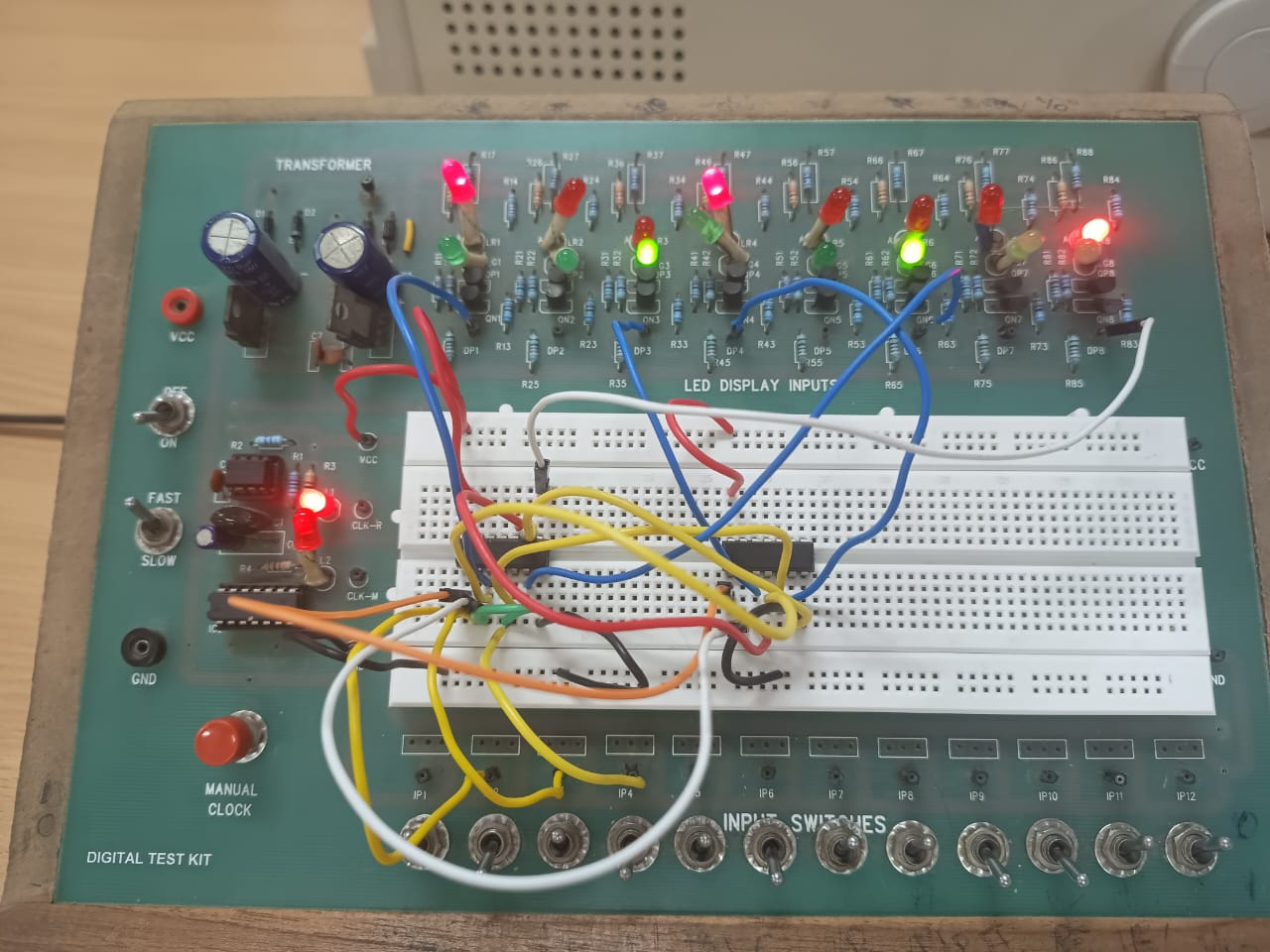
1. First of all, we connected three switches parallel to each other from the battery.
2. We connected the first two switches with input pins of XOR Gate and its output with another input pin of XOR Gate and the other input pin with third switch.
3. We connected the output pin of second XOR Gate with bulb indicating **SUM**.
4. We connected the first two switches parallelly with input pins of AND Gate.
5. We connected the third switch and output pin of first XOR Gate with another AND Gate.
6. Then, we connected the output pin of both the AND Gate as input of another XOR Gate and then to LED bulb to ground and this bulb will indicate **CARRY**.

Observation:

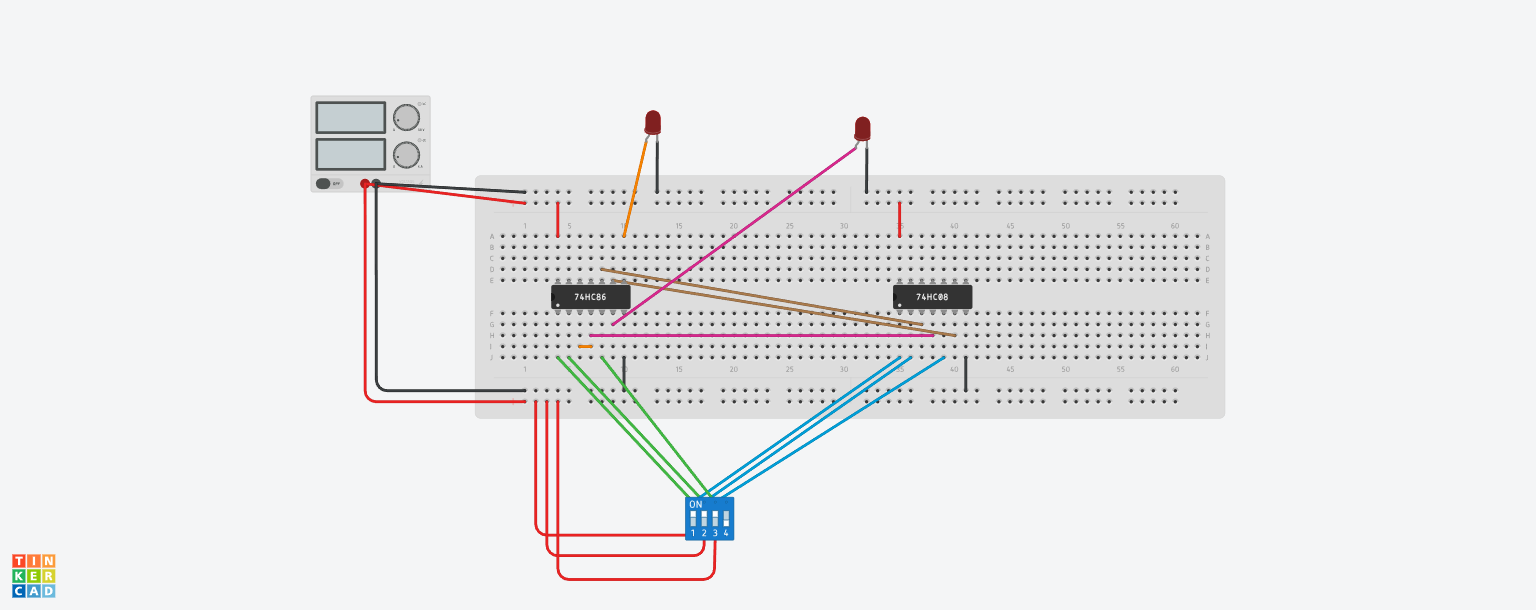
We observed the SUM and CARRY in following ways:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **SUM** | **CARRY** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Tinkercad simulation and Lab photo:



In the above photo D6 is SUM and D8 is CARRY.



Link: <https://www.tinkercad.com/things/gzVVFdnUTm1-l2e4/editel?sharecode=S2mLU75YEWhru_Dsqm_cmnswpD31DiOiepIZx9IPM7I>