Mikroişlemci Sistemleri

Dr. Öğr. Üyesi Erkan Uslu

10

YTÜ-CE

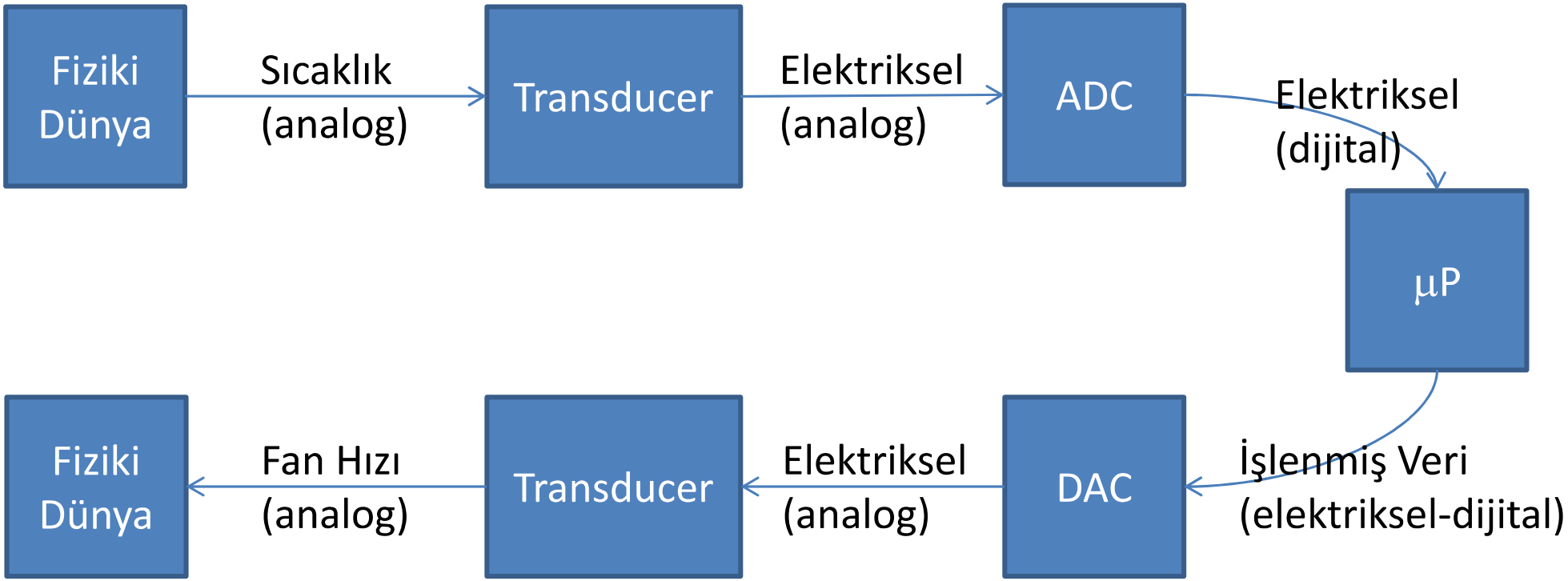
Ders-10 Konular

- DAC (digital to analog converter)
  - Binary weighted DAC
  - R/2R ladder DAC
  - DAC entegresi : DAC0830
  - DAC örneği
- ADC (analog to digital converter)
  - Parallel ADC
  - Ramp converter ADC
  - ADC entegresi : ADC0804
  - ADC örneği

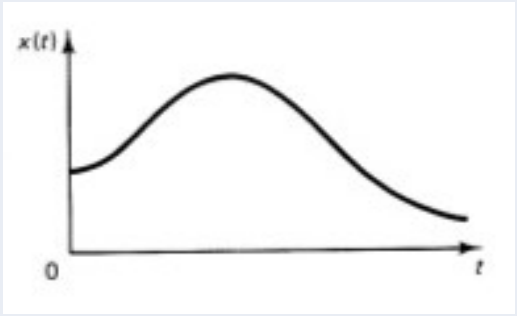
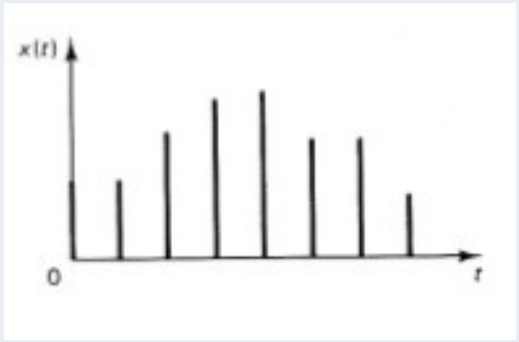
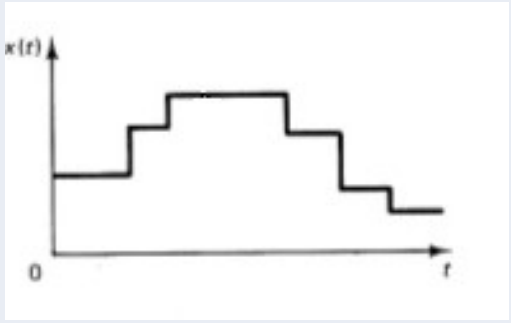
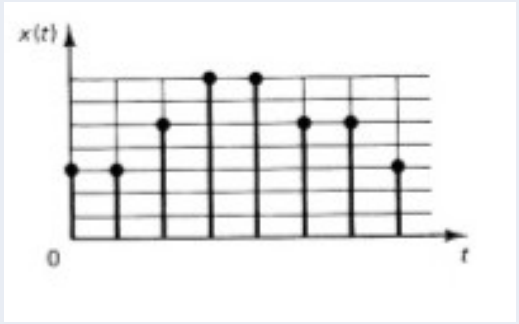
DAC – digital to analog converter
ADC – analog to digital converter

- μP dijital değerlerle çalışır, ama fiziki dünya analogtur.
- Sıcaklık, basınç, nem, hız, ses … : analog değerlerdir.
- Fiziki dünya ile μP arasında etkileşim için Analog↔Dijital dönüştürücü gerekli.

DAC – digital to analog converter
ADC – analog to digital converter

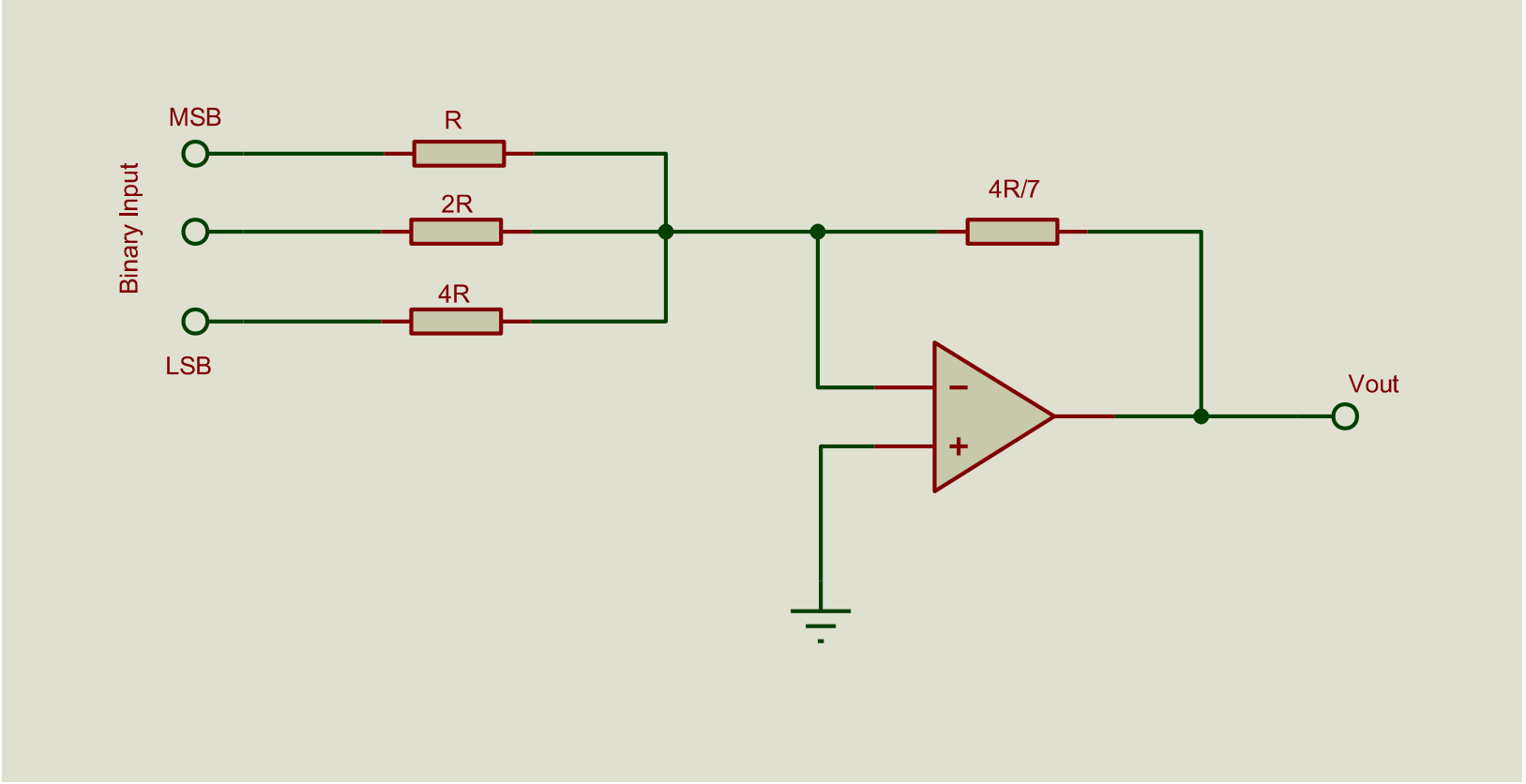


Analog-Dijital Sinyal

	Zamanda Sürekli Sinyal	Zamanda Ayrık Sinyal
Genliği Sürekli Sinyal		
Genliği Ayrık Sinyal		

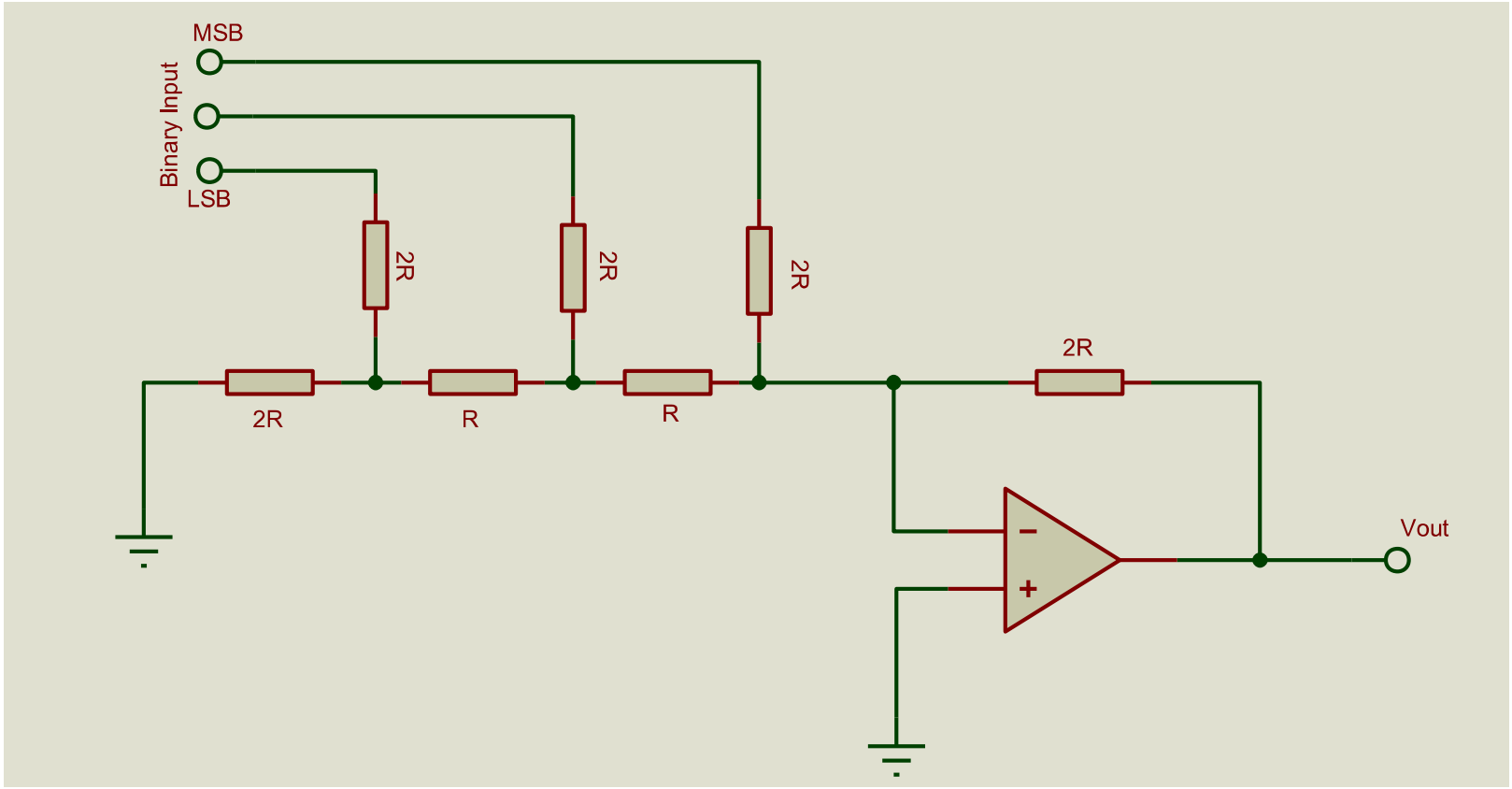
DAC (digital to analog converter)

Binary weighted DAC

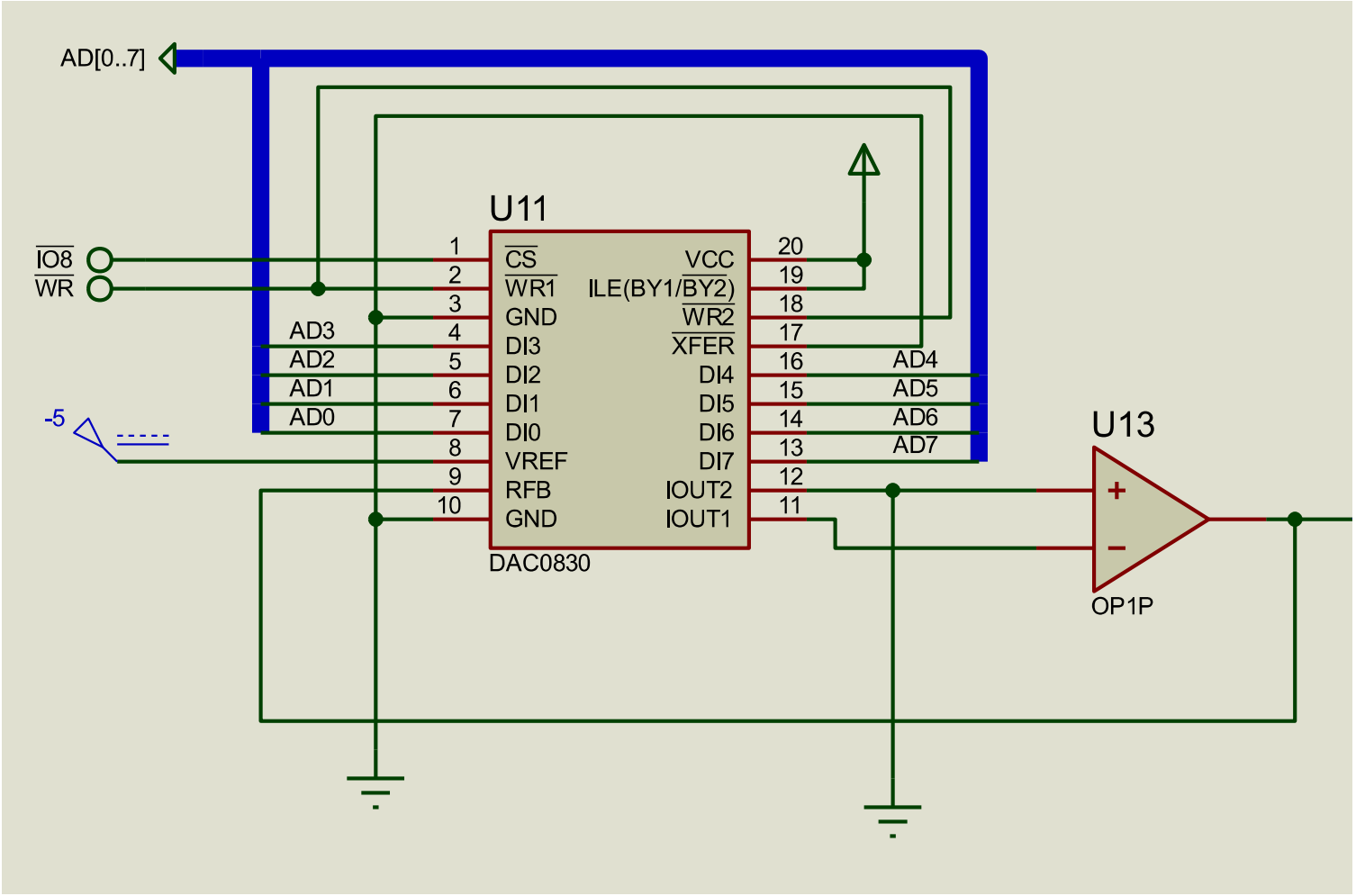


DAC (digital to analog converter)

R/2R ladder DAC



DAC0830


AD[0..7]
U11
IO8
WR
-5
AD3
AD2
AD1
AD0
1 CS
2 WR1
3 GND
4 DI3
5 DI2
6 DI1
7 DI0
8 VREF
9 RFB
10 GND
20 VCC
19 ILE(BY1/BY2)
18 WR2
17 XFER
16 DI4
15 DI5
14 DI6
13 DI7
12 IOUT2
11 IOUT1
AD4
AD5
AD6
AD7
DAC0830
U13
+
–
OP1P

DAC0830

$\overline{CS}$: **Chip Select** (active low). The CS in combination with ILE will enable WR1.

ILE: Input Latch Enable (active high). The ILE in combination with CS enables WR1.

$\overline{WR_1}$: **Write 1.** The active low WR1 is used to load the digital input data bits (DI) into the input latch. The data in the input latch is latched when WR1 is high. To update the input latch–CS and WR1 must be low while ILE is high.

$\overline{WR_2}$: **Write 2** (active low). This signal, in combination with XFER, causes the 8-bit data which is available in the input latch to transfer to the DAC register.

$\overline{XFER}$: **Transfer control signal** (active low). The XFER will enable WR2.

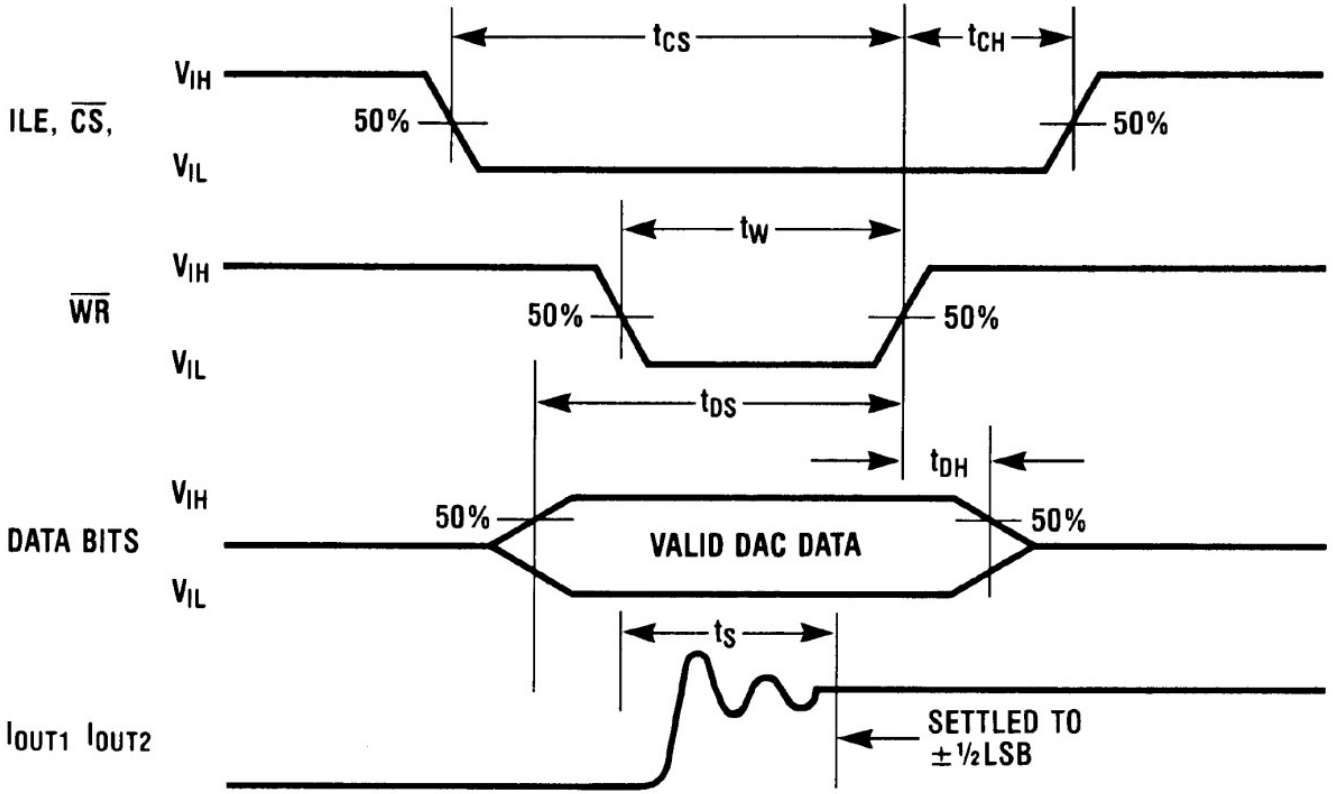
DI_0-DI_7: **Digital Inputs.**

IOUT1: DAC Current Output 1 - IOUT2: DAC Current Output 2 : to OPAMP

Rfb: Feedback Resistor for R-2R

VREF: Reference Voltage Input. This input connects an external precision voltage source to the internal R-2R ladder. **VCC - GND**

DAC0830

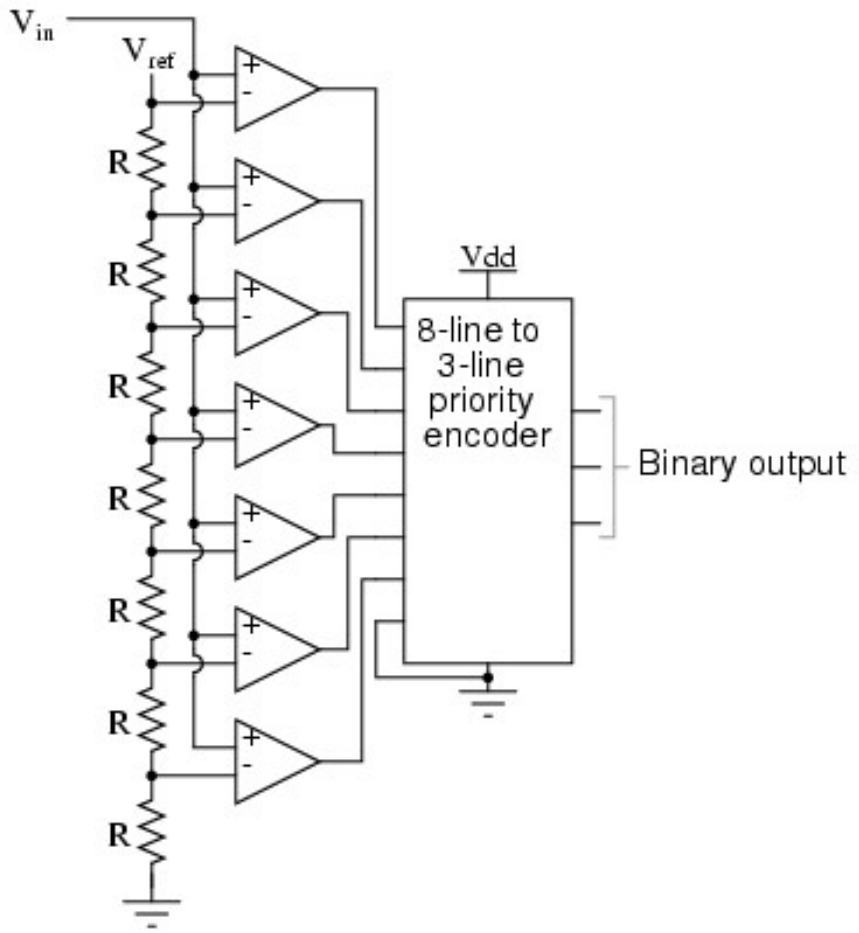

ILE, $\overline{CS}$,
V_{IH}
V_{IL}
t_{CS}
t_{CH}
50%
50%
$\overline{WR}$
t_W
50%
50%
DATA BITS
t_{DS}
t_{DH}
50%
50%
VALID DAC DATA
t_S
I_{OUT1} I_{OUT2}
SETTLED TO
±½LSB

Örnek

```
MOV DX, 1000H
MOV AL, 00H
TEKRAR:
OUT DX, AL
CALL DELAY
INC AL
JMP TEKRAR
```

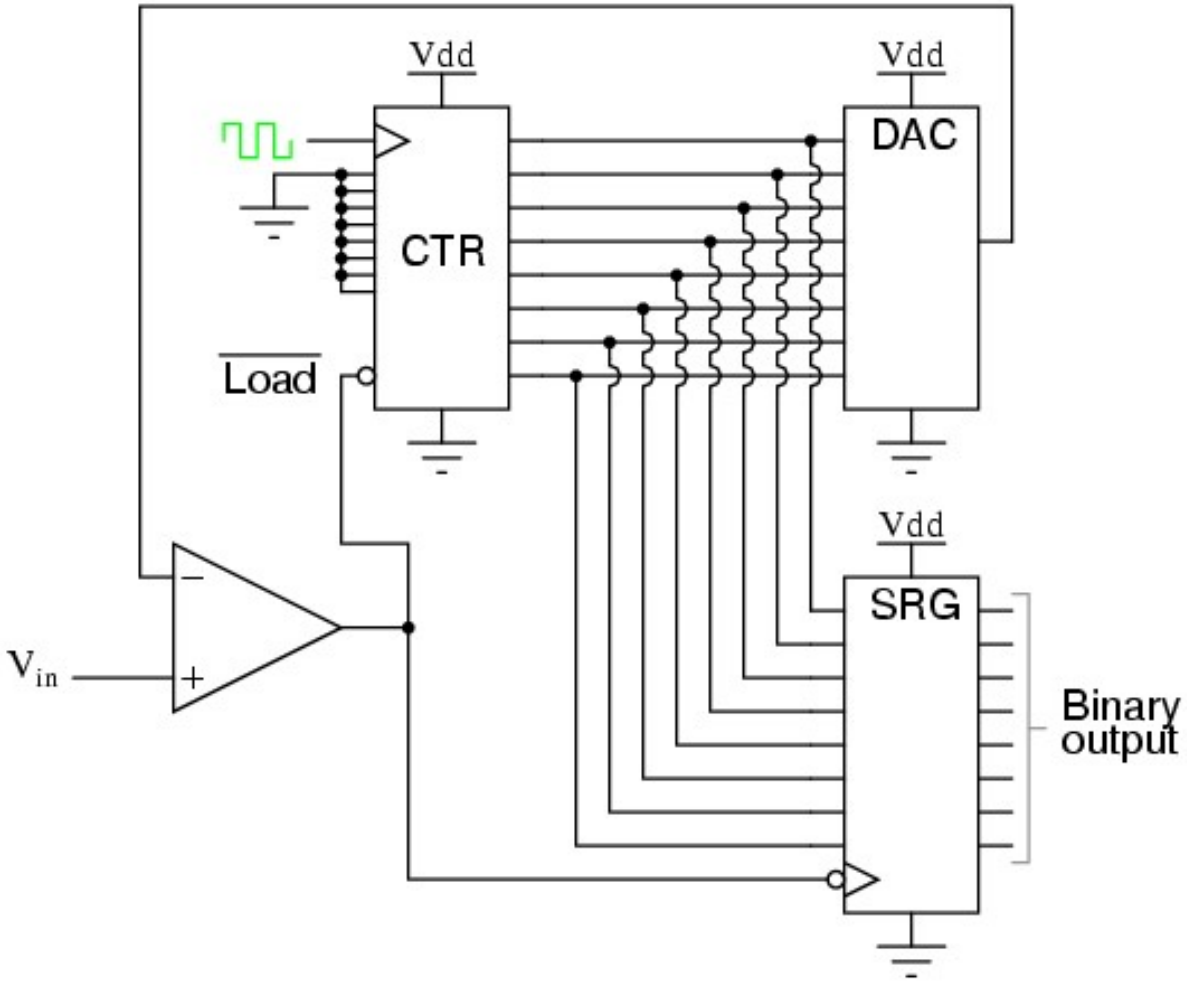
ADC (analog digital converter)

- Parallel ADC

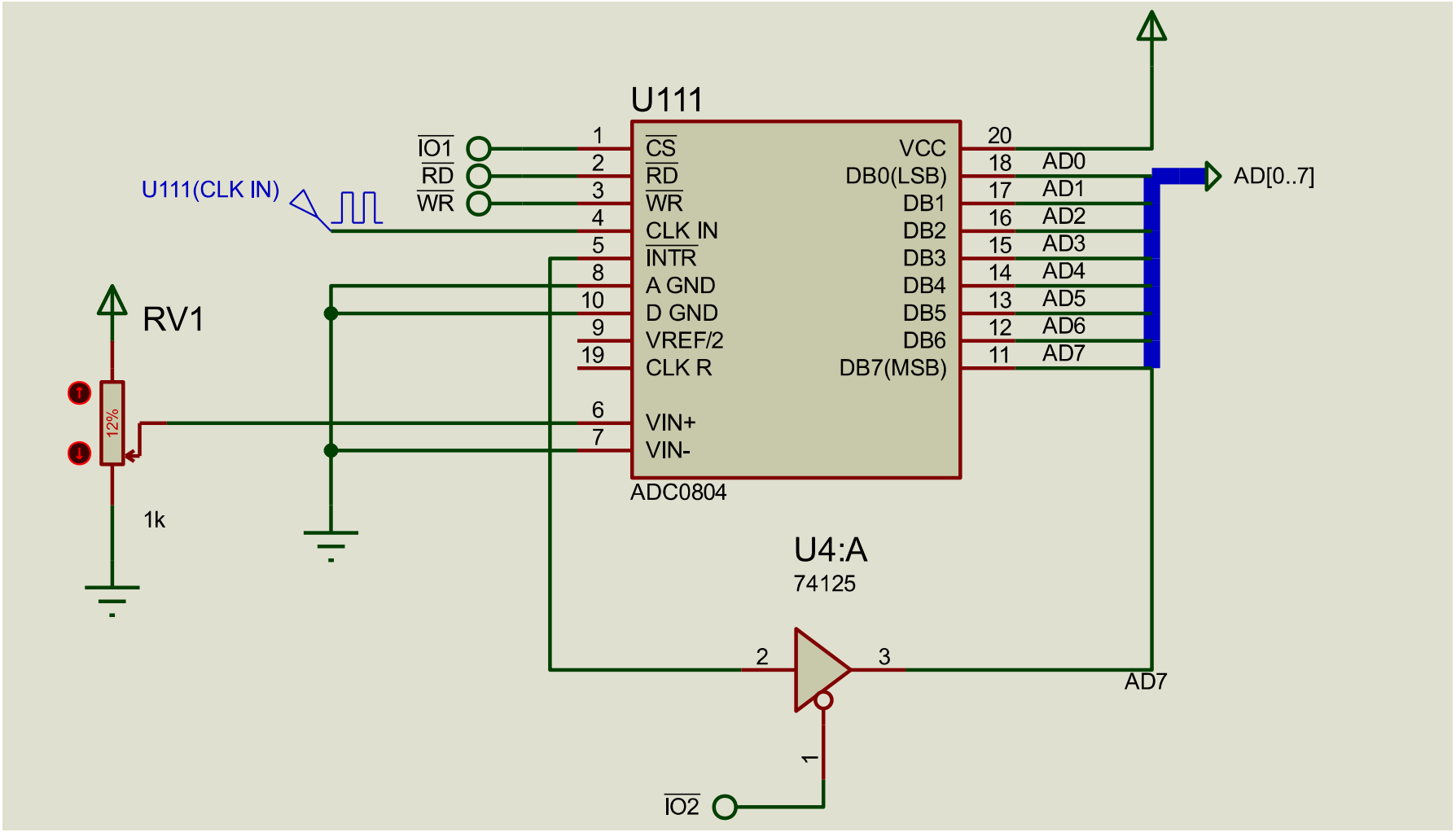


ADC (analog digital converter)

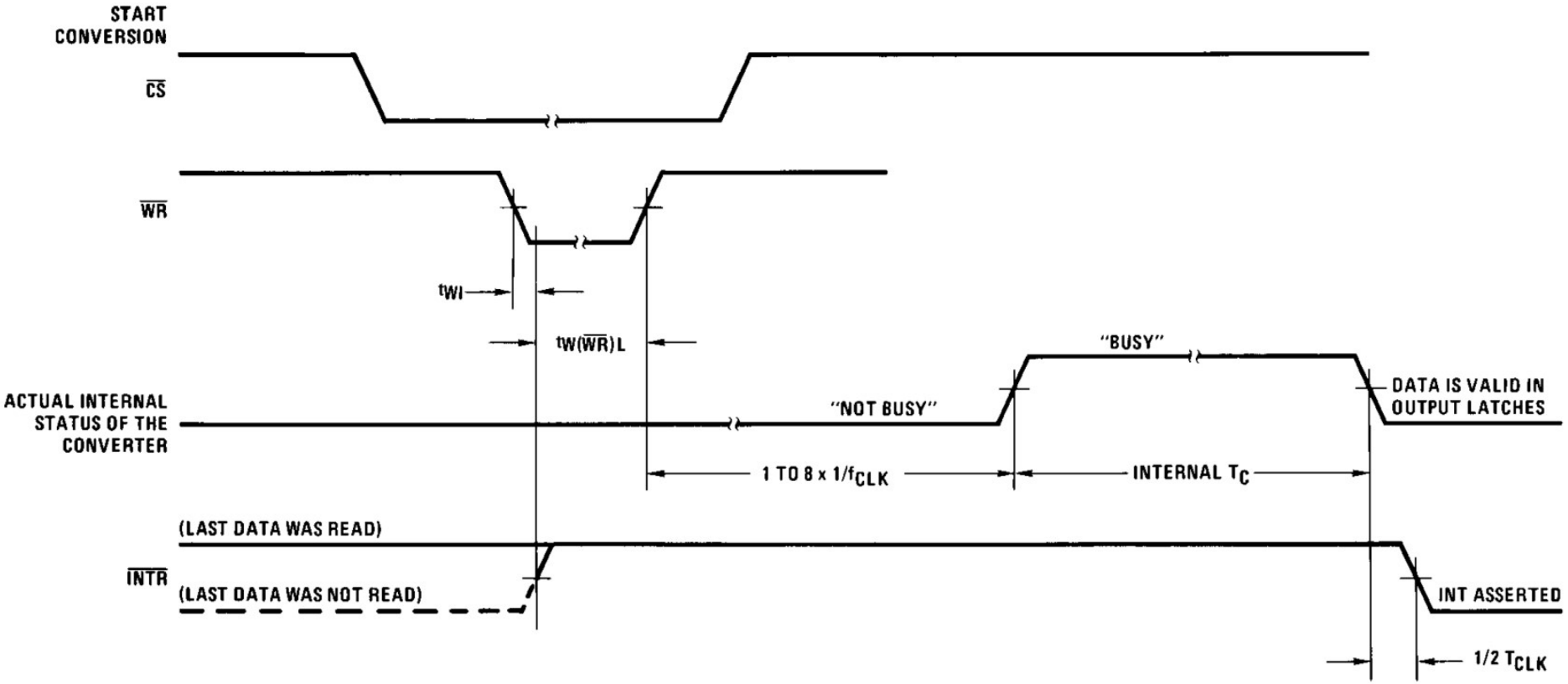
- Ramp converter



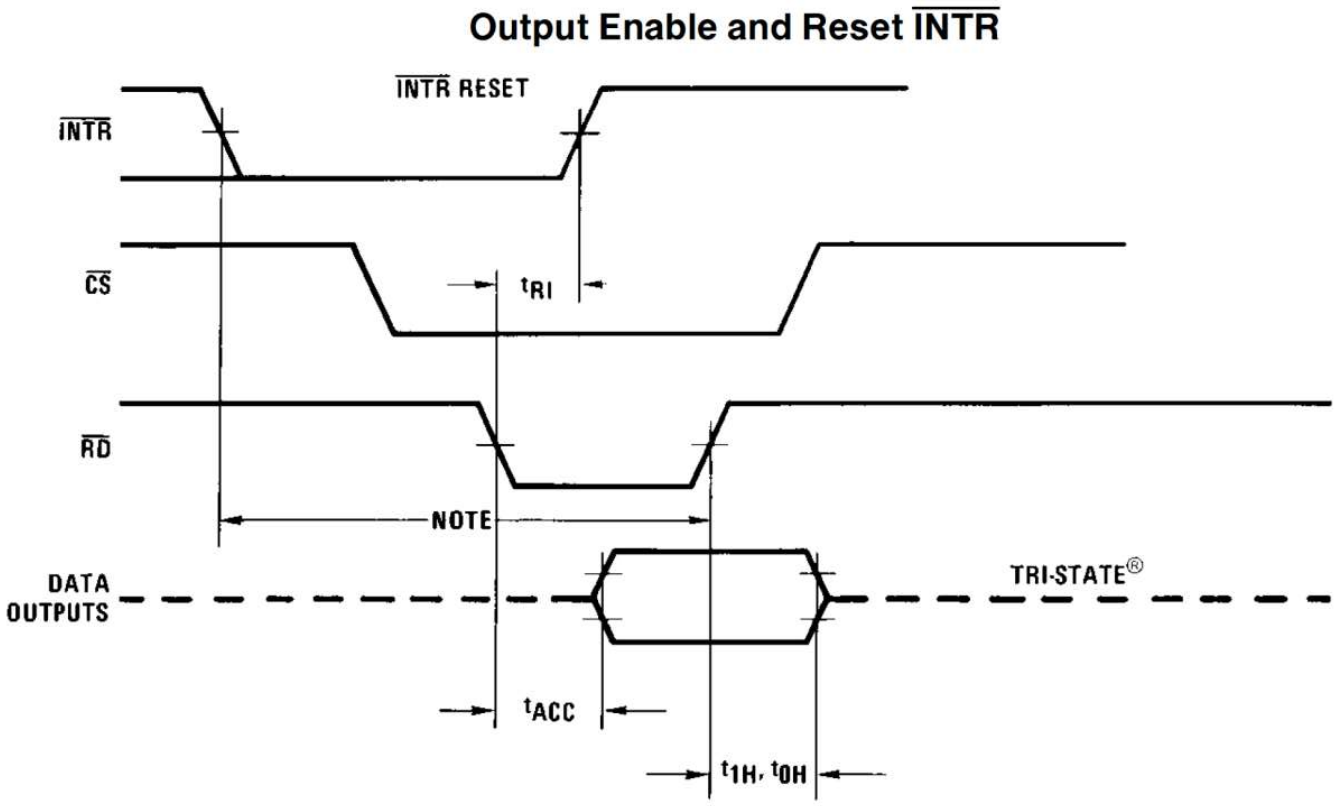
ADC0804


U111
IO1
RD
WR
U111(CLK IN)
1
2
3
4
5
8
10
9
19
6
7
CS
RD
WR
CLK IN
INTR
A GND
D GND
VREF/2
CLK R
VIN+
VIN-
ADC0804
VCC
DB0(LSB)
DB1
DB2
DB3
DB4
DB5
DB6
DB7(MSB)
20
18
17
16
15
14
13
12
11
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD[0..7]
RV1
12%
1k
U4:A
74125
2
3
1
IO2
AD7

ADC0804


START CONVERSION
CS
WR
tWI
tW(WR)L
"BUSY"
ACTUAL INTERNAL STATUS OF THE CONVERTER
"NOT BUSY"
DATA IS VALID IN OUTPUT LATCHES
1 TO 8 x 1/fCLK
INTERNAL TC
(LAST DATA WAS READ)
INTR
(LAST DATA WAS NOT READ)
INT ASSERTED
1/2 TCLK

ADC0804


Output Enable and Reset INTR
INTR RESET
INTR
CS
tRI
RD
NOTE
DATA OUTPUTS
TRI-STATE®
tACC
t1H, t0H

Örnek

```
TEKRAR:
MOV DX, 0200H
MOV AL, 00H
OUT DX, AL
MOV DX, 0400H
INTR_KONTROL:
IN AL, DX
TEST AL,  80H
JNZ INTR_KONTROL
MOV DX, 0200H
IN AL, DX
CALL DELAY
JMP TEKRAR
```