Yıldız Technical University
Computer Engineering
2023-2024 Spring
BLM2022 Computer Organization
Homework 2

Question 1)

Implement the single cycle RISC-V processor given as attachment that supports lw, sw, add, sub, slt, or, and, beq, addi, slti, ori, andi, jal instructions in Verilog. Create a testbench that checks the design for each instruction.

Question 2)

Using the design from Q1 as the base, extend the processor design to support sra instruction. Draw the block diagram and indicate any changes on control signals or building blocks. Then implement your design on Verilog. Create a testbench that checks the design for each instruction.

Note: Turn in your answers as [StudentNo].zip file structured as follows with a maximum of 3-minute video explaining your design and testbench results.