Mikroişlemci Sistemleri

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5

YTÜ-CE
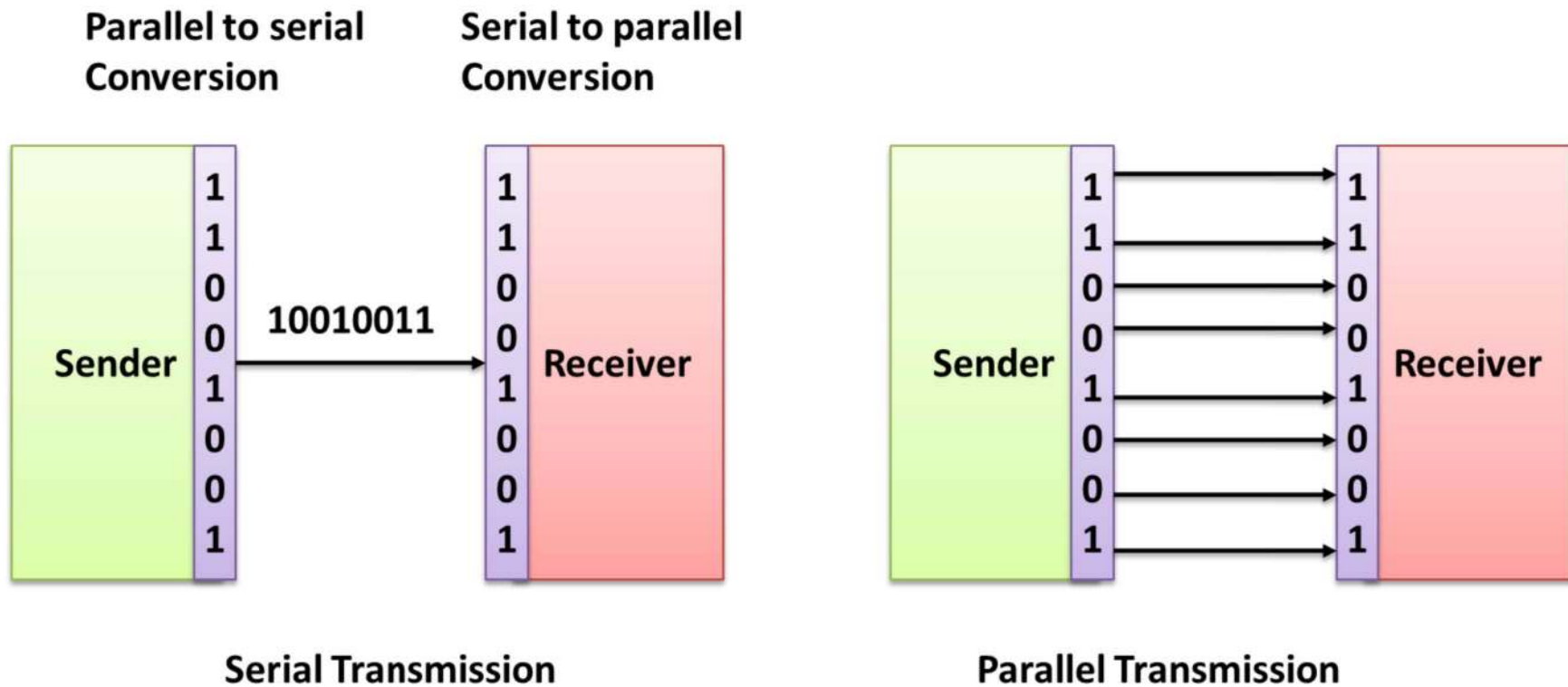
Ders-5 Konular

- Paralel Seri Haberleşme
- Seri Haberleşme
  - Synchronous/Asynchronous
  - Simplex/Duplex
  - Baud Rate
  - Error Correction
- Yazılımsal Seri Haberleşme
  - Transmit
  - Receive
- 8251 USART
  - 8251 Blok Diyagram
  - Yazmaçlar
  - Mode Word / Command Word
  - Status Word

Veri İletişimi: Seri-Paralel

- Seri
  - Daha az maliyet
  - Daha yavaş
- Paralel
  - Daha hızlı
  - Kısa mesafeler için

Veri İletişimi: Seri-Paralel

Parallel to serial Conversion

Serial to parallel Conversion
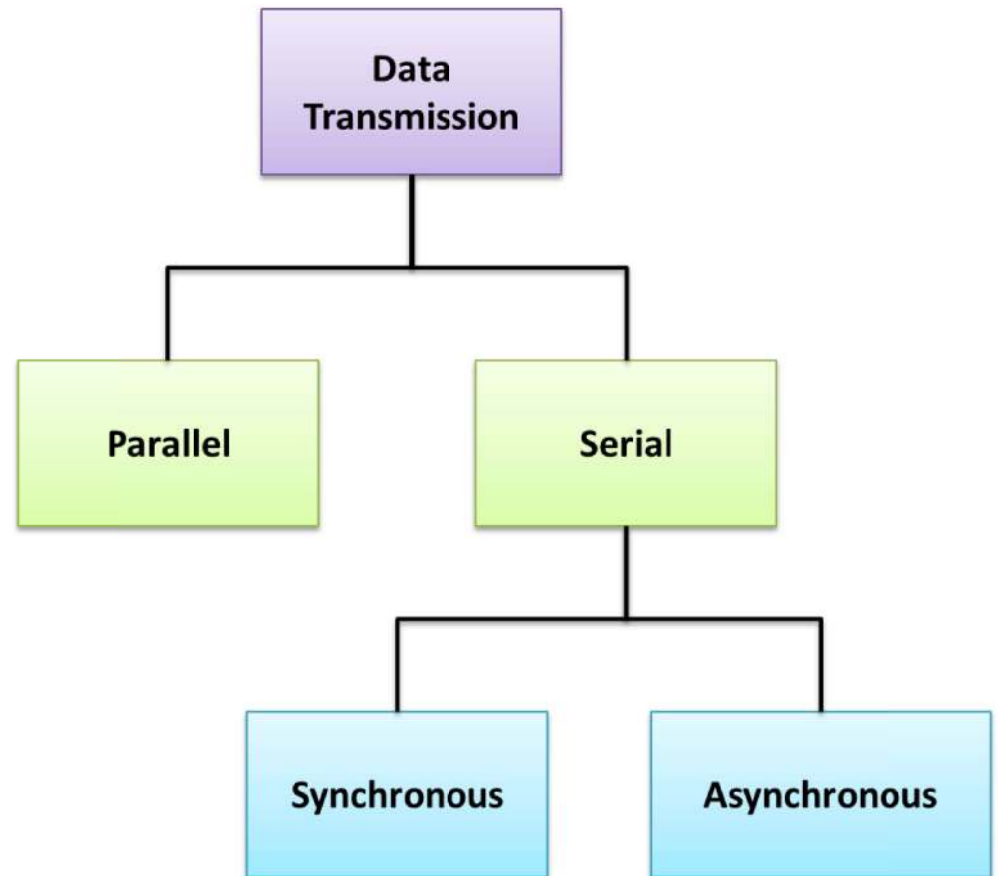
Serial Transmission

Parallel Transmission
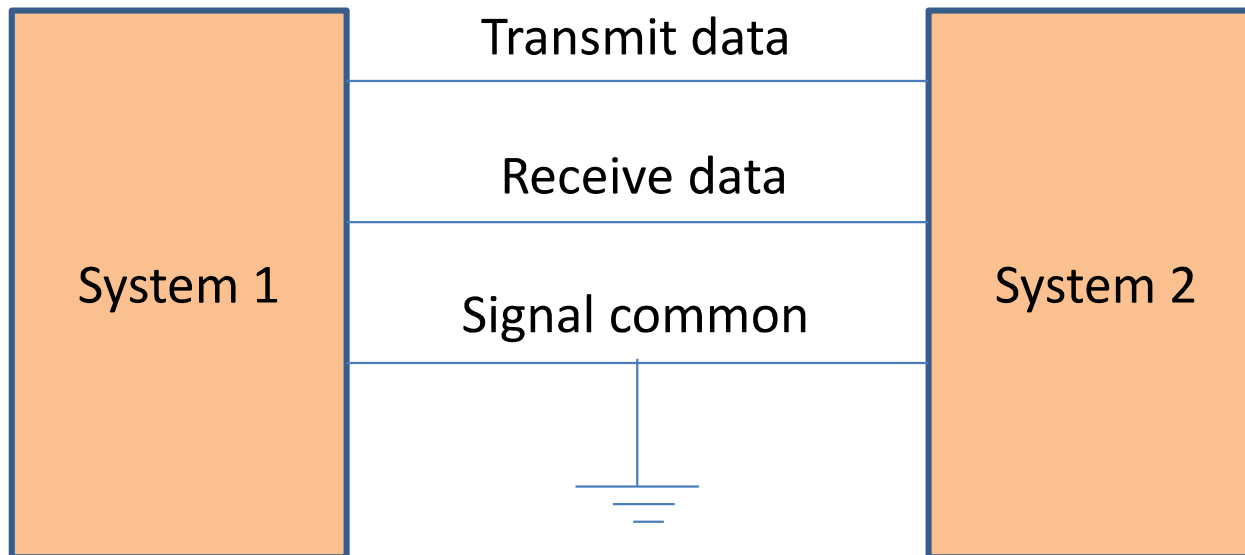
Seri İletişim

- Synchronous (Senkron)
  - Sender and receiver must synchronize
    - Done in hardware using phase locked loops (PLLs)
  - Block of data can be sent
  - More efficient : Less overhead than asynchronous transmission
  - Expensive
- Asynchronous (Asenkron)
  - Each byte is encoded for transmission
    - Start and stop bits
  - No need for sender and receiver synchronization

Seri İletişim

Transmission Gaps

Sender a Data Data Data Receiver

Asynchronous transmission

CLK

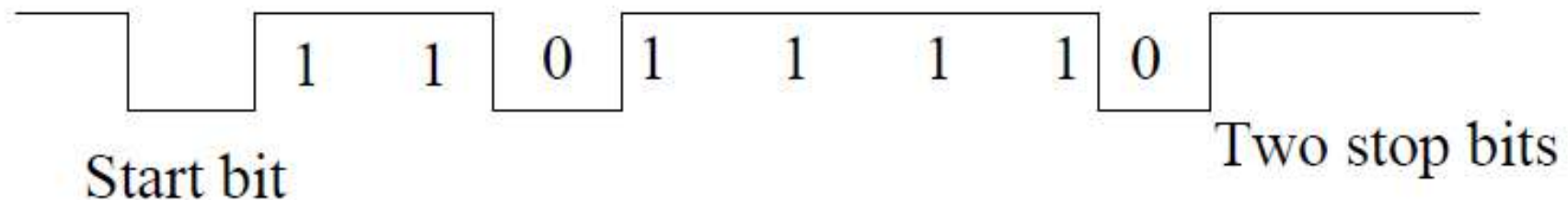Sender Data Data Data Data Data Receiver

Synchronous transmission
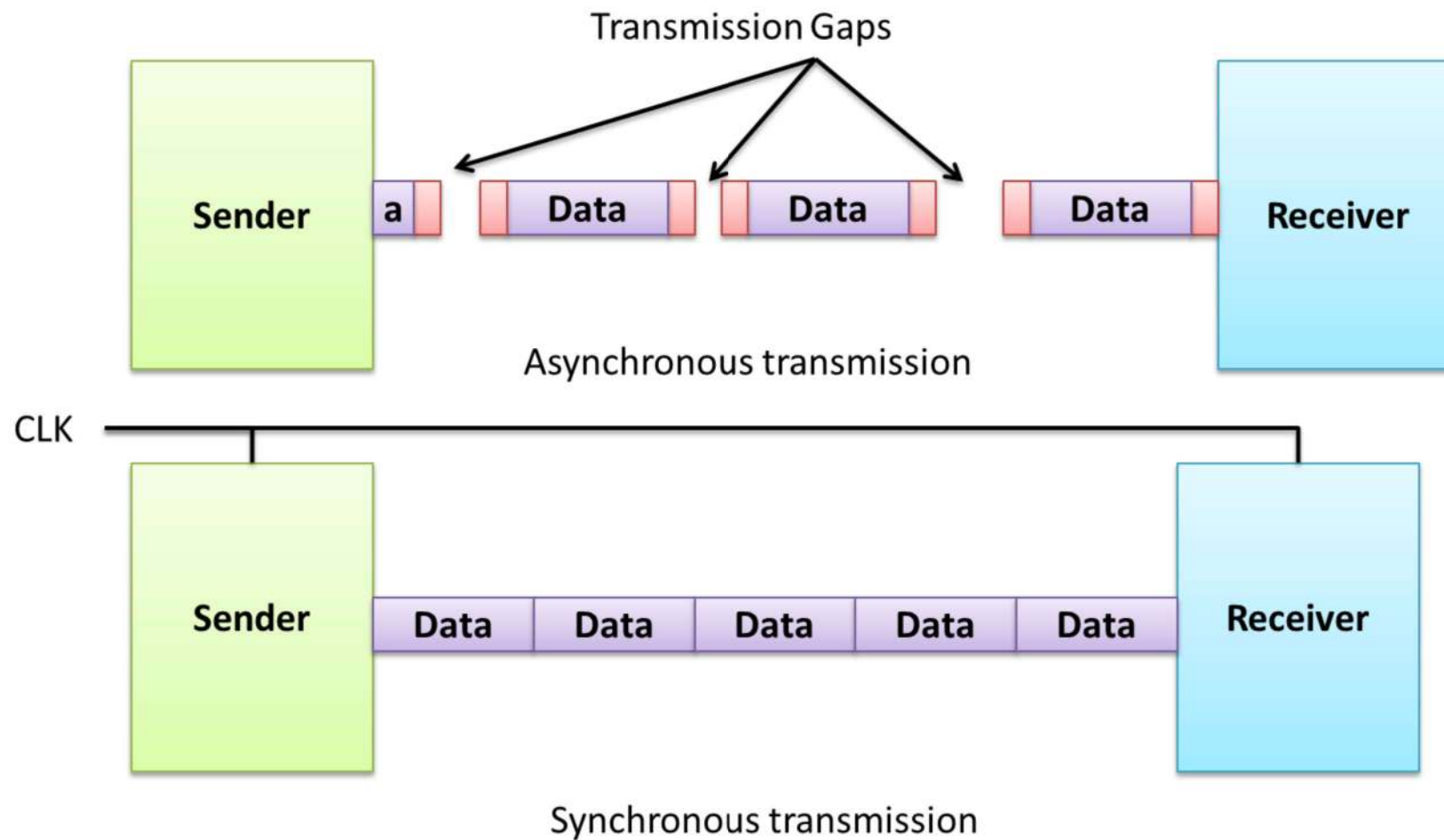
Asynchronous Comm.

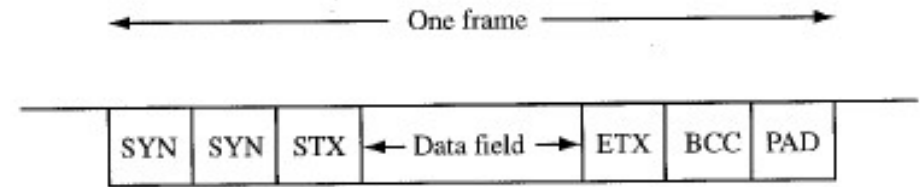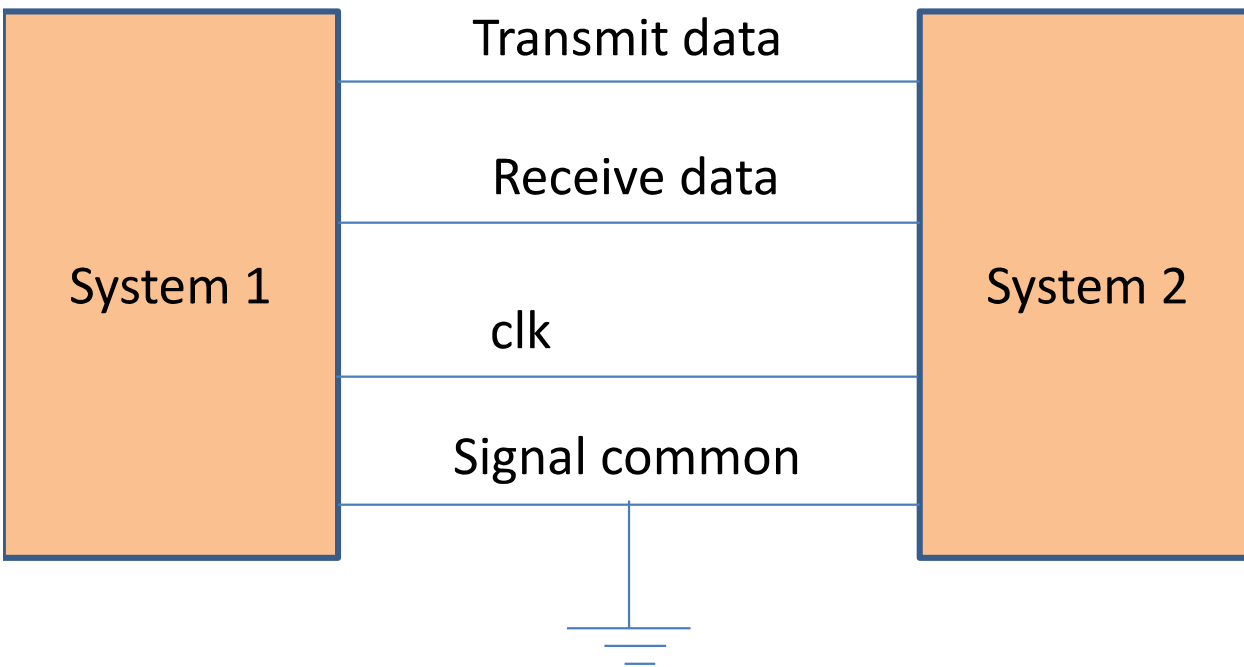- Ortak bir CLK veya senkron işaretine ihtiyaç duymaz
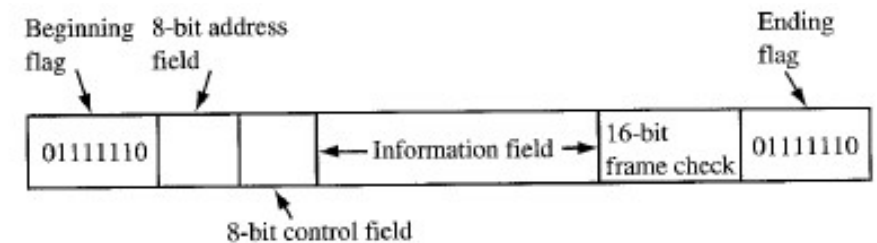
Asynchronous Comm.

- Veri bitler halinde gönderilir.
- Alıcı taraf iletişimin başladığını/bittiğini başta ve sonda bulunan START ve STOP bitleri ile anlar.
- Hat boşta iken lojik 1 değerindedir.

Synchronous Comm.

System 1 — System 2

Transmit data

Receive data

clk

Signal common

One frame

| SYN | SYN | STX | ← Data field → | ETX | BCC | PAD |

BISYNC: Each block of data has synch characters. The size of block data can be 100 or more bytes. BCC checks for errors.

Beginning flag | 8-bit address field | | Information field → | 16-bit frame check | Ending flag

| 01111110 | | | ← Information field → | 16-bit frame check | 01111110 |

8-bit control field

Serial Data Link Control: Developed by IBM used for computer networking (Token Ring). After Flag byte the network address is sent. Control Byte stores information about sequence of data etc. Data is thousands of bits. 16 bit field is used for error checking.

Simplex/Duplex

- Simplex
  - Data are transmitted in one directions
  - Example: CPU to printer

- Duplex
  - Data flow in both direction
  - Half Duplex (Transmission goes on way at a time)
  - Full Duplex (Both ways simultaneously)

Simplex/Duplex
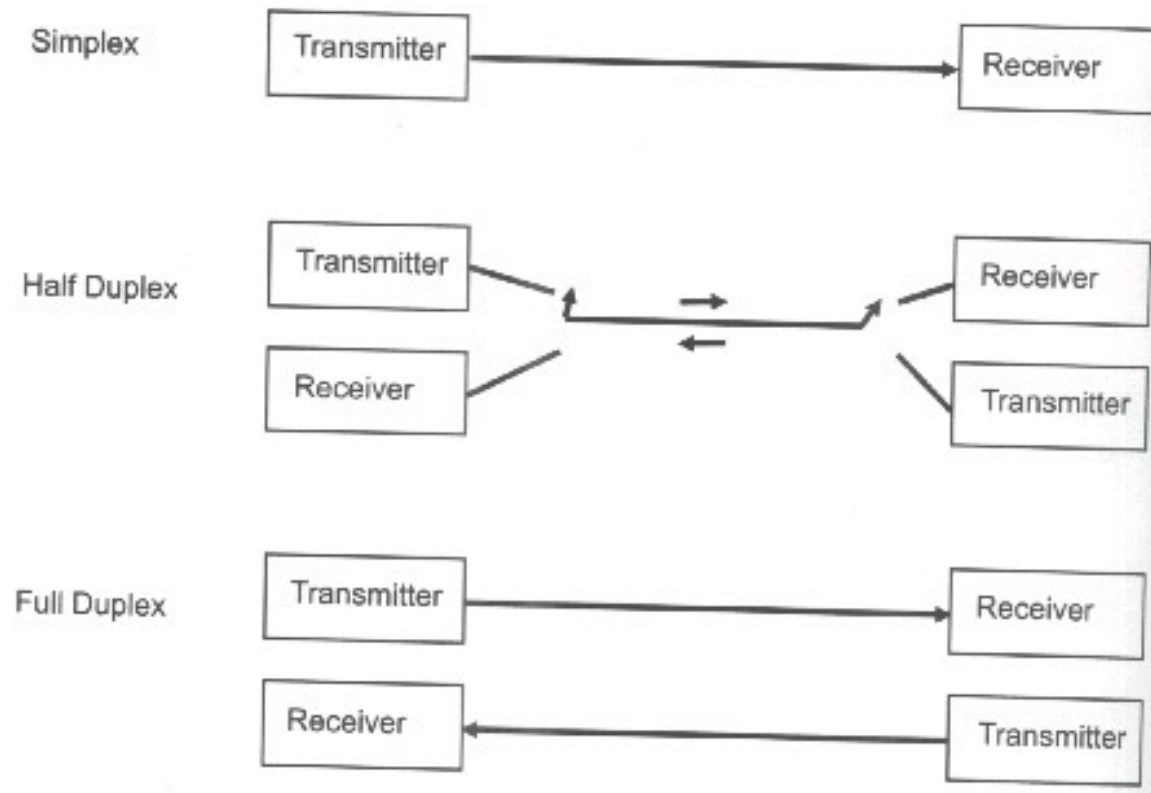
Transmission Rate

- Rate at which bits are transmitted (BAUD)
- Number of signal changes per second
- Bit time: how long the Bit stay On or Off
- Printer, Terminal Baud Adjustable (50-9600)
- 1200Baud means: Bit stay for 1/1200=0.83ms

Örnek

- What is the data rate in bits/sec and character rate if the bit time is 3.33 ms (1 start, 8 data, 2 stop)
  - Bit rate = 1 / 3.33 ms = 300 bits/sec
  - 11 x 3.33 ms = 36.63 ms required to transmit a character so character rate = 1/36.63 ms = 27.3 char/sec
- Modems typically transmit data over the telephone network at 9600, 14400, 28800 or 56K bps.
- If 1 MByte file is to be transmitted to another computer using a modem calculate the transmission time (1 start, 7 data, 1 parity, 1 stop)
  - 9600 bps: 1048576x10/ 9600 bits/sec = 1092 s = 18 minutes and 12 sec
  - 28800 bps: 364 s = 6 minutes and 4 sec

Error Check

- Parity Check
  - Even parity: When odd numbers of 1 make D7=1
    - Send Even number of 1
  - Odd parity: When even number of 1 make D7=1
    - Send Odd number of 1
- Check Sum
  - Used for block of data
  - Sum of all Bytes without carry and 2's complements
  - Total Sum Result should be Zero
- Cyclic Redundancy Code (CRC)
  - Synchronous Communication
  - Stream of Data can be represented by Cyclic polynomial that divided by a **constant polynomial**
  - Reminder to set **Bits** and Send out as check for error

Yazılımsal Seri İletişim - Transmit
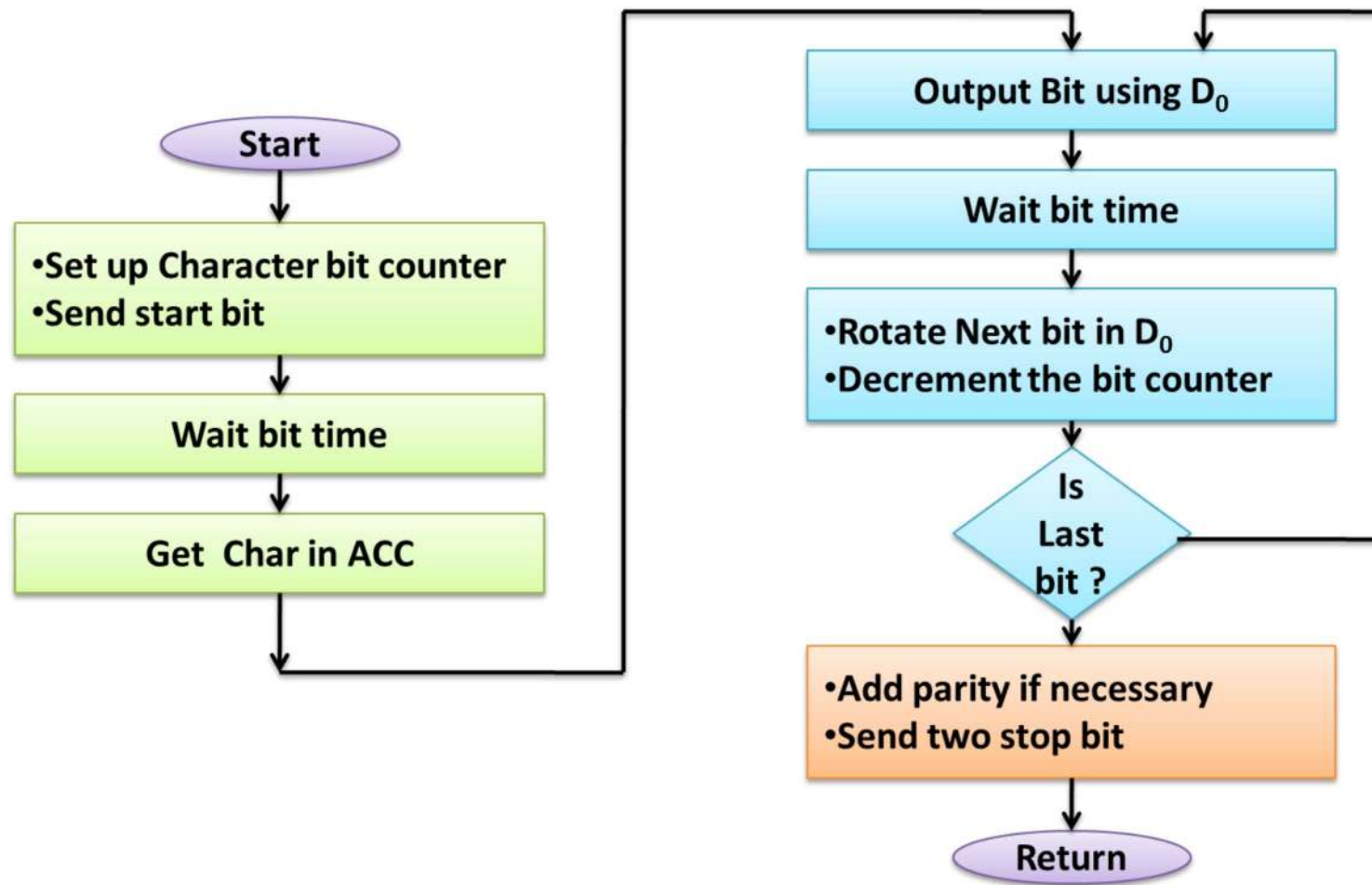
Yazılımsal Seri İletişim - Transmit

```
;Function:   Serial data transmitter.  DELAY
;            procedure determines data rate.
;Inputs:     Character to be transmitted assumed
;            passed in AL.
;Ouputs:     Serial data on bit 0 of DPORT.

;Destroys:   AL,CX,flags.

            EXTRN       DELAY:NEAR
            DPORT       EQU  00H

CODE        SEGMENT
            ASSUME      CS:CODE

FIG10_3     PROC        NEAR
            MOV         CX,10       ;10 bits/char
            CLC                     ;Start bit
            RCL         AL,1        ;Move to position 0
TRANS:      OUT         DPORT,AL    ;Transmit bit
            CALL        DELAY       ;Wait
            RCR         AL,1        ;Next bit
            STC                     ;Stop bit
            LOOP        TRANS       ;Do 10 times
            RET
FIG10_3     ENDP
            CODE        ENDS
            END
```
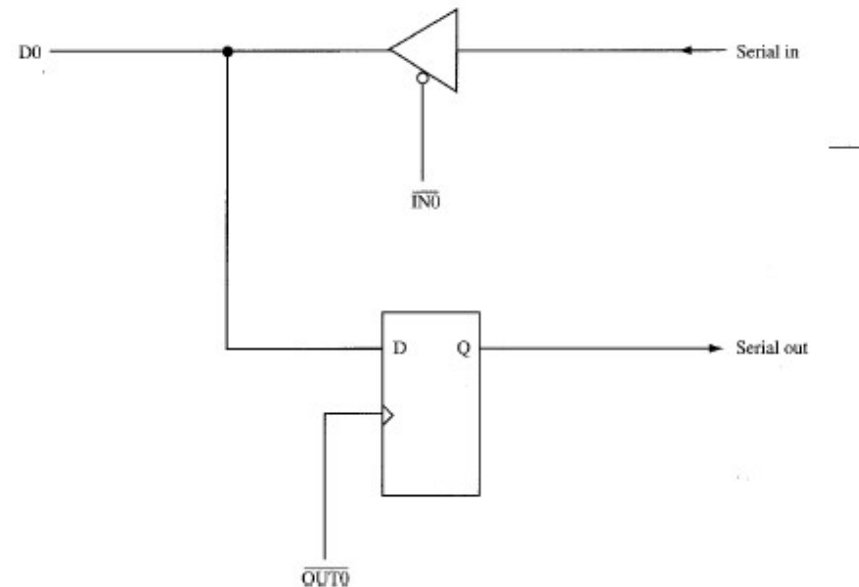
Yazılımsal Seri İletişim - Receive
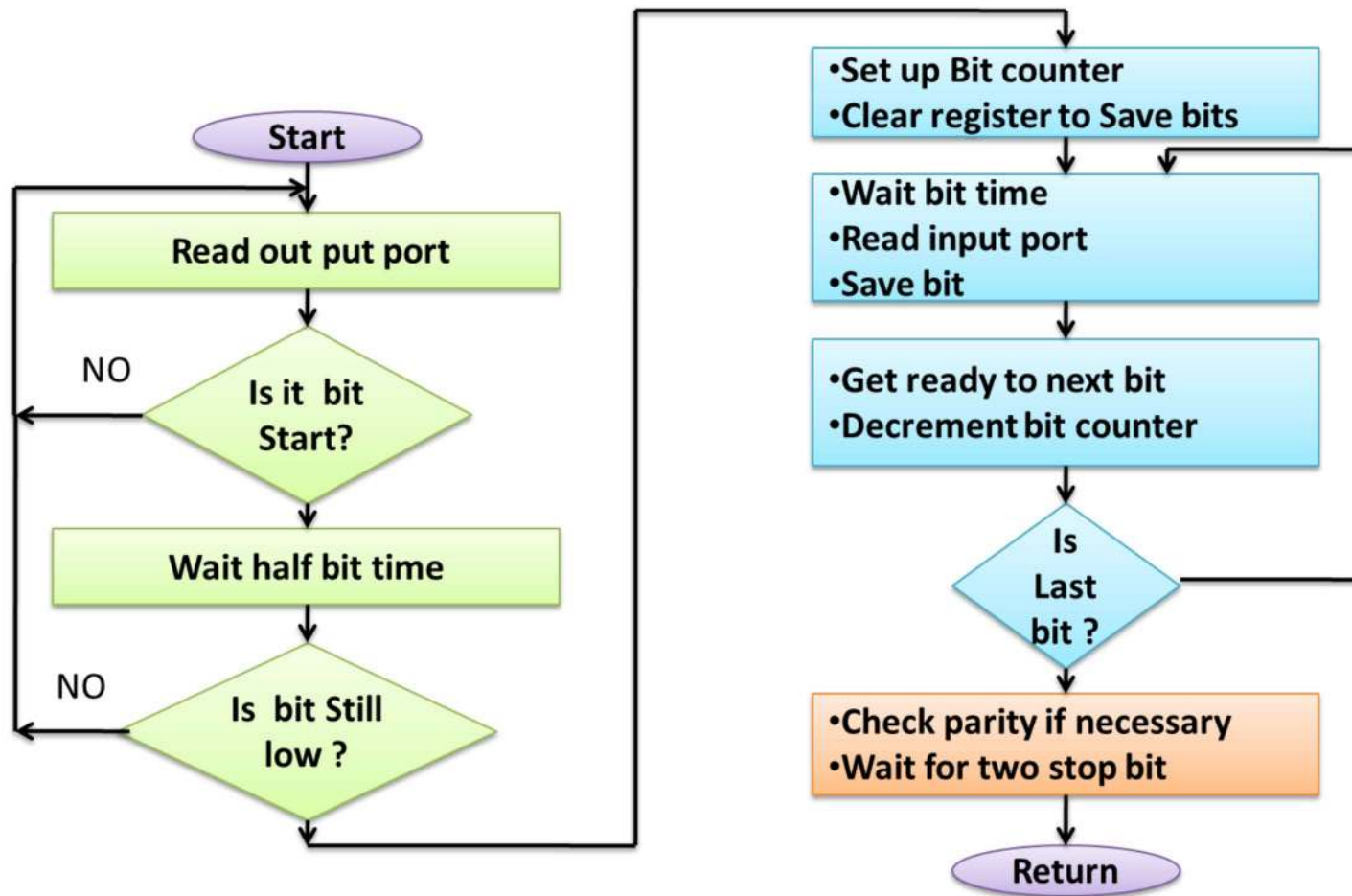
8251 USART

- USART: universal Synchronous/Asynchronous Receiver/Transmitter

8251

8251A

Provides internal timing; frequency must be at least 30 times the data bit rate of the receiver or transmitter → CLK

Mode register

Sync character 1

Sync character 2

Control register

V_cc ← +5 V

GND

Receiver shift reg. ← Serial input
RxD

Primarily needed when interface is on a separate PC board

8286 (optional) ⟷ D7-D0

OE
T

Data-in buffer reg.
Data-out buffer reg.

TxE → Indicates trans. empty

Reset → RESET

IRn → RxRDY

IR(n + 1) → TxRDY

RD → RD

WR → WR

Transmitter shift reg. — TxD → Serial output

DSR
DTR
CTS
RTS
SYNDET

Modem control

Status register

Ready
Delay*

IO/M → Address decoder → CS

RxC
TxC

Clock

A0 → C/D

Address bus

Data bus

Control bus

8251 Yazmaçlar

$\overline{CS}$	$C/\overline{D}$	$\overline{RD}$	$\overline{WR}$	Anlam
1	X	X	X	Data-bus tristate
0	X	1	1	Data-bus tristate
0	1	0	1	Status → CPU
0	1	1	0	Mode, Control, Sync← CPU
0	0	0	1	Data → CPU
0	0	1	0	Data ← CPU

8251 İlk Ayarlama

Mod Yazmacı

Parity type:
0 — Odd
1 — Even

Number of data bits:
00 — 5
01 — 6
10 — 7
11 — 8

| S2 | S1 | EP | PEN | L2 | L1 | B2 | B1 |

Number of stop bits:
00 — Invalid
01 — 1
10 — $1\frac{1}{2}$
11 — 2

Parity enable:
0 — No parity bit
1 — Parity bit present

Baud rate factor:
00 — Synchronous mode
01 — Factor = 1
10 — Factor = 16
11 — Factor = 64

(a) Asynchronous mode

External synchronous detect:
0 — SYNDET is output
1 — SYNDET is input

Parity enable:
0 — No parity bit
1 — Parity bit present

| SCS | ESD | EP | PEN | L2 | L1 | 0 | 0 |

Number of sync characters:
0 — 2 characters
1 — 1 character

Parity type:
0 — Odd
1 — Even

Number of data bits:
00 — 5
01 — 6
10 — 7
11 — 8

When 00 these bits
indicate synchronous
mode

(b) Synchronous mode

Kontrol Yazmacı

Causes $\overline{RTS}$ output to be active

Enter hunt mode

Receiver is enabled

Transmitter is enabled

EH	IR	RTS	ER	SBRK	RxE	DTR	TxEN

Indicates internal reset

Causes all three error bits in status to be cleared

Causes break by forcing TxD low

Forces $\overline{DTR}$ output low
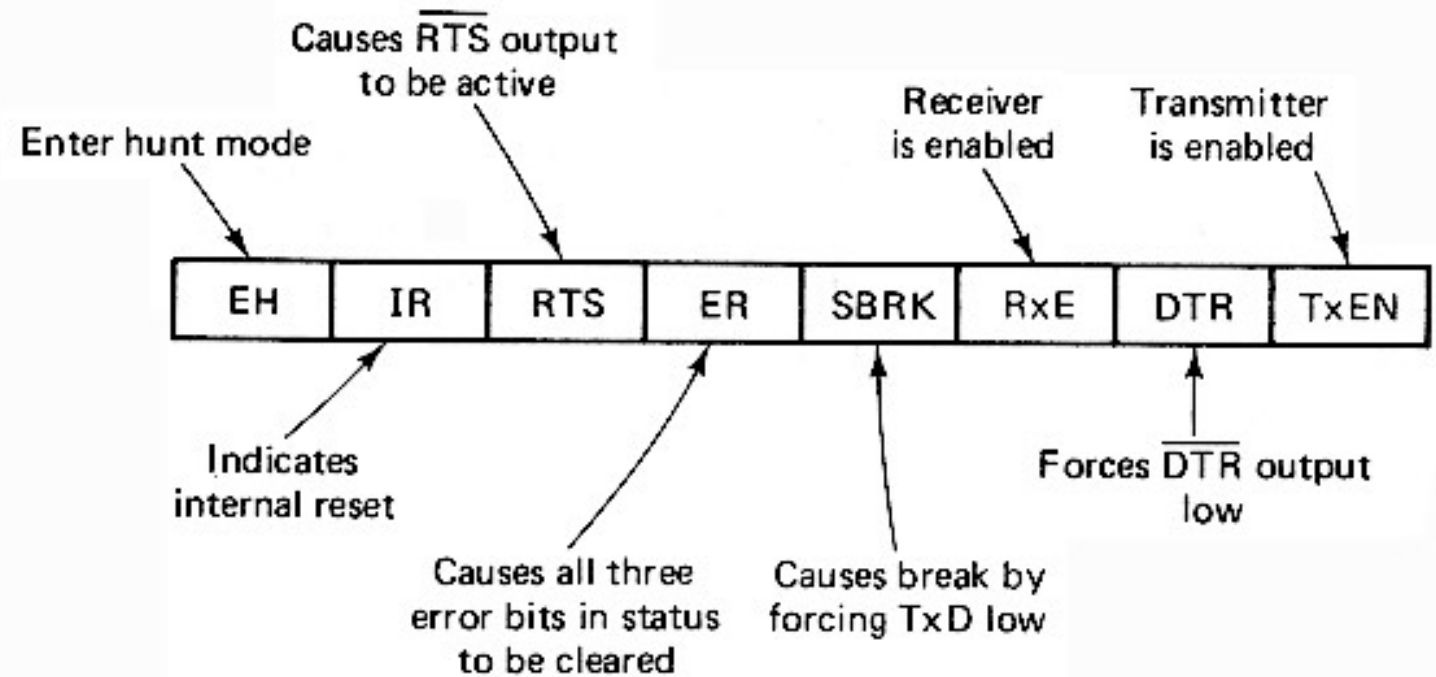
Note: In all cases action is taken when the bit is set to 1.

Durum Yazmacı

When 1 it indicates
$\overline{DSR}$ pin is active

Indicates data-out buffer register
empty; unlike the TxRDY
pin, this bit is not affected
by $\overline{CTS}$ pin and TxEN
control bit

| DSR | SYNDET | FE | OE | PE | TxE | RxRDY | TxRDY |

Same as
SYNDET pin

Same as RxRDY pin

Same as TxE pin

When 1 it indicates
the occurrence of a:

Framing error

Overrun error

Parity error