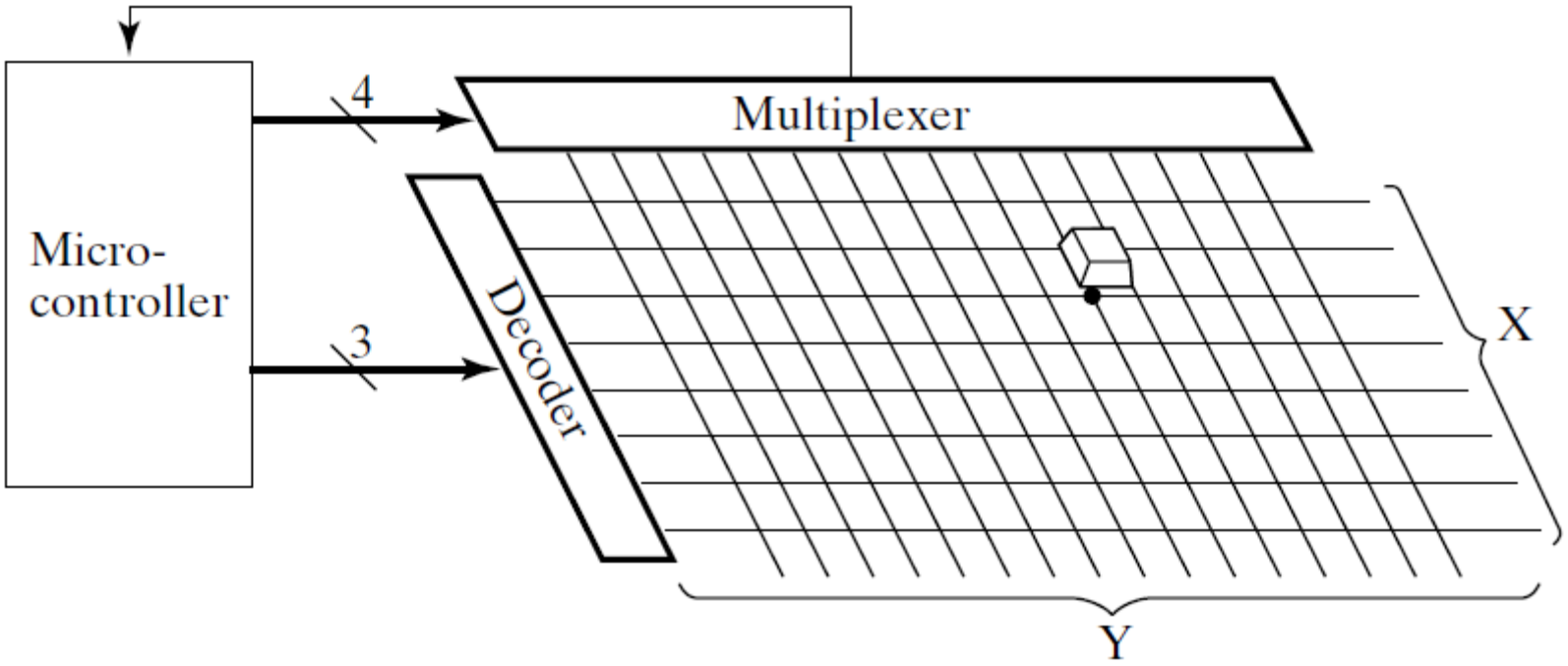
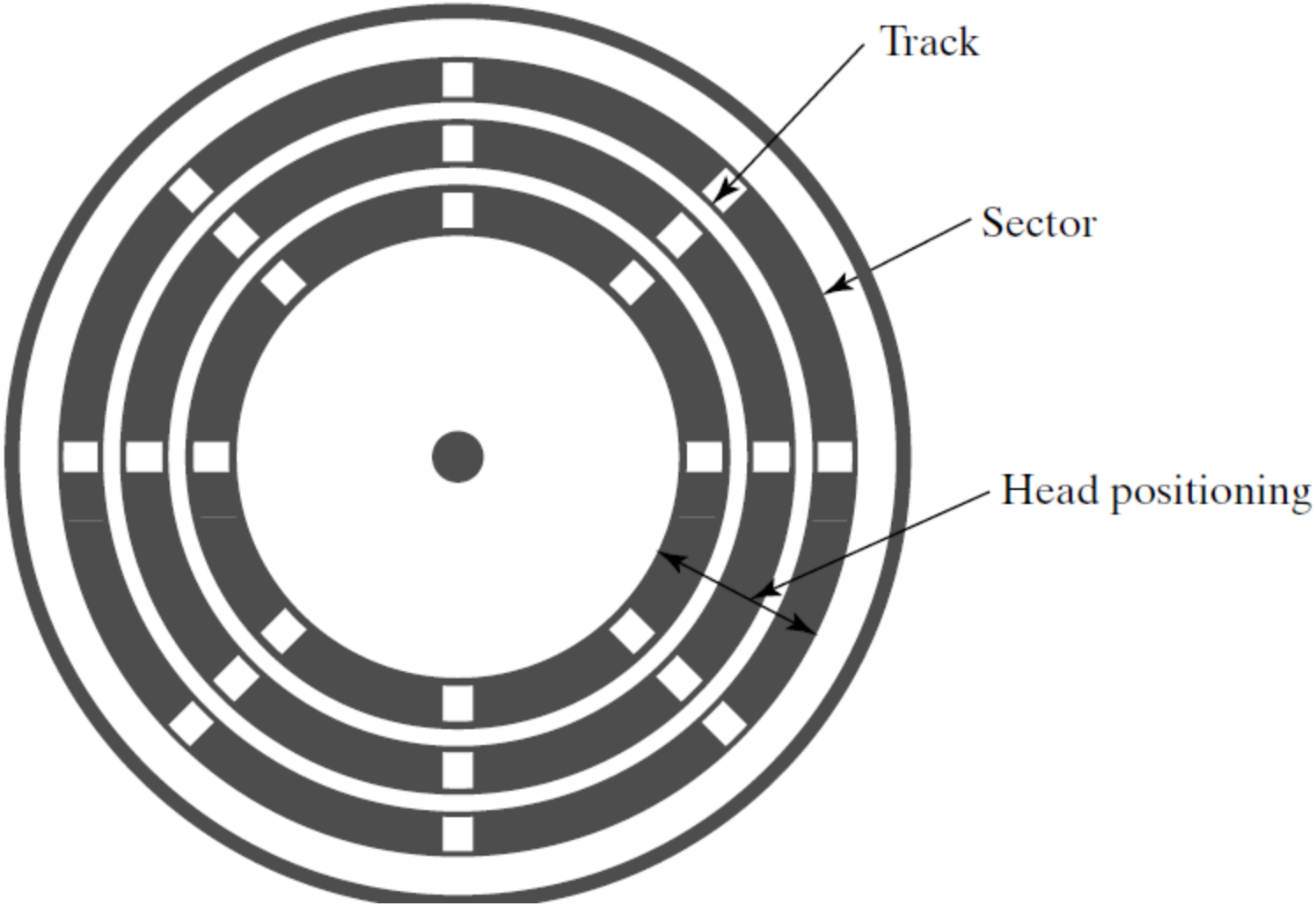
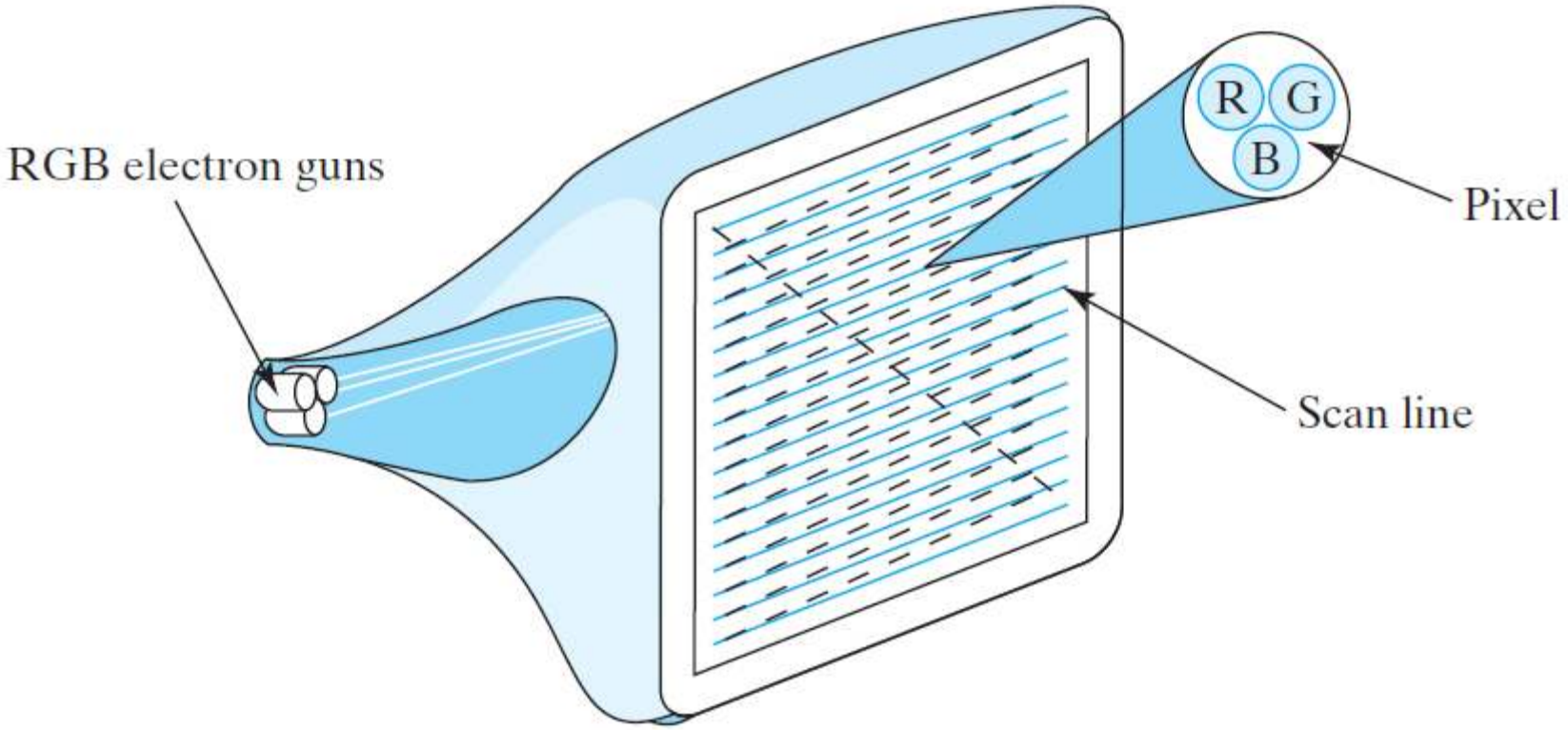
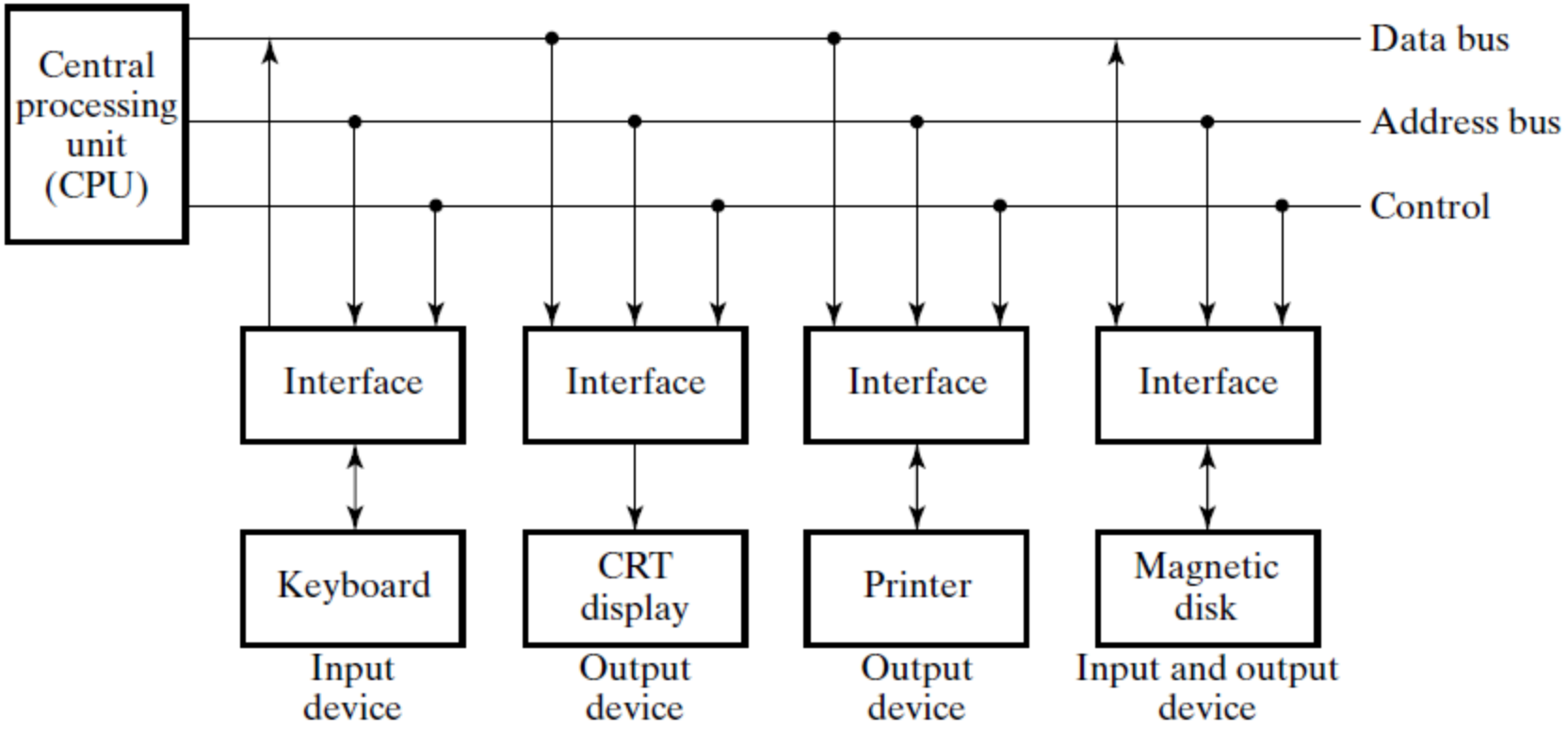
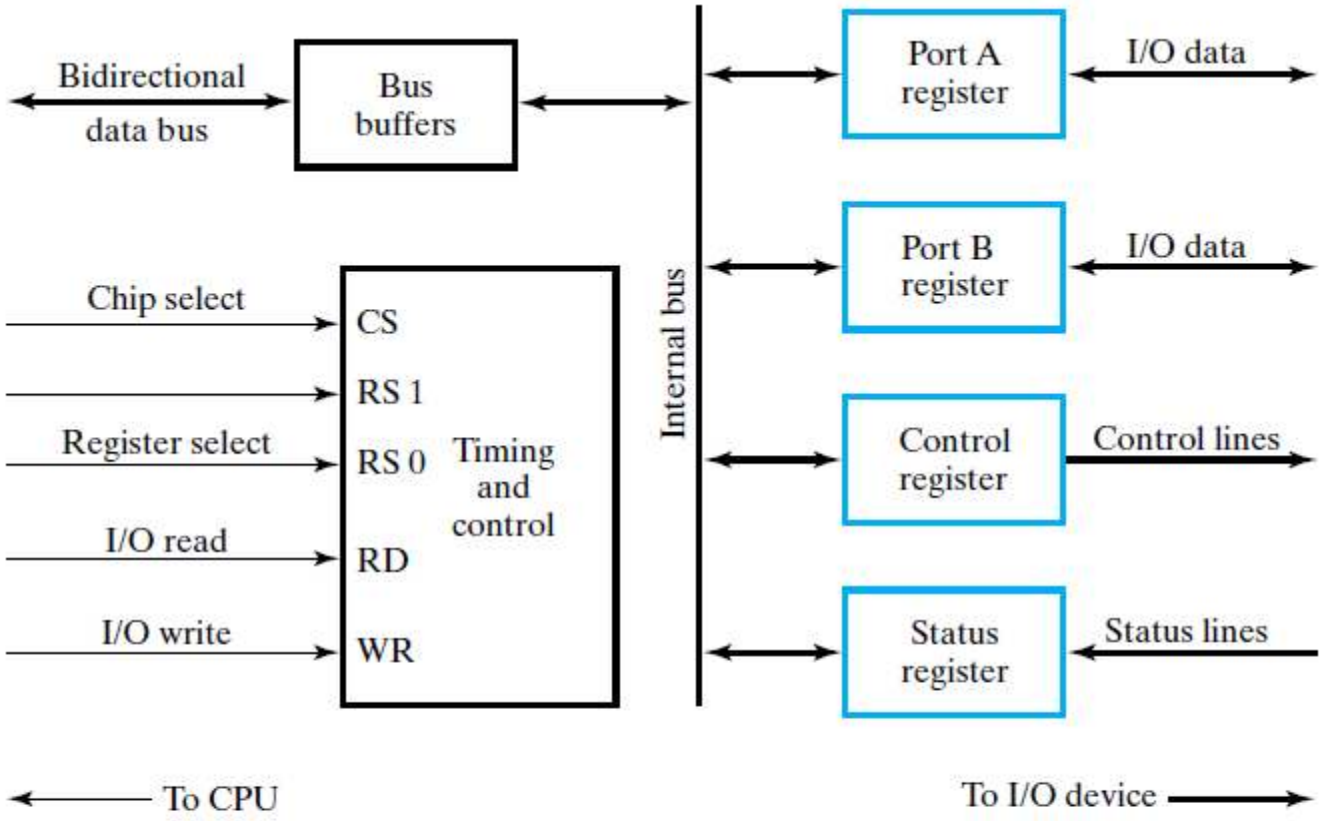
# Input- Output


Micro-
controller
4
3
Multiplexer
Decoder
X
Y

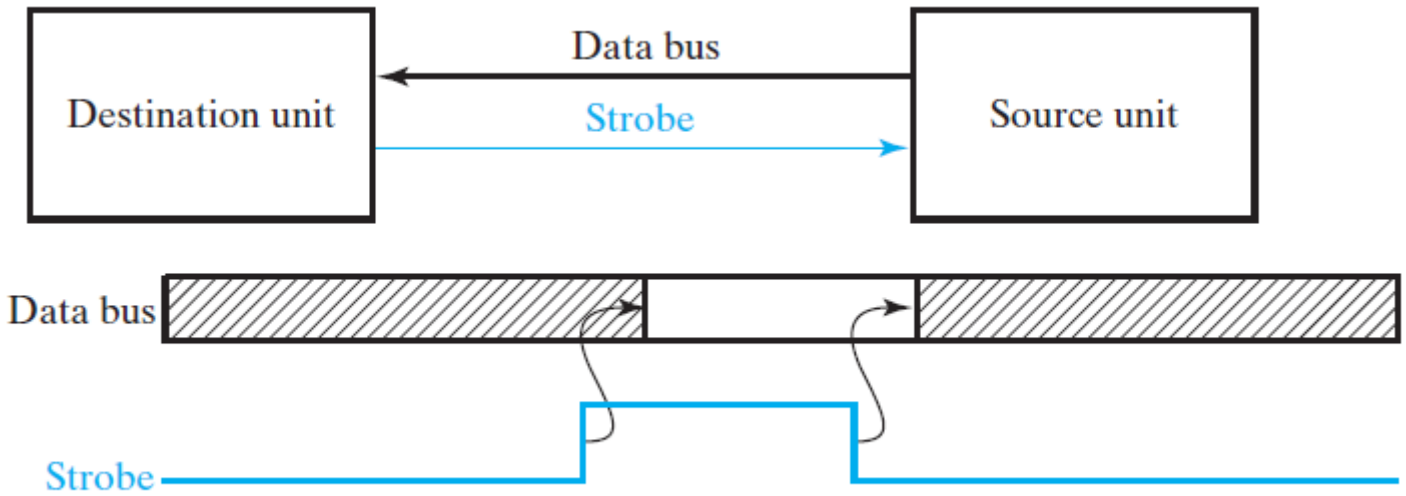

Track
Sector
Head positioning


RGB electron guns
R
G
B
Pixel
Scan line

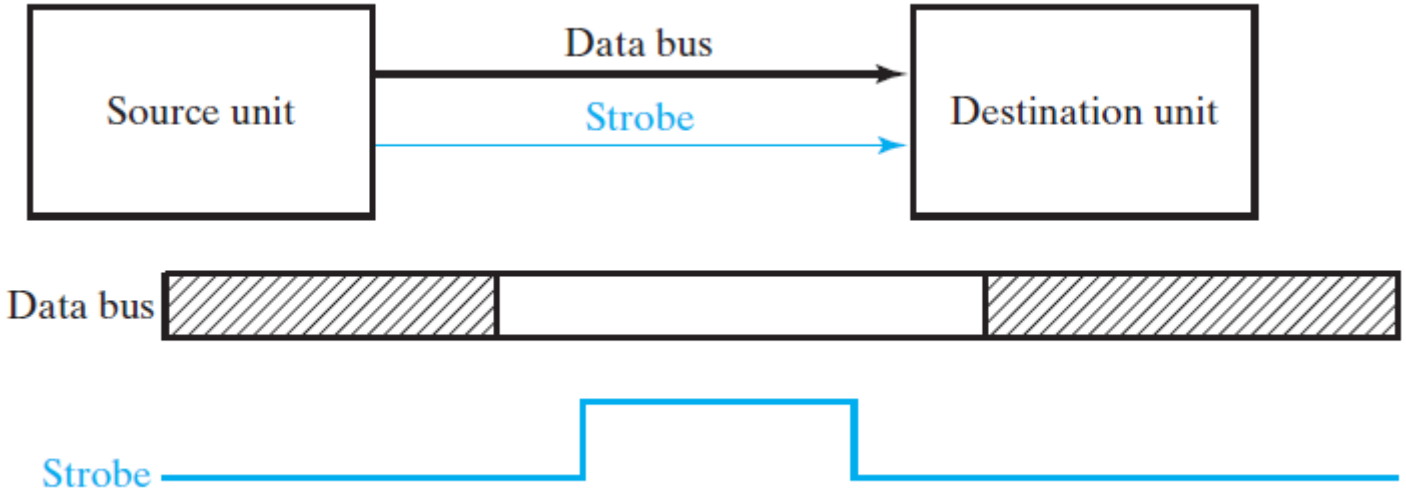

Central processing unit (CPU)
Data bus
Address bus
Control
Interface
Interface
Interface
Interface
Keyboard
CRT display
Printer
Magnetic disk
Input device
Output device
Output device
Input and output device




| CS | RS1 | RS0 | Register selected |
|---|---|---|---|
| 0 | x | x | None: data bus in high-impedance state |
| 1 | 0 | 0 | Port A register |
| 1 | 0 | 1 | Port B register |
| 1 | 1 | 0 | Control register |
| 1 | 1 | 1 | Status register |




(a) Destination-initiated transfer




(b) Source-initiated transfer

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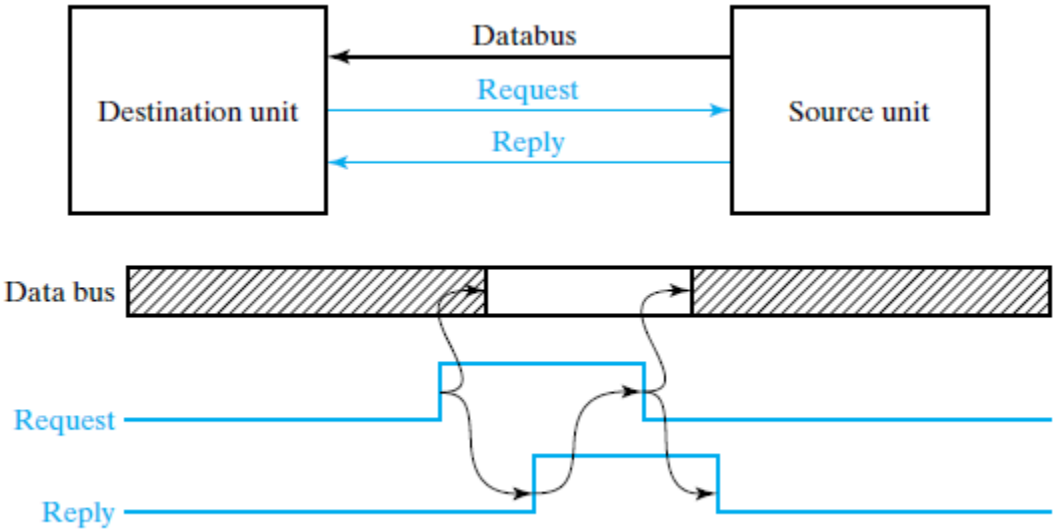
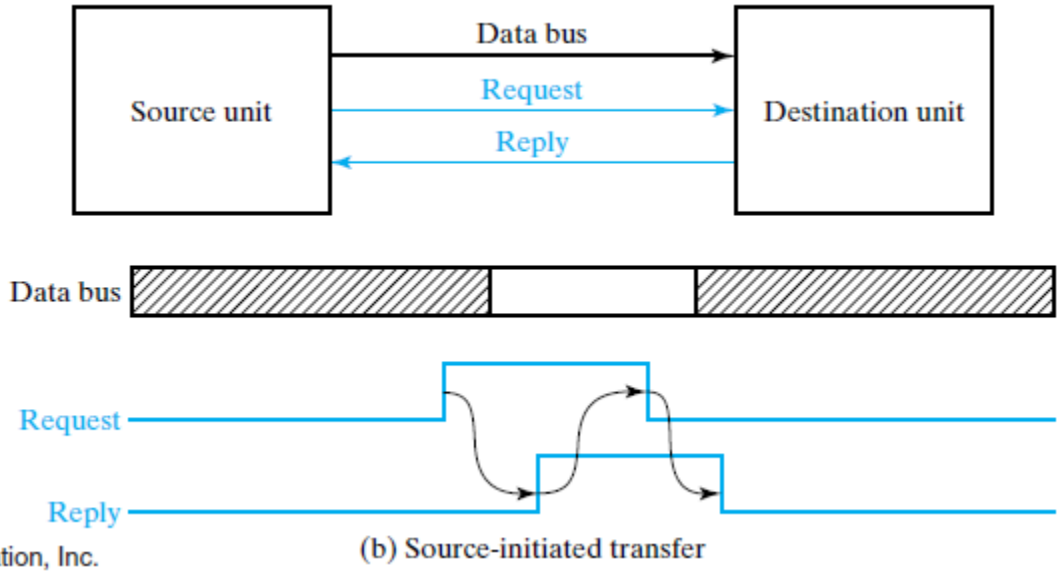



(a) Destination-initiated transfer




(b) Source-initiated transfer

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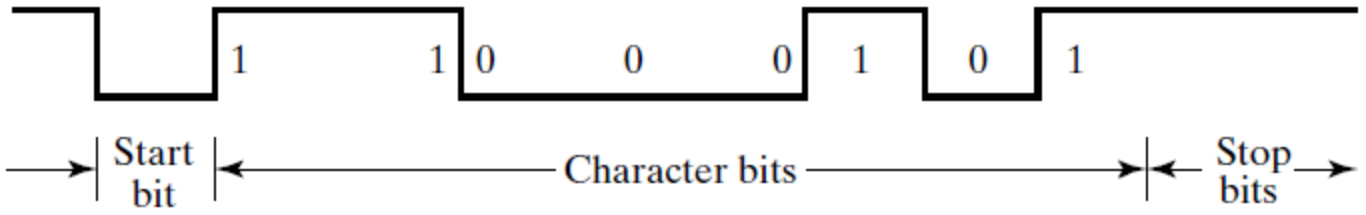
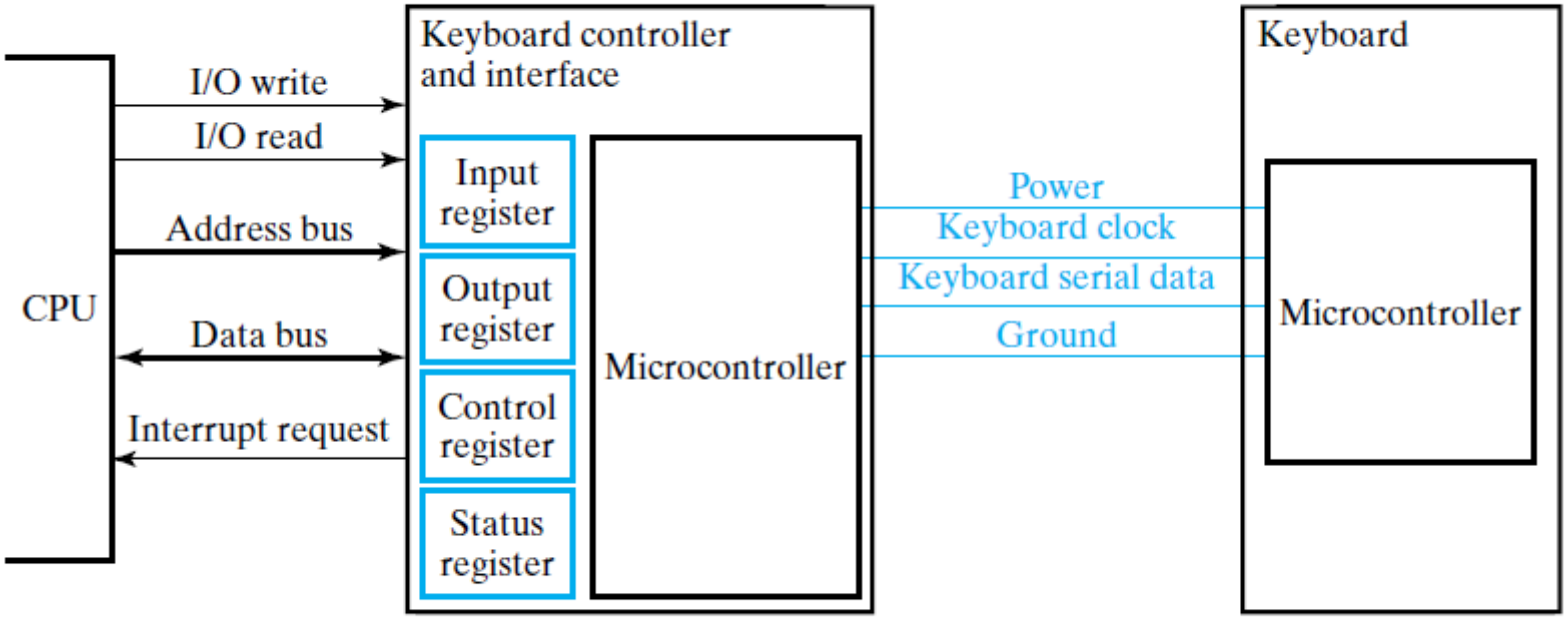
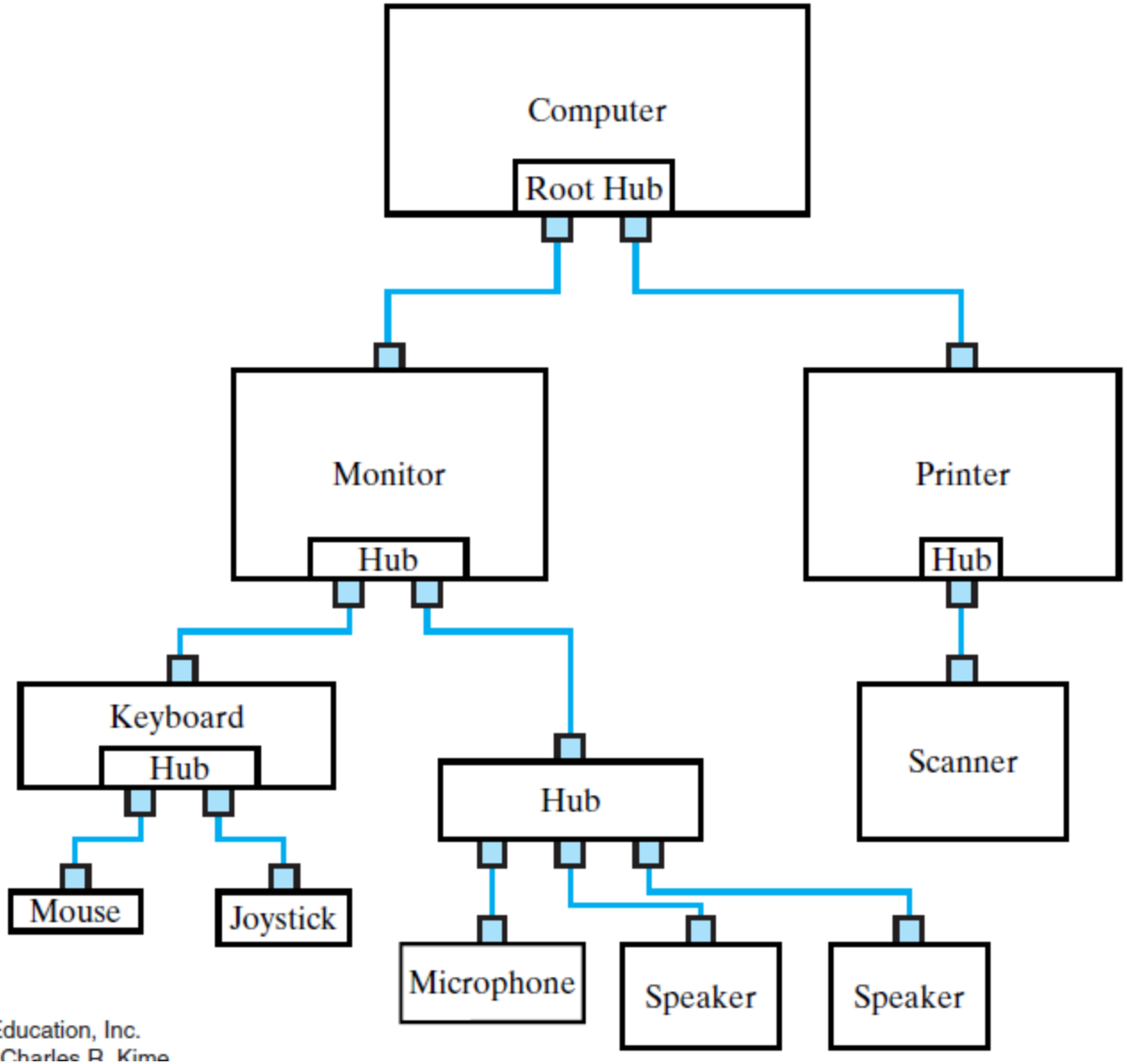

1
1
0
0
0
1
0
1
Start bit
Character bits
Stop bits


CPU
I/O write
I/O read
Address bus
Data bus
Interrupt request
Keyboard controller and interface
Input register
Output register
Control register
Status register
Microcontroller
Power
Keyboard clock
Keyboard serial data
Ground
Keyboard
Microcontroller

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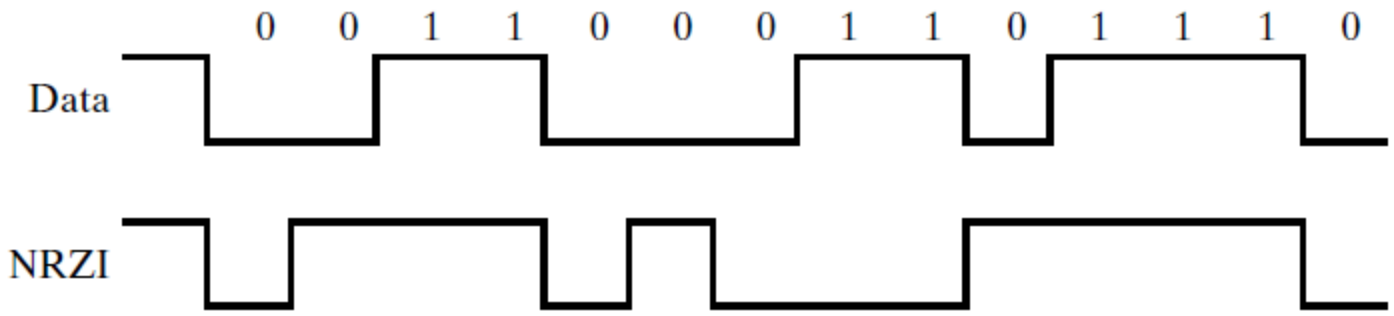
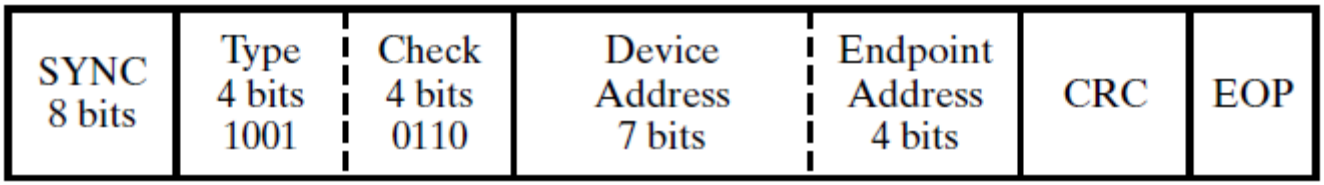
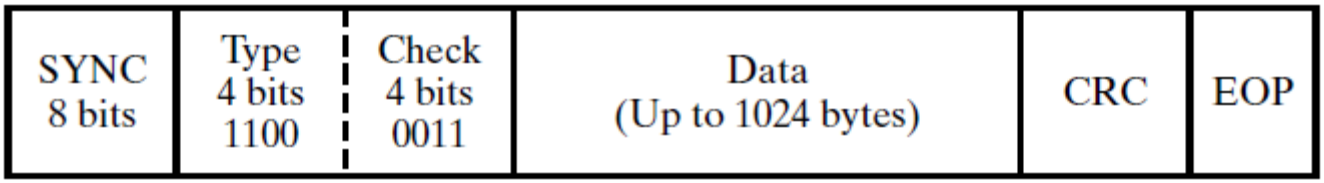

0 0 1 1 0 0 0 1 1 0 1 1 1 0
Data
NRZI

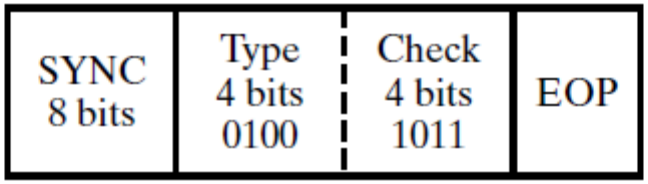
(a) General packet format



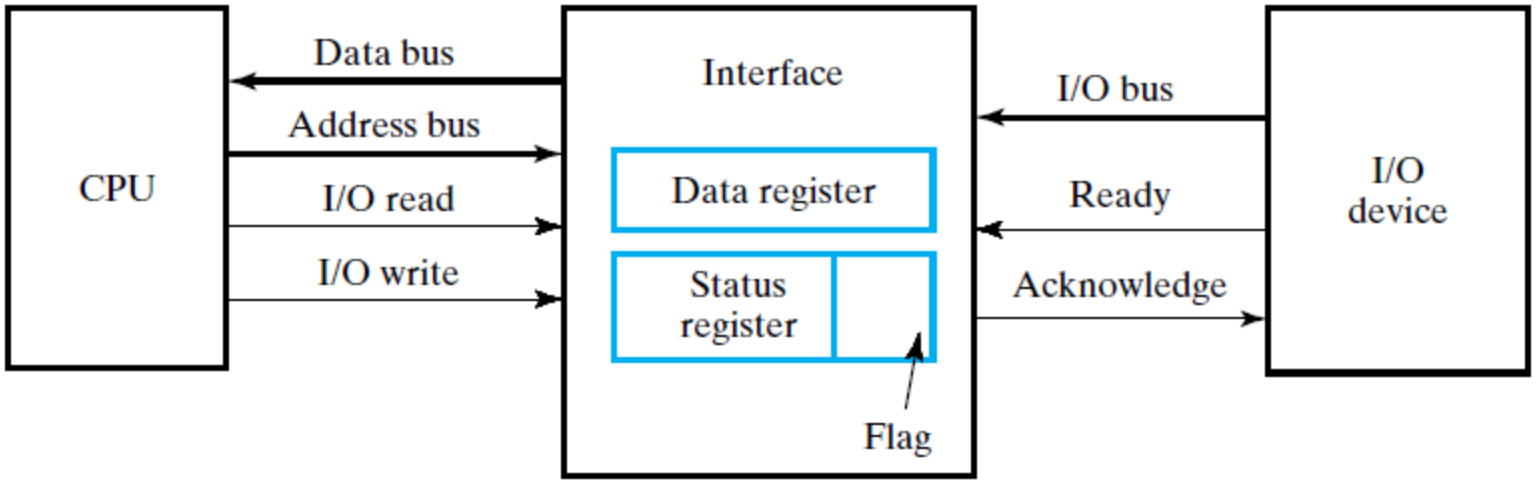

(b) Output packet

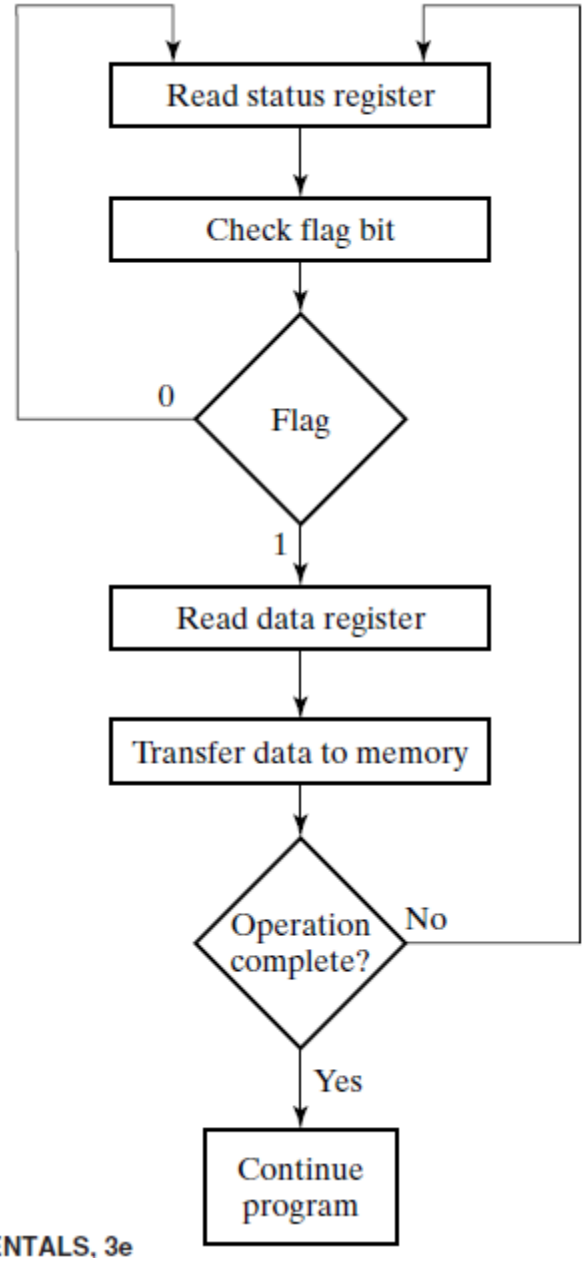


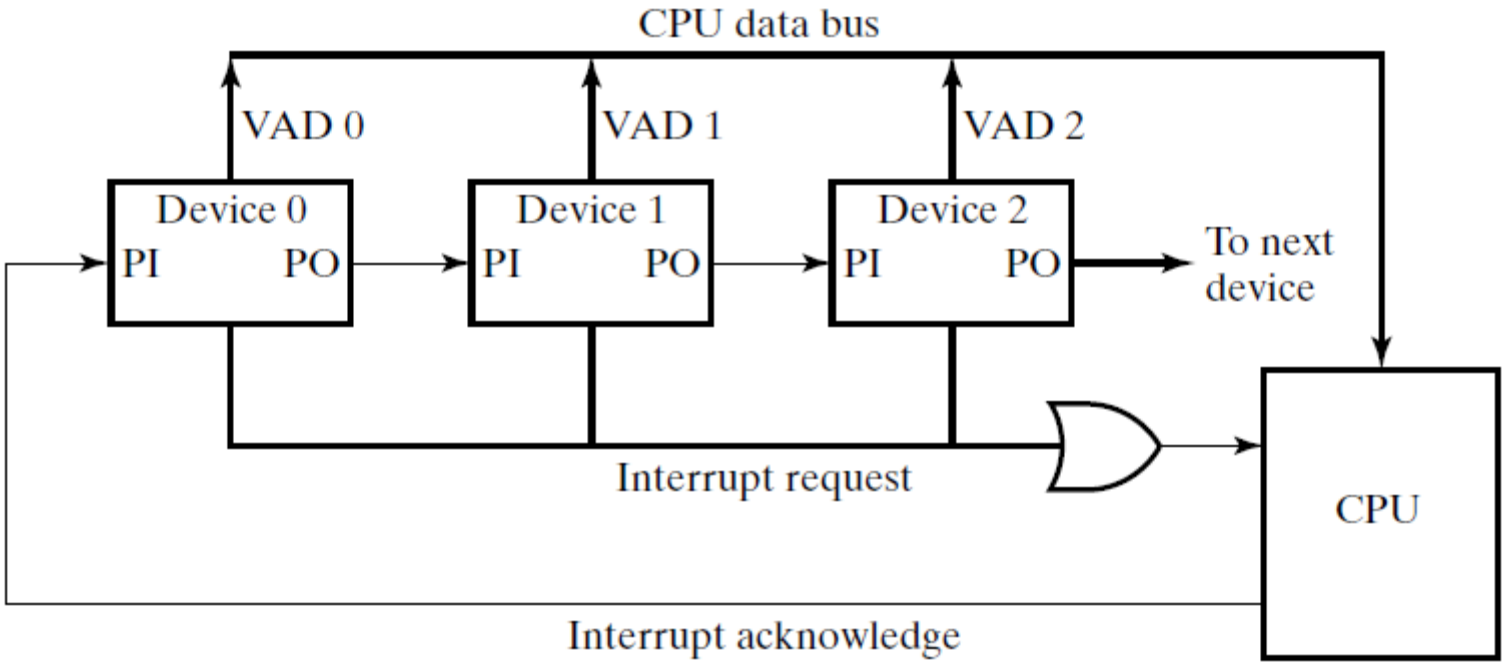

(c) Data packet (Data0 type)

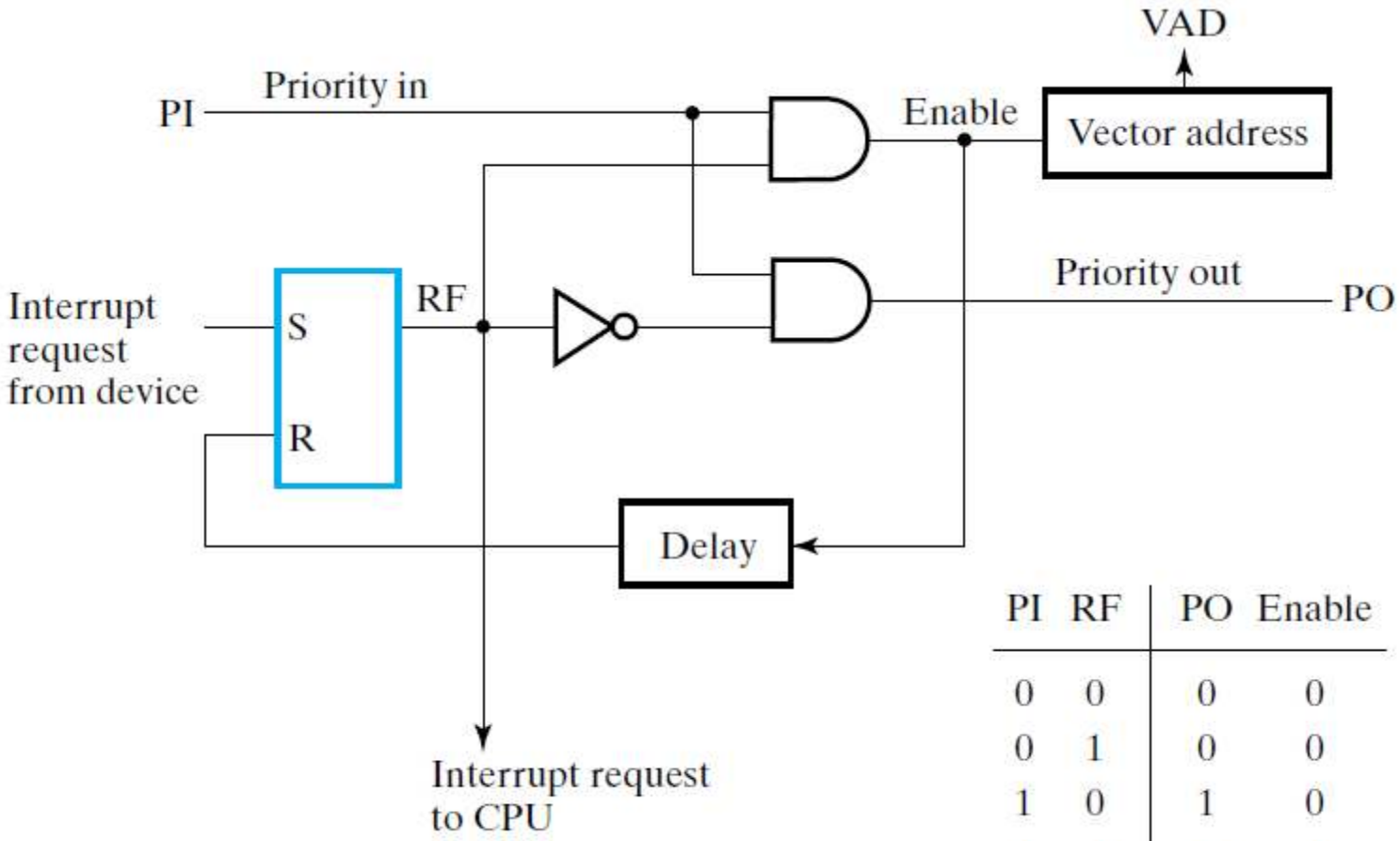



(d) Handshake packet (Acknowledge type)

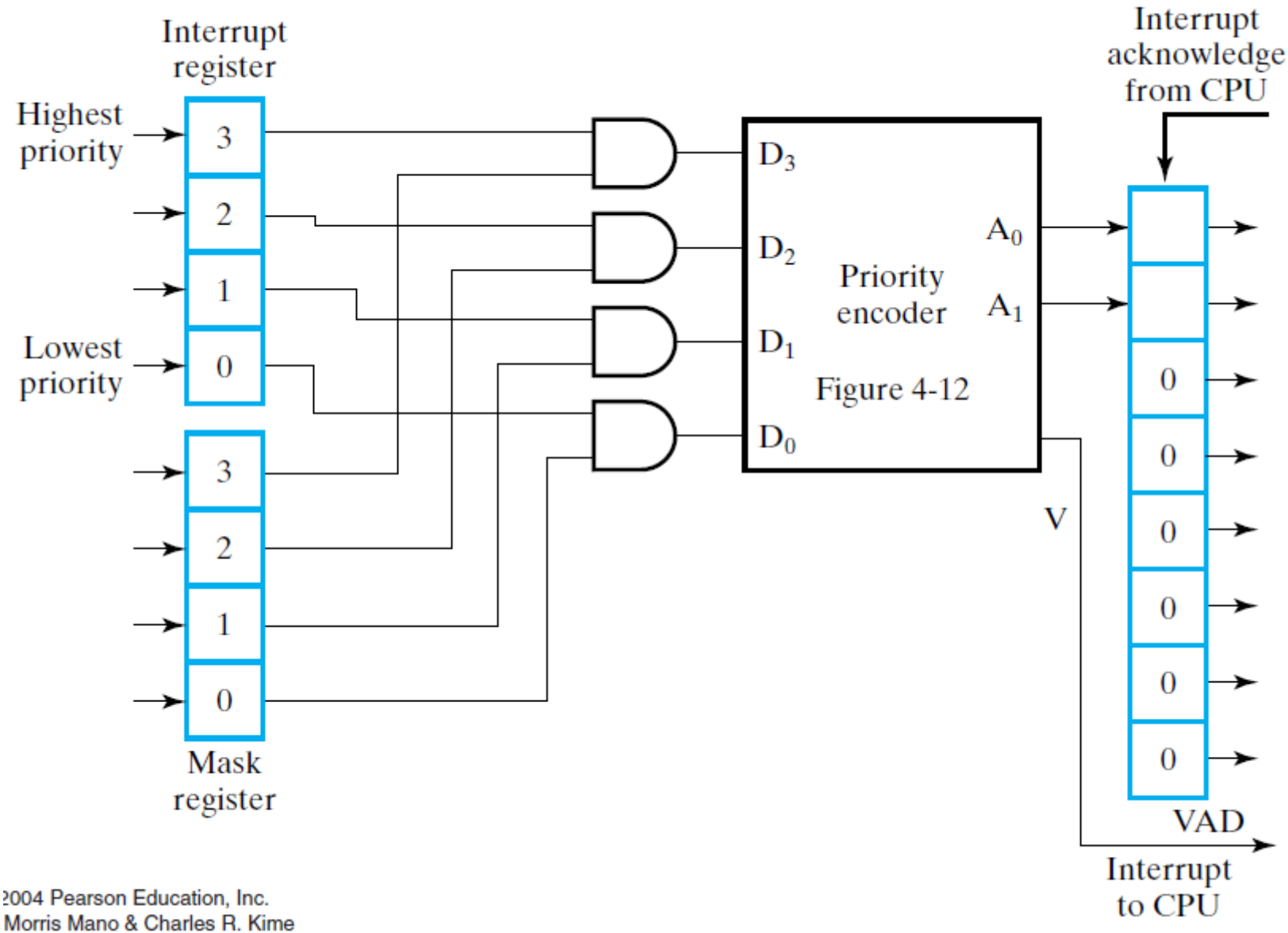

CPU
Data bus
Address bus
I/O read
I/O write
Interface
Data register
Status register
Flag
I/O bus
Ready
Acknowledge
I/O device


Read status register
Check flag bit
Flag
0
1
Read data register
Transfer data to memory
Operation complete?
No
Yes
Continue program


CPU data bus
VAD 0
VAD 1
VAD 2
Device 0
PI
PO
Device 1
PI
PO
Device 2
PI
PO
To next device
Interrupt request
CPU
Interrupt acknowledge




| PI | RF | PO | Enable |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

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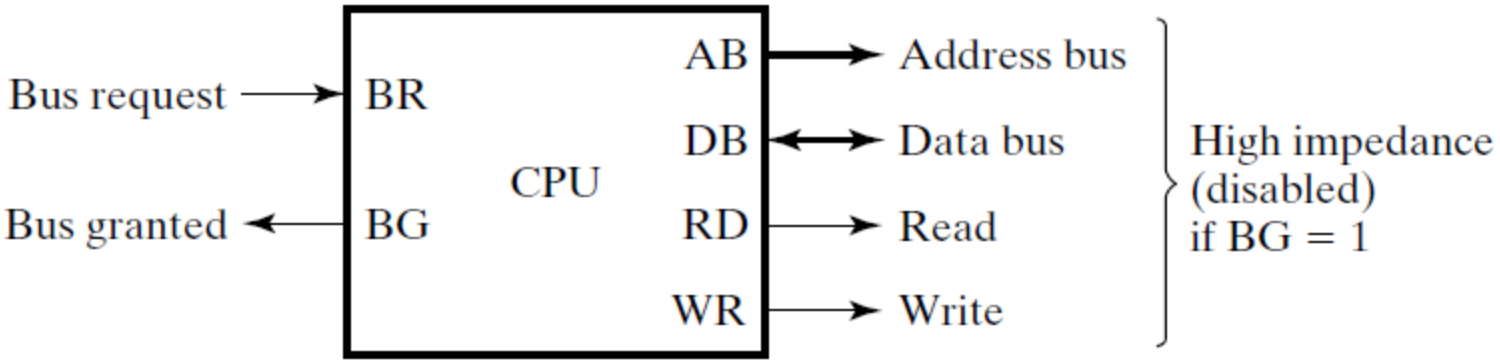
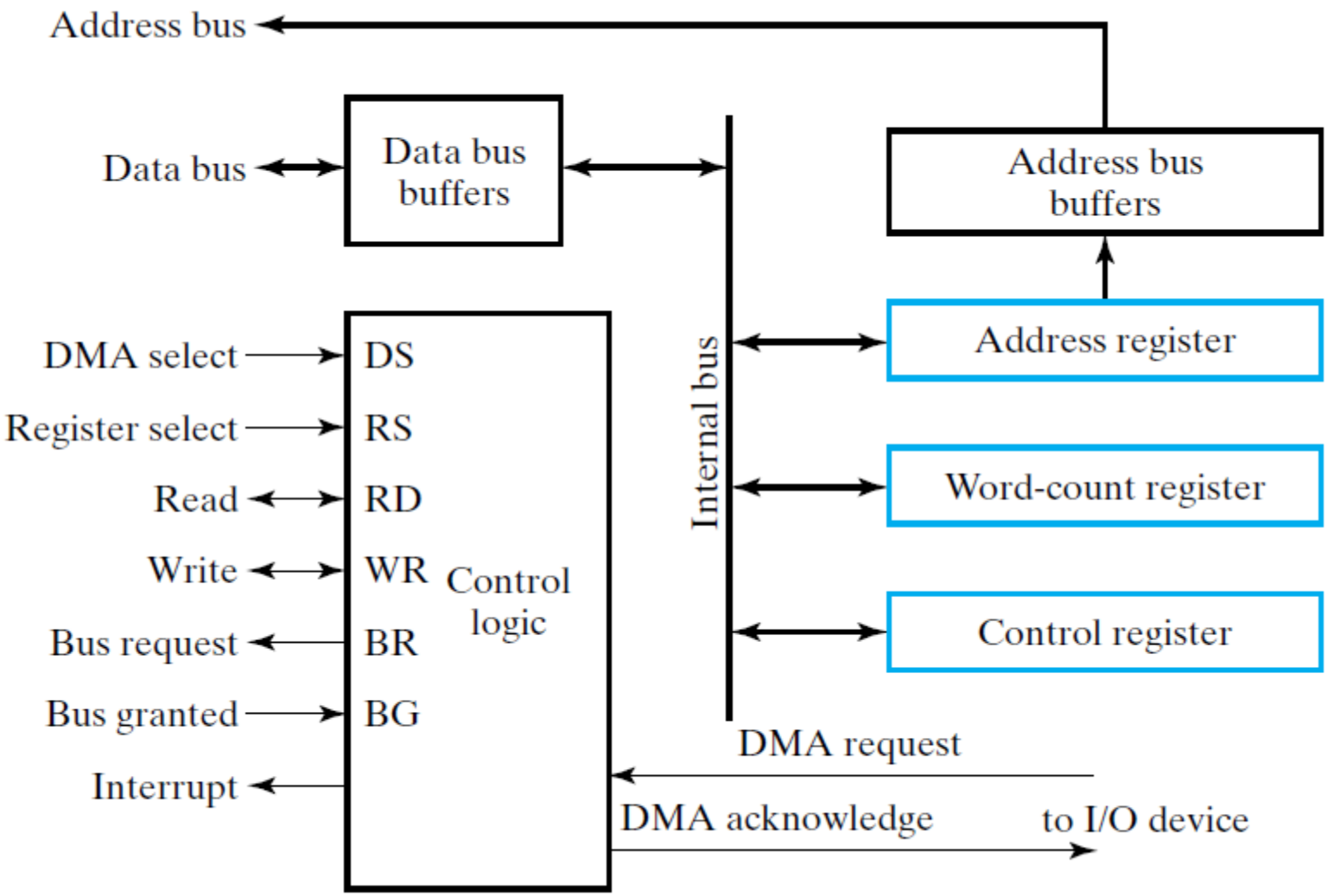
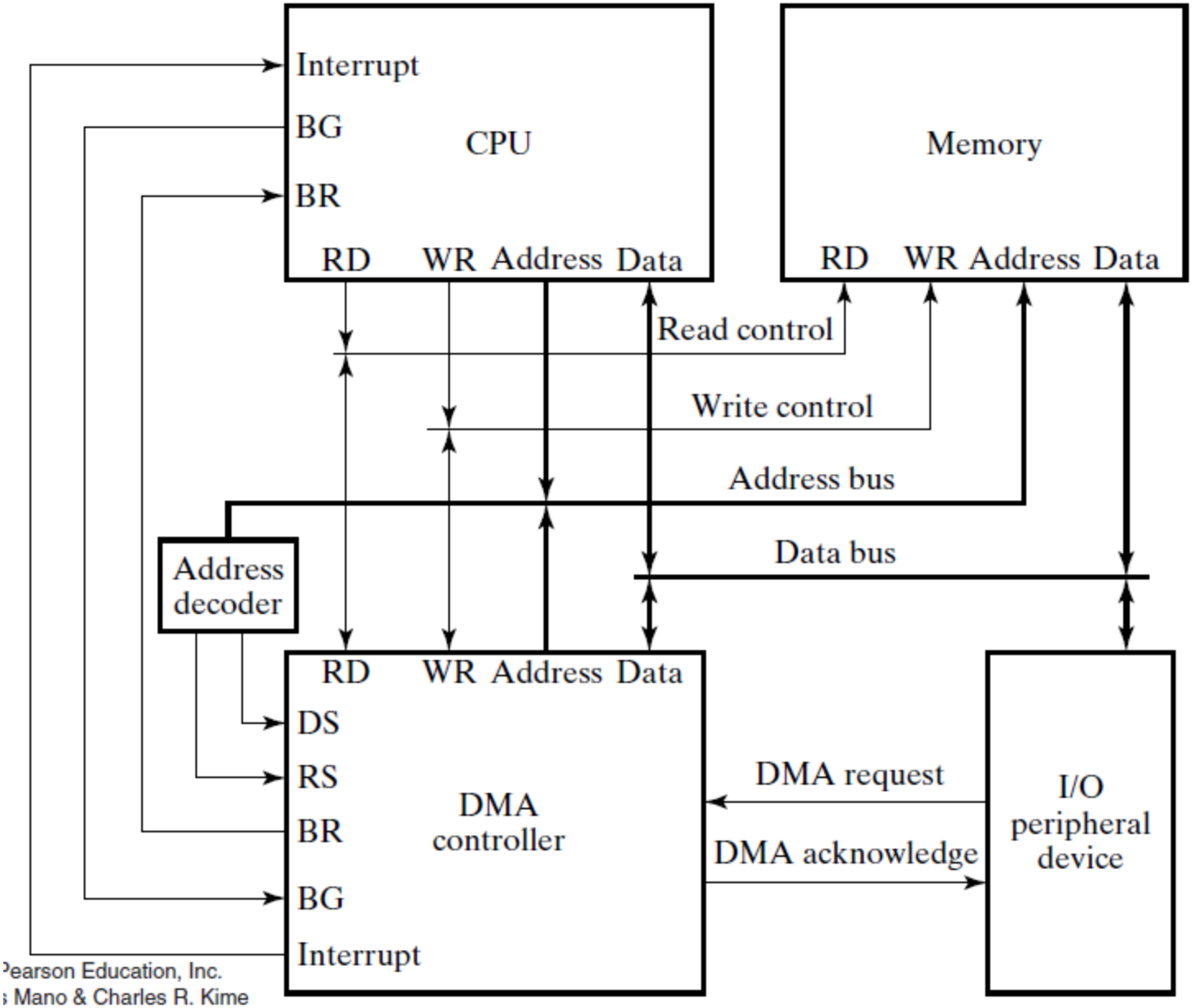

Bus request
BR
Bus granted
BG
CPU
AB
DB
RD
WR
Address bus
Data bus
Read
Write
High impedance
(disabled)
if BG = 1


Address bus
Data bus
Data bus buffers
Address bus buffers
Internal bus
Address register
Word-count register
Control register
DMA select
Register select
Read
Write
Bus request
Bus granted
Interrupt
DS
RS
RD
WR
BR
BG
Control logic
DMA request
DMA acknowledge
to I/O device

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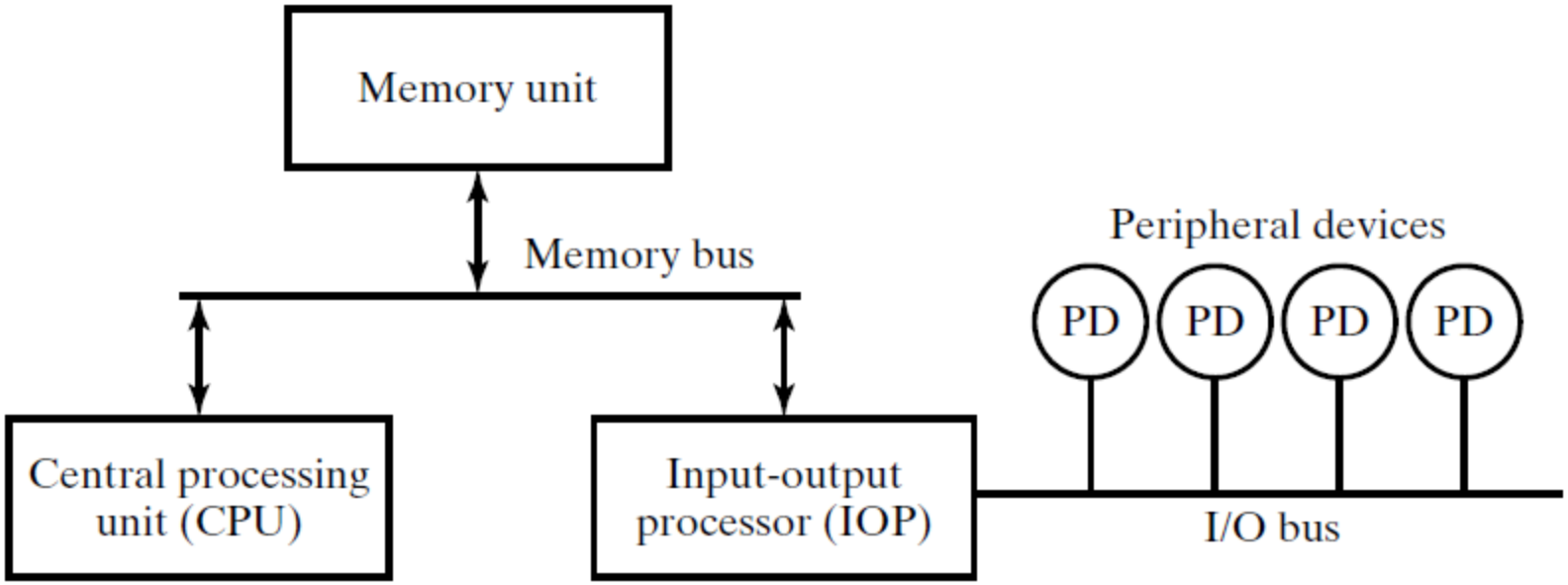
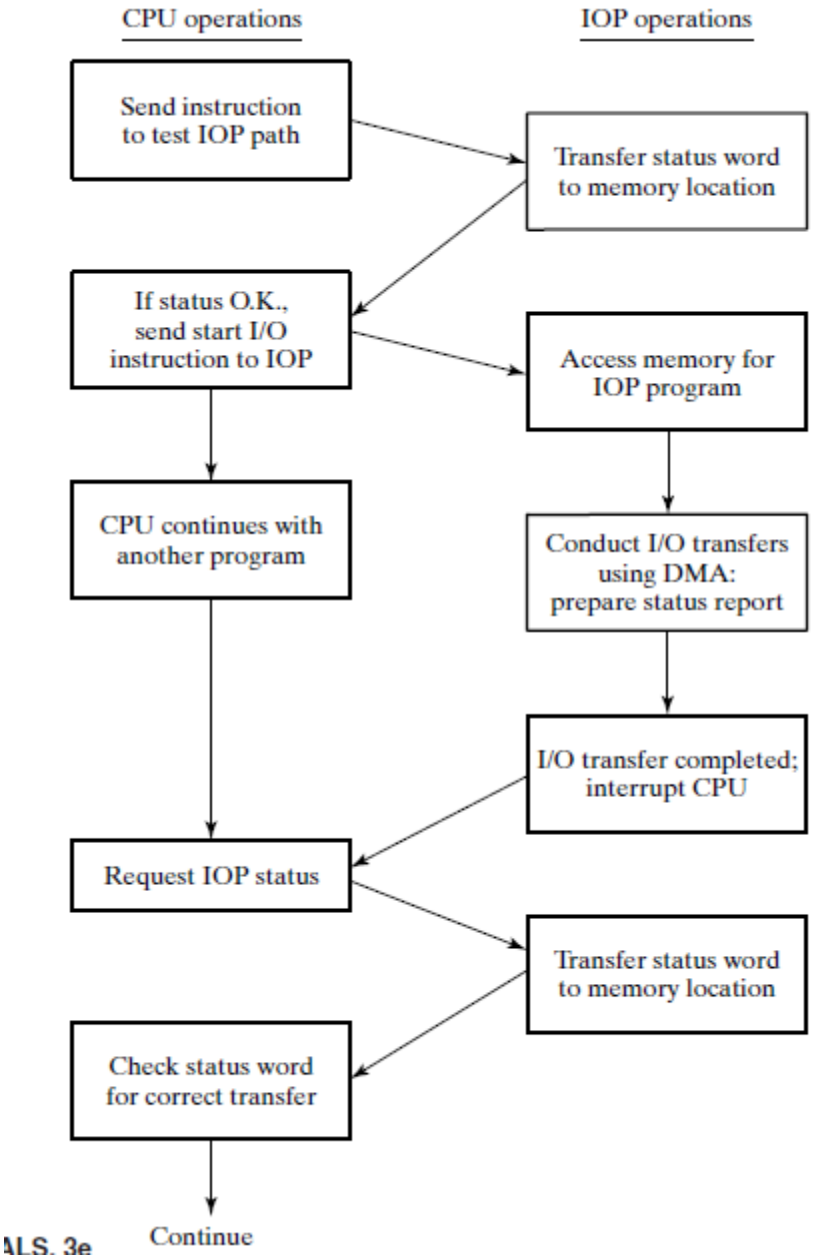

Memory unit
Memory bus
Peripheral devices
PD
PD
PD
PD
Central processing unit (CPU)
Input-output processor (IOP)
I/O bus


CPU operations
IOP operations
Send instruction to test IOP path
Transfer status word to memory location
If status O.K., send start I/O instruction to IOP
Access memory for IOP program
CPU continues with another program
Conduct I/O transfers using DMA: prepare status report
I/O transfer completed; interrupt CPU
Request IOP status
Transfer status word to memory location
Check status word for correct transfer
Continue

ALS, 3e