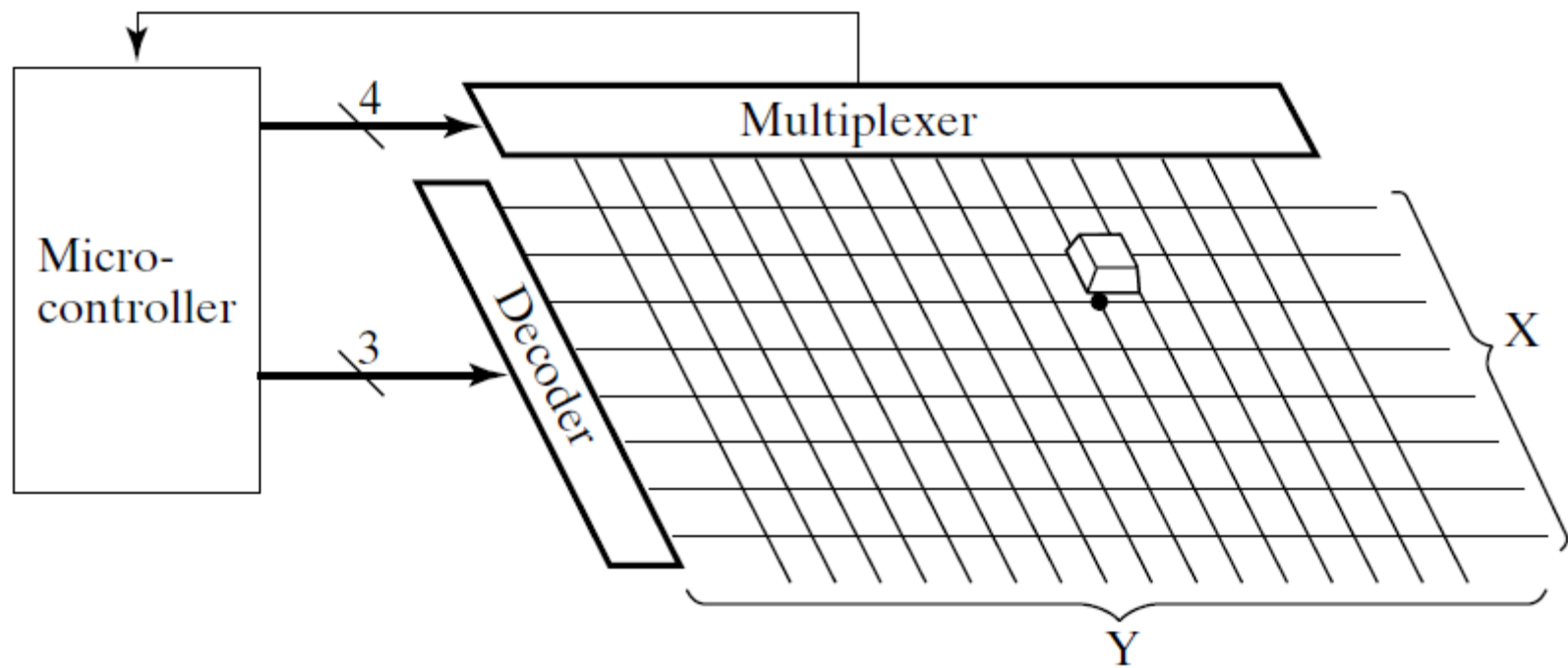
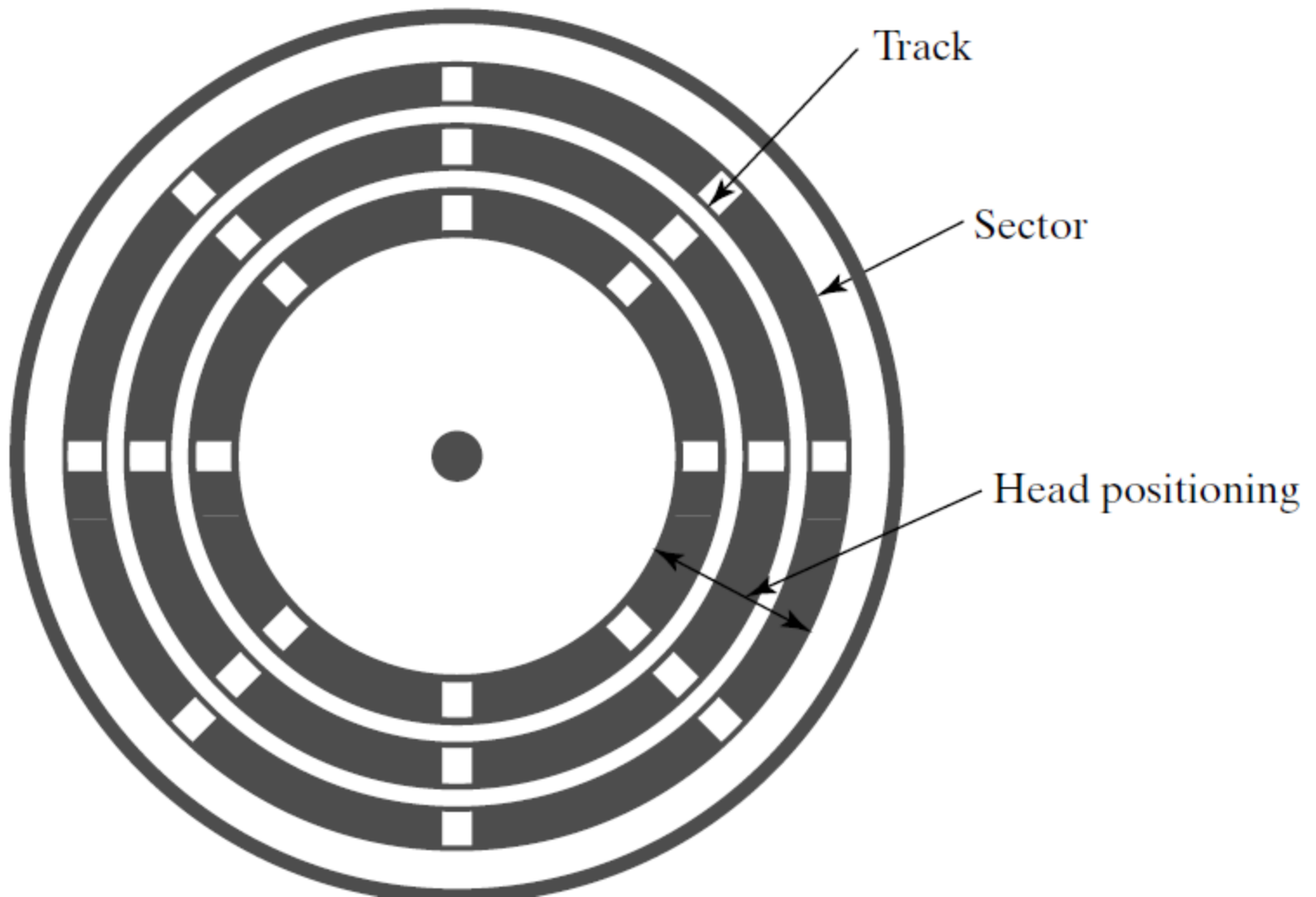
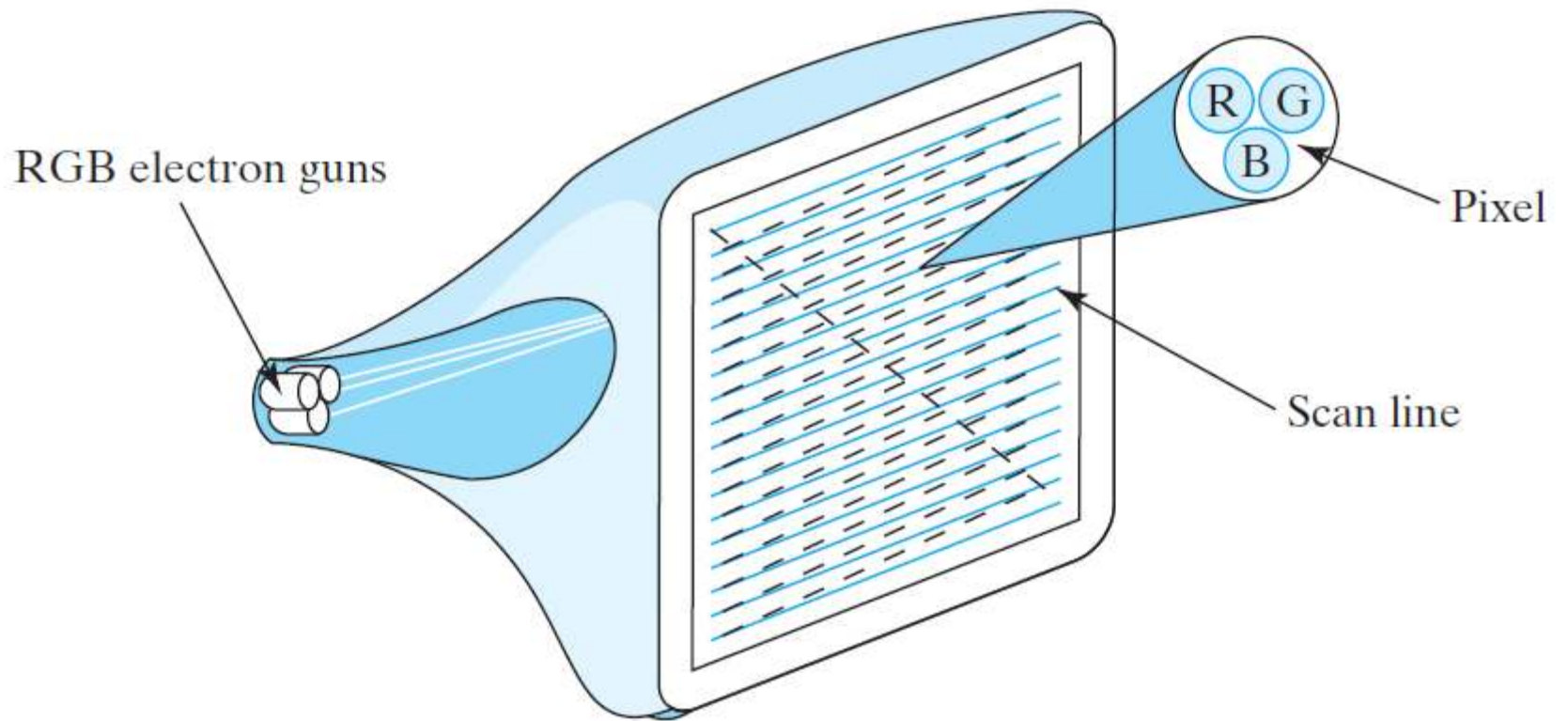
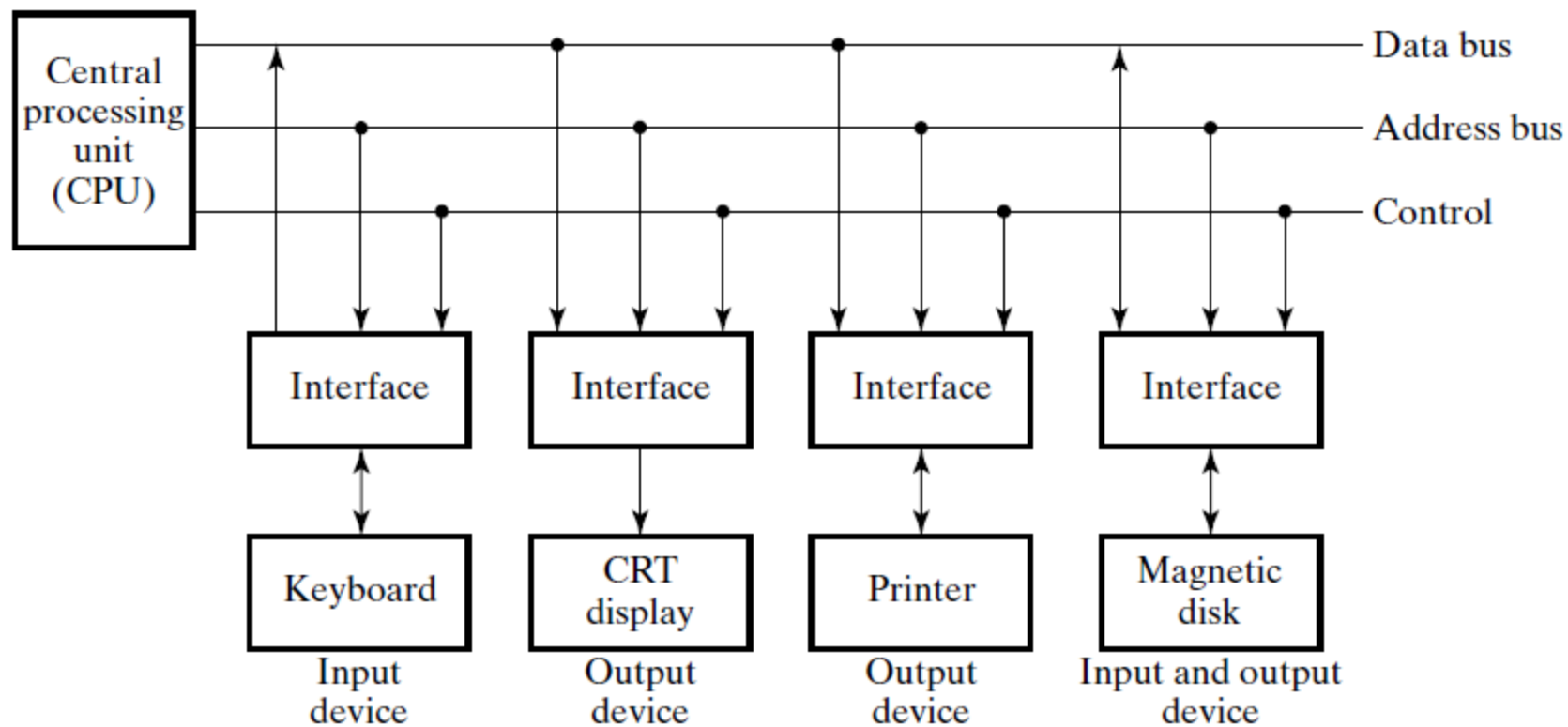


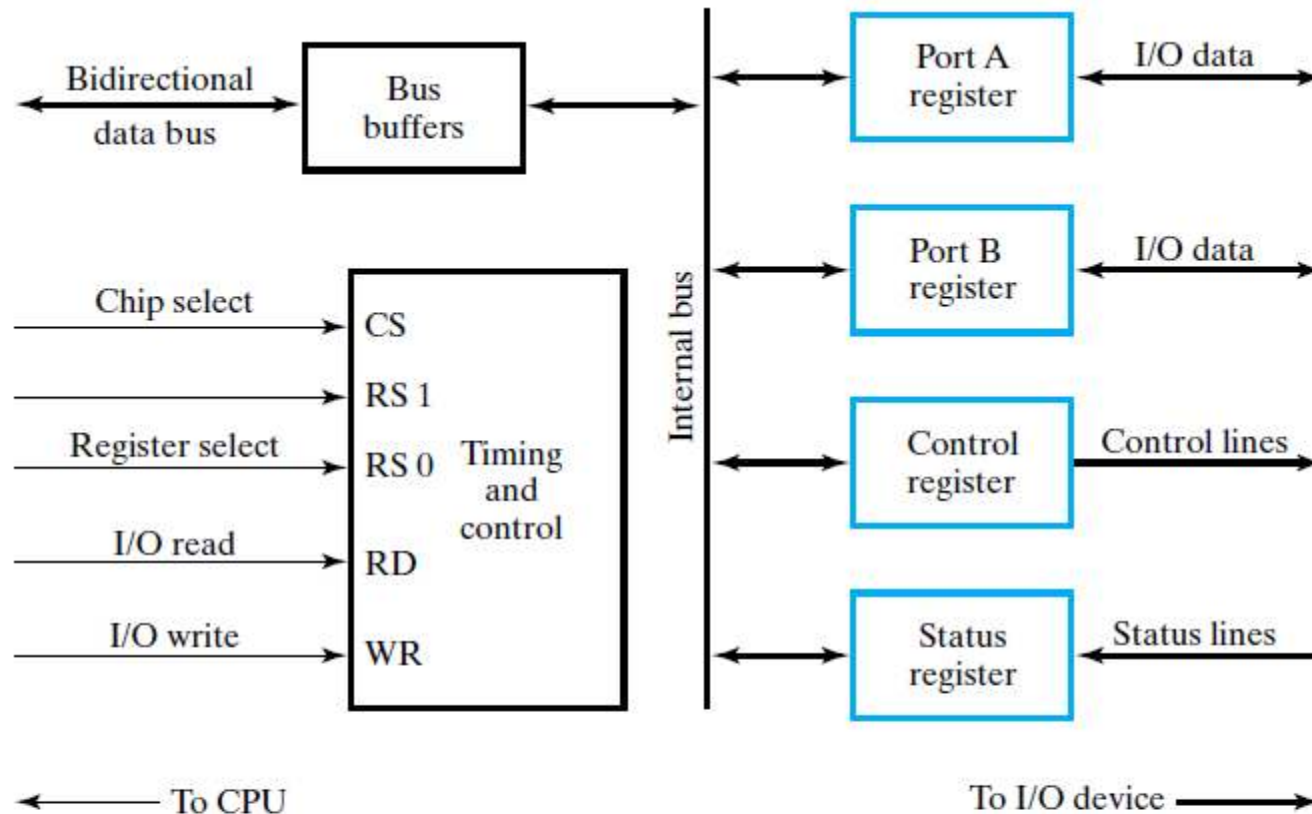
Input- Output



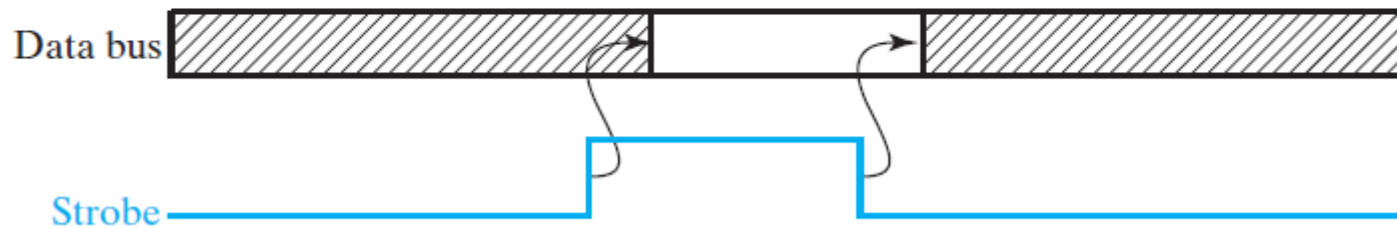
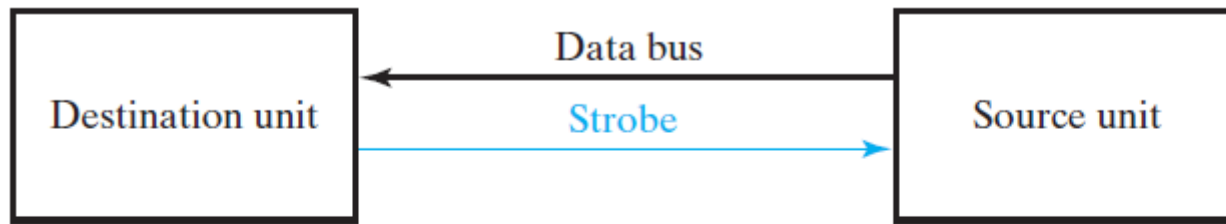




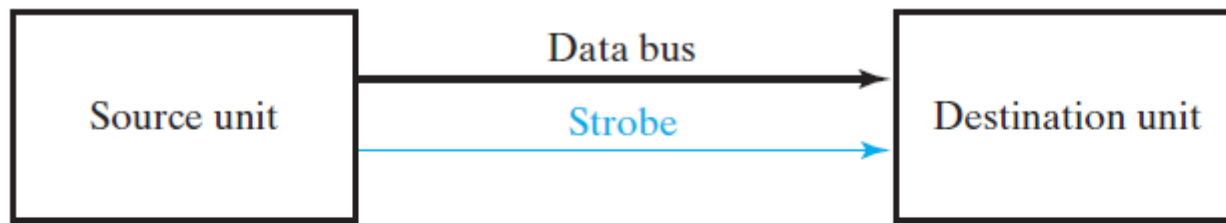




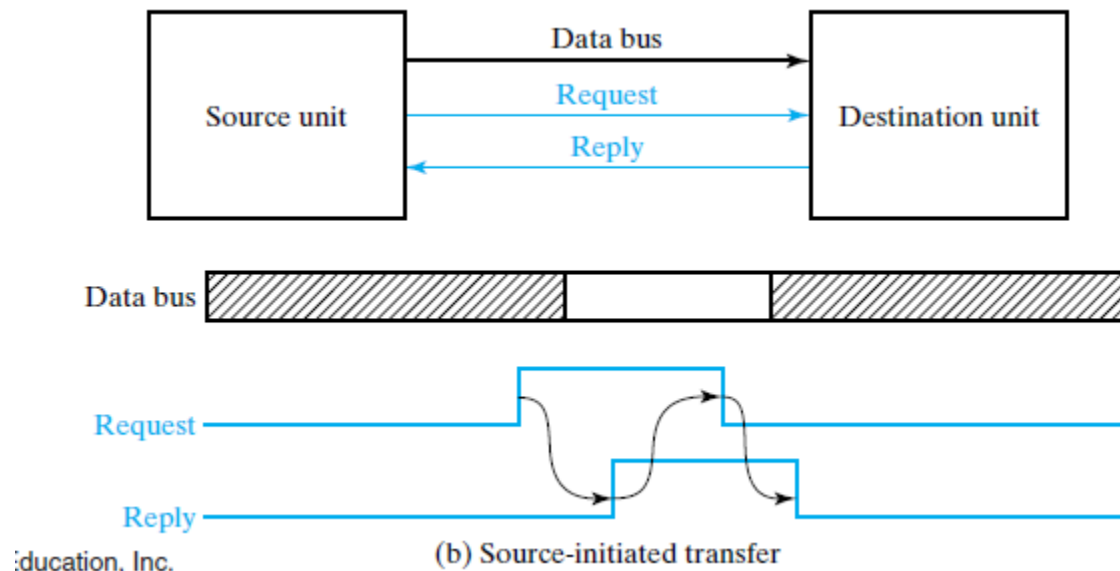
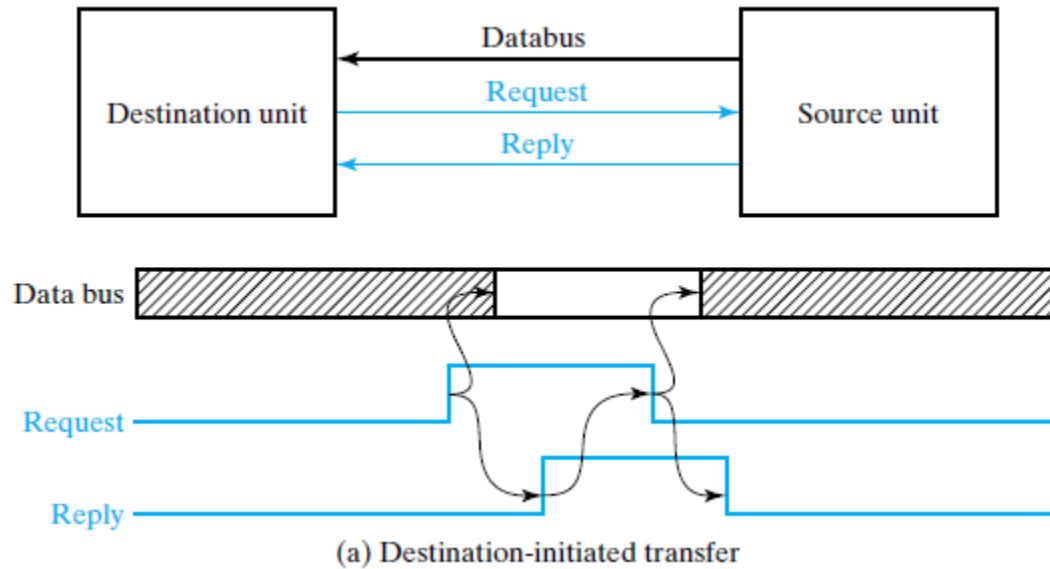
CS	RS1	RS0	Register selected
0	x	x	None: data bus in high-impedance state
1	0	0	Port A register
1	0	1	Port B register
1	1	0	Control register
1	1	1	Status register

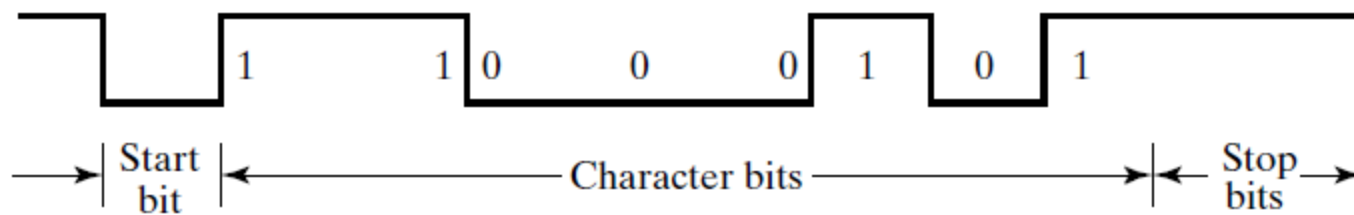


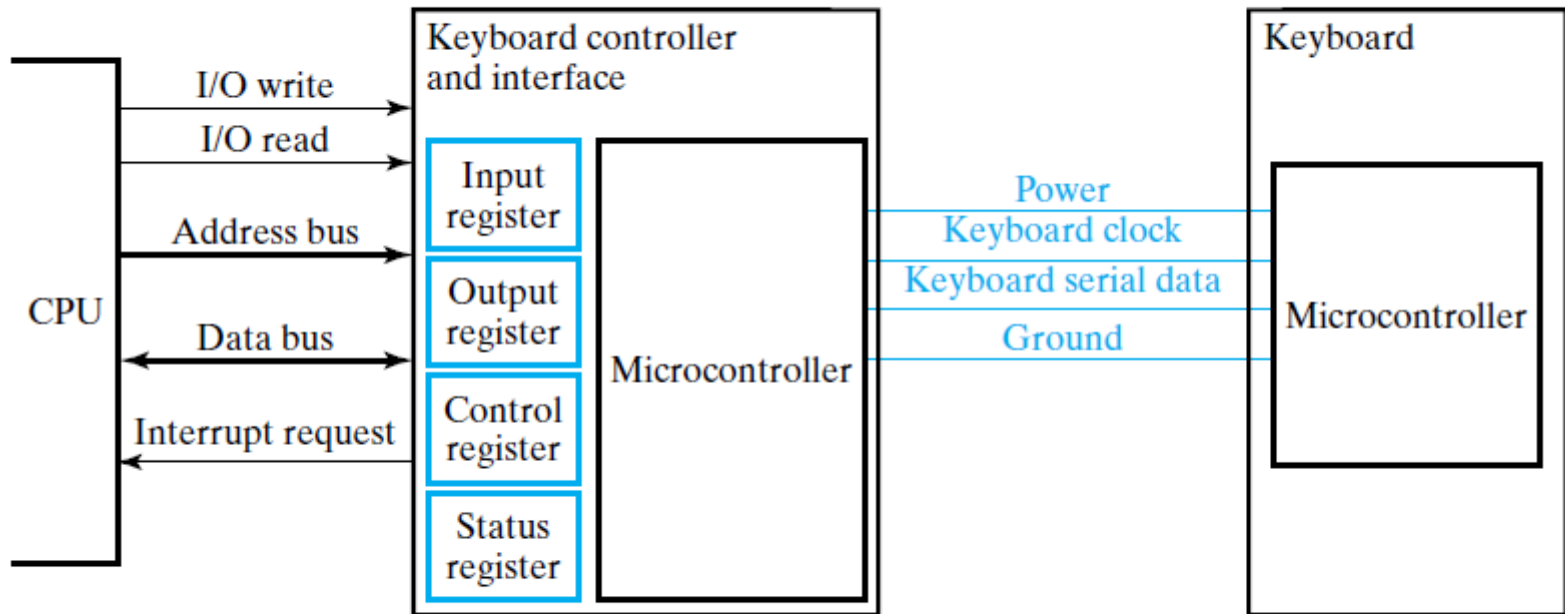
(a) Destination-initiated transfer

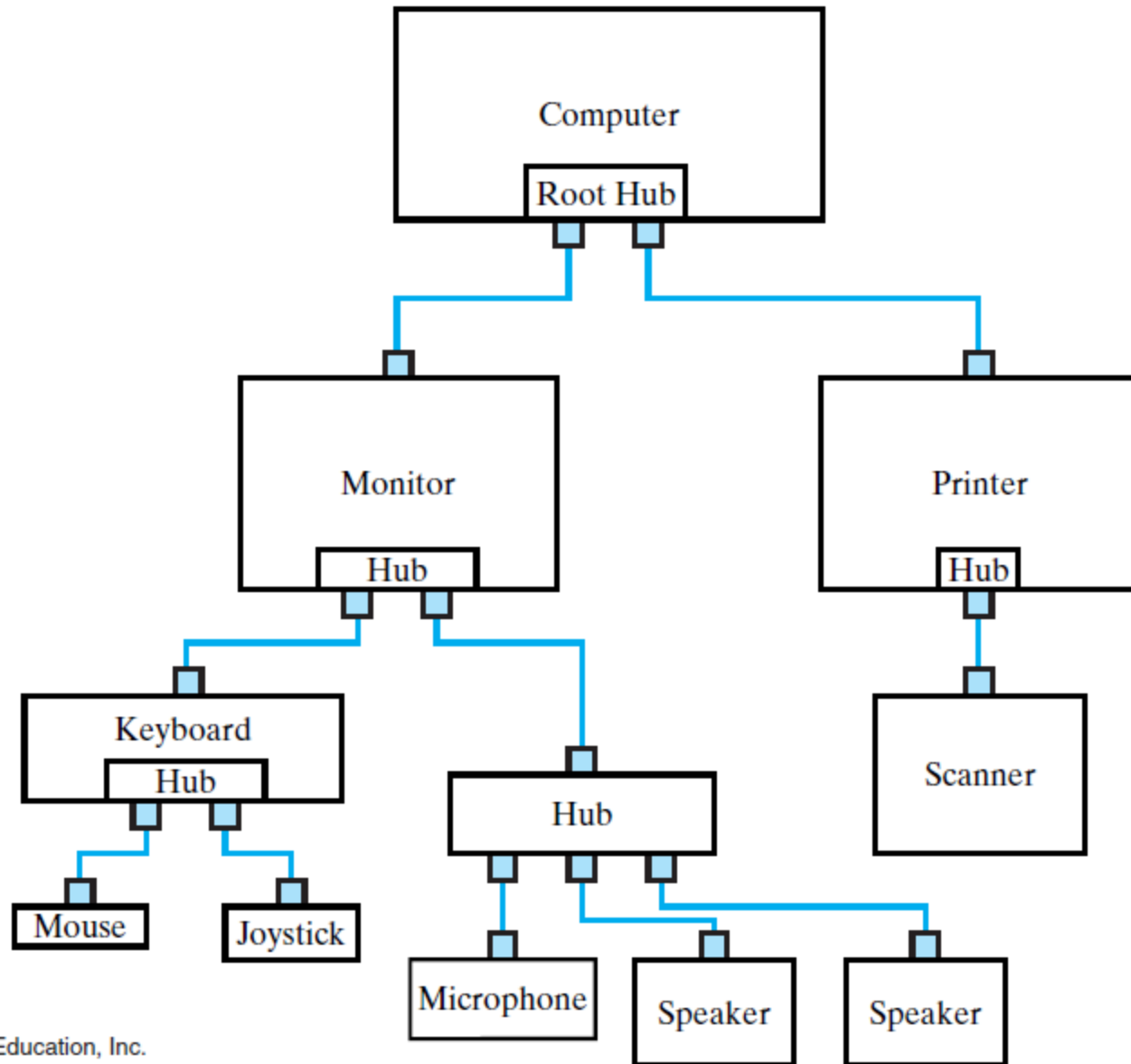


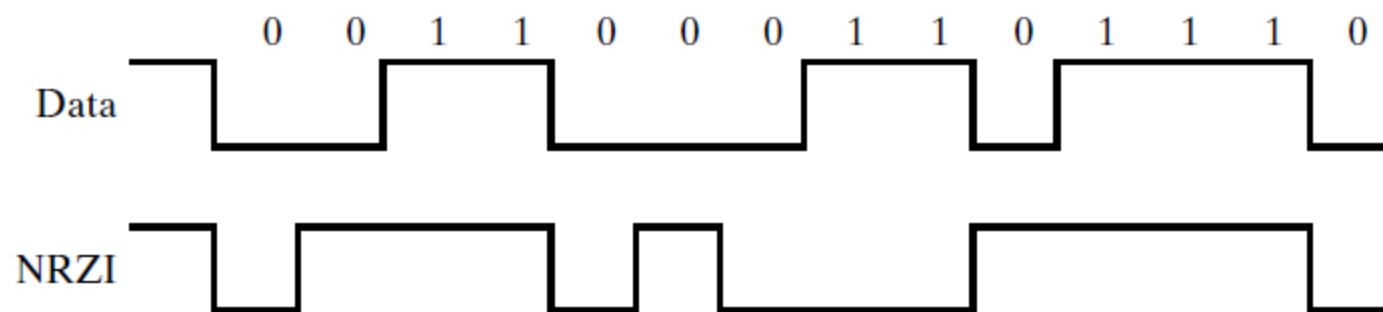
(b) Source-initiated transfer











SYNC	PID	Packet Specific Data	CRC	EOP
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(a) General packet format

SYNC 8 bits	Type 4 bits 1001	Check 4 bits 0110	Device Address 7 bits	Endpoint Address 4 bits	CRC	EOP
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(b) Output packet

SYNC 8 bits	Type 4 bits 1100	Check 4 bits 0011	Data (Up to 1024 bytes)	CRC	EOP
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(c) Data packet (Data0 type)

SYNC 8 bits	Type 4 bits 0100	Check 4 bits 1011	EOP
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(d) Handshake packet (Acknowledge type)

