CSE350

DIGITAL ELECTRONICS AND PULSE TECHNIQUES

Lab- 02

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Section- 02

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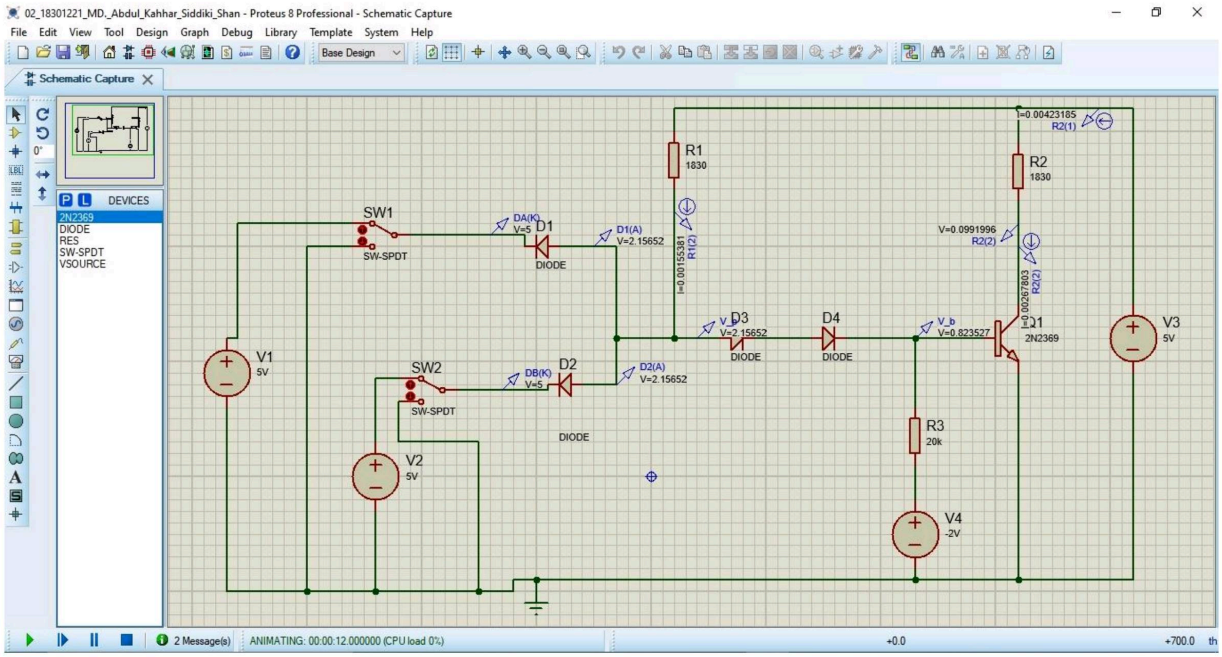
Circuit diagram of NAND gate:



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3.

Input A	Input B	V_{DA}	V_{DB}	V_p	I_{R1}	I_{R2}	V_b	Output Y
0	0	0.6586	0.6586	0.6588	0.00237	$1.7236e^{-01}$	-0.516	5
0	1	0.6765	-4.3232	0.6767	0.0023	$1.722e^{-11}$	-0.499	5
1	0	-4.3232	0.6765	0.6767	0.0023	$1.722e^{-011}$	-0.499	5
1	1	-2.8434	-2.8434	2.1565	0.001553	0.002678	0.8235	0.0992

4.

Input A	Input B	V_p	V_b	Output Y
1	0	0.676729	-0.499	5
1	1	2.1565	0.823527	0.09919

Report

1. Assume that Logic High has been applied to both inputs of the circuit shown in fig: 1. draw the partial circuit consisting of only those components which remain active.

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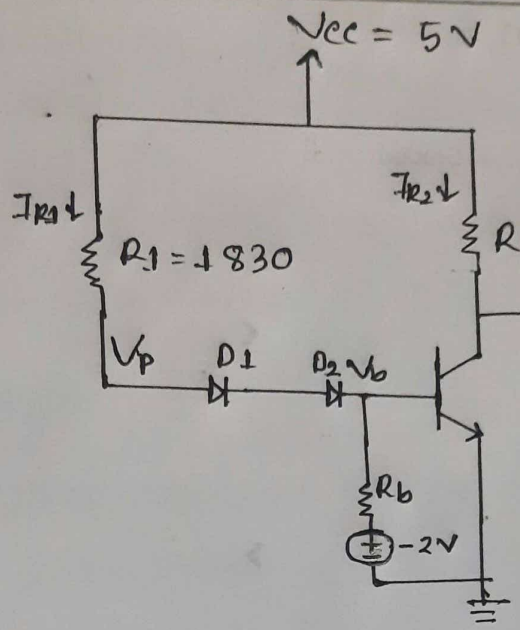


$R_1 = 1830$

$R_2 = 1830$

$V_p = 2.15652$

$V_b = 0.823527$

$R_b = 20k$

In saturation

2. Explain the logic operation in the table 2 (Laboratory task step 4) How did you reach that logic operation from NAND operation of figure 1.

→ In table-4, we can see that, when the input is low, a the output is high. When the input is high, the output is low. which is the behaviour of an inverter. In inverter when we provide low input, it will give high output and while input high, the output is low. So, while input A constant and, we are changing the input value of B, the

circuit is working as an inverter.

3. Explain briefly how NAND operation is performed in the circuit.

→ NAND gate made with two gates and they are AND gate, not gate. Actually it provide the reverse output of AND gate. Describing it with example below:

Case-01:

Input A=0, Input B=0:

Here when the both input are low, diode D_1 and D_2 are turned on and current will flow through it. The voltage of V_P= 0.65588V. which is not enough to active Diode D_3 and D_4 as anode voltage of D_3 less than cathode voltage of D_3. So, D_3 and D_4 will be open circuit. So, transistor will be in cut off mode. So, the will be no current through the transistor. So, the output voltage will be equal to Vcc and output voltage is high.

Case-02:

Input A = 0, Input B = 1

As one input is high, it will create open circuit in diode D_1. But, other one is low and diode D_2 will be on. Current will flow through it. Vp voltage will not be enough to activate the diode D_3 and D_4. So, they will be on open circuit. The transistor will be in cut off mode. So, the output voltage will be high.

case-03:

Input A = 1, Input B = 0

It will work same as case-02. only D_1 will be active and D_2 will be open circuit. D_3 and D_4 will be open circuit. ~~Trans~~ as Vp is low. Transistor will be in cut off mode. High output will generate in output.

Case-04:

Input A = 1, Input B = 1:

As both inputs are high, the diode D_1 and D_2 will be on Open circuit as their cathode voltage is higher than anode voltage. But, the voltage of Vp will be enough to turn on diode D_3 and D_4. As a result the transistor

4. will work. Actually, the transistorz is working on saturation mode. In addition, we get lowerz output in the output voltage which is 0.09919 V.

To sum up, in the above mentioned way. the NAND operation performed in the circuit.

4. Using products data, find the operation mode of Q_1 when one of the inputs in High and other one is low.

→ From the proteus data, while one input is high and another input is low, the transis operation in cut off mode. Here, $I_B = I_c = I_E = 0$ which is the characteristic of cut off mode. The output voltage is also High.

Here, $V_E > V_B$

$V_c > V_B$

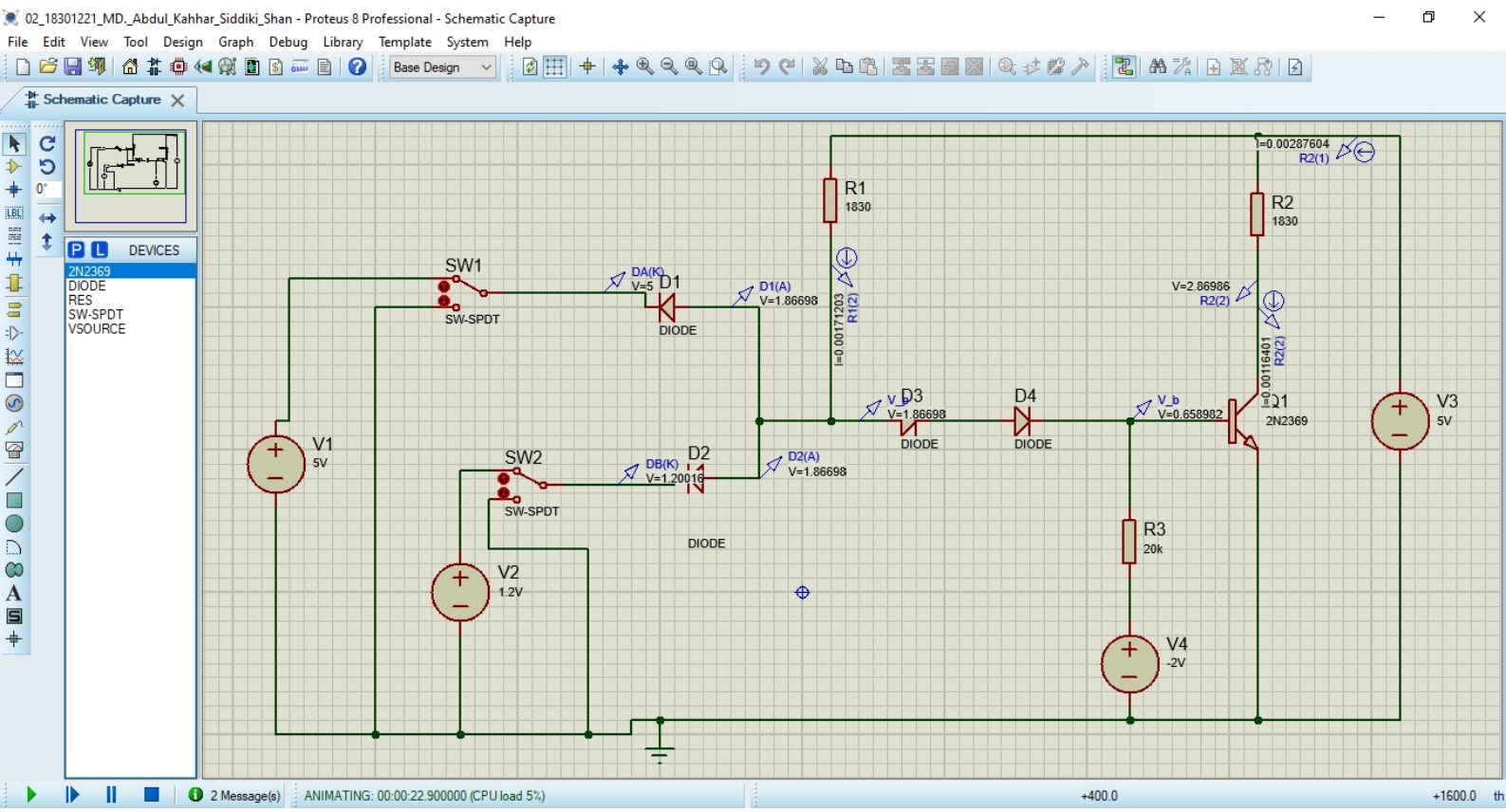
$I_B = I_c = I_E = 0$

So, it is in cut off

(Verified)

5. What is the maximum value of inputs A, B to keep the output High? (Use simulation data)

→ After analysing the simulation data, i found that the maximum value of inputs A, B to keep the output high is 1.2V. Below i will show the screen shot of that simulation data.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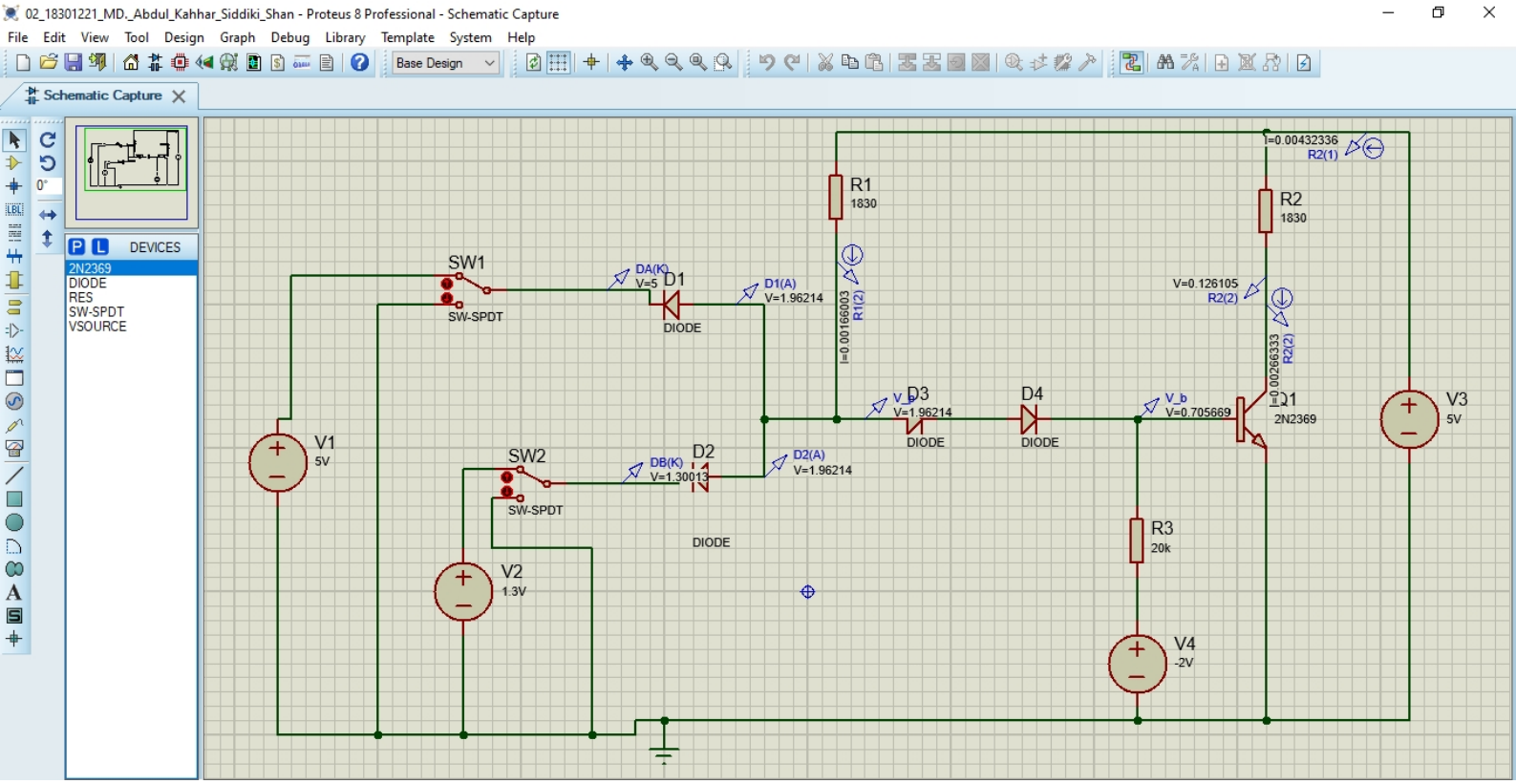
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
2N2369
DIODE
RES
SW-SPDT
VSOURCE
SW1
SW-SPDT
DA(K)
V=5
D1
DIODE
D1(A)
V=1.86698
R1
1830
I=0.00171203
R1(2)
I=0.00287604
R2(1)
R2
1830
V=2.86986
R2(2)
I=0.00116401
R2(2)
V_b
V=0.658982
Q1
2N2369
V3
5V
V_D
V=1.86698
D3
DIODE
D4
DIODE
V1
5V
SW2
SW-SPDT
DB(K)
V=1.20016
D2
DIODE
D2(A)
V=1.86698
R3
20k
V2
1.2V
V4
-2V
2 Message(s)
ANIMATING: 00:00:22.900000 (CPU load 5%)
+400.0
+1600.0


02_18301221_MD._Abdul_Kahhar_Siddiki_Shan - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
2N2369
DIODE
RES
SW-SPDT
VSOURCE
SW1
SW-SPDT
DA(K)
V=5
D1
DIODE
D1(A)
V=1.96214
R1
1830
I=0.00166003
R1(2)
I=0.00432336
R2(1)
R2
1830
V=0.126105
R2(2)
I=0.00266333
R2(2)
V_b
V=1.96214
D3
DIODE
D4
DIODE
V_b
V=0.705669
Q1
2N2369
V3
5V
V1
5V
SW2
SW-SPDT
DB(K)
V=1.30013
D2
DIODE
D2(A)
V=1.96214
R3
20k
V2
1.3V
V4
-2V