

CSE350

DIGITAL ELECTRONICS AND PULSE TECHNIQUES

Lab- 01



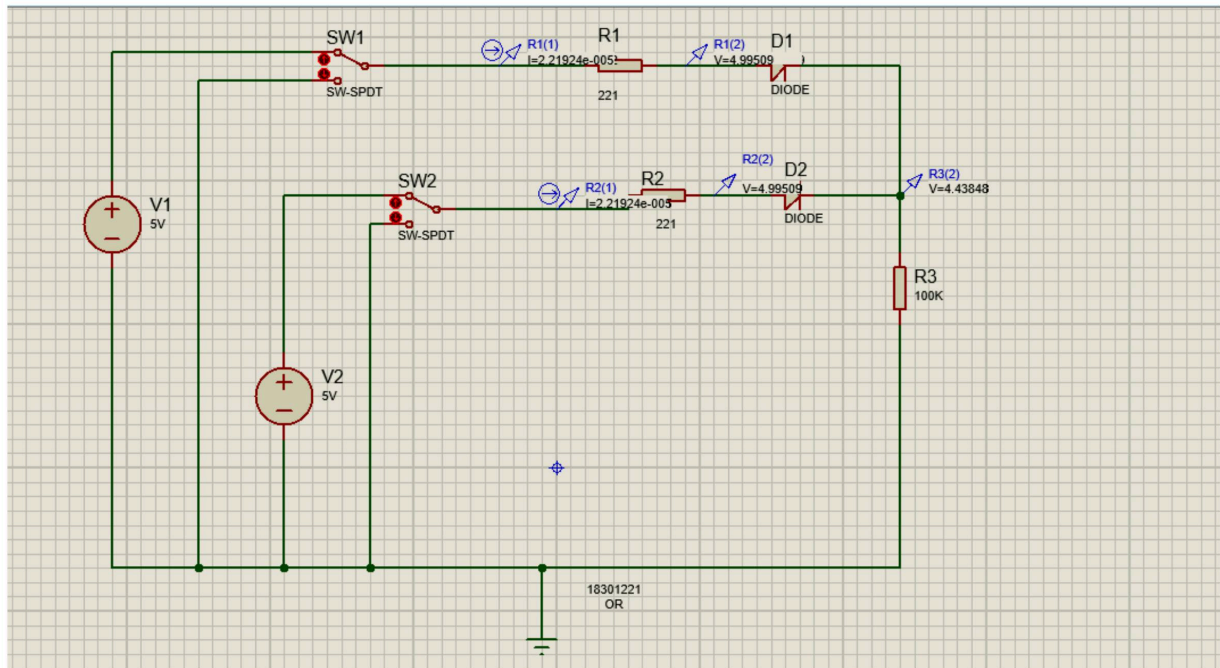
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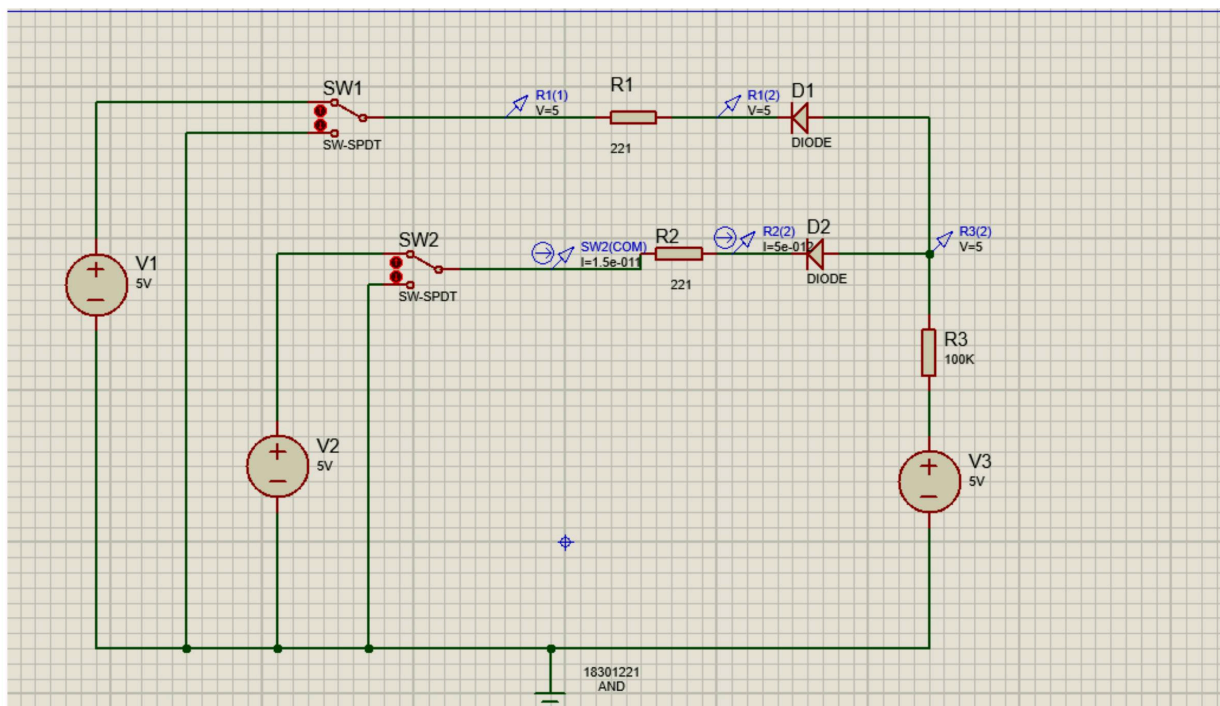
Section- 02

Date of Submission- 3 July, 2021

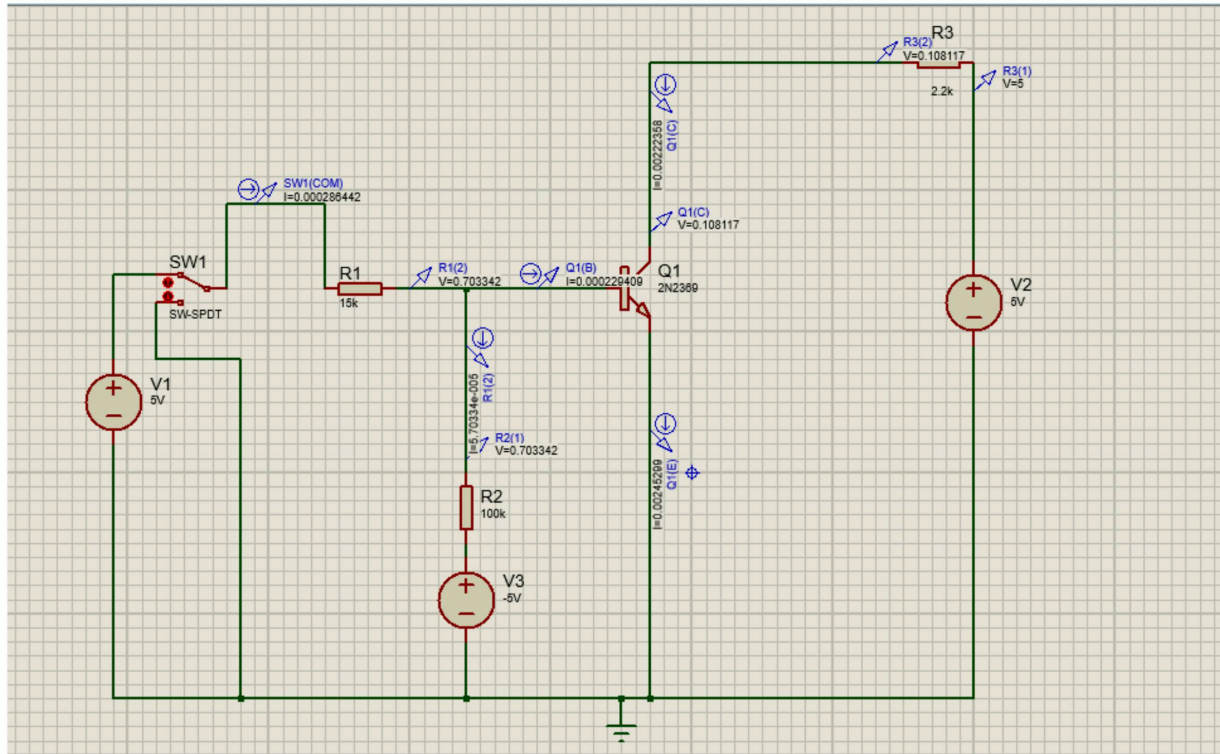
OR gate:



AND gate:



Inverter:



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OR Gate

V_A	V_B	V_{R1}	V_{R2}	I_{R1}	I_{R2}	$V_R = Y$
0	0	0	0	$1.19332e-020$	$1.19332e-020$	$1.38663e-015$
0	5	0	0.00976	$-4.42583e-012$	$4.41584e-005$	4.41583
5	0	0.00976	0	$4.41584e-005$	$-4.42583e-012$	4.41583
5	5	0.00491	0.00491	$2.21924e-005$	$2.21924e-005$	4.43848

AND Gate:

V_A	V_B	V_{R1}	V_{R2}	I_{R1}	I_{R2}	$V_R = Y$
0	0	0.0049	0.0049	$2.21924e-005$	$2.21924e-005$	0.5615
0	5	0.01	0.01	$4.41583e-005$	$-9.42e-012$	0.58416
5	0	0	0.01	$-9.42e-012$	$4.41583e-005$	0.58416
5	5	0	0	$5e-012$	$5e-012$	5

Inverter:

V_i	V_{R1}	V_{R2}	V_{Rc}	I_1	I_2	I_B	I_c	Y
0	0.652	4.347	0	$4.34782e-005$	$4.34782e-005$	$-3.195e-012$	$1.729e-011$	5
5	4.30	5.7033	4.89	0.0002864	$5.70334e-005$	0.0002294	0.0022235	0.108

Report:

1. Explain the operation of diode AND circuit.

→ AND always does the min operation in diode.

V_A	V_B	Y
0	0	0.5615
0	5	0.58416
5	0	0.58416
5	5	5

Here we can see that the output voltage is low because ~~electricity~~ current is flowing through it. It happens when input is low. But, when input is high it will create an open circuit and output voltage is high. As it is in open circuit, current is zero.

2. (For both circuits) Will the diodes D_1 and D_2 will work if $V_A = V_B = 6V$ and $V_R = 5V$

For OR circuit:

AND circuit:

V_A	V_B	V_R
0	0	$1.66396e^{-015}$
0	6	5.40839
6	0	5.40839
6	6	5.43216

V_A	V_B	V_R
0	0	0.056
0	6	0.5841
6	0	0.5841
6	6	5

Here, For OR circuit, we can see that for higher input, we are getting higher output. So, ~~the Diode~~ according to the table, D_1 and D_2 will work for $V_A = V_B = 6$, and $V_R = 5$.

For AND circuit, If input voltage $V_A = V_B = 6$, the diode will act as a open circuit and no current will flow through it. Because of open circuit, the output voltage will be high and it is 5V. So, diode will not work as it is in open circuit.

3. What is the function of $R_2 = 100k$ at the base of an inverter in figure 3?

→ Here, R_2 biases the transistor to the appropriate on-off threshold. The output is inverted since the collector-emitter voltage of transistor is taken as output. It is high when input is low and in cutoff. $R_2 = 100k$ helps to supply more current when through I_B when the transistor is on and in saturation mode. Because of huge resistance, only a negligible amount of current flow through the R_2 resistor. It helps to increase the current supply through base I_B .

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4. Verify that the transistor will be operating in the saturation and cut off region in two cases for the inverter circuit (Use proteus data for verification).

→ When input is low, the transistor will be in cut off mode. The voltage difference in collector will be high and it is 5V. Also, $V_E > V_B$ and $V_C > V_B$. $I_B = 0$, $I_C = 0$, $I_E = 0$

→ When input is high, the transistor will be in saturation mode. The voltage in $Q1(c)$ is 0.108117V. $V_B = 0.703342V \approx 0.8V$. The value of $Q1(c) \approx 0.2/0.1V$. The output voltage is low.

According to above data, the transistor will be operating in saturation and cut off region
(Verified)

5. Assuming OR Gate, Draw the output.

