CSE350

DIGITAL ELECTRONICS AND PULSE TECHNIQUES

Lab- 03

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Section- 02

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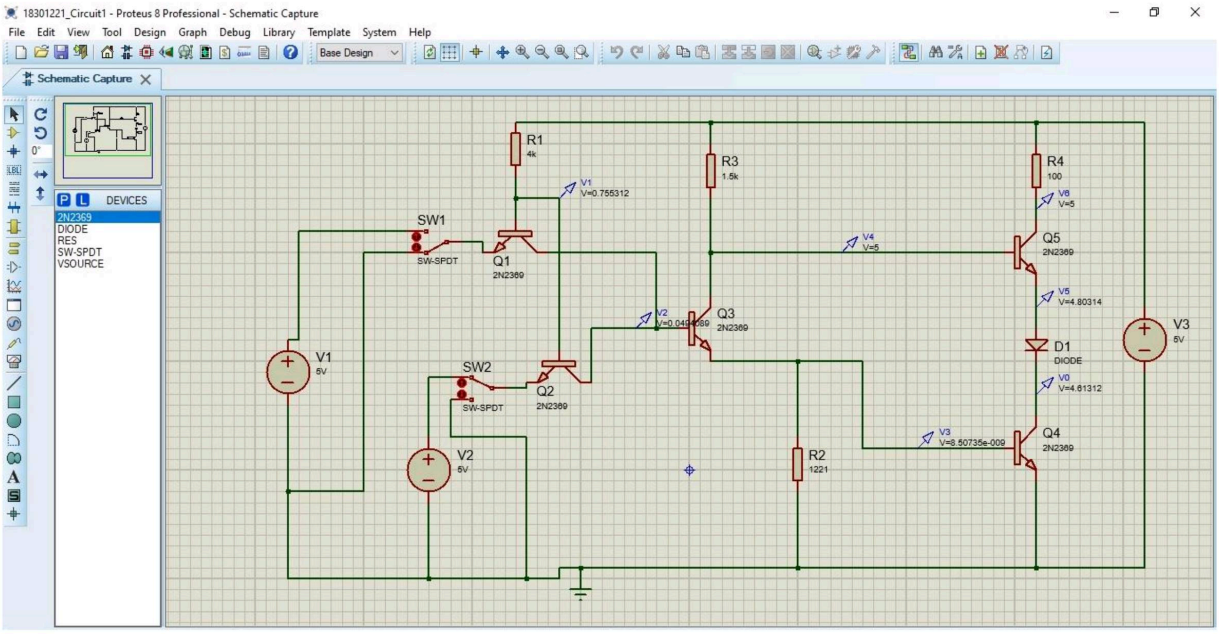
Circuit diagram of TTL-NAND gate:



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ID: 18301221
Last foure digit: 1221
$R_2 = 1221$

Input A	Input B	Input (VA)	Input (VB)	V_0	V_1	V_2	V_3	V_4	V_5	V_6
0	0	0	0	4.61312	0.71735	0.00769	$8.439e^{-9}$	5	4.80314	5
0	1	0	5	4.61312	0.75531	0.04941	$8.507e^{-9}$	5	4.80314	5
1	0	5	0	4.61312	0.75531	0.04941	$8.507e^{-9}$	5	4.80314	5
1	1	5	5	0.00948	2.66501	1.9552	1.04995	1.1423	0.576637	4.99668

Report:

1. Explain how figure 1 circuit is working as NAND gate.

In figure-1 we have two input V_A and V_B. I am describing how they working as NAND gate:

When V_A and V_B low:

When input voltage V_A and V_B are low, the current will flow through Q_1 and Q_2. As a result voltage of V_2 will be low and Q_3 and Q_4 will be in cut in mode. current will flow through R_4 and Q_5 and output voltage will be high.

When V_A low and V_B high:
At this case Q_2 will be on cut off mode. Current will flow through Q_1. As a result, the voltage will be low in V_1 and it will not be able to supply enough voltage to V_2 ~~which will~~ turn on Q_3. ~~and Q~~ so, Q_3 and Q_4 will be in cut off. Current will flow through R_4 and output of V_o will be high.

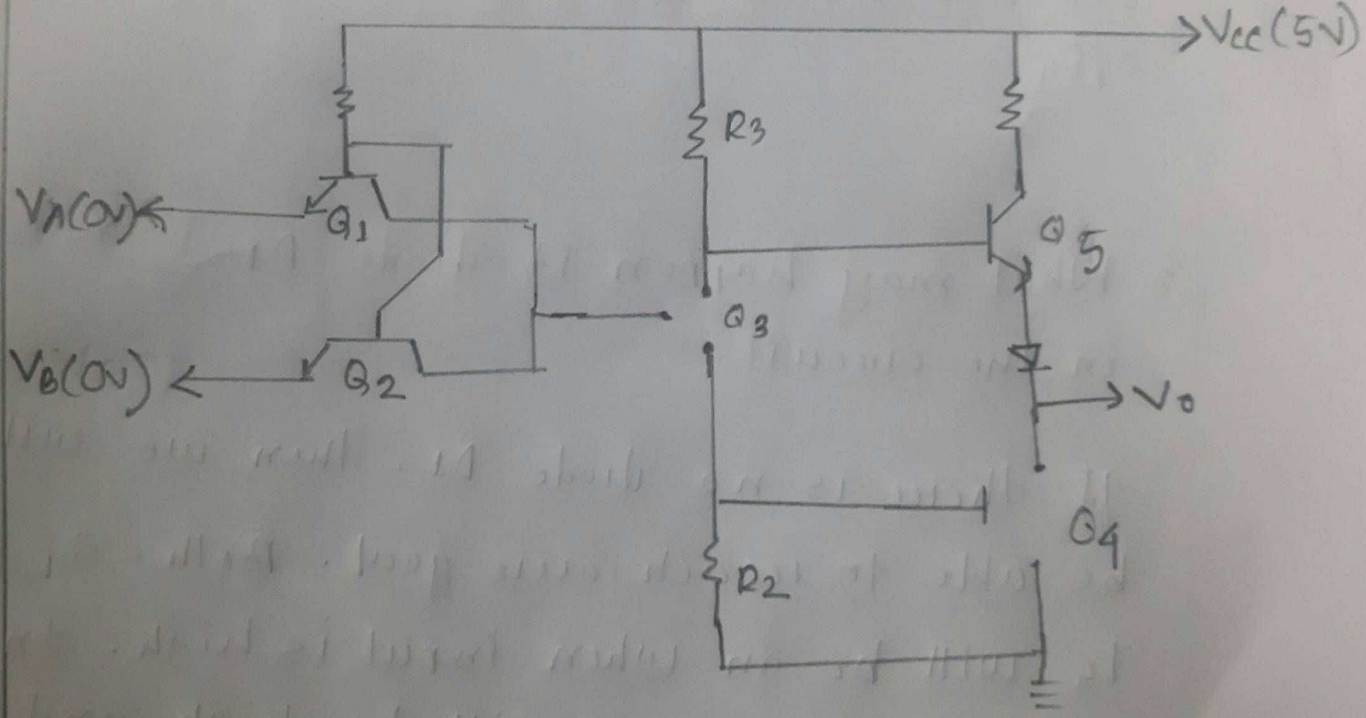
When V_A high and V_B low:
It will work same as previous step. current will flow through Q_2. V_1 will be low and Q_3, Q_4 will be in cut off mode. Current will flow through R_4 and Q_5. The output voltage will be high.

When V_A and V_B High:
In this case, Q_1 and Q_2 will be in cut off mode. As a result V_1 will be high. ~~As~~ so, it can supply enough voltage to V_2 to on Q_3. V_3 voltage will be high as well and Q_4 will be turn on. Q_5 will be in cut off mode as V_4 will not have enough voltage to turn on Q_4. So, the output voltage of V_o will be low.

From the characteristic of NAND gate we know that when all input are high, the output

is low. For all other cases, the output is high. In the above description, the same thing is happening. For this reason figure 1 is working as a NAND gate.

3. Draw the active portion of circuit when both inputs are low.



Here Q_3 and Q_4 are in cut off region and they are not active.

Q_1, Q_2 and Q_5 are on active region.

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4. What is the function of T_3?

→ Here T_3 working as a switch. It is supply complementary voltage to T_4 ~~and T_5. When~~ for it is base voltage. When, T_3 is off, the T_5 transistor will be on. On the other hand, when T_3 is on, T_4 will also on and T_5 will be off. It act as a switch. When it is on, T_4 on and T_5 off.

5. What may happen if diode D_1 is not used in the circuit?

If there is no diode D_1, then we will not be able to reach our goal. Both, Q_4 and T_5 will be on when input is high. In addition, the output will be high and it will not be in saturation mode. So, the system will not work as NAND gate and we will not be able to reach our goal.

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6. What is the mode of operation of the T_5 transistor when at least one input is low. Verify it from proteus data.

→ When at least one input is low, the T_5 transistor will be on Saturation mode. In saturation mode $V_{EE} = 0.2\ V$

Here, $V_{EE} = 5 - 4.80314$
$= 0.19686$

2. What do you understand by totem pole stage?

→ Totem pole means the addition of an active pull up the circuit in the output of the Gate which results in a reduction of propagation delay. It consits of pull up and pull down transistor along with diode registor. In this totem pole stage, it has two complimentary transistor which amplify one another.

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7. Design a TTL NOR gate with Totem Pole output stage.