ELE 404 Design Project

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Table of Contents

Introduction:

The purpose of this project is to design a circuit using BJTs or MOSFETs while maintaining the requirements given to us in the manual. This project focuses on testing inverting/non-inverting transistor amplification as well as single-stage and multistage amplifiers.

Objectives:

The objectives can be laid out in the manual

- Power Supply: +15 V relative to ground
- Total quiescent current drawn from the power supply: No larger than 8mA
- No-load voltage gain (at 1 kHz): |Avo| = 50 (± 10%)
- Maximum no-load output voltage swing (at 1 kHz): no smaller than 8 V peak to peak
- Loaded voltage gain (at 1 kHz and with RL = 1 kΩ): no smaller than 90% of the no-load voltage gain
- Maximum loaded output voltage swing (at 1 kHz and RL = 1 kΩ): no smaller than 4 V peak to peak
- Input resistance (at 1 kHz): no smaller than 50 kΩ
- Amplifier type: inverting or non-inverting
- Frequency response: 20 Hz to 50 kHz (−3dB response)
- Type of transistors: BJT
- Number of stages (transistors): no more than 3
- Resistances permitted: values smaller than 220 kΩ from the E24 series
- Capacitors permitted: 0. 1 μF, 1. 0 μF, 2. 2 μF, 4. 7 μF, 10 μF, 47 μF, 100 μF, 220 μF
- Other components (BJTs, diodes, Zener diodes, etc.): only from your ELE404 lab kit.

Additional Requirements

- The output voltage must be free from distortions (clipping etc.) under all test conditions
- The source resistance rs, must be 600 Ω under all test conditions

Design Proposal Justification:

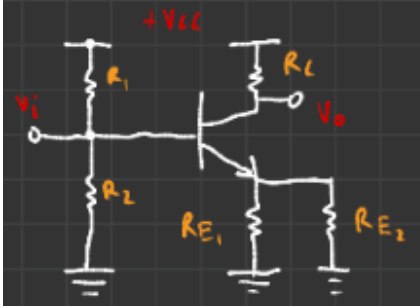
For my circuit design, I have implemented the strategy of using a Common Emitter (CE) followed by a Common Collector (CC) to achieve the requirements of the design. The reasoning behind this is due to the properties and characteristics of each. The CE design has a high voltage gain and is ideal for amplification. The CE design has a low input impedance, which might have loading effects on the preceding circuit. Though, It provides voltage gain, which is required for driving the low impedance base of the common collector stage. The CC configuration has a high input impedance, which reduces loading effects on the preceding circuit. It also provides low output impedance, making it suitable for driving capacitive or high-impedance loads. Furthermore, it provides unity voltage gain, preserving the amplifier's overall gain. In addition, starting with the CE configuration followed by the CC configuration can result in a circuit with high input impedance and high voltage gain, making it appropriate for a wide range of applications. This arrangement provides better stability because of the decoupling of the input and output stages, which reduces the risk of unwanted feedback. Furthermore, utilizing both configurations allows the circuit's behaviour to be analyzed and improved depending on the required specifications.

Calculations and analysis:

ELE 404 - Design Project

Assume: $V_{BE,ON} = 0.7V$

$V_{CE\,SAT} = 0.3\,V$



* For bias current stability, the voltage across the emmitter should be at least 3 V_{BE}

$V_{E_1} = (3)(0.7) = \boxed{2.1V}$

$V_{C_1,mid} = V_E + 0.3 = \boxed{2.4V}$

$V_C = \frac{1}{2}(V_{cc} + V_E)$

$= \frac{1}{2}(15 + 2.1 + 0.3)$

$= \boxed{8.7V}$ → max Swing

In a CE, $R_O = R_C$ → set $R_C = 47\,k\Omega$ (An assumption because of availability)

Average for V_{C_1} → $\frac{8.7 + 2.4}{2} = \boxed{5.55V}$

$I_{C_1} = \frac{15 - 5.55}{47K} = \boxed{0.201\,mA}$

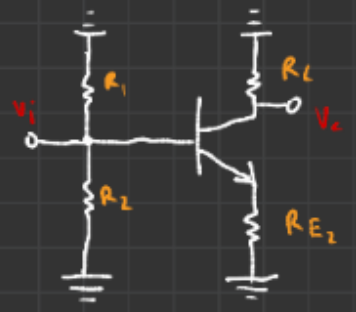
$I_{B_1} = \frac{I_C}{\beta} = \frac{0.201}{100} = \boxed{2.01\,\mu A}$

$I_{E_1} = \frac{I_{C_1}}{\alpha} = \frac{0.201}{0.99} = \boxed{0.203\,mA}$

$R_{E_1} = \frac{V_E}{I_E} = \frac{2.1}{0.203} = \boxed{10.34\,k\Omega}$

AC Analysis

Assume $R_{E_2} \ll R_{E_1}$



$g_{m_1} = \mu_0 (I_C)$

$= \mu_0 (0.201)$

$= \boxed{8.04\ ms}$

$A_{VO} = \dfrac{-g_{m_1} R_{C_1}}{1 + g_{m_1} R_{E_2}}$

$R_{E_2} = \left(\dfrac{g_{m_1} R_C}{A_{VO}} - 1\right)\left(\dfrac{1}{g_{m_1}}\right)$

$= \left(\dfrac{8.04 \times 47}{50} - 1\right)\left(\dfrac{1}{8.04}\right)$

$= \boxed{0.94\ k\Omega}$

$R_\pi = \dfrac{\beta}{g_{m_1}}$

$= \dfrac{100}{8.04}$

$= \boxed{12.44}$

$R_{i_1} = r_\pi + (\beta + 1) R_{E_2}$

$= 12.44 + (101) \times 0.94$

$= \boxed{107.38\ k\Omega}$

$V_B = V_{CC} \cdot \dfrac{R_2}{R_1 + R_2}$

$\dfrac{R_1 \cdot R_2}{R_1 + R_2} = 107.38 k\Omega$ ①

$\boxed{2.8} = 15 \cdot \dfrac{R_2}{R_1 + R_2}$

$2.1V + 0.7V$

$\boxed{0.186 = \dfrac{R_2}{R_1 + R_2}}$

Voltage division

$2.8 = 15 \cdot \dfrac{R_2}{R_1 + R_2}$

$\therefore \dfrac{R_2}{R_1 + R_2} = 0.186$ ②

$R_2 - 0.186 R_2 = 0.186$

$0.814 R_2 = 0.186 R_1$

$4.376 R_2 = R_1$

Sub ② → ①

$\dfrac{4.376 R_2^2}{5.376 R_2} = 107.38 k\Omega \Rightarrow$

$\boxed{R_2 = 132.07\ k\Omega}$

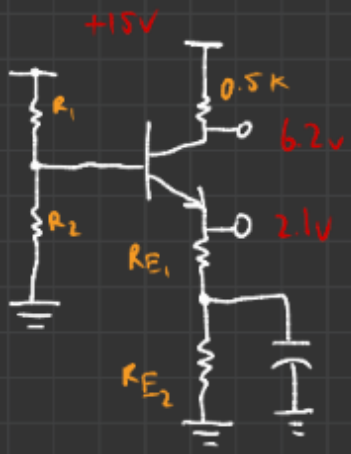
$\boxed{R_1 = 570.58\ k\Omega}$

Check for I

$I = \frac{15}{132.07 + 570.58} = 0.021\ mA$

$\therefore\ 0.021\ mA \gg 2.01\ \mu A$ So valid.

Suppose $R_O = 0.5\ k\Omega$



$I_{C_2} = \frac{15 - 8.7}{0.5} = 12.6\ mA$

$I_{E_2} = \frac{12.6}{0.99} = 12.73\ mA$

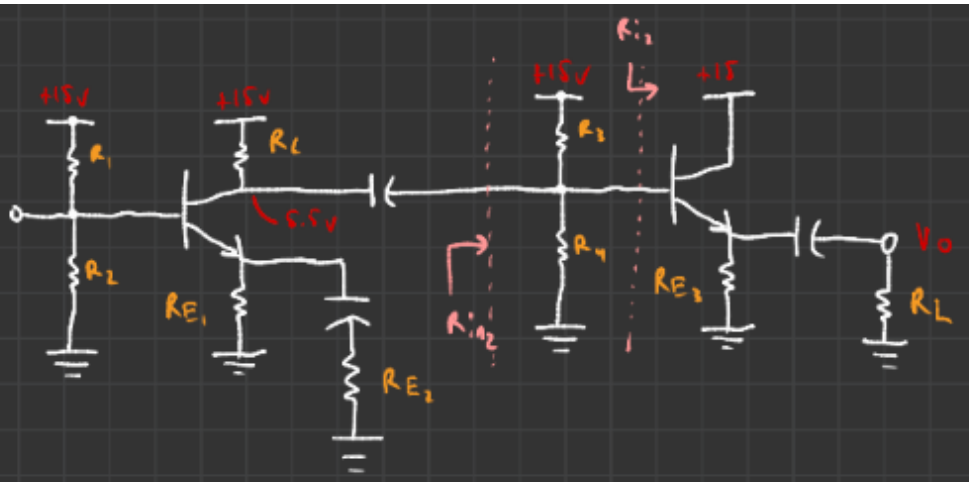
$R_{E_1} = \frac{2.1}{12.73} = 0.165\ k\Omega$

$g_{m_2} = 40 \cdot I_C = 504\ mS$

$R_{E_2} = \left(\frac{504 \cdot 10.5}{50} - 1\right)\left(\frac{1}{504}\right) = 8.02 \times 10^{-3}\ k\Omega$

$R_i = \frac{100}{504} + (101)(8.02 \times 10^{-3}) = 1.007\ k\Omega$

The value of R_i can not be greater than $1.007\ k\Omega$, as the total resistance is lower than the smallest resistance. I can not achieve the desired results, so I have to add a Common-Collector (CC).



Voltage division

$$5.5 = 15\left(\frac{R_4}{R_4+R_3}\right) \Rightarrow$$

$$\frac{R_4}{R_4+R_3} = \boxed{0.367}$$

$$R_4 - 0.367R_4 = 0.367R_3$$

$$0.633R_4 = 0.367R_3$$

$$1.725R_4 = R_3 \quad (1)$$

$5.5 - 0.7 = 4.8$

Assume: $I_{B_2} = \frac{1}{20} I_{C_1}$

$$= \frac{1}{20} \times 0.261$$

$$= \boxed{10.05\,\mu A}$$

$I_{C_2} = \beta I$

$= 1.005\,mA$

$I_{E_2} = \boxed{1.015\,mA}$

$$R_{E_3} = \frac{4.8}{1.015}$$

$$= \boxed{4.73\,k\Omega}$$

$$R_B = (R_3 // R_4) = 0.367R_3$$

$$= \frac{4.8 - (1.015)(4.73)}{10.05\,\mu A}$$

$$= 94$$

Sub from equation (1)

$$\frac{R_3R_4}{R_3+R_4} = 94$$

$$\frac{1.725R_4^2}{2.725R_4} = 94$$

$0.633 R_4 = 94$

$R_4 = 59.5 k\Omega$

$R_3 = 1.725 R_4 \times 59.5$

$R_3 = 102.64 k\Omega$

$\frac{V_{c1}}{V_i} = \frac{-g_{m_1}(R_{c_1} // R_{i_2})}{1 + g_{m_1} R_{E_2}}$

$g_{m_2} = 40 \cdot I_c$

$= 40.6 ms$

$= \frac{-8.04\left(50 // \frac{100}{40.6} + 101 \cdot 4.73\right)}{1 + 8.04 \times 0.94}$

$= \frac{-8.04\,(50 // 480.14)}{8.5576}$

$= -42.54 \, V/V$

$A_{VO} = -42.54 \times 0.995$

$= -42.32 \frac{V}{V}$

Change R_{E_2}, so it is more closer to $-50 \frac{V}{V}$

$\frac{-50}{0.995} = -50.25$

$R_{E_2} = \left(\frac{(-g_{m_1}(50 // 480.19)}{-50.25} - 1\right)\left(\frac{1}{g_{m_1}}\right) = 0.919 k\Omega$

$R_{i_1} = r\pi + (\beta + 1)\, 0.919$

$= 105.259 k\Omega$

$R_1 // R_2 // 105.23 k\Omega = 50k$

$\frac{105.23x}{105.73 + x} = 50$

$x = 95.26$

$R_1 // R_2 = 95.76$

$0.186 R_1 = 95.76 \Rightarrow \frac{R_2}{R_1+R_2} = 0.186$

$R_1 = 514.83 k\Omega$

$R_2 - 0.186 R_2 = 0.186 R_1$

$0.814 R_2 = 95.76$

$R_2 = 117.64 k\Omega$

Check I:

$I = \frac{15}{514.83 + 117.6}$

$= 0.0237 > 2.08 \mu A$

∴ Valid

Final Design

4.75kΩ ≈ 4.7K

0.919 ≈ 0.91

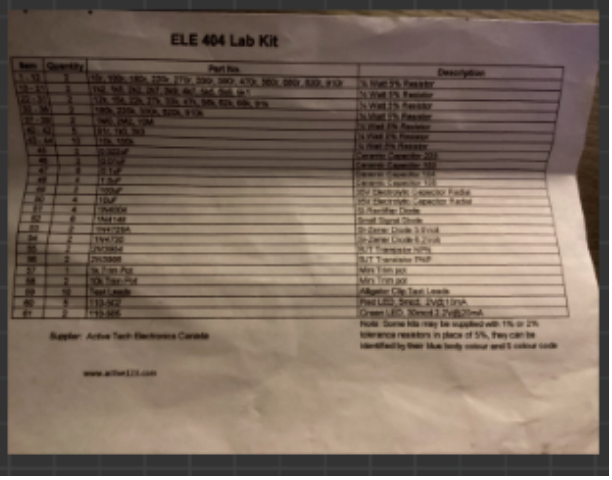
102.6 ≈ 100K

10.34 ≈ 10K

514.83 ≈ 510K

59.5 ≈ 62K

117.6 ≈ 120K



The resistor values for the circuit were solved using formulas learned in lectures and labs. The chosen(assumption) resistors were selected in accordance with the ELE 404 Lab Kit. Resistor values have been adjusted to resistor values found in the E24 manual. The capacitor values used in the circuit were chosen in accordance with similarities in circuits from labs done prior to this design project, 10uF and 100uF.

Circuit under test:

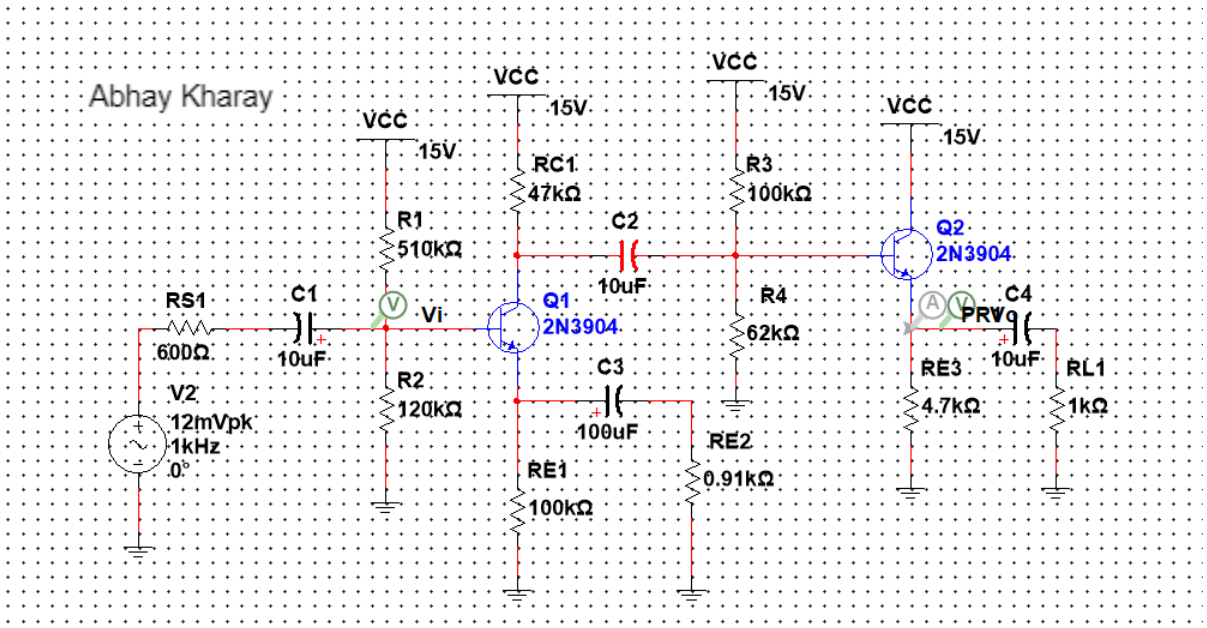


Figure 1: Proposed Circuit Design on Multisim

Experimental Results:

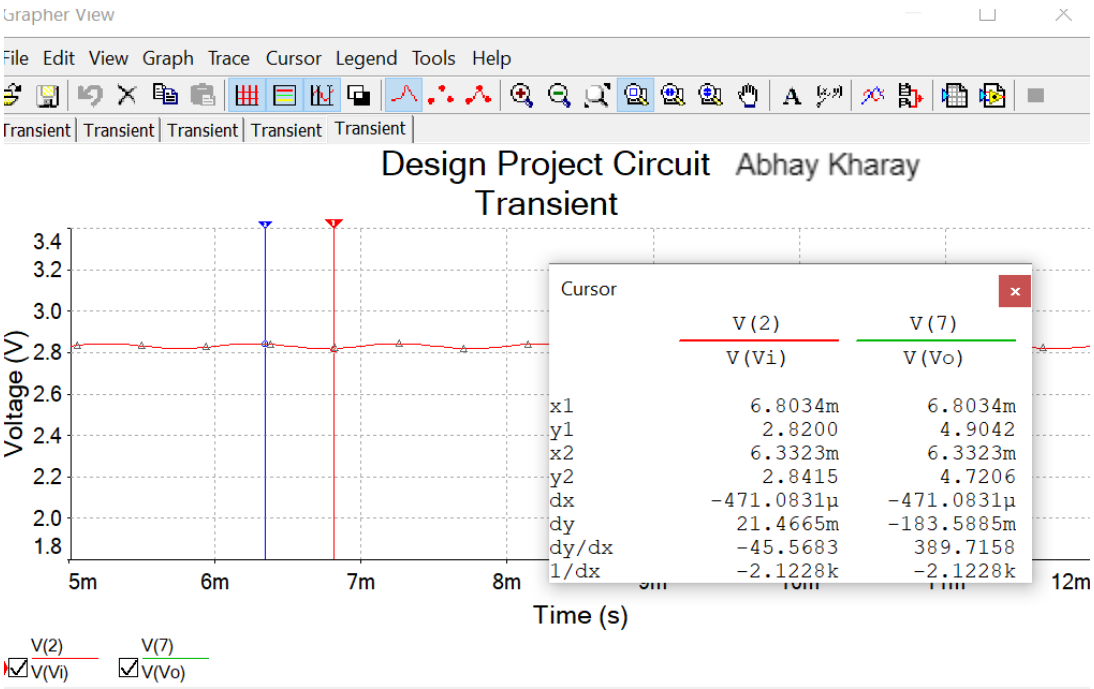


Figure 2: Vi Graph

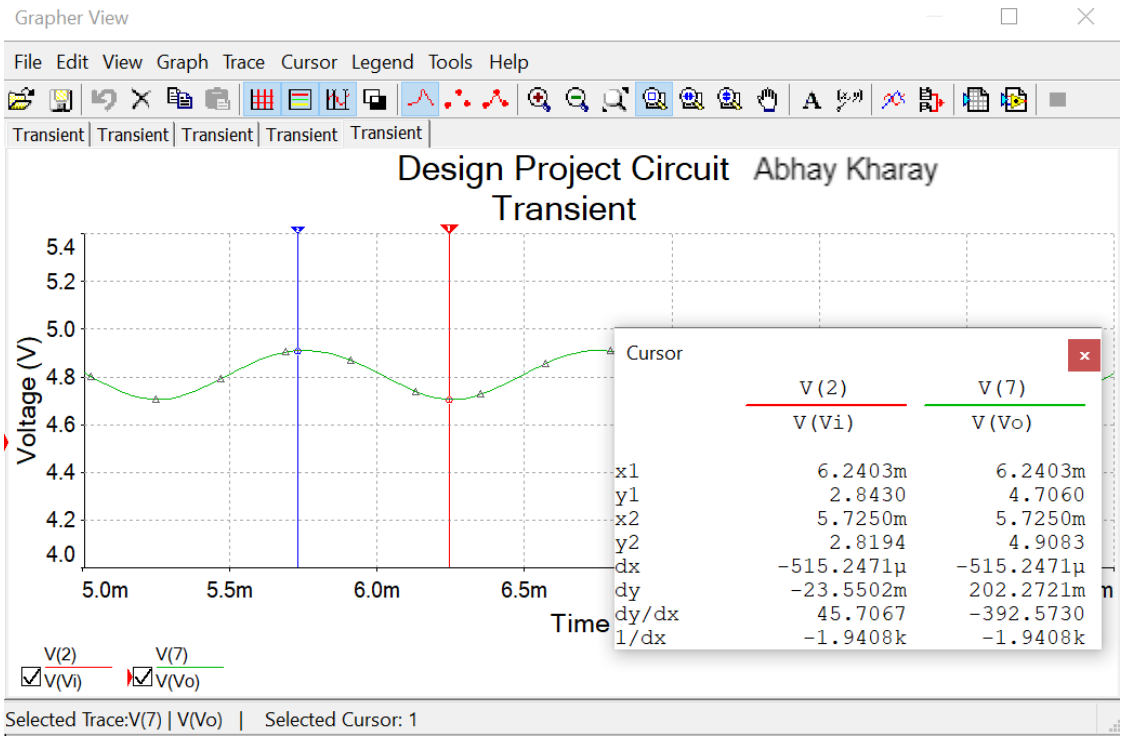


Figure 3: Loaded Vo Graph

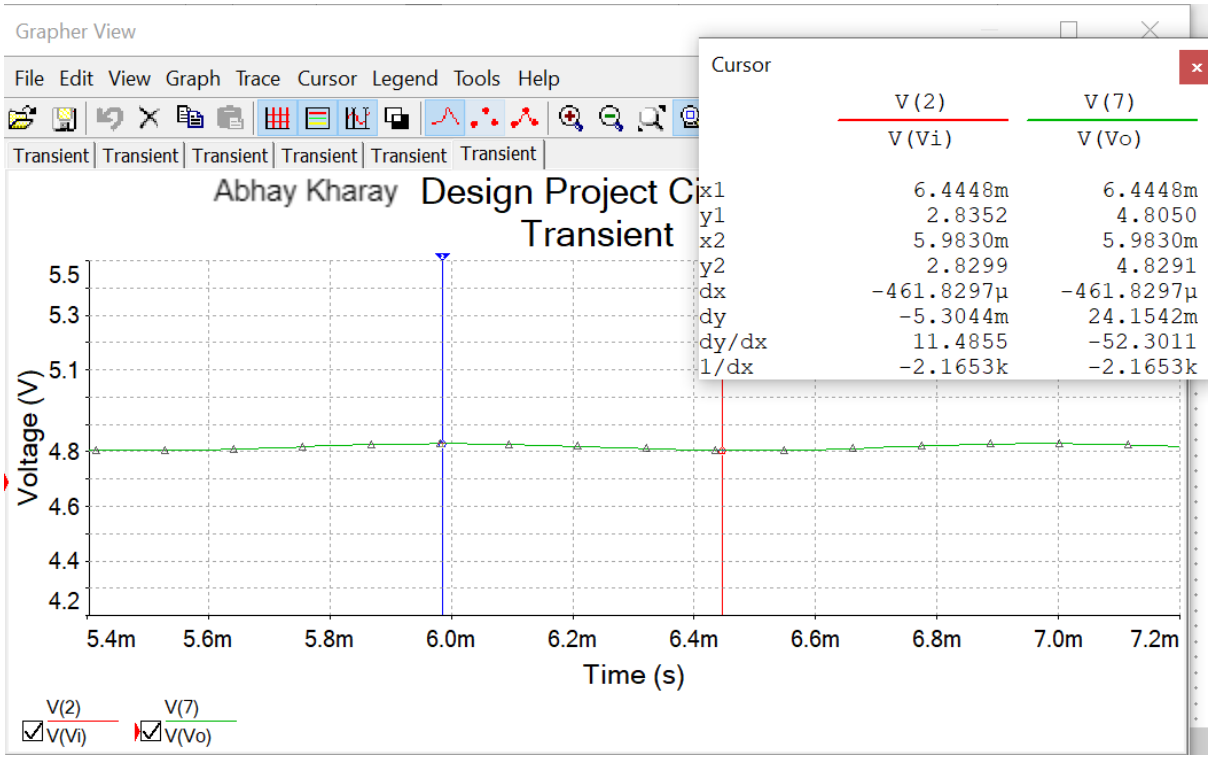
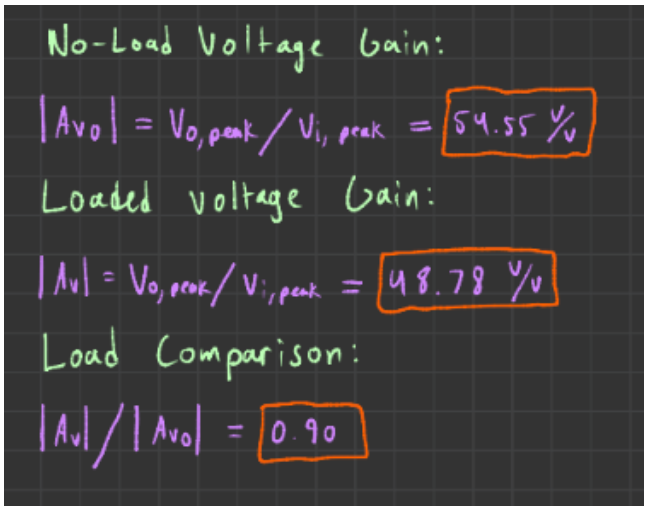


Figure 4: No-Load Vo Graph

The output voltage peak value and the voltage input peak value must be determined to compute the no-load voltage gain. This can be done by dividing the output voltage by the input voltage. The same steps need to be taken to calculate the loaded voltage gain.



There could be a 90% error meaning the numbers can be between 45 and 55, and because the values are in between them the values are valid.

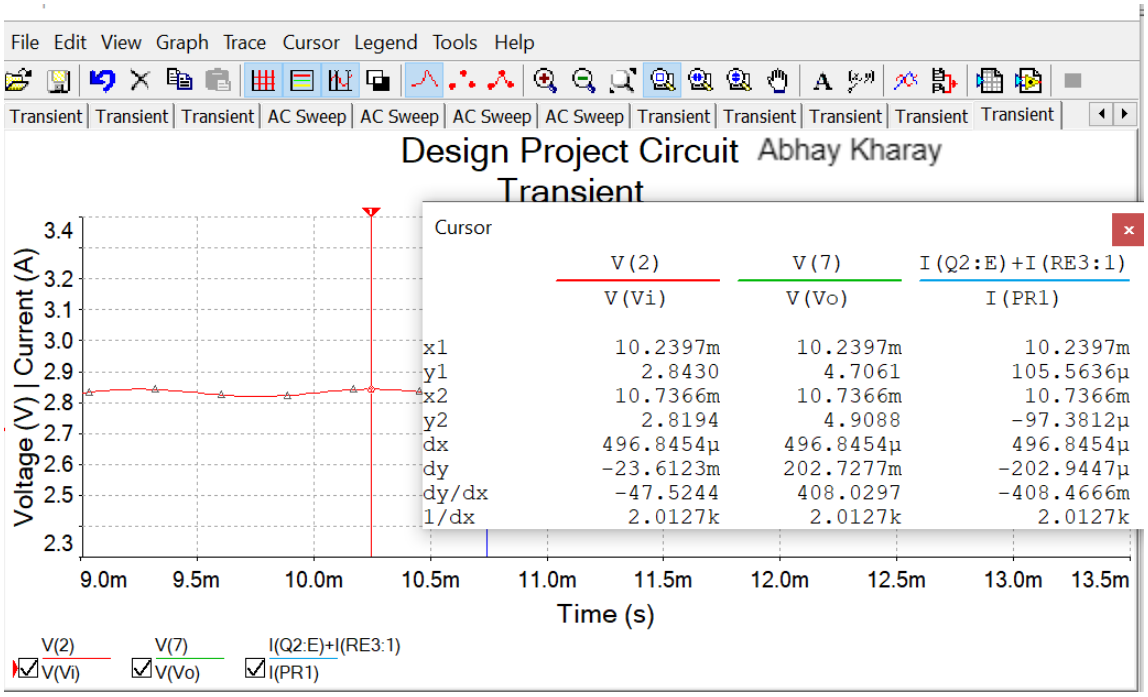


Figure 5: Quiescent Current Graph

For all the design specifications to be met, the quiescent current drawn from the power supply must not be greater than 8mA. However, when a transient ammeter is added to the circuit, amperes can be measured. As shown in the graph above A = 202.944µA or 0.203mA which is less than 8mA and therefore meets the requirements.

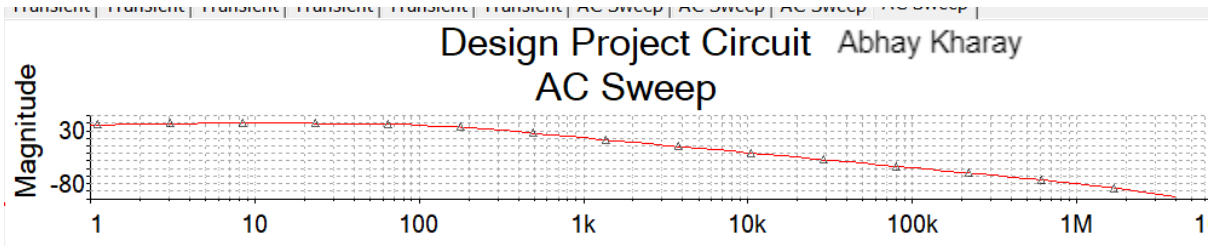


Figure 6: AC Sweep Graph

The requirement states to have a frequency response between 20k and 50k. In order to show this, AC Sweep must be utilized. This allows the examination of output voltage and current through the circuit responding to different frequencies. Therefore, the frequency is in range.

Conclusion and Remarks:

Overall, the circuit design was completed, however, there are discrepancies which include multisim values and calculated values. The reasoning behind this may be due to a change in values with regard to resistors used. The resistor values used in the design were rounded to suit the available resistances from the E24 series. Perhaps the values were changed in multisim causing differences in current and voltage in the circuit. Another reason for the undesired discrepancies may be due to human error, which includes rounding while doing calculations. Other than these two discrepancies, the circuit was built correctly and all requirements have met to satisfaction. However, the only problem is R1 resistor is greater than the limit of 220 ohms. It is laborious to find a substitute because Rin needs to be greater or equal to 50 ohms as stated in the requirements. Choosing Rc as 47 ohms is also a more logical reason due to the fact that it is a resistor value given in the E24 series. The goal was to make the most practical circuit with the components that were given. The skills and knowledge gained during this project will be necessary for future projects, serving as a firm basis for further investigation and innovation in electrical circuit design.