IEEE-SSCS Chipathon 2025 Digital Circuits Track Standard Cell Design

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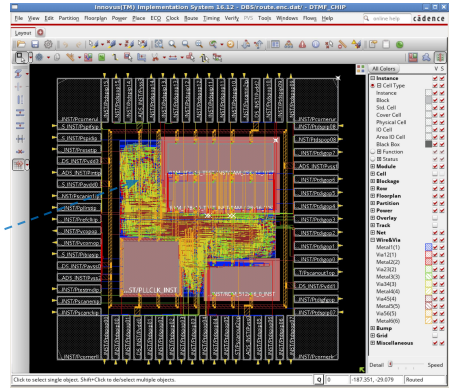
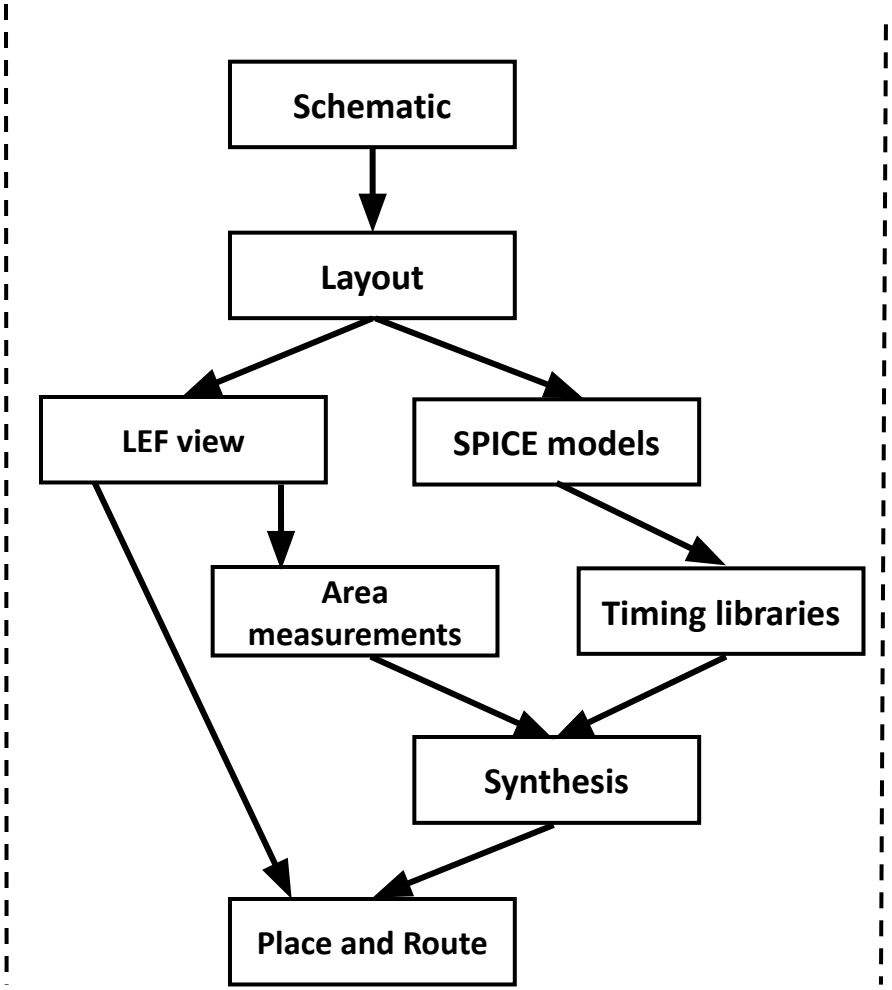
Standard Cell or SoC Design

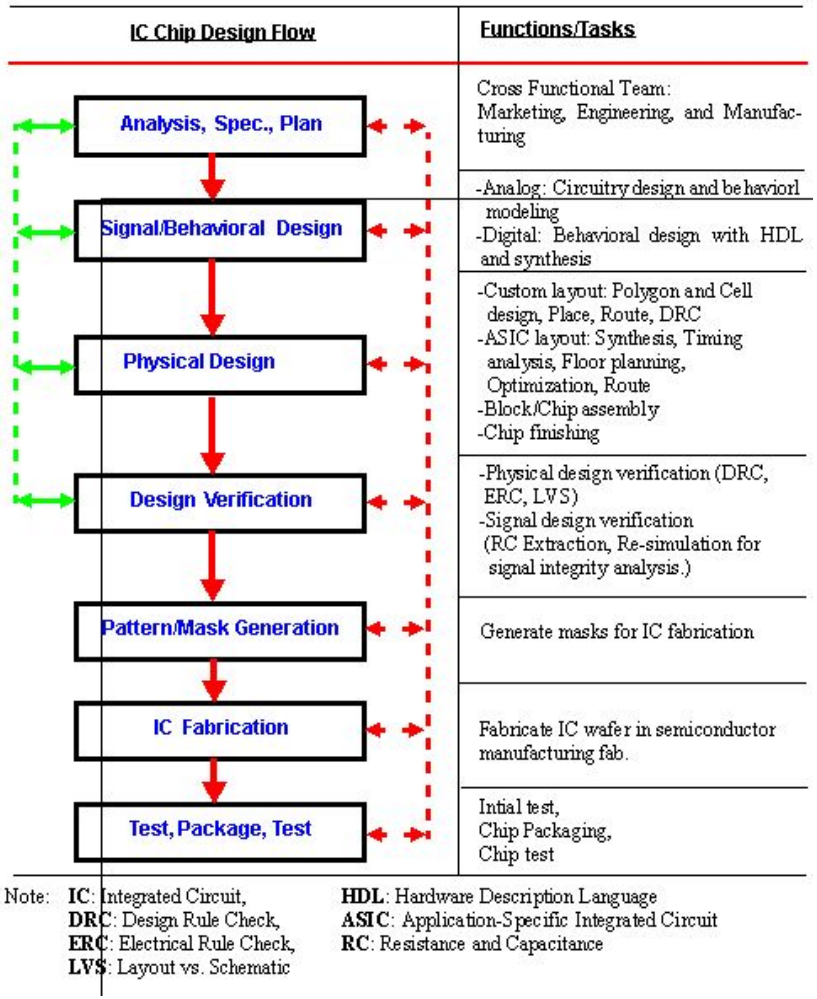
- Using pre-made layouts and stitching them together via software.
- Standard-cells are often the same height (although they do not have to be).
- This is often called Application-Specific Integrated Circuit (ASIC) or System on Chip (SoC) design as it is application oriented.
- They are designed on a grid, so that all contacts (cuts) and routes (wires) can connect through these grids.
- HDL simulation is key and like the same concept in custom-based designs!
  - Verify everything!
  - Tools are only good as much as you can test things!

standard cells



System on Chip (SoC) Design Flow





EDA Tools Used

- For this competition, the Synopsys Tool sets are planned on being utilized.
- This includes the following for standard-cell creation.
- Standard-Cell Characterization (Synopsys)
  - PrimeLib
  - NanoTime
  - Hspice
- Layout
  - Magic
- Schematic
  - Xschem
- Validation of Layout
  - Netgen (LVS), ngspice (simulation)
- Synthesis
  - Design Compiler (Synopsys) or Yosys
- Place & Route
  - Fusion Compiler (Synopsys) and/or ICC2
  - OpenROAD (flow scripts or openlane)

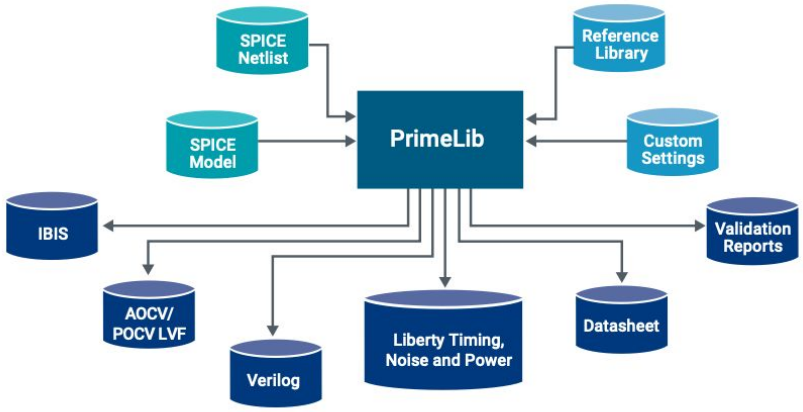
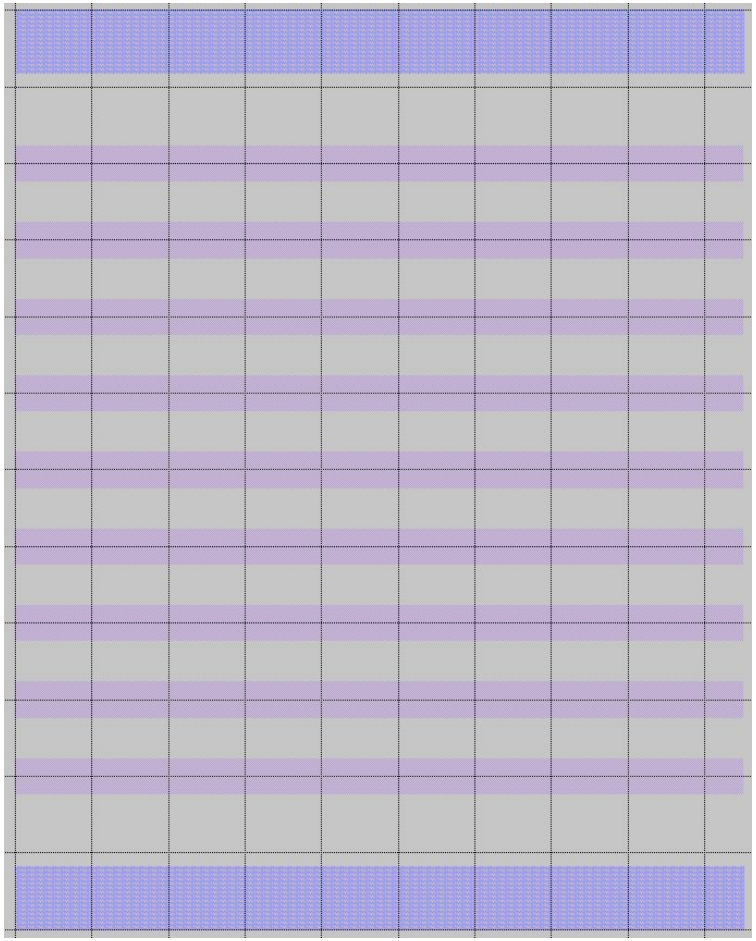


Figure 2: PrimeLib input and outputs

[Synopsys]

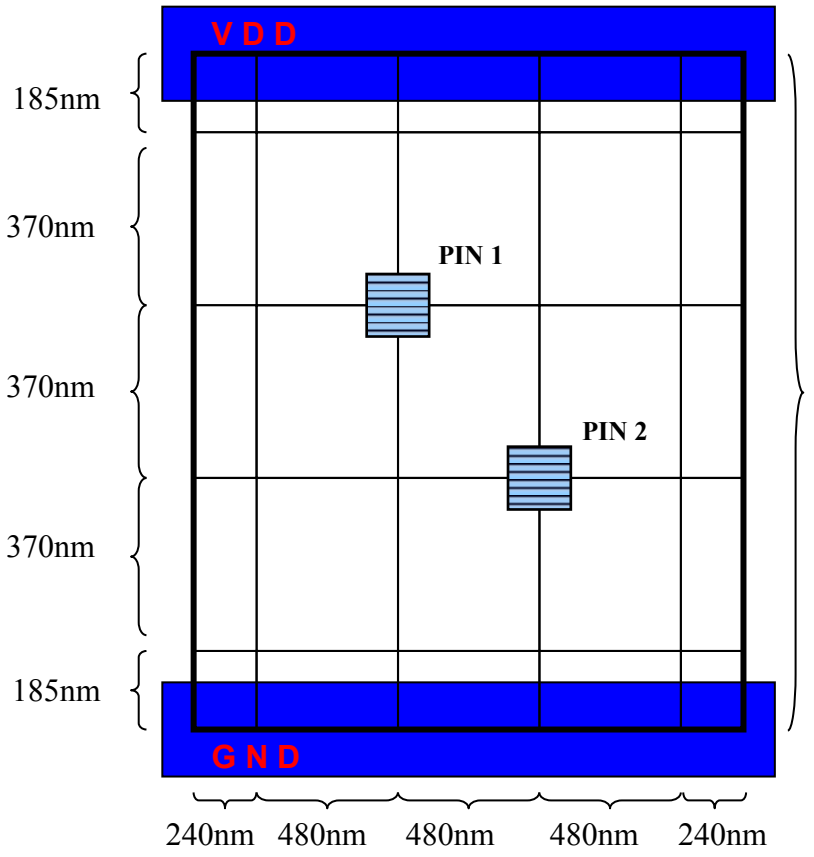
Selecting Standard Cell Tracks

- An example of a 12-track setup can be seen to the right.
  - Note that although being 12 tracks tall, the cell can only accommodate 9 routed wires
  - Power rails take space on these tracks as well.
  - Tracks will vary by library vendor and are typically 12T, 9T, and 7T.
- Cells of different heights provide a simple solution for trading off speed vs area.
  - But they cannot typically be mixed within the same design!
  - Cell height is measured in terms of routing tracks of the lowest non-interconnect metal layer.
  - A track is the smallest section of space that can accommodate a drawn wire.



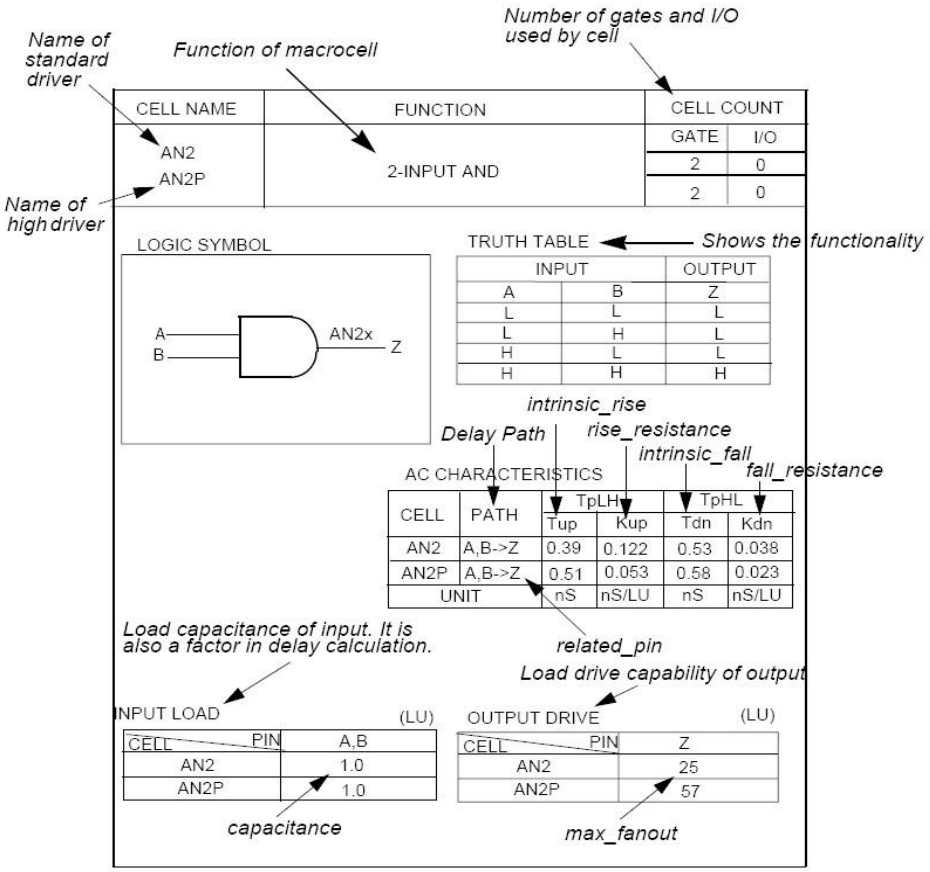
Layout Creation and Routing Grid

- Pins should placed on the grid (reduce routing efforts).
- Staggered if possible (reachable by both horizontal and vertical layers).
- Power signals routed through abutment (increase density).



Power rails designed to allow abutment.

Logic Gate Datasheet/.lib View



- Correlation between datasheet and Liberty File (.lib) representation of a 2 input AND gate
- Libraries are “characterized” to obtain their respective gate characterics by a library characterizer (e.g., PrimeLib)

```
pin(A,B) {
  direction : input ;
  capacitance : 1 ;
}
pin(Z) {
  direction : output ;
  function : "A * B" ;
  timing() {
    intrinsic_rise : 0.39 ;
    intrinsic_fall : 0.53 ;
    rise_resistance : 0.122 ;
    fall_resistance : 0.038 ;
    related_pin : "A B" ;
```