Experiment: 1
Study of voltage multiplier using clamper and peak detector circuit

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***Abstract*—This report presents the study and implementation of voltage multipliers using clamper and peak detector circuits.Also, First we implement the clamper and peak detector circuits alone then we approach towards the implementation of voltage doubler & quadruple. The results obtained in the form of CSV file are then plotted using MATLAB. The results obtained from practical implementation are compared with theoretical expectations.**

I. Components Required

- Diode – IN4007
- Signal generator
- Capacitor 10uF
- Breadboard, wires, CRO, and multimeter for testing

II. Theory

A. Clamper Theory

A clamper is a circuit that ”clamps” a signal to a different DC level without changing the appearance of the applied signal. The different types of clampers are positive, negative, and biased clampers. A clamping network must have at least a capacitor and a diode.

B. Peak Detector

Peak detector circuits determine the peak (maximum) value of an input signal. It stores the peak value of input voltages for an infinite duration until reset. The peak detector circuit follows the highest value of an input signal and stores it.

C. Voltage Multiplier

Voltage multiplier circuits are used to generate a higher DC voltage from an AC input without a transformer. They achieve this by using a network of diodes and capacitors to rectify and store charge, progressively increasing the output voltage in stages.

III. Results

A. Clamper Circuit

- Implemented clamper circuit for an input voltage of 5Vpp.
- Positive clamper circuit:

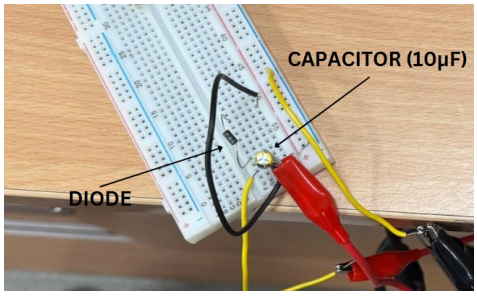

Fig. 1. Positive Clamper Circuit

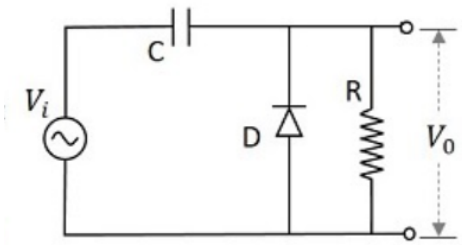

Fig. 2. Positive Clamper Circuit Diagram

- During the **positive half cycle** of the AC input, the diode becomes **reverse-biased** because the n-side is connected to the more positive side, and the p-side is connected to the negative side/ground , As you can see in the circuit diagram.
- As a result, the diode does not conduct, and the capacitor charges through the input voltage to the peak value of the input.
- Since the diode blocks the current, the output voltage V_{OUT} is equal to the input voltage during this half-cycle
- During the **negative half cycle**, the diode becomes **forward-biased**, allowing current to flow through it.
- The capacitor, which was charged during the positive half cycle, now acts as a voltage source and shifts the input waveform upwards.
- This results in the entire waveform being **clamped** to a positive voltage level, effectively raising the baseline of the AC signal, As you can see in the graph below the baseline is changed from 0 to 2(because capacitor was charged upto peak voltage).

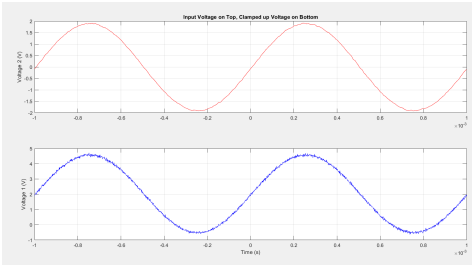

Fig. 3. Positive Clamper Circuit Graph

- Negative clamper circuit:

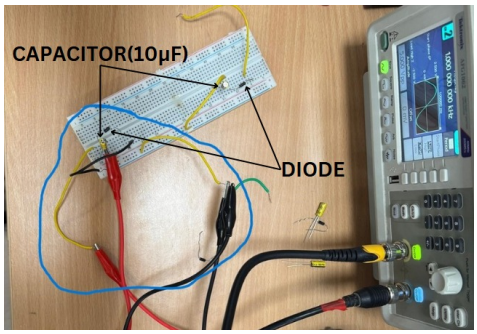

Fig. 4. Negative Clamper Circuit

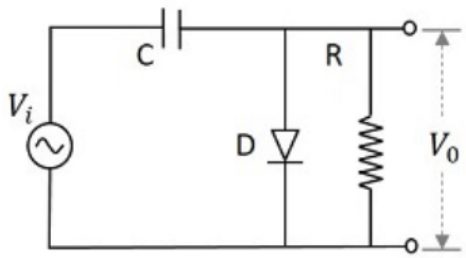

Fig. 5. Negative Clamper Circuit Diagram

- During the **positive half cycle**, the diode is **forward-biased** because the p-side is at more positive voltage, while the n-side is connected to negative side/ground.
- The diode conducts, allowing the capacitor to charge to the peak input voltage but with reversed polarity compared to the positive clamper.
- The output voltage during this cycle is clamped near zero since the diode bypasses the input to ground.
- During the **negative half cycle**, the diode becomes **reverse-biased** and stops conducting.
- The charged capacitor now adds its voltage to the input signal, effectively shifting the entire waveform downward.
- This results in the waveform being **clamped** to a negative voltage level, lowering the baseline of the AC signal,As you can see in the graph below the baseline is changed from 0 to -2(because capacitor was charged upto peak voltage) .

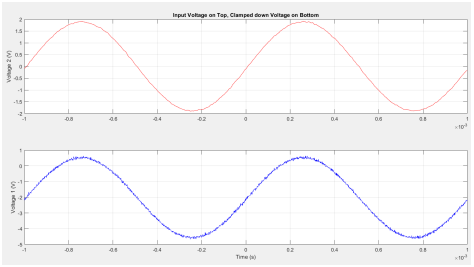

Fig. 6. Negative Clamper Circuit Graph

B. Peak Detector Circuit

- Implemented a Peak Detector Circuit for an input voltage of 5Vpp.
- Positive Peak Detector Circuit:

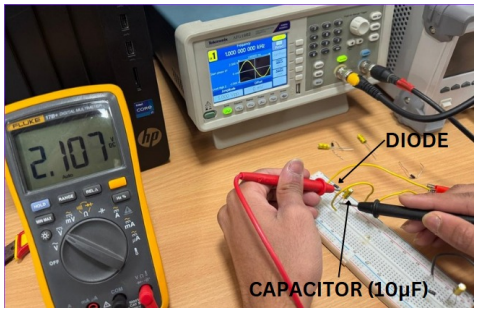

Fig. 7. Positive Peak Detector Circuit

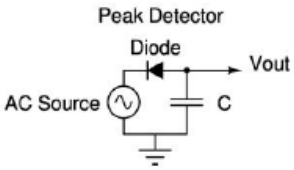

Fig. 8. Positive Peak Detector circuit diagram

- During the **positive half cycle** of the AC input, the diode becomes **forward-biased** as the p-side is at a higher potential than the n-side.
- The diode conducts, allowing the capacitor C to charge up to the peak value of the input voltage minus the diode's forward voltage drop ($V_{\text{peak}} - V_D$).
- Once the capacitor is charged to the peak value, the diode becomes **reverse-biased** as the input voltage starts to decrease below the capacitor's voltage.
- The capacitor holds the peak voltage, and the output voltage V_{OUT} remains at the peak value since the diode prevents the capacitor from discharging back into the source.
- Key Point:

- $V_{OUT} \approx V_{peak} - V_D$, where V_D is the forward voltage drop of the diode.
- Assuming an ideal diode, $V_D = 0$, so $V_{OUT} = V_{peak}$.

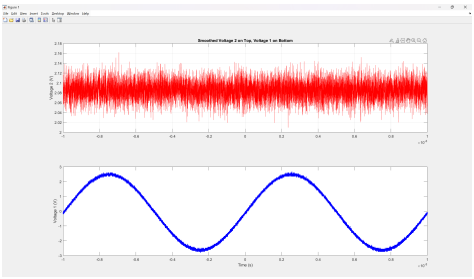

Fig. 9. Positive Peak Detector Graph

- Negative Peak Detector Circuit:

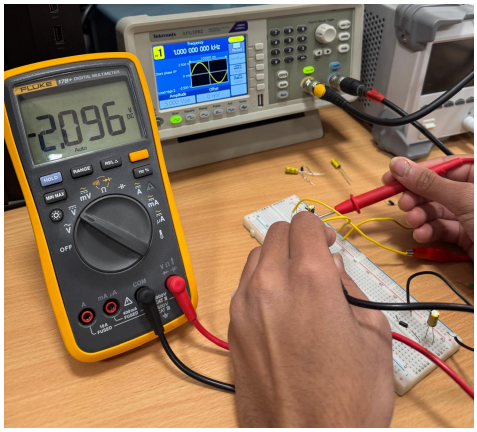

Fig. 10. Negative Peak Detector Circuit

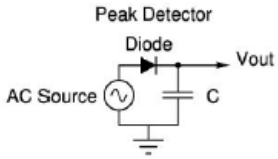

Fig. 11. Negative Peak Detector Circuit Diagram

- During the **negative half cycle** of the AC input, the diode becomes **forward-biased** as the cathode is at a lower potential than the anode.
- The diode conducts, and the capacitor C charges to the negative peak value of the input voltage ($V_{peak}^{-} + V_D$).
- As the input voltage starts rising back toward zero, the diode becomes **reverse-biased**, preventing the capacitor from discharging.
- The capacitor holds the most negative peak, and the output voltage V_{OUT} stays at that value.
- Key Point:
- $V_{OUT} \approx V_{peak}^{-} + V_D$, where V_D is the diode's forward voltage drop.
- For an ideal diode, $V_D = 0$, resulting in $V_{OUT} = V_{peak}^{-}$.

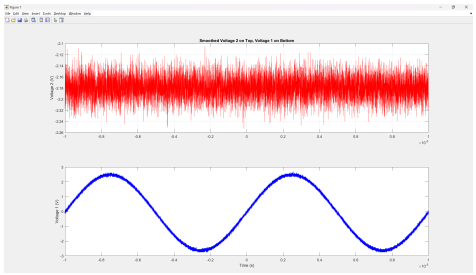

Fig. 12. Negative Peak Detector Graph

C. Voltage Doubler Circuit

- Implemented a voltage Doubler Circuit for an input voltage of 4Vpp.

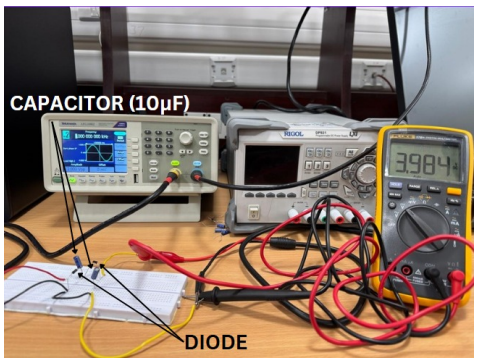

Fig. 13. Voltage Doubler Circuit

- As you can see we gave 4Vpp(peak is 2V) so by implementing the voltage doubler circuit we got output voltage double to the input voltage i.e 4V(approx)

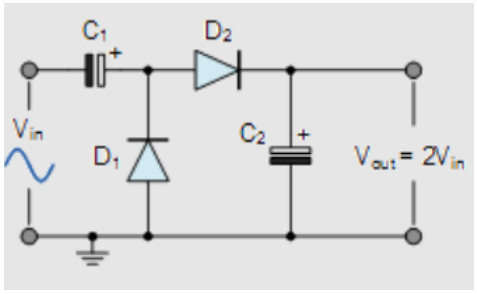

Fig. 14. Voltage Doubler Circuit Diagram

- The voltage doubler circuit uses two diodes and two capacitors to double the peak voltage of the AC input.
- During the **negative half cycle** of the AC input:
  - The first diode becomes **forward-biased**, charging the first capacitor C_1 to the peak input voltage V_{peak}.
- During the **positive half cycle**:
  - The second diode becomes **forward-biased**, and the second capacitor C_2 charges using the voltage from the AC source and C_1, effectively doubling the voltage.
- The output voltage V_{OUT} across C_2 becomes approximately $2V_{peak}$ (neglecting diode drops), As you can see in the graph below we get a straight line at 4V(approximately, since diode is not ideal).

- Key Point:
  - $V_{OUT} \approx 2V_{peak}$ in an ideal case.
  - The circuit is commonly used in applications requiring higher DC voltages from lower AC sources.

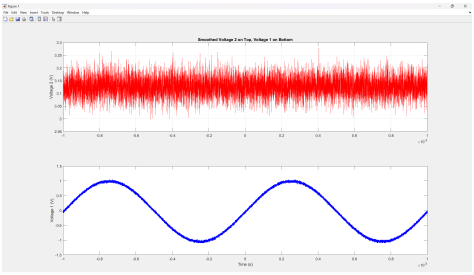

Fig. 15. Voltage Doubler Graph

D. Voltage Quadruple

- Implemented a voltage Quadruple Circuit for an input voltage of 5Vpp.

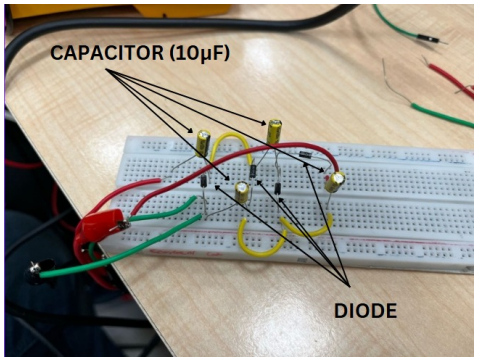

Fig. 16. Voltage Quadruple Circuit

- As you can see we gave 5Vpp(peak is 2.5V) so by implementing the voltage quadruple circuit we got output voltage four times to the input voltage i.e 10V(approx)

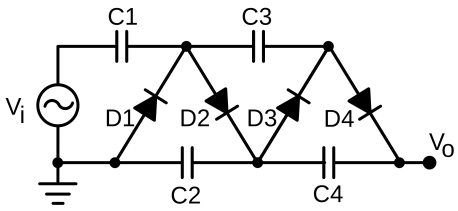

Fig. 17. Voltage Quadruple Circuit Diagram

- The voltage quadrupler extends the voltage doubler principle by using four diodes and four capacitors.
- During alternate half cycles:
  - Capacitors charge sequentially, each adding V_{peak} to the total output.
  - The diodes direct the current in such a way that each capacitor adds its voltage to the next stage.
- The final output voltage V_{OUT} across the last capacitor is approximately $4V_{peak}$, As you can see in the graph below we get a straight line at 10V(approximately, since diode is not ideal).

- Key Point:
  - $V_{OUT} \approx 4V_{peak}$ in an ideal case.
  - Voltage quadruplers are used in applications that require high DC voltages without using a transformer.

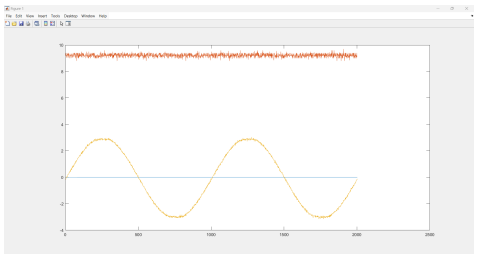

Fig. 18. Voltage Quadruple Graph

IV. Discussion

- A voltage drop is observed in the peak detector and voltage multiplier circuits, which deviates from theoretical expectations.
- The key reasons for this voltage drop include:
  - **Diode Forward Voltage Drop**: The silicon diodes used (such as 1N4007) have a forward voltage drop (0.7V), which accumulates over multiple stages.
  - **Capacitor Leakage and ESR**: Non-ideal capacitors exhibit leakage current and Equivalent Series Resistance (ESR), leading to charge loss and reduced voltage storage.
  - **Load Resistance Effects**: The presence of the multimeter or other connected loads can drain charge from the circuit, resulting in a lower measured voltage.
  - **Frequency Dependence**: At improper input signal frequencies, capacitors may not fully charge or discharge, reducing peak output voltage.
  - **Parasitic Effects**: Wire resistance, PCB trace inductance, and stray capacitance contribute to energy loss in the circuit.
  - **Temperature Variation**: The forward voltage drop of diodes decreases with temperature (2mV/°C), causing slight variations in output voltage.
  - **Measurement Errors**: Multimeter impedance and oscilloscope probe characteristics can introduce minor inaccuracies in the observed voltage values.

V. Conclusion

The implementation of voltage multipliers using clamper and peak detector circuits was successfully carried out, and the results were observed to be in agreement with theoretical expectations, with some minor deviations due to practical circuit limitations.

VI. References

1) Fundamentals of Microelectronics by Behzad Razavi
2) Microelectronic circuits by Adel Sedra and Kenneth Smith