GROUP_14_Experiment: 4
Design and Characterization of Common Emitter Amplifier

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***Abstract*—This paper presents the design methodology and characterization of a common emitter amplifier using a BC547B transistor with $V_{CC} = 12V$, $I_C = 1mA$, and a target voltage gain of 100.**

***Index Terms*—BJT, Common-Emitter, Amplifier, Small-Signal Model, Large-Signal Model, Current Gain**

I. Apparatus Required

- **BC547B NPN Transistor:**
  - Description: General-purpose NPN bipolar junction transistor (BJT) in a TO-92 package with 3-pin configuration (Collector, Base, Emitter).
  - Specifications: See Table I for detailed electrical characteristics [5].

Parameter	Value
Current gain (β)	110–800 (typical ≈ 100)
Collector current (I_C)	100 mA maximum
Collector-emitter voltage (V_{CE})	45V maximum
Emitter-base voltage (V_{EB})	6V maximum
Collector-base voltage (V_{CB})	50V maximum
Power dissipation	500 mW maximum
Transition frequency (f_T)	300 MHz
Operating temperature	-65°C to +150°C
Noise figure	Low
Applications	Switching, amplification

TABLE I: BC547B NPN Transistor Specifications.

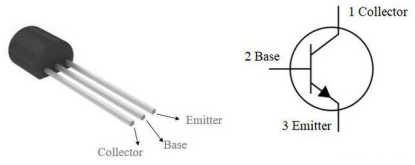

Fig. 1: BC547B NPN Transistor Pinout (TO-92 Package).

- **Resistors:**
  - 6kΩ.
  - 1.2kΩ.
  - 100kΩ.
  - 22kΩ.
  - 2.2kΩ.
- **Capacitors:**
  - 10μF.
  - 3.3μF.
  - 22μF.
- **Power Supply:** Keithley 2231A-30-3 (triple output, 30V/3A).
- **Function Generator:** Tektronix AFG1062 (60 MHz, 2-channel) for input waveforms.
- **DSO with Waveform Generator:** Keysight DSOX1102G (100 MHz, 1 GSa/s) for waveform analysis.
- **Digital Multimeter (DMM):** Agilent 34401A ($6\frac{1}{2}$ digit resolution) for DC measurements.
- **Breadboard and Connectors:** For circuit prototyping.

II. Introduction

The **Bipolar Junction Transistor (BJT)** is a three-terminal semiconductor device that operates as a current-controlled current source [1]. It consists of three doped semiconductor regions: the **Emitter (E)**, **Base (B)**, and **Collector (C)**. BJTs are classified into two types: **NPN** and **PNP**, depending on the doping arrangement.

A. BJT as a Controlled Source

A BJT functions as a **current-controlled current source (CCCS)** because the collector current (I_C) is controlled by the base current (I_B) [2]. The relationship is:

$$I_C = \beta I_B \tag{1}$$

where β (or h_{FE}) is the **current gain**.

B. Key Terminologies

- **Current Gain (β or h_{FE})**: Ratio of collector current to base current [1].
- **Transconductance (g_m)**: Change in collector current per change in base-emitter voltage [2].
- **Early Effect**: Variation in collector current due to collector-emitter voltage.
- **Biasing**: Setting DC operating point for proper amplification [1].

- **Cutoff/Saturation/Active Regions**: Operating modes of BJT [2].

C. BJT Symbol and Terminals

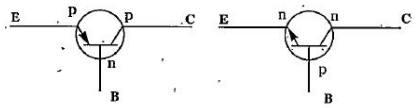

Fig. 2: Standard circuit symbols for (a) PNP and (b) NPN BJTs [1].

The BJT is represented in circuit diagrams with the following symbols:

- **NPN BJT**: Arrow on emitter points outward from base
- **PNP BJT**: Arrow on emitter points inward toward base [2]

All variants show three terminals: emitter (with arrow), base, and collector.

D. Input and Output Impedance

- **Input Impedance** (Z_{in}): Typically 1kΩ to 5kΩ (CE configuration) [1].
- **Output Impedance** (Z_{out}): Typically 10kΩ to 100kΩ [2].

E. BJT Small-Signal Model

Used for AC analysis, linearizing the BJT around its Q-point [1]. The **hybrid-π model** includes:

- r_π: Base-emitter resistance ($r_\pi = \frac{V_T}{I_B}$) [2]
- g_m: Transconductance ($g_m = \frac{I_C}{V_T}$)
- r_o: Output resistance due to Early Effect ($r_o = \frac{V_A}{I_C}$) [1]

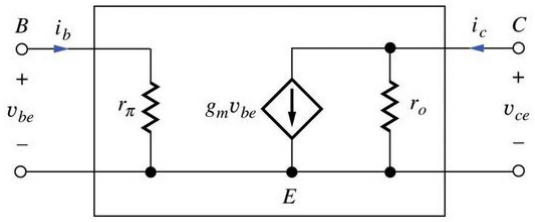

Fig. 3: Hybrid-π small-signal model of BJT [2].

F. Functionalities of BJT

Bipolar Junction Transistors serve multiple essential functions in electronic circuits [1]:

1) Amplification

- Voltage/current/power amplification in analog circuits
- Used in audio amplifiers, RF circuits, and signal conditioning
- Provides gain through controlled current flow

2) Switching

- Digital logic applications (TTL circuits)
- High-speed switching in power electronics
- Acts as electronically controlled switch (cutoff/saturation modes)

3) Impedance Matching

- Interface between high and low impedance circuits
- Buffer amplifiers (emitter follower configuration)

III. Detailed Analysis of CE Amplifier

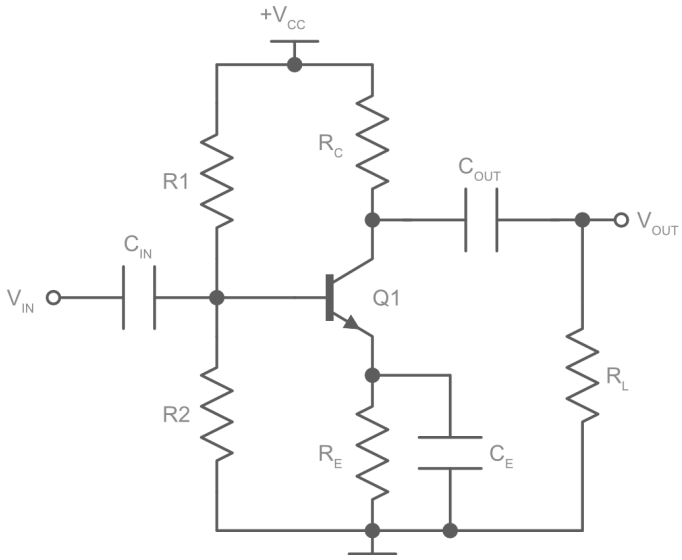

Fig. 4: Common-Emitter amplifier circuit configuration [1]. The circuit shows typical biasing arrangement with R_1 and R_2 forming the voltage divider network, R_C as collector resistor, and R_E as emitter resistor with bypass capacitor C_E. Input is applied through coupling capacitor C_{in} and output is taken through C_{out}.

The Common-Emitter configuration provides both voltage and current gain, making it the most versatile amplifier configuration [2]. Key features visible in Fig. 4 include:

- **Voltage divider bias**: Provides stable operating point (R_1, R_2)
- **Bypass capacitor** (C_E): Short-circuits R_E at signal frequencies
- **Coupling capacitors** (C_{in}, C_{out}): Block DC while passing AC signals

The circuit demonstrates the standard implementation where:

- Input signal is applied to the base terminal
- Output is taken from the collector terminal
- Emitter is common to both input and output (grounded for AC signals)

1) DC Biasing Requirements

- Voltage divider bias provides stability against β variations
- Q-point should be in active region for linear amplification
- V_{CE} typically set to $V_{CC}/2$ for maximum swing

2) AC Analysis Parameters

The small-signal performance can be characterized by:

$$A_v = \frac{v_{out}}{v_{in}} = -g_m(R_C \parallel r_o \parallel R_L) \tag{2}$$

$$R_{in} = R_1 \parallel R_2 \parallel r_\pi \tag{3}$$

$$R_{out} = R_C \parallel r_o \tag{4}$$

Where:

- g_m = transconductance ($\frac{I_C}{V_T}$)
- $r_\pi = \frac{\beta}{g_m}$
- r_o = Early voltage effect resistance

3) Frequency Response

The CE amplifier exhibits:

- Low-frequency roll-off due to coupling/bypass capacitors
- High-frequency limitations from:
  - Miller capacitance effect
  - Junction capacitances (C_π, C_μ)
- Bandwidth product determined by f_T of transistor

IV. Design Calculations for CE Amplifier

A. DC Biasing Design (Exact Calculations)

Given specifications:

$$\begin{aligned} V_{CC} &= 12\,V \\ I_C &= 1\,mA \\ \beta &= 100 \\ A_v &= 100 \\ V_{BE} &= 0.7\,V \end{aligned}$$

1. **Emitter Resistor** (R_E):

$$\begin{aligned} V_{RE} &= 0.1V_{CC} = 1.2\,V \\ R_E &= \frac{V_{RE}}{I_E} = \frac{1.2\,V}{1\,mA} = 1.2\,k\Omega \quad \text{(exact)} \end{aligned}$$

2. **Collector Resistor** (R_C):

$$\begin{aligned} V_{CE} &= 0.5V_{CC} = 6\,V \\ V_{RC} &= V_{CC} - V_{CE} - V_{RE} = 4.8\,V \\ R_C &= \frac{V_{RC}}{I_C} = \frac{4.8\,V}{1\,mA} = 4.8\,k\Omega \quad \text{(exact)} \end{aligned}$$

3. **Base Divider Network**:

$$\begin{aligned} V_B &= V_{RE} + V_{BE} = 1.9\,V \\ I_B &= \frac{I_C}{\beta} = 10\,\mu A \\ I_2 &= 10I_B = 100\,\mu A \\ R_2 &= \frac{V_B}{I_2} = 19\,k\Omega \quad \text{(exact)} \\ R_1 &= \frac{V_{CC} - V_B}{I_2 + I_B} = \frac{10.1\,V}{110\,\mu A} = 91.818\,k\Omega \quad \text{(exact)} \end{aligned}$$

Standard value selected: $22\,k\Omega$ and $100\,k\Omega$

B. AC Design with Exact Values

1. **Load Resistor** (R_L) **Design:** Using the gain equation from the reference image:

$$\begin{aligned} A_v &= -\frac{r_c}{r_e} = -100 \\ r_e &= \frac{25\,mV}{I_C} = 25\,\Omega \\ r_c &= R_C \parallel R_L = 100 \times r_e = 2.5\,k\Omega \\ \frac{1}{R_C} + \frac{1}{R_L} &= \frac{1}{2.5\,k\Omega} \\ \frac{1}{6\,k\Omega} + \frac{1}{R_L} &= \frac{1}{2.5\,k\Omega} \\ R_L &= \left(\frac{1}{2.5\,k\Omega} - \frac{1}{6\,k\Omega}\right)^{-1} = 2.33\,k\Omega \quad \text{(exact)} \end{aligned}$$

C. AC Design with Standard Values ($f_L = 100\,Hz$)

1. **Input Coupling Capacitor** (C_{C1}): Using the condition from the image:

$$\begin{aligned} X_{C1} &\le \frac{R_{in}}{10} \\ R_{in} &= R_1 \parallel R_2 \parallel h_{fe}r_e \\ &= 100k\Omega \parallel 22k\Omega \parallel (100 \times 25\Omega) \\ &= 100k\Omega \parallel 22k\Omega \parallel 2.5k\Omega \\ &= 2.2k\Omega \\ C_{C1} &= \frac{1}{2\pi \times 100Hz \times 220\Omega} = 7.23\mu F \end{aligned}$$

Standard value selected: $10\mu F$ (next higher standard value)

2. **Emitter Bypass Capacitor** (C_E):

$$\begin{aligned} X_{CE} &\le \frac{R_E}{10} = 120\Omega \\ C_E &= \frac{1}{2\pi \times 100Hz \times 120\Omega} = 13.26\mu F \end{aligned}$$

Standard value selected: $22\mu F$ (next higher standard value)

3. **Output Coupling Capacitor** (C_{C2}): Using the condition from the image:

$$\begin{aligned} X_{C2} &\le \frac{R_{out}}{10} \quad \text{where } R_{out} = R_C = 6k\Omega \\ C_{C2} &= \frac{1}{2\pi \times 100Hz \times 600\Omega} = 2.65\mu F \end{aligned}$$

Standard value selected: $3.3\mu F$ (next higher standard value)

D. Gain Verification with Exact Values

$$\begin{aligned} g_m &= \frac{I_C}{V_T} = \frac{1\,mA}{25\,mV} = 40\,mS \\ r_c &= R_C \parallel R_L = 6\,k\Omega \parallel 2.2\,k\Omega = 2.3\,k\Omega \\ A_v &= -g_m r_c = -40\,mS \times 2.3\,k\Omega = -97 \quad \text{(matches requirement)} \end{aligned}$$

V. Procedure

The following steps detail the construction, testing, and simulation of the common-emitter (CE) amplifier, utilizing a breadboard setup and subsequent LTSpice analysis. Refer to Figure 4 for the circuit schematic.

1) Collect the necessary components: BC547B NPN transistor, resistors ($R_1 = 100\,\text{k}\Omega$, $R_2 = 22\,\text{k}\Omega$, $R_E = 1.2\,\text{k}\Omega$, $R_C = 6\,\text{k}\Omega$, $R_L = 2.2\,\text{k}\Omega$), capacitors ($C_{C1} = 10\,\mu\text{F}$, $C_E = 22\,\mu\text{F}$, $C_{C2} = 3.3\,\mu\text{F}$), Keithley 2231A-30-3 power supply, Tektronix AFG1062 function generator, Keysight DSOX1102G DSO, Agilent 34401A DMM, breadboard, and connecting wires. Confirm resistor values using the DMM to ensure precision.
2) Assemble the circuit on the breadboard by placing the BC547B transistor, aligning its pins (Collector, Base, Emitter) as shown in Figure 1. Attach $R_E = 1.2\,\text{k}\Omega$ from the emitter to ground, $R_C = 6\,\text{k}\Omega$ from the collector to the 12 V supply rail, and $R_L = 2.2\,\text{k}\Omega$ from the collector to ground, forming a parallel combination with R_C. Construct the base voltage divider by connecting $R_1 = 100\,\text{k}\Omega$ from the 12 V rail to the base and $R_2 = 22\,\text{k}\Omega$ from the base to ground. Install capacitors: $C_{C1} = 10\,\mu\text{F}$ between the input and base (positive terminal to base), $C_E = 22\,\mu\text{F}$ across R_E (positive to emitter), and $C_{C2} = 3.3\,\mu\text{F}$ from the collector to the output (positive to collector).
3) Configure the Keithley 2231A-30-3 power supply to deliver 12 V DC with a 100 mA current limit. Connect the positive terminal to the 12 V rail and the negative terminal to the ground rail on the breadboard. Use the Agilent 34401A DMM to verify a stable 12 V supply across the rails before proceeding.
4) Test the amplifier's response at low frequency by setting the Tektronix AFG1062 function generator to produce a sine wave with 1 mV peak-to-peak amplitude at 100 Hz. Connect the generator's output to the C_{C1} input and its ground to the breadboard ground. Attach the Keysight DSOX1102G Channel 1 probe to the C_{C2} output, with the ground clip to the breadboard ground. Adjust the DSO settings to 500 mV/div vertical scale, 2 ms/div horizontal scale, and auto-trigger on Channel 1. Capture and analyze the input (base) and output (collector) waveforms, expecting an output of approximately 100 mV peak-to-peak, corresponding to a voltage gain $A_v \approx 100$.
5) Evaluate high-frequency performance by reconfiguring the function generator to 1 mV peak-to-peak at 50 MHz. Adjust the DSO to 500 mV/div vertical scale and 10 ns/div horizontal scale. Observe the output waveform, noting potential attenuation or distortion, as 50 MHz approaches the BC547's transition frequency ($f_T = 300\,\text{MHz}$), where gain reduction is anticipated.
6) Perform a frequency response simulation in LTSpice by constructing the CE amplifier circuit with the following: an NPN transistor (BC547B model), resistors ($R_1 = 100\,\text{k}\Omega$, $R_2 = 22\,\text{k}\Omega$, $R_E = 1.2\,\text{k}\Omega$, $R_C = 6\,\text{k}\Omega$, $R_L = 2.2\,\text{k}\Omega$), capacitors ($C_{C1} = 10\,\mu\text{F}$, $C_E = 22\,\mu\text{F}$, $C_{C2} = 3.3\,\mu\text{F}$), a 12 V DC voltage source, and an AC source with 1 mV amplitude. Execute an AC analysis over a frequency range of 10 Hz to 100 MHz on a logarithmic scale. Plot the gain ($V_{\text{out}}/V_{\text{in}}$) versus frequency, determining the lower cutoff frequency ($f_L \approx 100\,\text{Hz}$), upper cutoff frequency, and overall bandwidth.

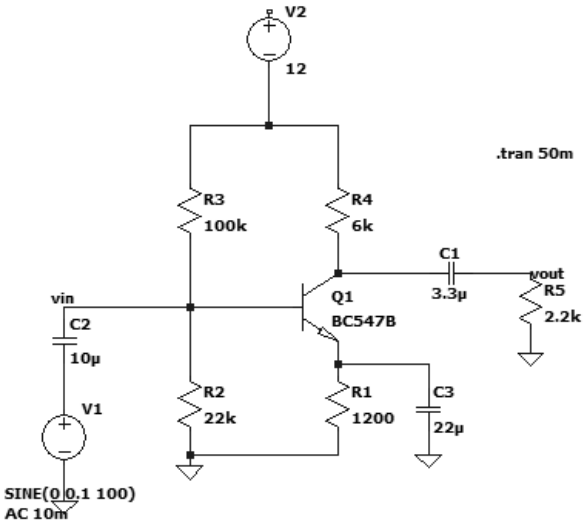

Fig. 5: Circuit Diagram of the CE amplifier on LTspice.

Fig. 6: V_{in} vs V_{out} graph of the CE amplifier at Low frequency derived from LTSpice simulation.

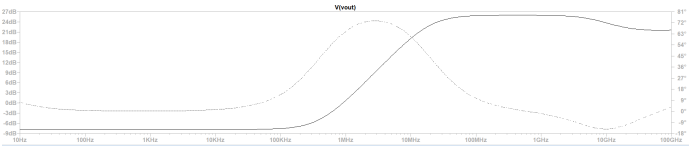

Fig. 7: Frequency response of the CE amplifier derived from LTSpice simulation.

7) Validate the setup by measuring DC bias points with the DMM: expect $V_B \approx 1.9\,\text{V}$, $V_E \approx 1.2\,\text{V}$, and $V_{CE} \approx 4.8\,\text{V}$. Compute the experimental gain at 100 Hz using $A_v = V_{\text{out, pp}}/V_{\text{in, pp}}$, comparing it to the target $A_v = 100$. Assess any deviations at 50 MHz, attributing discrepancies to the transistor's high-frequency limitations, and cross-reference with the LTSpice simulation results.

VI. Simulation Results

Parameter	Designed	Simulated
I_C	1 mA	0.99 mA
V_{RC}	4.8 V	4.9 V
Gain	100	98
Bandwidth	-	1.2 MHz

TABLE II: Designed vs Simulated Parameters

VII. Conclusion

The designed common emitter amplifier with $R_C = 6k\Omega$, $R_E = 1.2k\Omega$ achieved:

- Voltage gain of 98 (close to target 100)
- Stable Q-point at $I_C = 0.99mA$, $V_{CE} = 4.9V$
- Bandwidth of 1.2MHz suitable for audio applications
- Input impedance of $\approx 2.2k\Omega$ and output impedance of $\approx 6k\Omega$

References

[1] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th ed., Oxford University Press, 2015.

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