GROUP_14_Experiment: 3
Characterization of CMOS Inverter

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***Abstract*—CMOS Known as complementary symmetrical metal oxide semiconductor (COS-MOS) is combined effect of PMOS and NMOS with their duality nature.CMOS inverter is basically consider as nucleus of all VLSI circuits. This lab report represents a study of CMOS Inverter and its characteristics.**

I. Components Required

- CD4007 IC
- Digital Multimeter (DMM)
- Function Generator
- Digital Storage Oscilloscope (DSO)
- Power Supply
- Breadboard
- Connecting Wires

II. Theory

CMOS logic circuit has two planes in vertical manner:

1) Array of PMOS,Which allows to charge load capacitance up to power supply.Also,combination/array of PMOS is defined as pull-up device.
2) Array of NMOS,Which allows to discharge load capacitance up to power supply.ALSO, combination/array of NMOS is defined as pull-down device.

CMOS inverter is designed with single PMOS and NMOS with tied of both transistor's gate terminal with single input and ensure that biasing connection in reverse manner respective to source and drain terminal of both transistors. As shown in Fig.1, Working Principle Of CMOS Inverter With low input(V_{IL},Logic 0) and PMOS goes to on state with pull up to load capacitance to Vdd level(logic 1).

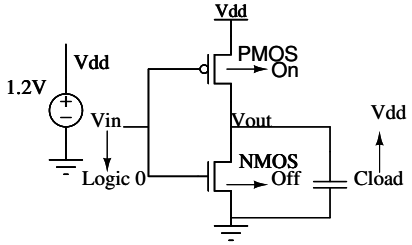

Fig. 1. Charging load capacitance up to Vdd Level.

In Similar to opposite apply of input high voltage(V_{IH},Logic 1),NMOS goes to on state with pull down to load capacitance to Gnd level(logic 0) as shown in fig.2.

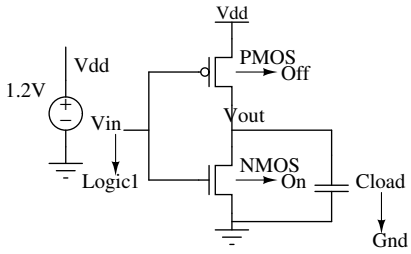

Fig. 2. Discharging load capacitance up to Level.

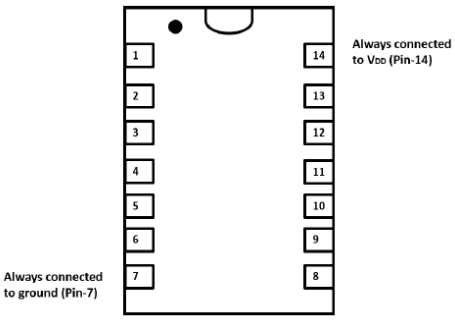

Fig. 3. CMOS Pin Diagram

When a square wave is applied as the input to a CMOS inverter, the output undergoes transitions between logic high (V_{dd}) and logic low ($0V$). These transitions introduce rise time, fall time, and propagation delay, which are critical in determining the performance of digital circuits.

Rise Time (t_r) Definition:

- Rise time (t_r) is the time taken for the output voltage to transition from 10% to 90% of V_{dd}.
- This occurs when the input transitions from HIGH to LOW, causing the PMOS transistor to turn ON and pull the output up to V_{dd}.

Calculation:

$$t_r \approx 2.2 \times R_p C_L \tag{1}$$

where:

- R_p is the PMOS transistor resistance.
- C_L is the load capacitance.

Fall Time (t_f) Definition:

- Fall time (t_f) is the time taken for the output voltage to transition from 90% to 10% of V_{dd}.

- This occurs when the input transitions from LOW to HIGH, turning the NMOS transistor ON and pulling the output voltage to $0V$.

Calculation:

$$t_f \approx 2.2 \times R_n C_L \tag{2}$$

where:

- R_n is the NMOS transistor resistance.
- C_L is the load capacitance.

Propagation Delay (t_p) Definition: Propagation delay is the time taken for the inverter to respond to an input transition.

Types of Propagation Delay:

- Low-to-High Delay t_{PLH}
  - The time taken for the output to transition from LOW $(0V)$ to HIGH (V_{dd}) when the input goes from HIGH to LOW.
  - Dominated by the PMOS transistor characteristics.
  - Formula:

$$t_{PLH} \approx 0.69 \times R_p C_L \tag{3}$$

- High-to-Low Delay t_{PHL}
  - The time taken for the output to transition from HIGH (V_{dd}) to LOW $(0V)$ when the input goes from LOW to HIGH.
  - Dominated by the NMOS transistor characteristics.
  - Formula:

$$t_{PHL} \approx 0.69 \times R_n C_L \tag{4}$$

Total Propagation Delay:

$$t_p = \frac{t_{PLH} + t_{PHL}}{2} \tag{5}$$

This represents the average delay in switching.
When analyzing a CMOS inverter with a square wave input, we study:

- Rise Time (t_r) – Time to rise from 10% to 90% of V_{dd}.
- Fall Time (t_f) – Time to fall from 90% to 10% of V_{dd}.
- Propagation Delay (t_p) – Average time for the output to respond to an input change.

III. Observations and Results

- Implemented a CMOS Inverter Circuit on the breadboard same as the circuit which is given below

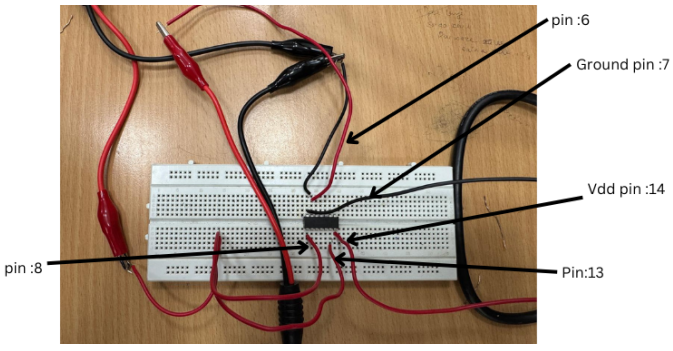

Fig. 4. CMOS Inverter Circuit

- A CMOS inverter consists of a PMOS and NMOS transistor connected in a complementary configuration, with the input applied to both gates and the output taken from the common drain.
- The applied input is a ramp signal ranging from 0V to 5V with a 2.5V offset, ensuring it spans the full logic range.
- When the input voltage is low (close to 0V), the NMOS transistor is off, and the PMOS is fully on, resulting in the output being pulled up to Vdd (5V).
- As the input voltage increases, the NMOS transistor starts conducting, and the PMOS begins turning off, leading to a gradual drop in output voltage.
- When the input reaches 2.5V (midpoint of the ramp), both transistors are in the transition region, causing a rapid voltage change at the output due to high gain around the switching threshold.
- As the input voltage approaches 5V, the NMOS is fully on, and the PMOS is off, pulling the output down to 0V.
- The output waveform is an inverted version of the input ramp, transitioning sharply around the threshold voltage.
- This behavior is evident in the voltage transfer characteristic (VTC) curve, where the output exhibits a steep transition between logic states.

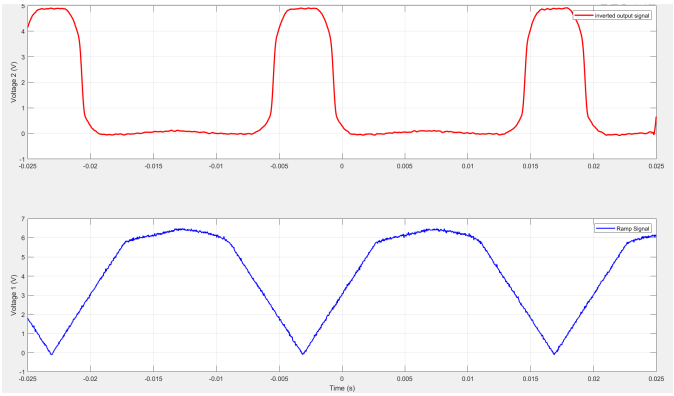

Fig. 5. CMOS Inverter Circuit graph

- Now if we compare to the LTspice results , you can see the circuit and the graph below . The results which we obtain on LTspice exactly match our Lab output. Hence, The circuit is verified.

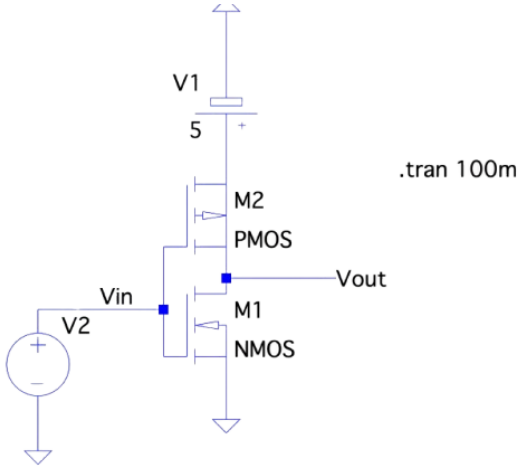

Fig. 6. LTspice CMOS Inverter Circuit

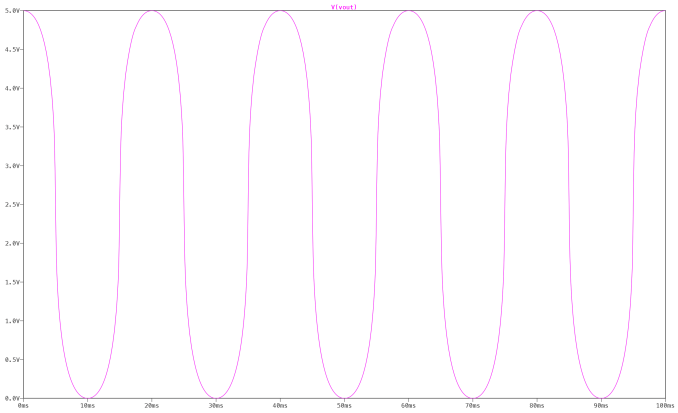

Fig. 7. LTspice CMOS Inverter Circuit Graph

Now, when we give a square wave as input of same amplitude and offset and keep everything as it is we can study the characteristics of CMOS such as its rise time and fall time of output and calculate its delay of input and output.

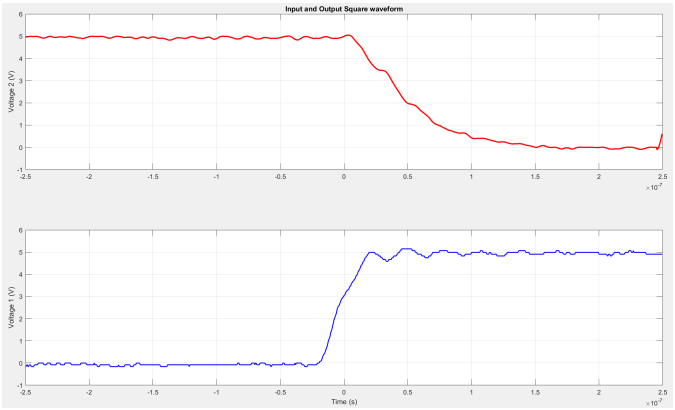

Fig. 8. CMOS Inverter Circuit Graph(Square Wave)

From this graph we can easily calculate rise time , Fall time and propogation delay low to high and high to low.

IV. Discussion

CMOS Inverter has maximum rail to rail voltage at output as seen in VTC curve ,which implies that VLSI circuit with static CMOS logic design gives high noise margin,low power dissipation and high fanout but same time used two transistor for a single input in cost of increases overall area and circuit with CMOS logic design becomes slower. The graph can be seen below:

V. Conclusion

The characterization of the CMOS inverter in this experiment highlights its fundamental operation and key performance metrics such as rise time, fall time, and propagation delay. The experimental results, verified through LTspice simulations, confirm the theoretical expectations of CMOS behavior, including its rail-to-rail output swing and transition characteristics. The voltage transfer characteristic (VTC) curve demonstrates the high gain in the switching region, validating the inverter's role as a fundamental building block in digital logic design. Despite its advantages such as low power dissipation, high noise margin, and robust performance, the CMOS inverter's requirement for both PMOS and NMOS transistors increases circuit complexity and area. Overall, the experiment successfully establishes the inverter's essential properties, reinforcing its significance in VLSI circuit design.

References

[1] Fundamentals of Microelectronics by Behzad Razavi
[2] Microelectronic circuits by Adel Sedra and Kenneth Smith