GROUP_14_Experiment: 5
Design of Current Mirror Using BC547B Transistors

Siddhant Shah (B23334) *, Akash Goel(B23032) †, Om Maheshwari (B23089) ‡, and Somya Bhadada (B23052) §
* b23334@students.iitmandi.ac.in
† b23032@students.iitmandi.ac.in
‡ b23089@students.iitmandi.ac.in
§ b23052@students.iitmandi.ac.in

***Abstract*—This paper presents the design methodology of a current mirror circuit using a BC547B transistor.**

***Index Terms*—Current Mirror, BC547B, Bipolar Junction Transistor (BJT), Reference Current, Current Matching**

I. Apparatus Required

- **BC547B NPN Transistor:**
  - Description: General-purpose NPN bipolar junction transistor (BJT) in a TO-92 package with 3-pin configuration (Collector, Base, Emitter).
  - Specifications: See Table I for detailed electrical characteristics [5].

Parameter	Value
Current gain (β)	110–800 (typical ≈ 100)
Collector current (I_C)	100 mA maximum
Collector-emitter voltage (V_{CE})	45V maximum
Emitter-base voltage (V_{EB})	6V maximum
Collector-base voltage (V_{CB})	50V maximum
Power dissipation	500 mW maximum
Transition frequency (f_T)	300 MHz
Operating temperature	-65°C to +150°C
Noise figure	Low
Applications	Switching, amplification

TABLE I: BC547B NPN Transistor Specifications.

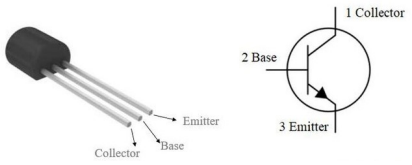

Fig. 1: BC547B NPN Transistor Pinout (TO-92 Package).

- **Resistors:** 1kΩ.
- **Power Supply:** Keithley 2231A-30-3 (triple output, 30V/3A).
- **Digital Multimeter (DMM):** Agilent 34401A ($6\frac{1}{2}$ digit resolution) for DC measurements.
- **Breadboard and Connectors:** For circuit prototyping.

II. Introduction

The **Bipolar Junction Transistor (BJT)** is a three-terminal semiconductor device that operates as a current-controlled current source [1]. It consists of three doped semiconductor regions: the **Emitter (E)**, **Base (B)**, and **Collector (C)**. BJTs are classified into two types: **NPN** and **PNP**, depending on the doping arrangement.

A. Current Mirror

A **current mirror** is an analog circuit designed to copy (or mirror) a reference current (I_{REF}) from one active device (typically a BJT or MOSFET) to another, maintaining a constant output current (I_{OUT}) regardless of load variations. It is widely used in analog integrated circuits for biasing and active load purposes [2].

1) Basic Principle

The current mirror operates based on the matching characteristics of two transistors. If both BJTs are identical and share the same V_{BE} (base-emitter voltage), then the collector current of the second transistor will mirror that of the first.

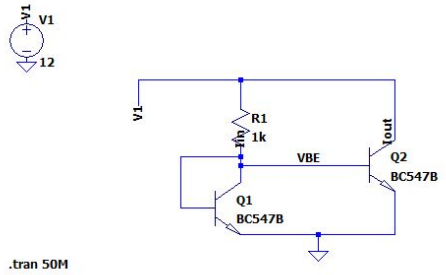

Fig. 2: Basic BJT current mirror circuit using matched NPN transistors [1].

2) Working

- The reference current I_{REF} flows through transistor Q_1 whose collector and base are shorted.

- Transistor Q_2 shares its base with Q_1 and mirrors the same base-emitter voltage (V_{BE}).
- The reference current I_{REF} is set by the resistor R and is given by:

$$I_{REF} = \frac{V_{CC} - V_{BE}}{R} \tag{1}$$

- Assuming matched transistors and negligible base current, the output current is:

$$I_{OUT} \approx I_{REF} = \frac{V_{CC} - V_{BE}}{R} \tag{2}$$

- The accuracy of current mirroring depends on matching of V_{BE}, transistor β, and thermal characteristics.

3) Small-Signal Behavior

The output impedance of the current mirror is primarily determined by the output resistance of Q_2, which increases the mirror's ability to act as a constant current source.

$$r_o = \frac{V_A}{I_C} \tag{3}$$

where V_A is the Early voltage, and I_C is the collector current.

4) Applications

- Biasing circuits in analog ICs
- Active loads for amplifier stages
- Current reference generation
- Differential amplifier stages

5) Advantages

- Provides stable and predictable current source
- Simple implementation using BJTs
- Reduces the need for large resistors in IC design

6) Limitations

- Sensitive to transistor mismatches and temperature variations
- Limited output compliance range
- Finite output impedance affects precision

III. Procedure

The following steps outline the systematic construction, testing, and simulation of the current mirror circuit, using both a physical breadboard setup and LTSpice software. Refer to Figure **??** for the schematic of the current mirror.

1) **Component Collection:** Gather the required components: two identical NPN transistors (e.g., BC547B), resistors ($R_{\text{ref}} = 1\,\text{k}\Omega$, $R_{\text{load}} = 1\,\text{k}\Omega$), Keithley 2231A-30-3 power supply, Agilent 34401A DMM, breadboard, and connecting wires.
2) **Breadboard Assembly:** Construct the current mirror circuit on the breadboard:
   - Connect the collector of transistor Q_1 to the positive 9 V rail.
   - Join the base and collector of Q_1 together and connect a 1 kΩ resistor (R_{ref}) between this node and ground. This resistor sets the reference current.
   - Connect the base of Q_2 to the base of Q_1 (common base node).
   - Connect the emitter of both transistors to ground.
   - Attach a 1 kΩ (or even of higher value) load resistor (R_{load}) from the collector of Q_2 to the 9 V rail.
3) **Power Supply Configuration:** Set the Keithley power supply to provide 12 V DC with a current limit of 50 mA. Connect the positive terminal to the 12 V rail and the negative terminal to the ground rail. Use the Agilent 34401A DMM to verify voltage stability across the rails.
4) **Current Verification:** Use the DMM to measure the voltage across R_{ref} and compute the reference current $I_{\text{ref}} = V_{R_{\text{ref}}}/R_{\text{ref}}$. Similarly, measure the voltage across R_{load} to compute the output current $I_{\text{out}} = V_{R_{\text{load}}}/R_{\text{load}}$. Verify that $I_{\text{out}} \approx I_{\text{ref}}$, indicating proper mirroring behavior.
5) **Performance Under Load:** Vary the value of R_{load} (e.g., 470 Ω, 2.2 kΩ) and repeat the above measurements to examine the output current regulation. Note that a well-designed current mirror maintains nearly constant I_{out} despite varying R_{load}.
6) **LTSpice Simulation:** Simulate the current mirror using LTSpice:
   - Construct the same circuit using BC547B models.
   - Apply a 12 V DC voltage source.
   - Use a parameter sweep for R_{load} and perform a DC operating point analysis.
   - Observe and plot I_{ref} and I_{out} to verify current mirroring and output current constancy.

Fig. 3: LTSpice output showing current mirroring behavior across R_{load}.

NOTE: During LTspice simulation we kept the voltage as 12V and we didn't applied a load resistor at Q_2 but while performing the experiment you have to take a Load resistor and keep the voltage low not 12V , we kept 9V. The load resistor can be kept high as compared to Reference resistor and it is required at Q_2 because we need more voltage drop at Q_2 then Q_1 then only it will show the output in DMM. Instead of using resistor for voltage drop you can also connect Q_2 with different value of voltage source lesser than the voltage source at Q_1 in order to get output.

7) **Analysis and Validation:** Compare simulated and experimental values of I_{ref} and I_{out}. Discuss the current matching accuracy and potential sources of mismatch, such as V_{BE} differences or Early effect. Validate performance against theoretical expectations.

IV. Results

1) So from the LTspice simulation you can see that when we kept input voltage as 12V we got current on reference

resistor to be 11.3mA and current at Q_2 12.8mA. This difference is because we didn't connected the load resistor.

2) When we performed practically we gave input voltage to Q_1 as 9V and Q_2 to a lower voltage and compared the result of current at both Q_1 and Q_2 it wads nearly same. You can see below the images of the circuit and the result in DMM.

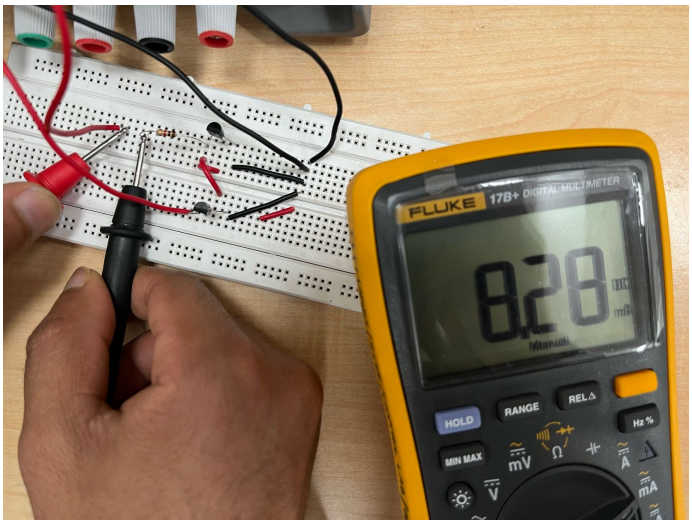

Fig. 4: Image showing current across R_{Ref}.

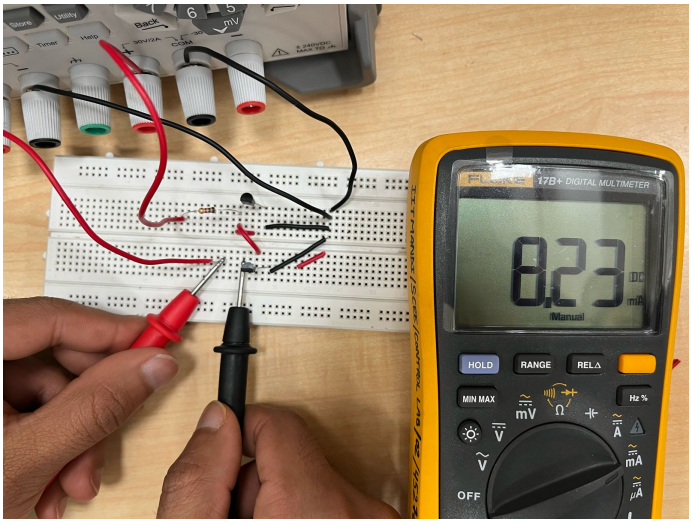

Fig. 5: Image showing current across R_{Load}.

V. Conclusion

The experiment successfully demonstrated the working principle of a basic current mirror using two matched NPN transistors (BC547B). Both LTSpice simulations and practical breadboard implementations verified that the output current (I_{out}) closely tracks the reference current (I_{ref}), confirming the mirror's ability to replicate current accurately across branches. The circuit maintained a near-constant output current even when different load resistances were used, reflecting the fundamental behavior of current mirrors as active loads or current sources. The results thus validate the theoretical expectations and showcase the reliability of current mirrors in analog circuit applications.

VI. Discussion

In the LTSpice simulation, the circuit was modeled without a load resistor at the output transistor (Q_2), and the supply voltage was set to 12 V. Under these conditions, the output current (I_{out}) slightly exceeded the reference current (I_{ref}). This discrepancy is explained by the Early effect, where differences in the collector-emitter voltage (V_{CE}) influence the output current due to the finite output resistance of the transistor.

Practically, the setup used a 9 V supply and included a load resistor at Q_2, ensuring a greater voltage drop and bringing V_{CE} values of both transistors closer. This setup resulted in more accurate current mirroring with $I_{\text{out}} \approx I_{\text{ref}}$. The use of a load resistor also improved visibility of current flow on the DMM, which is critical in practical measurements.

Additional observations include:

- **Transistor Matching:** While identical transistor models were used, manufacturing variations can introduce minor differences in base-emitter voltage (V_{BE}), affecting current accuracy.
- **Compliance Voltage:** The output current remained stable for varying R_{load}, as long as the transistor operated in the active region. However, for very high R_{load}, the output transistor may enter saturation, deviating from ideal behavior.
- **Simulation vs Practical Results:** The practical setup introduced real-world non-idealities such as contact resistance on the breadboard, slight variations in component values, and measurement errors, none of which are accounted for in simulation.

Overall, this experiment highlights the importance of both simulation and physical implementation when validating analog circuit behavior. It also underscores key design considerations in practical applications of current mirrors, such as matching conditions, supply voltage selection, and output compliance requirements.

References

[1] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th ed., Oxford University Press, 2015.

[2] R. Boylestad and L. Nashelsky, *Electronic Devices and Circuit Theory*, 11th ed., Pearson, 2013.

[3] A. Sedra, K. Smith, *Microelectronic Circuits*, 7th ed. Oxford University Press, 2014.

[4] B. Razavi, *Fundamentals of Microelectronics*, 2nd ed. Wiley, 2013.

[5] ON Semiconductor, "BC547 Datasheet," 2021. [Online]. Available: https://www.onsemi.com/pdf/datasheet/bc547-d.pdf