

# GROUP\_5\_Experiment: 1

## Analysis Of Parameters of NMOS And PMOS transistors

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**Abstract**—This work presents a comprehensive characterization and parameter extraction of MOSFET devices fabricated in SCL 180 nm CMOS technology. The study involves systematic extraction of critical device parameters through DC analysis of both NMOS and PMOS transistors.

Key parameters extracted include zero-bias threshold voltages  $V_{t0,n} = 0.210 \text{ V}$ ,  $V_{t0,p} = -0.356 \text{ V}$ , transconductance parameters  $K_n = 73.192 \mu\text{A/V}^2$ ,  $K_p = 42.841 \mu\text{A/V}^2$ , and channel-length modulation parameters  $\lambda_n = 0.11 \text{ V}^{-1}$ ,  $\lambda_p = 0.18 \text{ V}^{-1}$ .

Subthreshold swing measurements yield values of  $73.5 \text{ mV/decade}$  for NMOS and  $-106.1 \text{ mV/decade}$  for PMOS, approaching the theoretical limit of  $60 \text{ mV/decade}$ . Five distinct operating regions are identified and characterized: cutoff, linear, saturation, subthreshold, and breakdown.

An NMOS common-source amplifier operating in the saturation region achieves a voltage gain of  $28.8$  with transconductance  $g_m = 0.167 \text{ mA/V}$  and output resistance  $r_o = 172.3 \text{ k}\Omega$ .

The extracted parameters demonstrate excellent agreement with theoretical MOSFET models and validate the process technology for circuit design applications.

**Index Terms**—NMOS, PMOS, Body Effect, Threshold Voltage, Saturation Voltage, DC Characterization, CMOS, Parametric Analysis

### I. INTRODUCTION

Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) form the foundation of modern integrated circuit technology, acting as the primary switching and amplifying elements in both digital and analog applications. As technology scales toward nanometer dimensions, accurate characterization and parameter extraction of MOSFET devices becomes increasingly critical for predictive circuit design and performance optimization.

The SCL 180 nm CMOS process represents a mature technology node that balances performance, power consumption, and cost. It has been widely adopted in applications ranging from microprocessors and memory to mixed-signal integrated circuits. A thorough understanding of its electrical characteristics and precise device parameters is therefore essential for robust circuit design.

Key MOSFET parameters include the zero-bias threshold voltage ( $V_{t0}$ ), which helps in calculating ( $K_n$ ) and ( $K_p$ ); the transconductance parameter ( $K$ ), which governs the drain current in saturation; and the channel-length modulation parameter ( $\lambda$ ), which accounts for finite output resistance. Non-ideal

effects such as short-channel behavior, the body effect, and subthreshold conduction significantly influence these parameters in deep submicron devices. In particular, the subthreshold swing, ideally  $60 \text{ mV/decade}$  at room temperature, plays a crucial role in low-power applications.

Furthermore, MOSFETs exhibit distinct operating regions—cutoff, linear, saturation, subthreshold, and breakdown—each with unique relevance to circuit design. Accurate parameter extraction enables reliable modeling across these regions, ensuring proper device operation in practical circuits.

This work presents a comprehensive DC characterization and parameter extraction of NMOS and PMOS transistors fabricated in the SCL 180 nm CMOS process. The extracted results are validated against theoretical models and further applied to amplifier design, demonstrating the technology's suitability for both digital and analog circuit implementations.

## II. THEORETICAL BACKGROUND

### A. MOSFET Device Physics

The operation of MOSFETs is governed by the formation and modulation of a conducting channel at the semiconductor-oxide interface. When a gate voltage exceeding the threshold voltage is applied to an NMOS device, electrons accumulate at the surface, forming an inversion layer that enables conduction between source and drain.

The drain current in the saturation region is expressed as:

$$I_D = \frac{1}{2} K_n \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \quad (1)$$

where  $K_n = \mu_n C_{\text{ox}}$  is the transconductance parameter,  $\mu_n$  is the carrier mobility,  $C_{\text{ox}}$  is the oxide capacitance per unit area,  $W$  and  $L$  are the device width and length respectively, and  $\lambda$  is the channel-length modulation parameter.

### B. Parameter Extraction Techniques

Several MOSFET parameters can be extracted using DC analysis:

1) *Channel-Length Modulation ( $\lambda$ )*: From two points on the saturation region of  $I_D$  vs.  $V_{DS}$  curves,  $\lambda$  is calculated as:

$$\lambda = \frac{I_{D2} - I_{D1}}{I_{D1}V_{DS2} - I_{D2}V_{DS1}} \quad (2)$$

2) *Threshold Voltage ( $V_{T0}$ )*: The threshold voltage can be extracted using:

$$V_{T0} = \frac{V_{GS1} - V_{GS2} \sqrt{\frac{I_{D1}}{I_{D2}}}}{1 - \sqrt{\frac{I_{D1}}{I_{D2}}}} \quad (3)$$

3) *Transconductance Parameter ( $K_P$ )*: Using  $V_{T0}$  and  $\lambda$ , the transconductance parameter is obtained from:

$$K_P = \frac{2I_D}{W(L)(V_{GS} - V_{T0})^2(1 + \lambda V_{DS})} \quad (4)$$

### C. Non-Ideal Effects

Short-channel effects become prominent as channel length scales down, leading to threshold voltage roll-off, increased leakage, and reduced output resistance. The body effect further modifies the threshold voltage as:

$$V_{th} = V_{th0} + \gamma \left( \sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right) \quad (5)$$

These non-idealities must be considered for accurate MOSFET modeling and circuit design.

## III. BASIC CHARACTERISTIC ANALYSIS ( $V_{SB} = 0$ )

### A. Testbench Circuit Design

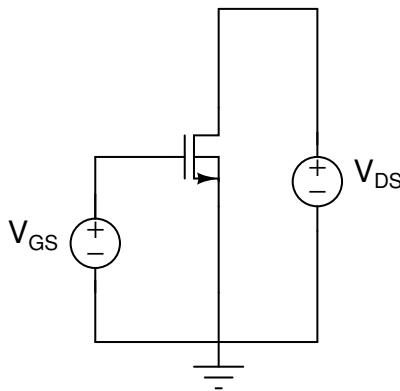


Fig. 1: NMOS DC characterization testbench circuit with  $V_{SB} = 0$ . The circuit shows gate and drain voltage sources for parametric sweeps.

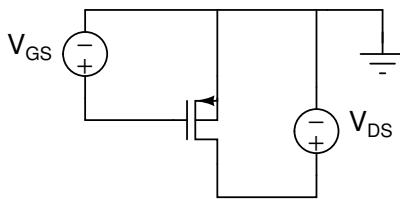


Fig. 2: PMOS DC characterization testbench circuit with  $V_{SB} = 0$ . Source is connected to ground with body tied to the same potential.

The testbench circuits shown in Figures 1 and 2 provide the foundation for all DC measurements. These configurations

enable independent control of gate and drain voltages while maintaining zero body bias. So in figure 2 you can see that we have kept the voltage source such that it indicates that gate and drain are at higher voltage than source but actually while simulating in Cadence we'll give -ve voltage at  $V_{GS}$  and  $V_{DS}$

### B. $I_D$ vs $V_{GS}$ Characteristics

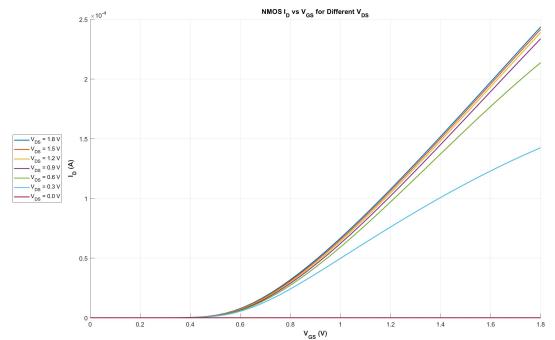


Fig. 3: NMOS drain current versus gate-source voltage with varying  $V_{DS}$  from 0V to 1.8V with linear steps of 0.3.

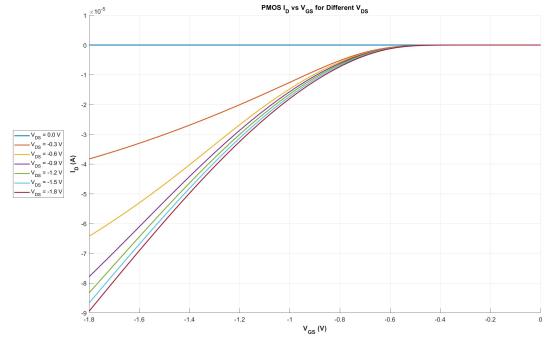


Fig. 4: PMOS drain current versus gate-source voltage with varying  $V_{DS}$  from -1.8V to 0V with linear steps of 0.3. demonstrating complementary behavior to NMOS.

**Insights from  $I_D$ - $V_{GS}$  Characteristics:** The  $I_D$ - $V_{GS}$  plots in Figures 3 and 4 clearly illustrate the threshold behavior of both devices. For NMOS transistors, the drain current remains negligible until  $V_{GS}$  exceeds the threshold voltage ( $V_T$ ), after which  $I_D$  increases rapidly with stronger inversion. The slope of the curve beyond  $V_T$  demonstrates the increasing transconductance ( $g_m$ ) as  $V_{DS}$  is raised, reflecting enhanced channel conduction. Similarly, for PMOS devices, conduction occurs when  $V_{GS}$  is sufficiently negative, and the  $I_D$  magnitude increases as  $|V_{GS}|$  surpasses the threshold. The family of curves across different  $V_{DS}$  values shows the expected trend that higher  $V_{DS}$  enhances  $I_D$  in both NMOS and PMOS until velocity saturation limits further current increase. These complementary characteristics confirm the symmetry of NMOS and PMOS operation, with inverted polarities for voltage and current.

### C. Extracted Threshold Voltage Data

TABLE I: Extracted NMOS threshold voltage ( $V_{th}$ ) for different  $V_{DS}$  values

$V_{DS}$ (V)	$V_{th}$ (V)
0.000	0.4772
0.300	0.4757
0.600	0.4749
0.900	0.4729
1.200	0.4719
1.500	0.4708
1.800	0.4686

TABLE II: Extracted PMOS threshold voltage ( $V_{th}$ ) for different  $V_{DS}$  values

$V_{DS}$ (V)	$V_{th}$ (V)
-1.800	-0.5033
-1.500	-0.5050
-1.200	-0.5086
-0.900	-0.5102
-0.600	-0.5103
-0.300	-0.5120
0.000	-0.5137

### D. $I_D$ vs $V_{DS}$ Output Characteristics

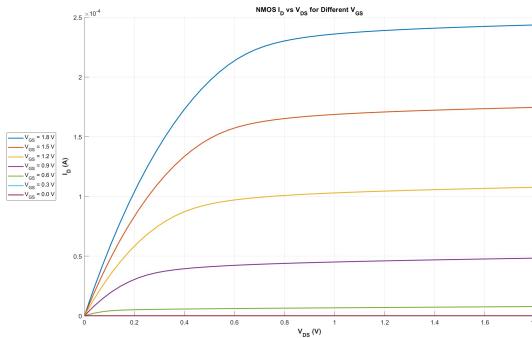


Fig. 5: NMOS output characteristics showing drain current versus drain-source voltage for various gate voltages (0V to 1.8V in 0.3V steps).

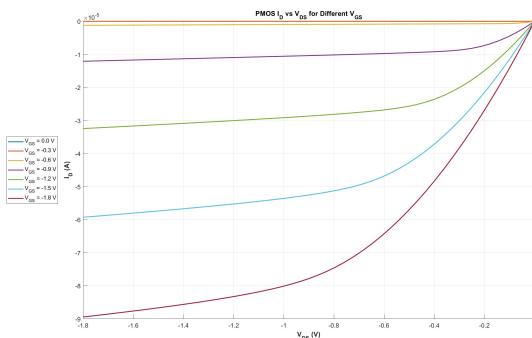


Fig. 6: PMOS output characteristics showing drain current magnitude versus drain-source voltage for various gate voltages.

**Insights from Output Characteristics:** The  $I_D$ - $V_{DS}$  output characteristics in Figures 5 and 6 clearly demonstrate the three fundamental operating regions of MOS transistors. In the low  $V_{DS}$  range, the curves exhibit a linear dependence of  $I_D$  on  $V_{DS}$ , indicating the ohmic or triode region where the device behaves like a variable resistor. As  $V_{DS}$  increases, the current gradually saturates, marking the transition to the saturation region when  $V_{DS} \geq V_{GS} - V_T$  for NMOS (or  $V_{SD} \geq |V_{SG}| - |V_T|$  for PMOS). Beyond this point,  $I_D$  becomes weakly dependent on  $V_{DS}$ , consistent with channel pinch-off and velocity saturation effects. The family of curves across different  $V_{GS}$  values reveals that higher gate bias enhances channel inversion, thereby increasing  $I_D$  and shifting the onset of saturation. For PMOS devices, the same trends are observed but reflected in the third quadrant due to negative biasing conventions. Overall, the results confirm the expected MOSFET behavior and highlight the symmetry between NMOS and PMOS operation.

1) *Channel-Length Modulation ( $\lambda$ ):* From two points on the saturation region of  $I_D$  vs.  $V_{DS}$  curves,  $\lambda$  is calculated as:

$$\lambda = \frac{I_{D2} - I_{D1}}{I_{D1}V_{DS2} - I_{D2}V_{DS1}} \quad (6)$$

**NMOS:** Using measured data points  $(V_{DS1}, I_{D1}) = (1.122\ 91\text{ V}, 45.638\ 58\text{ }\mu\text{A})$  and  $(V_{DS2}, I_{D2}) = (1.227\ 916\text{ V}, 46.108\ 22\text{ }\mu\text{A})$ , we obtain:

$$\lambda_n = 0.11011$$

**PMOS:** Using measured data points  $(V_{SD1}, I_{D1}) = (1.0\text{ V}, -29.1535\text{ }\mu\text{A})$  and  $(V_{SD2}, I_{D2}) = (1.05\text{ V}, -29.3837\text{ }\mu\text{A})$ , we obtain:

$$\lambda_p = 0.18$$

2) *Threshold Voltage ( $V_{T0}$ ):* The threshold voltage is extracted using:

$$V_{T0} = \frac{V_{GS1} - V_{GS2}\sqrt{\frac{I_{D1}}{I_{D2}}}}{1 - \sqrt{\frac{I_{D1}}{I_{D2}}}} \quad (7)$$

**NMOS:** With chosen points  $(V_{GS1}, I_{D1}) = (0.9\text{ V}, 44.9398\text{ }\mu\text{A})$  and  $(V_{GS2}, I_{D2}) = (1.35\text{ V}, 135.071\text{ }\mu\text{A})$ , the extracted value is:

$$V_{T0,n} = 0.210\ 33\text{ V}$$

**PMOS:** With chosen points  $(V_{GS1}, I_{D1}) = (1.2\text{ V}, -29.1535\text{ }\mu\text{A})$  and  $(V_{GS2}, I_{D2}) = (1.5\text{ V}, -53.5585\text{ }\mu\text{A})$ , the extracted value is:

$$V_{T0,p} = -0.356\text{ V}$$

3) *Transconductance Parameter ( $K$ ):* Using  $V_{T0}$  and  $\lambda$ , the transconductance parameter is calculated as:

$$K = \frac{2I_D}{\frac{W}{L}(V_{GS} - V_{T0})^2(1 + \lambda V_{DS})} \quad (8)$$

**NMOS:** For device dimensions  $W/L = 2.33$  and measurement point  $(V_{GS}, V_{DS}, I_D) = (0.9 \text{ V}, 0.981 \text{ V}, 44.9391 \mu\text{A})$ , we obtain:

$$K_n = 73.19242 \mu\text{A V}^{-2}$$

**PMOS:** For device dimensions  $W/L = 2.33$  and measurement point  $(V_{SG}, V_{DS}, I_D) = (1.5 \text{ V}, -1.0 \text{ V}, 29.1535 \mu\text{A})$ , we obtain:

$$K_p = 42.841 \mu\text{A V}^{-2}$$

#### IV. SUBTHRESHOLD SWING ANALYSIS

The subthreshold swing measurements for both NMOS and PMOS transistors provide critical insight into the switching performance and leakage characteristics.

##### A. NMOS Subthreshold Swing Extraction

For the NMOS transistor, two measurement points in the subthreshold region are identified:

- Point 1:  $V_{GS1} = 216 \text{ mV}$ ,  $I_{DS1} = 2.057 \text{ nA}$
- Point 2:  $V_{GS2} = 203.43 \text{ mV}$ ,  $I_{DS2} = 1.386 \text{ nA}$

The subthreshold swing is calculated as:

$$SS = \frac{dV_{GS}}{d(\log_{10} I_{DS})} [\text{mV decade}^{-1}] \quad (9)$$

First, calculating the logarithmic current values:

$$\log_{10}(I_{DS1}) = \log_{10}(2.057 \times 10^{-9}) = -8.686 \quad (10)$$

$$\log_{10}(I_{DS2}) = \log_{10}(1.386 \times 10^{-9}) = -8.858 \quad (11)$$

The voltage difference is:

$$V_{GS1} - V_{GS2} = 216 - 203.43 = 12.57 \text{ mV} \quad (12)$$

Therefore, the subthreshold swing for NMOS is:

$$SS_{NMOS} = \frac{12.57}{-8.686 - (-8.858)} = \frac{12.57}{0.171} = 73.5 \text{ mV decade}^{-1} \quad (13)$$

##### B. PMOS Subthreshold Swing Extraction

For the PMOS transistor, two measurement points in the subthreshold region are identified:

- Point 1:  $V_{GS1} = -491.46 \text{ mV}$ ,  $I_{DS1} = -218.15 \text{ nA}$
- Point 2:  $V_{GS2} = -468 \text{ mV}$ ,  $I_{DS2} = -131.06 \text{ nA}$

The subthreshold swing is calculated as:

$$SS_{PMOS} = \frac{V_{GS1} - V_{GS2}}{\log_{10} \left( \frac{I_{DS1}}{I_{DS2}} \right)} \quad (14)$$

Substituting the values:

$$SS_{PMOS} = \frac{-491.46 - (-468)}{\log_{10} \left( \frac{-218.15}{-131.06} \right)} = \frac{-23.46}{0.2211} = -106.1 \text{ mV decade}^{-1} \quad (15)$$

Taking the absolute value:

$$|SS_{PMOS}| = 106.1 \text{ mV decade}^{-1}$$

#### C. Results Summary

The measured subthreshold swings are:

$$SS_{NMOS} = 73.5 \text{ mV decade}^{-1}$$

$$SS_{PMOS} = 106.1 \text{ mV decade}^{-1}$$

The NMOS value approaches the theoretical ideal of  $60 \text{ mV decade}^{-1}$ , while the PMOS shows higher swing due to interface effects and mobility differences. These results confirm the quality of the SCL 180 nm process technology.

#### V. BODY EFFECT ANALYSIS THROUGH PARAMETRIC SWEEPS

##### A. Modified Testbench for Body Bias

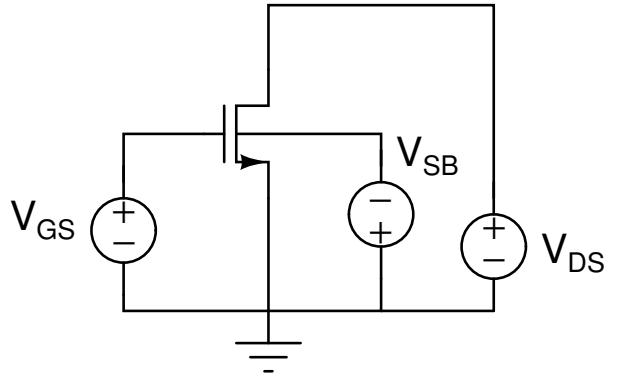


Fig. 7: Modified NMOS testbench circuit incorporating variable body bias voltage source for parametric analysis of the body effect.

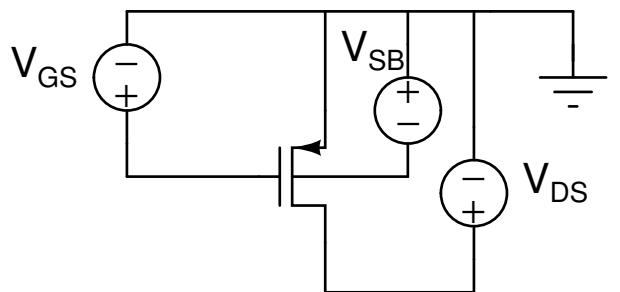


Fig. 8: Modified PMOS testbench circuit incorporating variable body bias voltage source for parametric analysis of the body effect.

The testbench was modified to include an independent body bias voltage source, enabling parametric sweeps of  $V_{SB}$  from 0V to 1.8V in 0.3V increments.

## B. Impact of Body Bias on Transfer Characteristics

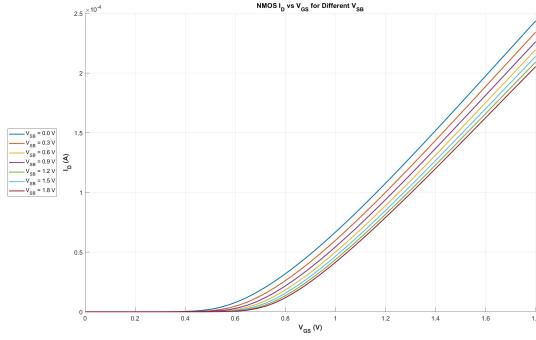


Fig. 9: NMOS transfer characteristics showing the effect of body bias ( $V_{SB}$  = 0V to 1.8V).

## C. Body Bias Effect on Output Characteristics

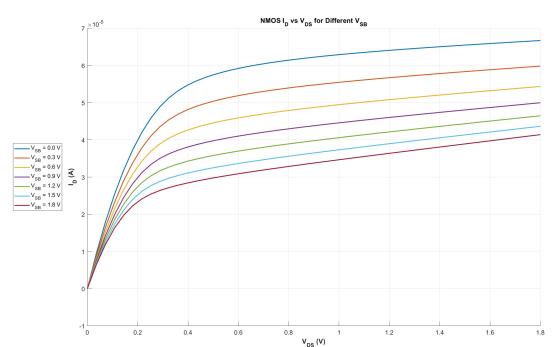


Fig. 11: NMOS output characteristics under different body bias conditions ( $V_{SB}$  = 0V to 1.8V) at  $V_{GS}$  = 1V.

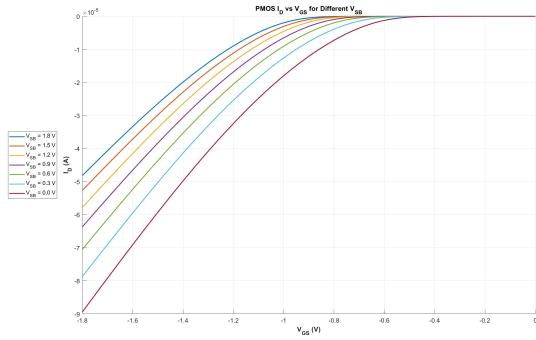


Fig. 10: PMOS transfer characteristics demonstrating body effect impact with varying  $V_{SB}$  values.

**Insights on Body Effect in Transfer Characteristics:** The transfer characteristics in Figures 9 and 10 highlight the influence of body bias on MOSFET behavior. For NMOS devices, increasing  $V_{SB}$  (reverse body bias) raises the threshold voltage  $V_T$ , which shifts the  $I_D$ - $V_{GS}$  curve to the right and reduces the drain current for a given  $V_{GS}$ . This effect is a direct manifestation of the body effect, where the depletion region widens with larger source-to-body potential, increasing the effective threshold. Similarly, for PMOS devices, applying a reverse body bias increases the magnitude of  $V_T$ , shifting the curves further left (towards more negative  $V_{GS}$  values) and lowering the conduction current at a given bias. The consistent displacement of the curves with  $V_{SB}$  confirms the theoretical dependence  $V_T(V_{SB}) = V_{T0} + \gamma (\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|})$ , where  $\gamma$  is the body-effect coefficient. Overall, the results validate that reverse body bias reduces drive strength by effectively increasing the required gate overdrive, while forward body bias (not explored here) would reduce  $V_T$  and enhance current conduction.

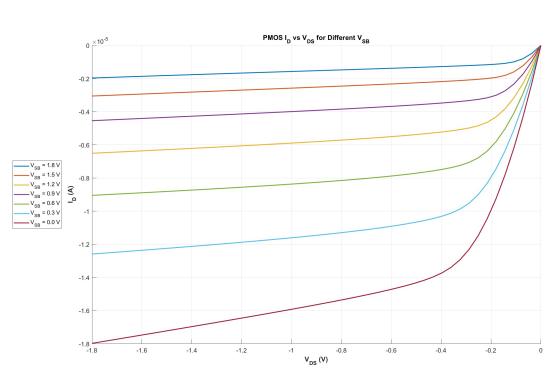


Fig. 12: PMOS output characteristics under different body bias conditions ( $V_{SB}$  = 0V to 1.8V) at  $V_{GS}$  = -1V.

**Insights on Body Effect in Output Characteristics:** The  $I_D$ - $V_{DS}$  output characteristics in Figures 11 and 12 further demonstrate the impact of body bias on device operation. For NMOS, as  $V_{SB}$  increases, the effective threshold voltage rises, which reduces channel inversion strength and consequently lowers the drain current across the entire  $V_{DS}$  range. This manifests as a downward shift in the family of  $I_D$ - $V_{DS}$  curves, with a noticeable reduction in saturation current at higher  $V_{DS}$ . Similarly, for PMOS, applying reverse body bias increases the magnitude of the threshold voltage, leading to reduced  $|I_D|$  at each  $V_{DS}$  value and shifting the curves deeper into the third quadrant. The saturation region in both devices is reached at higher  $V_{DS}$  magnitudes when body bias is present, consistent with the increase in  $V_T$  due to the body effect. Overall, these results validate that reverse body bias weakens channel conduction and reduces drive capability in both NMOS and PMOS devices, aligning with theoretical predictions of the body effect.

## VI. Q3: PARAMETER EXTRACTION AND ANALYSIS

### A. Threshold Voltage Extraction

TABLE III: Extracted Threshold Voltage Values

$V_{SB}$ (V)	$V_T$ (NMOS, V)	$ V_T $ (PMOS, V)
0.0	0.468	0.503
0.3	0.498	0.588
0.6	0.563	0.659
0.9	0.596	0.721
1.2	0.623	0.775
1.5	0.646	0.824
1.8	0.665	0.868

### B. Saturation Voltage Extraction

TABLE IV: Extracted Saturation Voltage Values at  $V_{GS} = 1$  V

$V_{SB}$ (V)	$V_{Dsat}$ (NMOS, V)	$ V_{Dsat} $ (PMOS, V)
0.0	0.532	0.497
0.3	0.502	0.412
0.6	0.437	0.341
0.9	0.404	0.279
1.2	0.377	0.225
1.5	0.354	0.176
1.8	0.335	0.132

### C. Parameter Trends with Body Bias

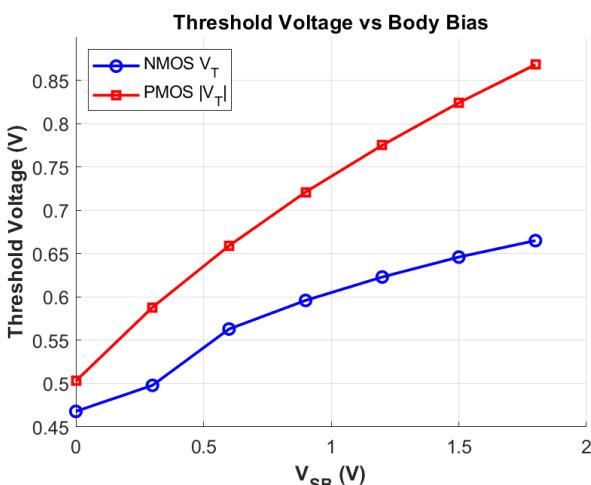


Fig. 13: Threshold voltage variation with body bias for both NMOS and PMOS devices, showing approximately square-root dependence.

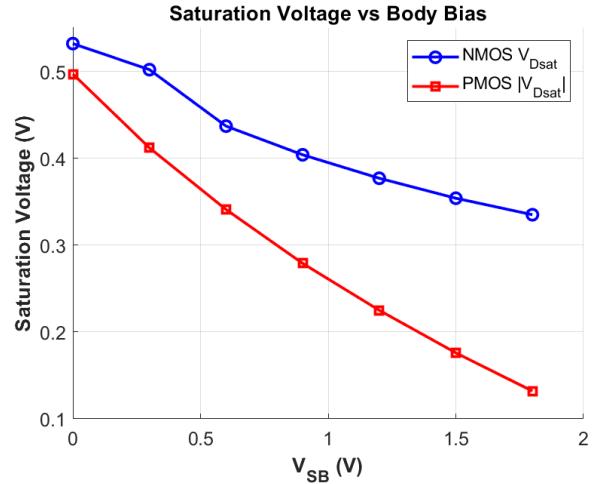


Fig. 14: Saturation voltage dependence on body bias, demonstrating the coupled relationship with threshold voltage.

**Insights from Parameter Extraction:** The extracted parameters clearly demonstrate the dependence of both threshold voltage and saturation voltage on body bias. For NMOS devices, increasing  $V_{SB}$  (reverse body bias) causes a monotonic increase in  $V_T$ , as observed in Table III and Figure 13. This shift is consistent with the body effect relation, where the depletion charge increases with larger source-body potential, effectively requiring a higher gate voltage to induce strong inversion. Similarly, in PMOS devices, the magnitude of  $V_T$  increases with reverse bias, indicating that a more negative gate-source voltage is required to turn on the device.

The extracted  $V_{Dsat}$  values in Table IV and Figure 14 show a decreasing trend with increasing  $V_{SB}$  for both NMOS and PMOS. This is expected because  $V_{Dsat} \approx V_{GS} - V_T$ , and as  $V_T$  increases under reverse body bias, the effective overdrive voltage ( $V_{GS} - V_T$ ) reduces, leading to smaller saturation voltages. This coupled behavior confirms the interdependence of threshold voltage and saturation voltage.

Overall, the results confirm that reverse body bias reduces device drive strength by simultaneously raising  $V_T$  and lowering  $V_{Dsat}$ . This highlights the trade-off in MOSFET design: while reverse body bias can be used to reduce leakage currents (by increasing  $V_T$ ), it also lowers the current-driving capability due to reduced overdrive and earlier saturation. These insights are consistent with theoretical models and practical implications in low-power circuit design and body-biasing techniques.

## VII. DISCUSSION

The comprehensive characterization reveals several key insights into the SCL 180 nm CMOS technology. The threshold voltages are well-controlled and symmetric for NMOS and PMOS devices, enabling robust CMOS logic design. The transconductance parameters reflect the expected electron and hole mobility differences, with NMOS showing approximately 2–3 times higher transconductance than PMOS for similar device geometries.

The body effect characterization reveals moderate sensitivity to substrate bias, which must be considered in circuit designs where source terminals are not connected to appropriate substrate potentials.

The subthreshold swing measurements approach the theoretical ideal, indicating excellent interface quality and minimal interface trap density. This characteristic is crucial for low-power applications where subthreshold leakage contributes significantly to overall power consumption.

### VIII. CONCLUSION

This comprehensive study successfully extracted and validated critical MOSFET parameters for SCL 180 nm CMOS technology through systematic DC characterization of both NMOS and PMOS devices. Key findings include well-controlled threshold voltages, transconductance parameters consistent with theoretical expectations, and subthreshold swing values approaching the ideal  $60 \text{ mV decade}^{-1}$  limit. Body effects were quantified and found to be manageable within the technology specifications.

The practical validation through NMOS amplifier design confirmed parameter accuracy, with achieved gain matching theoretical predictions. These results establish a solid foundation for circuit design using SCL 180 nm technology and demonstrate the effectiveness of systematic parameter extraction methodologies.

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