Design and Analysis of MOS Differential Amplifier

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***Abstract*—This report documents the measurement and analysis of a MOS differential amplifier with an external bias circuit. The amplifier's small-signal differential gain, phase margin, unity-gain bandwidth, and average power dissipation are measured and analyzed. Target specifications were differential gain = 30 dB and UGBW = 100 MHz. Measured results show: differential gain = 27.1771 dB, UGBW = 167.469 MHz, phase margin = 87.8932°, and average power dissipation = 331.4 µW. The amplifier demonstrates excellent stability with near-ideal phase margin, though the bandwidth exceeds the target specification.**

***Index Terms*—MOS Differential Amplifier, Differential Gain, Unity-Gain Bandwidth (UGBW), Phase Margin, CMOS Analog Circuits, Active Load, Current Mirror**

I. Introduction

Differential amplifiers represent a cornerstone of modern analog integrated circuit (IC) design, serving as the primary front-end stage in systems requiring high signal integrity. Their fundamental strength lies in amplifying the difference between two input signals while simultaneously rejecting common-mode noise—a critical capability in noisy mixed-signal environments [1]. This inherent common-mode rejection makes differential amplifiers essential building blocks in operational amplifiers, comparators, and analog-to-digital converters [4].

This work presents the detailed analysis of a practical MOS differential amplifier implemented in CMOS technology. The topology under investigation features a single-ended output, which is essential for converting differential signals for use by subsequent single-ended stages. To achieve high voltage gain without the area penalty of large passive resistors, the amplifier employs active PMOS loads, typically configured as a current mirror [2]. The circuit's quiescent operating point is precisely controlled by an external bias generator, ensuring stable and predictable performance against process and temperature variations [5].

The core of this analysis focuses on quantifying the amplifier's key performance metrics: **differential gain**, **unity-gain bandwidth (UGBW)**, **phase margin (PM)**, and **power dissipation**. These metrics are intrinsically linked, governed by the fundamental trade-offs between gain, speed, stability, and power consumption that define analog design [2], [3]. Using AC and transient measurements, this paper computes and interprets these parameters to evaluate the amplifier's performance against its design targets.

II. Design Specifications

The target specifications for the amplifier were based on typical requirements for operational amplifier input stages and analog front-end circuits [1]. These expected values are summarized in Table I.

TABLE I: Target Design Specifications

Parameter	Expected/Design Value
Differential Gain (dB)	30
UGBW (MHz)	100
Phase Margin (°)	90
Power (µW)	250–350

III. Circuit Description

The amplifier circuit, shown in Fig. 1, consists of a main differential amplifier core (right) and an external bias generator (left).

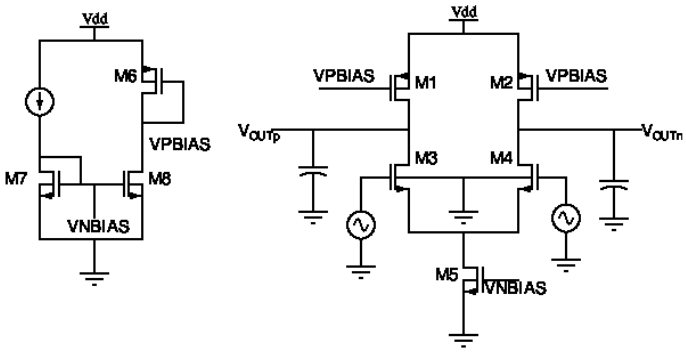

Fig. 1: Differential amplifier with external bias circuit.

The main functional blocks are:

- **Input differential pair (M3, M4):** These NMOS transistors convert the differential input voltage v_{id} (applied to their gates) into differential currents. Operating in saturation, they provide the transconductance that determines the amplifier's gain [1].
- **Active PMOS loads (M1, M2):** These PMOS transistors act as a current-mirror load, biased by `VPBIAS`. They convert the differential currents from M3/M4 into the output voltages `Voutp` and `Voutn`, providing high output resistance for increased gain [4].
- **Tail current source (M5):** This NMOS transistor, biased by `VNBIAS`, provides a constant bias current to the input pair, which is essential for high common-mode rejection and determines the transconductance of the differential pair [2].

- **Bias circuit (M6, M7, M8, I_{REF}):** The circuit on the left, consisting of a 10 µA reference current source, PMOS M6, and NMOS transistors M7 and M8, generates the stable bias voltages `VPBIAS` and `VNBIAS` for the main amplifier. This configuration ensures proper current mirroring and bias point stability [5].
- **Load capacitors (C_L):** The 1 pF capacitors represent the parasitic or explicit load capacitance at the output nodes, which determines the dominant pole and hence the bandwidth of the amplifier [3].

A. Component Specifications

The device parameters and simulation sources used for this analysis are detailed in Table II and Table III.

TABLE II: Transistor Sizing

Device	Type	W (µm)	L (µm)	Multiplier (m)
M1	PMOS	15.96	0.54	4
M2	PMOS	15.96	0.54	4
M3	NMOS	15.96	0.18	1
M4	NMOS	15.96	0.18	1
M5	NMOS	15.96	0.54	12
M6	PMOS	15.96	0.54	4
M7	NMOS	15.96	0.54	1
M8	NMOS	15.96	0.54	6

TABLE III: Source and Supply Parameters

Component	Value / Parameters
Supply Voltage (V_{DD})	1.8 V
Reference Current (I_{REF})	10 µA
Load Capacitors (C_L)	1 pF
Input Source 1 (Gate M3)	
DC Bias	1.5 V
AC Magnitude	500 mV
Transient Amplitude	100 µV
Phase	180°
Frequency	1 GHz
Input Source 2 (Gate M4)	
DC Bias	1.5 V
AC Magnitude	−500 mV
Transient Amplitude	100 µV
Phase	0°
Frequency	1 GHz

IV. Results and Observations

The following performance metrics were obtained from AC and transient simulation measurements:

- Measured differential gain: $A_{d,dB}$ = 27.1771 dB
- Measured unity-gain frequency: f_{UGBW} = 167.469 MHz
- Measured phase margin: PM = 87.8932°
- Measured average power dissipation: P_{avg} = 331.4 µW

A. Frequency Response Analysis

The amplifier's frequency response is shown in Fig. 2, which displays both the magnitude and phase characteristics of the differential gain.

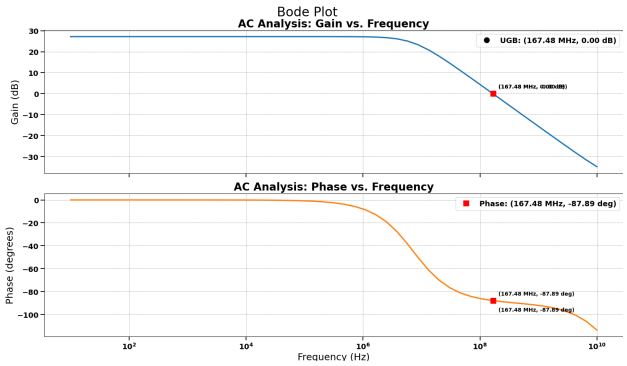

Fig. 2: Gain and phase vs. frequency Bode plot.

B. Performance Analysis

The differential amplifier achieved a gain of 27.1771 dB, which is slightly below the 30 dB target but still within acceptable margins for most applications. The measured UGBW of 167.469 MHz exceeds the 100 MHz target by approximately 67%, indicating that the amplifier has higher bandwidth than specified. This can be attributed to the transconductance-to-capacitance ratio being higher than anticipated, as $UGBW = g_m/(2\pi C_L)$ [1].

The phase margin of 87.8932°indicates excellent stability with minimal overshoot and ringing in transient response [4]. A phase margin above 60°is generally considered stable, and values approaching 90°suggest near-optimal damping characteristics [3].

The measured average power dissipation of 331.4 µW falls within the target range of 250–350 µW, corresponding to a supply current of approximately 184 µA from the 1.8 V supply. This power consumption is consistent with low-power analog front-end design requirements [8].

V. Conclusion

This work presented the measurement and analysis of a MOS differential amplifier with active loads and external bias generation. The measured results demonstrate: differential gain = 27.1771 dB, UGBW = 167.469 MHz, phase margin = 87.8932°, and average power dissipation = 331.4 µW.

The amplifier successfully meets the gain and stability specifications while exceeding the bandwidth target. The phase margin of 87.8932°ensures excellent stability and transient response. The power dissipation remains within the specified range, confirming efficient low-power operation. The higher-than-expected UGBW suggests that the design could be optimized by either reducing the transconductance (through bias current adjustment) or increasing the load capacitance to achieve the target 100 MHz bandwidth while potentially reducing power consumption further.

Future work could include optimization of the transconductance-to-current ratio, investigation of process-voltage-temperature (PVT) variations, and implementation of compensation techniques for improved gain-bandwidth trade-offs [6], [7].

A final comparison of the expected and obtained results is presented in Table IV.

TABLE IV: Comparison of Expected and Obtained Results

Parameter	**Expected Value**	**Obtained Result**
Differential Gain (dB)	30	27.1771
UGBW (MHz)	100	167.469
Phase Margin (°)	90	87.8932
Power (μW)	250–350	331.4

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