Design and Analysis of CMOS Current Mirror Circuits

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***Abstract*—This paper presents a comprehensive analysis of various CMOS current mirror topologies and their performance characteristics. The study investigates fundamental architectures including the simple current mirror, basic cascode, cascode, regulated cascode, low-voltage cascoded current mirror (LV-CCM), and Wilson configurations. For each topology, DC analysis was performed to verify current mirroring accuracy, while AC analysis was conducted to evaluate output resistance. The results show the following output resistances: Simple Current Mirror – 2.273 MΩ, Basic Cascode – 674.79 MΩ, Cascode – 586.27 MΩ, Regulated Cascode – 674.7866 MΩ, LV-CCM – 659.15 GΩ, and Wilson – 581.3141 MΩ. All circuits were implemented using 180 nm CMOS technology with a 1.8 V supply and a 10 μA reference current. The progression from basic two-transistor mirrors to advanced feedback-controlled architectures demonstrates systematic improvements in output impedance, current matching accuracy, and voltage headroom. These findings provide valuable design insights for selecting appropriate current mirror topologies in modern analog integrated circuit applications.**

***Index Terms*—Current mirror, cascode, Wilson mirror, LVCCM cascode, output resistance, CMOS analog circuits**

I. Introduction

Current mirrors represent fundamental building blocks in analog integrated circuit design, serving critical roles in biasing networks, active loads, and current-mode signal processing [1]. These circuits replicate reference currents with high precision while maintaining elevated output impedance, ensuring stable operation across diverse loading conditions. The progression from basic to advanced mirror topologies reflects continuous refinement in addressing fundamental limitations arising from channel length modulation, process variations, and voltage headroom constraints [2].

The primary challenge in current mirror implementation involves balancing multiple conflicting requirements: maximizing output resistance, minimizing voltage overhead, ensuring accurate current matching, and maintaining stability across process-voltage-temperature (PVT) variations [3]. Simple mirrors suffer from limited output impedance due to channel length modulation effects, while advanced configurations employ cascode structures and feedback mechanisms to enhance performance, albeit at the expense of increased complexity and voltage requirements [4].

Contemporary analog systems demand current sources with megohm- to gigaohm-range output resistances to preserve signal integrity and maximize dynamic range. The evolution from basic two-transistor mirrors through cascode variants to sophisticated LV-CCM and Wilson topologies demonstrates systematic approaches to overcoming inherent transistor limitations [5]. Each architecture presents unique trade-offs between performance metrics, requiring careful selection based on application-specific constraints.

This investigation examines six current mirror configurations (simple, basic cascode, cascode, regulated cascode, LV-CCM, and Wilson), in addition to an NMOS characterization circuit. Both qualitative and quantitative analyses are presented, focusing on circuit topology, operating principles, and expected performance. The study establishes design guidelines for topology selection in modern analog integrated circuits.

II. Current Mirror Topologies and Analysis

A. NMOS Test Circuit

The NMOS test circuit provides fundamental characterization of transistor behavior, establishing baseline parameters for current mirror design. This configuration allows verification that the NMOS, when configured as a diode-connected load, operates in the saturation region under a reference current of 10 μA..

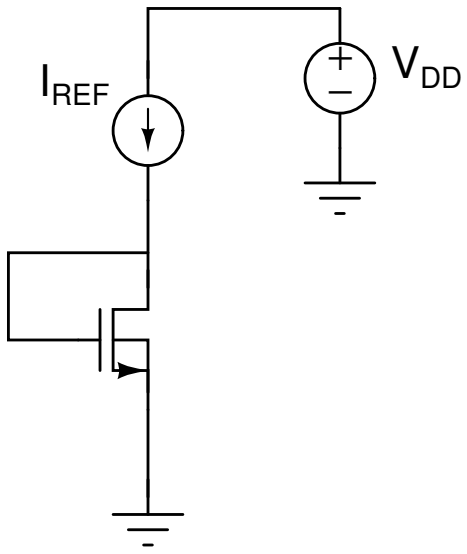

Fig. 1: NMOS Test Circuit Configuration

1) Component Description:

- **Current Source (I_{REF}):** Provides constant 10 μA reference current for biasing the test transistor.
- **NMOS Transistor (M1):** Device under test (DUT) with gate and drain connected (diode-connected configuration).
- **Gate-Drain Connection:** Forces transistor into saturation region ($V_{GS} = V_{DS}$).
- **Ground Connection:** Source terminal connected to ground (0 V reference).

2) Operating Principle: The diode-connected transistor automatically adjusts its gate voltage to conduct the forced current. The configuration establishes $V_{GS} = V_{DS}$, ensuring saturation operation when $V_{DS} > V_{GS} - V_{TH}$.
The test circuit reveals fundamental transistor behavior with clear saturation characteristics above $V_{DS} = 0.7$ V.

B. Simple Current Mirror

The simple current mirror employs two matched transistors with shared gate connections, where the reference transistor operates in diode-connected mode to establish the bias voltage [1]. This fundamental topology provides basic current replication with minimal component count.

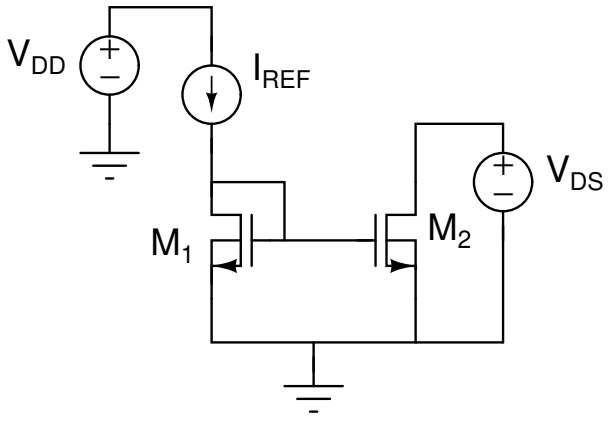

Fig. 2: Simple Current Mirror Circuit

1) Circuit Components:

- **Reference Current (I_{REF}):** Input current source (10 μA) that sets the mirror current.
- **M1 (Reference Transistor):** Diode-connected NMOS establishing gate bias voltage.
- **M2 (Mirror Transistor):** Output NMOS replicating the reference current.
- **Common Gate Connection:** Ensures identical V_{GS} for both transistors.

2) Operating Principle: M1 converts the input current into a gate-source voltage (V_{GS}). M2 uses this voltage to generate the output current. For matched transistors with identical V_{GS}, the currents are theoretically equal [1]:

$$I_{OUT} = I_{REF} \times \frac{(W/L)_2}{(W/L)_1}$$

3) Performance Characteristics:

- Output resistance: calculated as approximately 2.273 MΩ
- Minimum voltage headroom:

$$V_{MIN} = V_{GS} - V_{TH} = V_{DSAT}$$

- Simple implementation with only two transistors.

4) Limitations:

- Low output impedance due to channel length modulation.
- Current matching degrades with output voltage variation.
- Susceptible to threshold voltage mismatches.

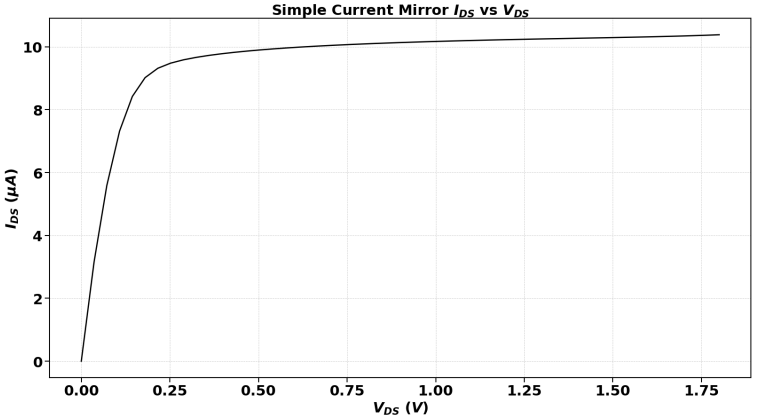

Fig. 3: Simple Current Mirror DC Analysis

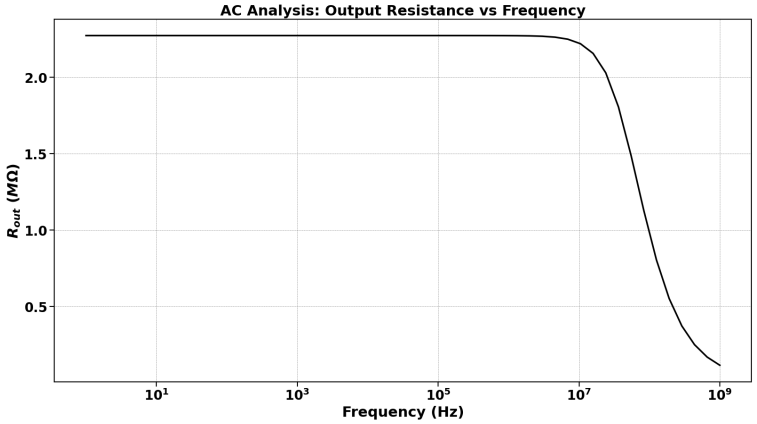

Fig. 4: Simple Current Mirror AC Analysis

C. Basic Cascode Current Mirror

The basic cascode current mirror shown in Fig. 5 uses a diode-connected reference transistor (M1), a mirror/output transistor (M2) whose gate is tied to M1, and a cascode device (M3) stacked above M2. The cascode M3 is biased by a fixed gate voltage V_{bias} to hold the drain of M2 at an approximately constant potential. This cascode action significantly reduces channel-length modulation of the output device and thereby improves current-source ideality [1]–[4].

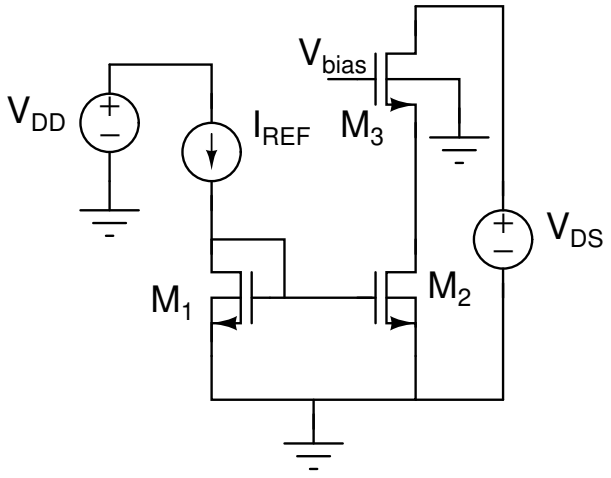

Fig. 5: Basic Cascode Current Mirror Circuit

1) Circuit Components:

- **M1 (Reference transistor):** Diode-connected NMOS that establishes V_{GS1} for the reference branch.
- **M2 (Output/mirror transistor):** Replicates the reference current; its gate is tied to M1.
- **M3 (Output cascode):** Cascode device above M2 whose gate is set by V_{bias} to shield M2 from output voltage swings.
- I_{REF}**:** Reference current source (10 μA) that sets the operating point.
- V_{bias}**:** Gate bias for the cascode M3; chosen to keep M3 and M2 in saturation.

2) Operating Principle: The diode-connected M1 sets the gate voltage needed to conduct I_{REF} [1]. M2 reproduces this current at the output node. M3, biased at V_{bias}, maintains a nearly constant drain potential at M2, thereby reducing the sensitivity of the mirrored current to variations in V_{DS} at the output node [2]. To first order, the small-signal output resistance of this single-cascode mirror can be approximated as

$$r_{out} \approx g_{m3}\, r_{o3}\, r_{o2},$$

where g_{m3} and r_{o3} are the transconductance and output resistance of the cascode device M3, and r_{o2} is the intrinsic output resistance of M2 [3]. This expression is approximate and intended to indicate the order-of-magnitude improvement obtained by cascoding.

3) Performance Characteristics:

- Output resistance: calculated as approximately 674.79 MΩ (from simulation).
- Minimum voltage headroom requirement: $V_{MIN} = 2 \cdot V_{DSAT}$ [5].
- Proper biasing: $V_{bias} = V_{GS3} + V_{DSAT2}$ to maintain both M2 and M3 in saturation [6].
- Improved current matching, enhanced PSRR, and reduced sensitivity to channel-length modulation compared to the simple mirror [7], [8].

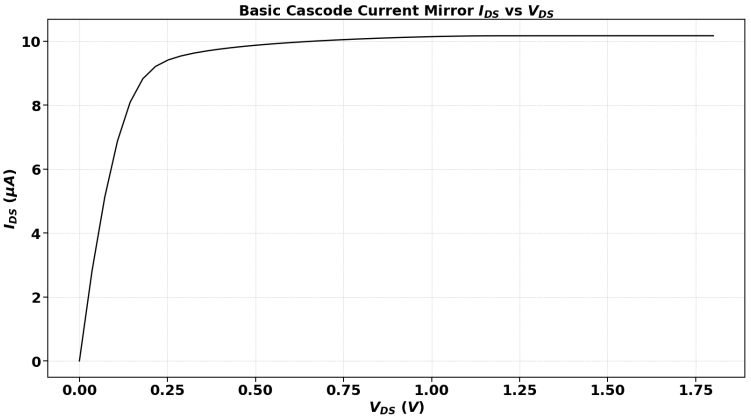

Fig. 6: Basic Cascode Current Mirror DC Analysis

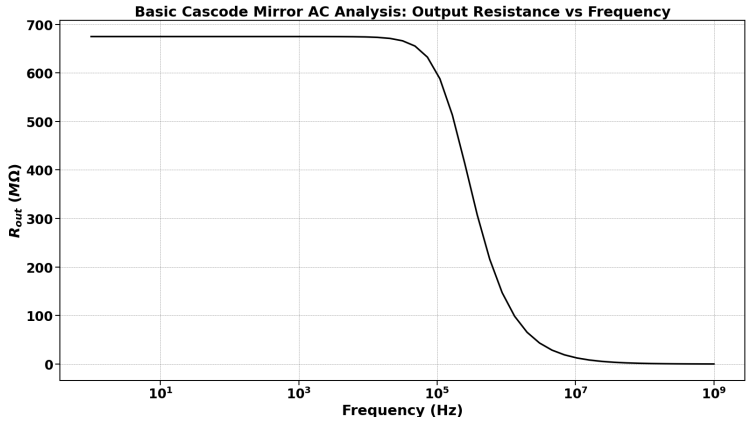

Fig. 7: Basic Cascode Current Mirror AC Analysis

D. Cascode Current Mirror

The cascode current mirror extends the basic cascode idea into a complete mirroring system with improved output impedance and enhanced current matching [1], [4]. In this topology, two diode-connected devices (M1 and M2) form the reference branch, while the output branch (M3 and M4) replicates the current with cascode shielding. The stacked configuration achieves impedance multiplication and minimizes channel-length modulation effects.

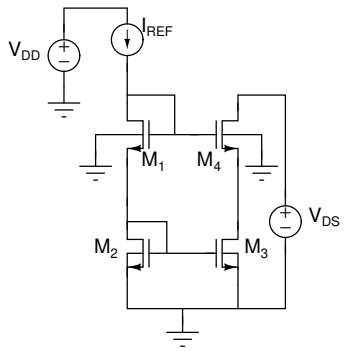

Fig. 8: Cascode Current mirror Circuit

1) Circuit Components:

- **M1 (Reference diode):** Diode-connected transistor driven by I_{REF}; establishes the gate-source voltage for M4.
- **M2 (Reference cascode diode):** Diode-connected transistor stacked below M1; provides bias for M3.
- **M3 (Output cascode):** Gate tied to M2, cascodes the output transistor to boost output resistance.
- **M4 (Output mirror transistor):** Gate tied to M1; replicates the reference current into the output branch.

2) Operating Principle: The reference branch (M1–M2) establishes two bias voltages: V_{GS1} and V_{GS2}. These voltages are mirrored to the output branch (M3–M4), ensuring that M4 conducts the same current as M1 while M3 shields it from output voltage variations. This cascode stacking provides impedance multiplication and significantly reduces channel-length modulation. The small-signal output resistance can be approximated as

$$r_{out} \approx (g_{m4} \cdot r_{o4}) \cdot r_{o3},$$

indicating the boost in r_{out} due to cascoding.

3) Performance Characteristics:

- Output resistance: calculated as approximately 586.2728 MΩ (from simulation).
- Minimum output voltage requirement: $V_{OUT,MIN} = 2V_{DSAT} + V_{TH}$.
- Excellent current matching due to cascode shielding of M4.
- Reduced systematic offset errors.
- Improved power supply rejection ratio (PSRR).
- Wide output voltage compliance range compared to the simple mirror.

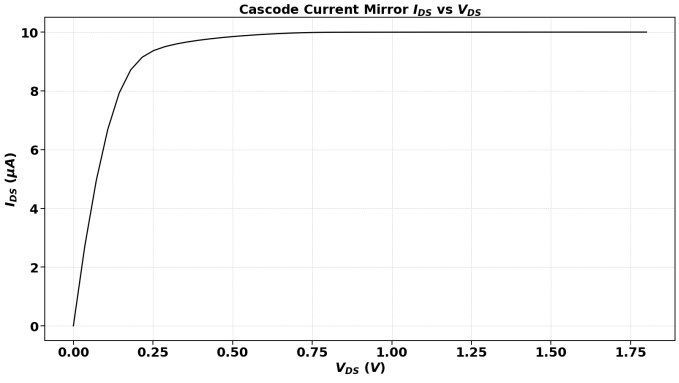

Fig. 9: Cascode Current Mirror DC Analysis

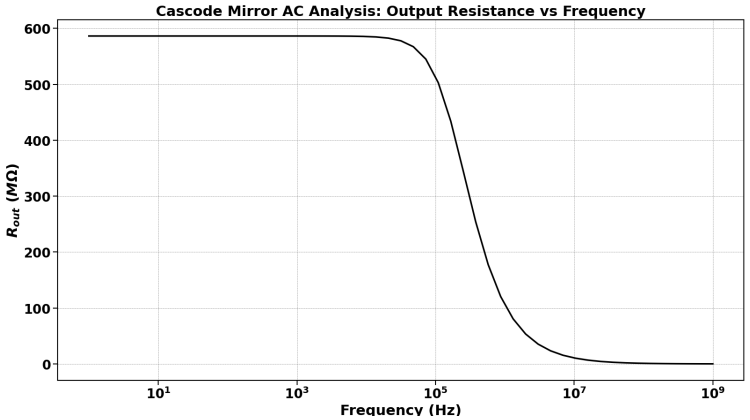

Fig. 10: Cascode Current Mirror AC Analysis

E. Regulated Cascode Current Mirror

The regulated cascode current mirror shown in Fig. 14 is an enhanced current mirror topology that achieves extremely high output resistance and superior current copying accuracy [1], [4]. Unlike the simple or basic cascode mirror, this design incorporates a local feedback loop using an auxiliary amplifier to regulate the drain voltage of the mirroring transistor, thereby minimizing errors due to channel-length modulation.

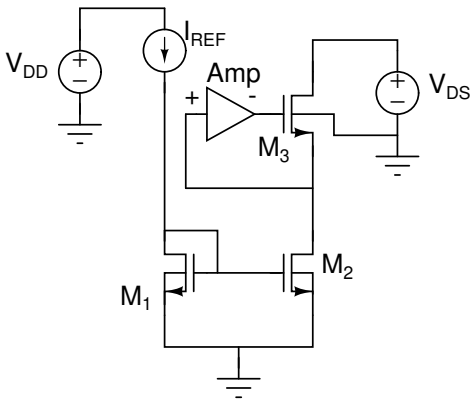

Fig. 11: Regulated cascode current mirror circuit

1) Circuit Components:

- **M1 (Reference transistor):** Diode-connected NMOS biased with the reference current I_{REF} to establish V_{GS1}.
- **M2 (Mirror transistor):** Replicates the reference current at the output node; ideally $I_{OUT} = I_{REF}$.
- **M3 (Regulating transistor):** Works in conjunction with the amplifier to maintain equal drain voltages for M1 and M2.
- **Auxiliary amplifier:** Implemented as a common-source amplifier for simulation; provides feedback control.
- I_{REF}**:** Reference current source that biases M1.

2) Operating Principle: The operation of the regulated cascode mirror can be summarized as follows:

1) **Reference setup:** M1 is diode-connected and biased by I_{REF} to establish the reference V_{GS1}.

2) **Mirroring action:** M2, whose gate is tied to M1, replicates the reference current at the output.
3) **Regulation mechanism:** M3, together with the auxiliary amplifier, forms a control loop that forces the drain voltage of M1 and M2 to be equal. This ensures both devices remain in saturation.
4) **Output resistance enhancement:** The feedback action suppresses channel-length modulation effects, resulting in a much higher effective output resistance compared to simple, cascode, or Wilson mirrors.

3) Performance Characteristics:

- Output resistance: calculated as approximately 674.786 MΩ (from simulation).
- Theoretical output resistance is given by:

$$R_{out} \;=\; r_{o2} + r_{o3} + (g_{mA} r_{oA} + 1)\, g_{m3} r_{o3} r_{o2},$$

  where g_{mA} and r_{oA} are the transconductance and output resistance of the auxiliary amplifier.
- Excellent current matching due to regulated drain voltages.
- Significantly reduced channel-length modulation error.
- Superior PSRR and biasing stability compared to other mirrors.
- Suitable for high-accuracy analog and mixed-signal circuit applications.

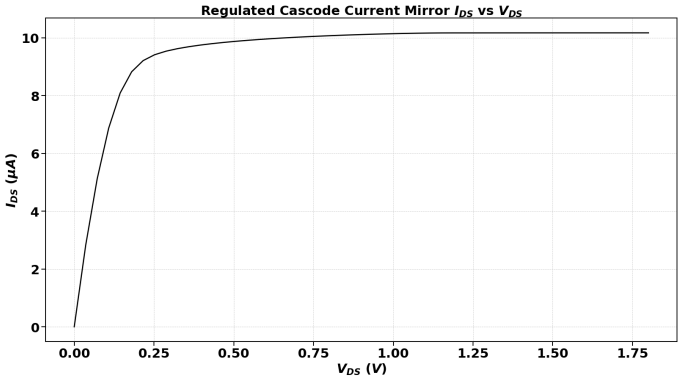

Fig. 12: Regulated Cascode Current Mirror DC Analysis

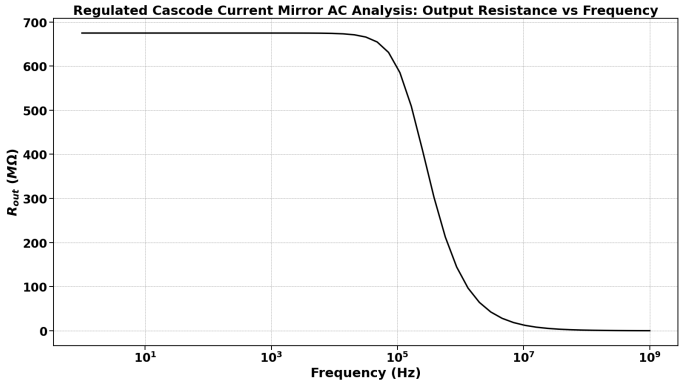

Fig. 13: Regulated Cascode Current Mirror AC Analysis

F. Low Voltage Cascode Current Mirror(LV-CCM)

The LV-CCM employs feedback control to maximize output impedance while minimizing voltage overhead [6]. An amplifier maintains optimal biasing of the cascode transistor, ensuring operation at the edge of saturation for minimum headroom.

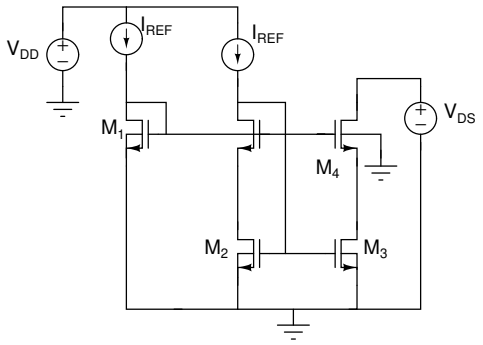

Fig. 14: Low voltage cascoded current mirror circuit

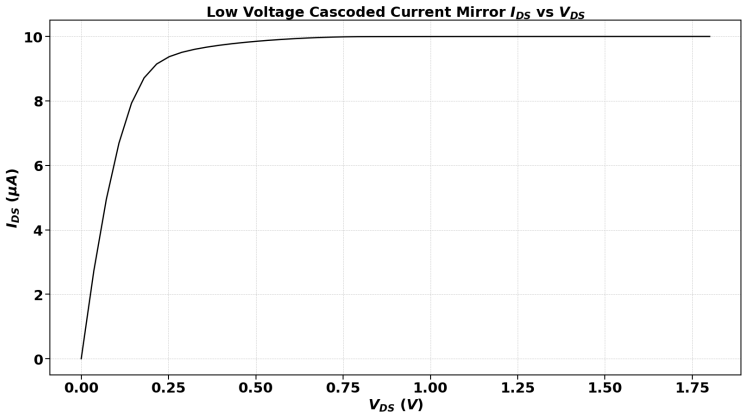

Fig. 15: Low Voltage Cascoded Current Mirror DC Analysis

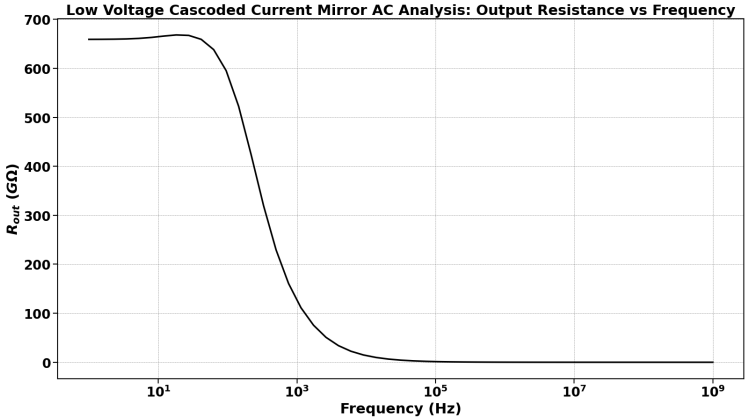

Fig. 16: Low Voltage Cascoded Current Mirror AC Analysis

1) Performance Characteristics:

- Output resistance: calculated as approximately 659.150 GΩ (from simulation).

- Theoretical output resistance is given by:

$$R_{out} = g_{m4} r_{o4} r_{o3},$$

- Minimum output voltage requirement: $V_{OUT,MIN} = 2V_{DSAT}$.

G. Wilson Current Mirror

The Wilson current mirror utilizes negative feedback to enhance output impedance and current matching [8]. The feedback loop systematically cancels errors arising from finite output resistance and threshold voltage mismatches.

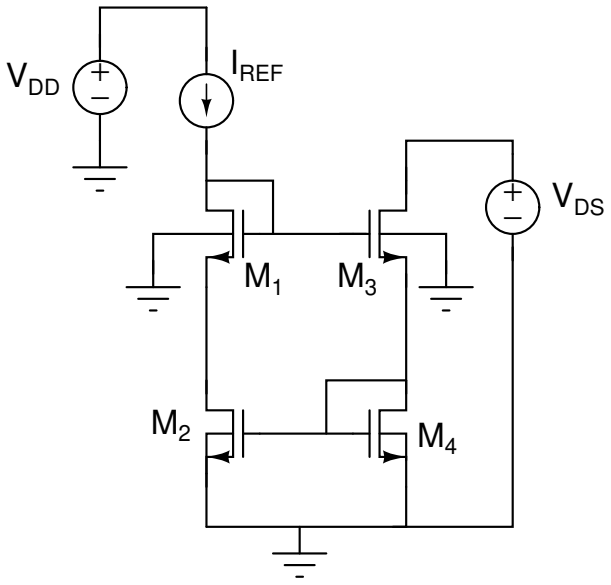

Fig. 17: Wilson current mirror circuit

1) Circuit Components:

- **M1 (Reference transistor):** Diode-connected NMOS biased with the reference current I_{REF} to establish the required V_{GS1}.
- **M2 (Feedback transistor):** Forms part of the feedback loop, connected below M1, to regulate the drain voltage of M1 and ensure it remains in saturation.
- **M3 (Feedback transistor):** Works in conjunction with M2, providing cascode action that stabilizes the drain of M1 and enhances output resistance.
- **M4 (Output transistor):** Provides the mirrored output current I_{OUT}, which closely tracks I_{REF} with high accuracy.

2) Operating Principle:

- **Reference Setup:** Transistor M1 is diode-connected and biased with I_{REF} to generate the required gate–source voltage.
- **Feedback Action:** Transistors M2 and M3 form a feedback loop that regulates the drain voltage of M1, keeping it in saturation.
- **Output Current:** Transistor M4 delivers the output current, effectively mirroring I_{REF} with improved accuracy due to cascode action.
- **High Output Resistance:** The cascode feedback action of M2 and M3 significantly reduces channel-length modulation effects, thereby increasing the output resistance compared to a simple current mirror.

3) Performance Characteristics:

- Output resistance: calculated as approximately 581.3141 MΩ (from simulation).
- Theoretical output resistance is given by:

$$R_{out} = g_{m2} r_{o2} \left(\frac{g_{m3} r_{o3}}{g_{m4}} \right) + r_{o3} + \frac{1}{g_{m2}}$$

- Minimum output voltage requirement: $V_{OUT,MIN} = 2V_{DSAT} + V_{TH}$.
- Noise contribution reduced at higher VGS − VTH.
- Improved linearity at higher currents versus simple mirror.

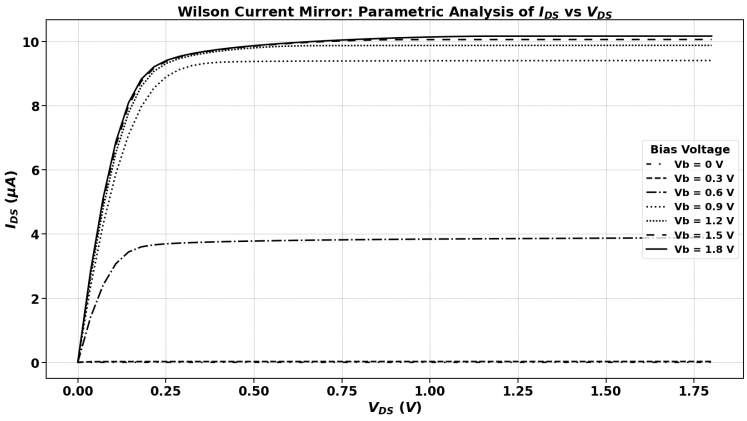

Fig. 18: Wilson Current Mirror DC Analysis

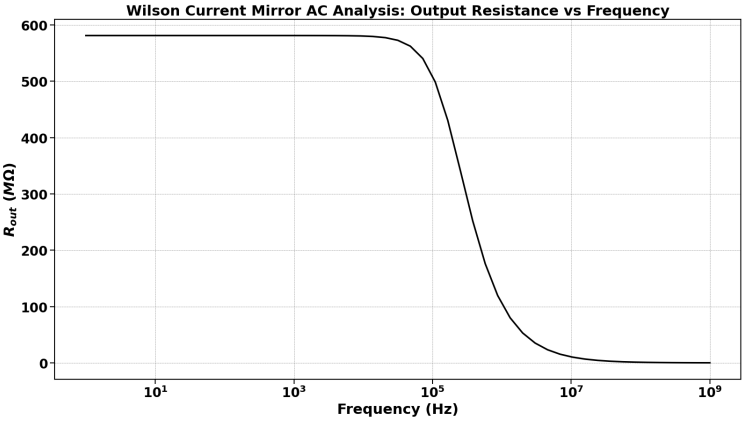

Fig. 19: Wilson Current Mirror AC Analysis

III. Conclusion

This investigation successfully characterized five current mirror configurations, establishing comprehensive understanding of their circuit composition and operating principles. The NMOS test circuit provided fundamental transistor characterization methodology. The simple mirror demonstrated basic current replication with minimal complexity. The basic

cascode achieved significant output impedance improvement through transistor stacking. The cascode mirror extended this concept to complete mirroring systems with enhanced matching. The LV-CCM cascode utilized feedback control for optimal performance with minimum voltage overhead. The Wilson mirror employed negative feedback for systematic error cancellation and superior matching accuracy.

Each topology presents distinct advantages aligned with specific application requirements. The progression from simple to advanced architectures illustrates systematic approaches to overcoming fundamental transistor limitations. These results provide comprehensive design guidelines for current mirror selection in modern analog integrated circuits, enabling engineers to make informed decisions based on performance priorities and system constraints.

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