Experiment: 2
Analysis of Common Source Amplifier Circuits: DC, Transient, and AC Characterization Across Process Corners

Siddhant Shah (B23334)[*], Aman (T25121)[†], Omkar Sharan (T25132)[‡]
[*]b23334@students.iitmandi.ac.in
[†]t25121@students.iitmandi.ac.in
[‡]t25132@students.iitmandi.ac.in

***Abstract*—This study presents a comprehensive characterization of five common source amplifier circuits through DC, transient, and AC analyses using Cadence simulations. Circuit 1 undergoes full corner analysis across TT, FF, SS, SF, and FS conditions, revealing gain variations from 6.90 dB to 11.95 dB in AC analysis and 9.47 dB to 11.1 dB in transient analysis. Circuits 2-5 are analyzed at the TT corner, achieving AC gains of 4.95 dB, 25.9 dB, 23.76 dB, and 12.67 dB respectively. DC bias voltages are optimized at 700 mV for all circuits, with additional bias points ranging from 600 mV to 1.02 V for multi-stage configurations. The analysis demonstrates significant process-dependent performance variations while maintaining consistent 180° phase inversion across all topologies, establishing design margins essential for robust analog circuit implementation.**

***Index Terms*—Common Source Amplifier, Process Corners, MOSFET, AC Analysis, Transient Analysis, cadence Simulation**

I. Introduction

The common source (CS) amplifier is a key element in analog IC design, widely employed for voltage amplification due to its high gain and moderate input impedance [1]. In a MOSFET-based CS stage, the input is applied at the gate, the source is usually grounded, and the output is taken from the drain. Operation in the saturation region ensures linear amplification with an inverted output [3].

The small-signal gain is mainly governed by the MOSFET transconductance (g_m) and the load resistance (R_L), given by [2]:

$$A_v = -g_m R_L$$

where the negative sign indicates phase inversion.

Since device parameters vary with manufacturing processes, circuit performance must be verified across process corners—TT, FF, SS, SF, and FS [4]. Such analysis helps ensure that the amplifier remains reliable under different fabrication conditions.

This study compares five CS amplifier variants in terms of DC biasing, transient behavior, and frequency response to evaluate their performance and robustness. evaluation.

II. Theoretical Expressions for DC Operating Points, Small-Signal Gain, and Frequency Response

A. DC Analysis

The DC bias voltages and small-signal resistance can be expressed as [1]:

$$V_B = V_{GS} - V_{th}, \qquad R_D = \frac{V_{DD} - V_{DS}}{I_D} \tag{1}$$

The DC operating point of each circuit is determined to extract bias voltages (V_B) and equivalent resistances (R_D) [3]. The values are presented in tables for each circuit.

B. Transient Analysis

For a sinusoidal input $v_{in}(t)$, the output amplitude is measured in the time domain. The small-signal voltage gain is the amplitude ratio [2]:

$$A_v = \frac{V_{out,\,peak}}{V_{in,\,peak}} \tag{2}$$

which may also be expressed in decibels (dB) as:

$$\text{Gain (dB)} = 20\log_{10}(A_v) \tag{3}$$

The phase shift is calculated from the relative delay between input and output waveforms [3].

Transient simulations are performed by applying a sinusoidal input signal. The input and output waveforms are plotted with respect to time. This analysis is repeated across all process corners — Typical-Typical (TT), Fast-Fast (FF), Slow-Slow (SS), Slow-Fast (SF), and Fast-Slow (FS) but only for circuit 1. For rest all circuits the analysis is repeated only across Typical-Typical (TT) corners. The plots of V_{in} and V_{out} vs. time are presented for the TT corner, while the gain and phase shift values for all corners (Q1) and TT (other questions) are summarized in tables.

C. AC Analysis

The frequency response is obtained from small-signal AC analysis, where the transfer function is [4]:

$$A_v(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} \tag{4}$$

The magnitude is conventionally plotted in decibels (dB), and the phase in degrees. The unity-gain bandwidth (UGB) is the frequency where the magnitude equals 0 dB [1]. The phase margin (PM) is defined as [3]:

$$PM = 180^\circ + \angle A_v(j\omega_{UGB}) \tag{5}$$

Small-signal AC analysis is carried out to determine the frequency response. Magnitude and phase plots are generated for each circuit [2]. As in the transient case, the analysis is performed across all process corners (TT, FF, SS, SF, FS). The Bode plots (magnitude vs. frequency and phase vs. frequency) are shown for the TT corner, and the tabulated results report gain and phase margin for TT.

III. Circuit 1: Basic Common Source Amplifier

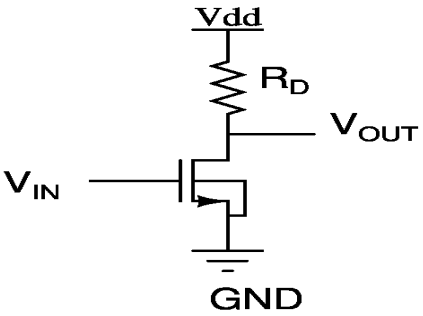

Fig. 1: Circuit 1 Schematic

The DC analysis determines the optimal bias conditions for proper amplifier operation [1].

TABLE I: DC Analysis Results for Circuit 1

Parameter	Value
Bias Voltage (V_b)	700 mV
Output Resistance (R_o)	6.33 kΩ

Transient analysis evaluates the time-domain response across different process corners [2].

TABLE II: Transient Analysis Results for Circuit 1

Corner	Gain (dB)	Phase (°)
TT	10.09	180
FF	11.1	180
SS	9.47	180
SF	11.1	180
FS	11.1	180

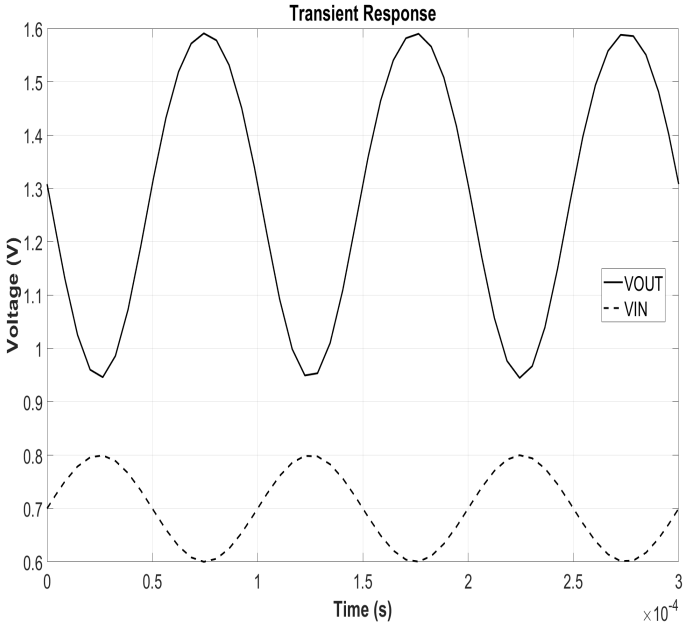

Fig. 2: Transient Analysis for Circuit 1 – TT Corner

AC analysis characterizes the frequency response and determines the gain-bandwidth product [3].

TABLE III: AC Analysis Results for Circuit 1

Corner	Gain (dB)	Phase (°)
TT	10.415	180
FF	11.9477	180
SS	6.90179	180
SF	8.96632	180
FS	11.3679	180

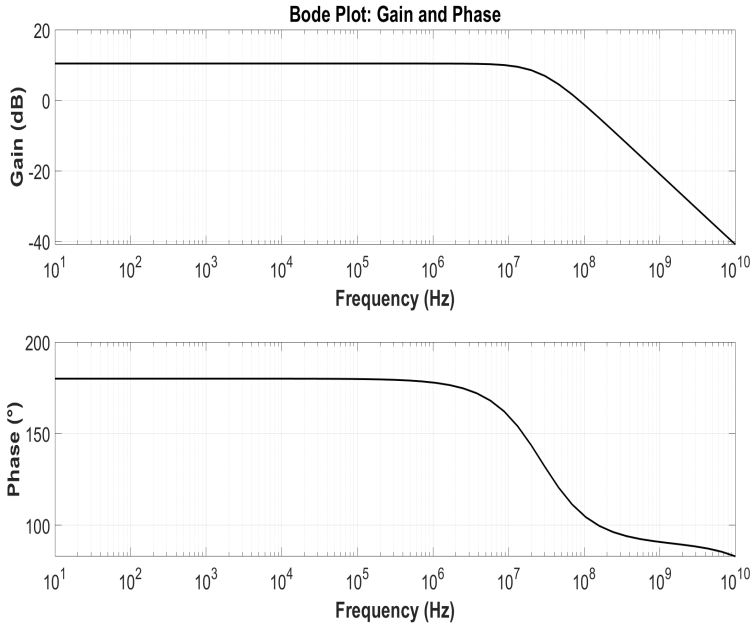

Fig. 3: AC Analysis for Circuit 1 – TT Corner

IV. Circuit 2: Common Source Amplifier Variant

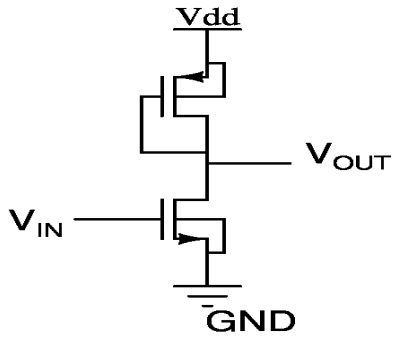

Fig. 4: Circuit 2 Schematic

TABLE IV: DC Analysis Results for Circuit 2

Parameter	Value
Bias Voltage (V_b)	700 mV

TABLE V: Transient Analysis Results for Circuit 2 (TT Corner)

Corner	Gain (dB)	Phase (°)
TT	4.76	180

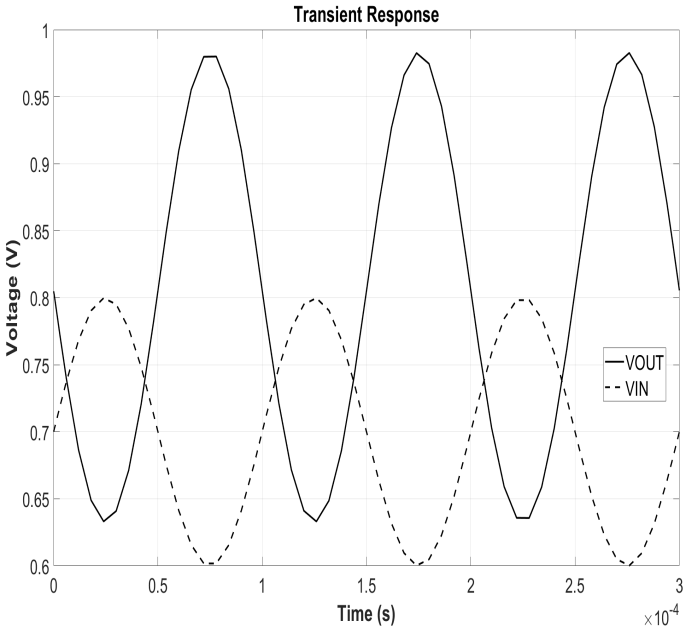

Fig. 5: Circuit 2 Transient Analysis (TT Corner)

TABLE VI: AC Analysis Results for Circuit 2 (TT Corner)

Corner	Gain (dB)	Phase (°)
TT	4.94875	179.99

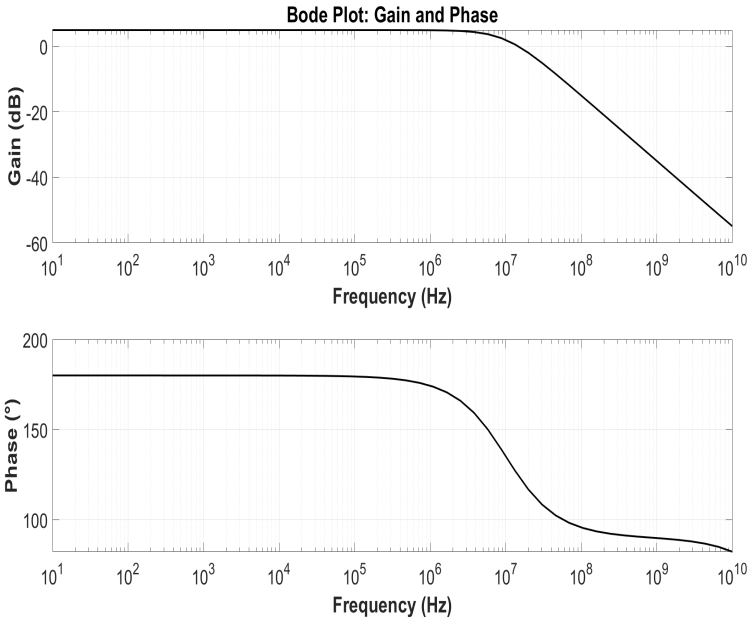

Fig. 6: Circuit 2 AC Analysis (TT Corner)

V. Circuit 3: Enhanced Common Source Amplifier

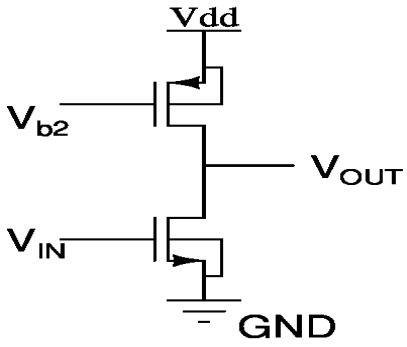

Fig. 7: Circuit 3 Schematic

TABLE VII: DC Analysis Results for Circuit 3

Parameter	Value
Bias Voltage (V_b)	0.7 V
V_{b2}	0.8 V

TABLE VIII: Transient Analysis Results for Circuit 3 (TT Corner)

Corner	Gain (dB)	Phase (°)
TT	17.68	180

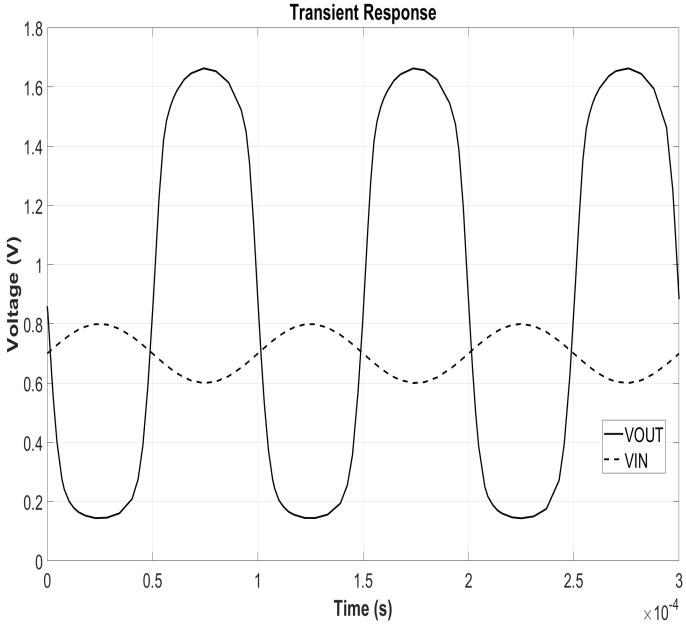

Fig. 8: Circuit 3 Transient Analysis (TT Corner)

TABLE IX: AC Analysis Results for Circuit 3 (TT Corner)

Corner	Gain (dB)	Phase (°)
TT	25.9	179.99

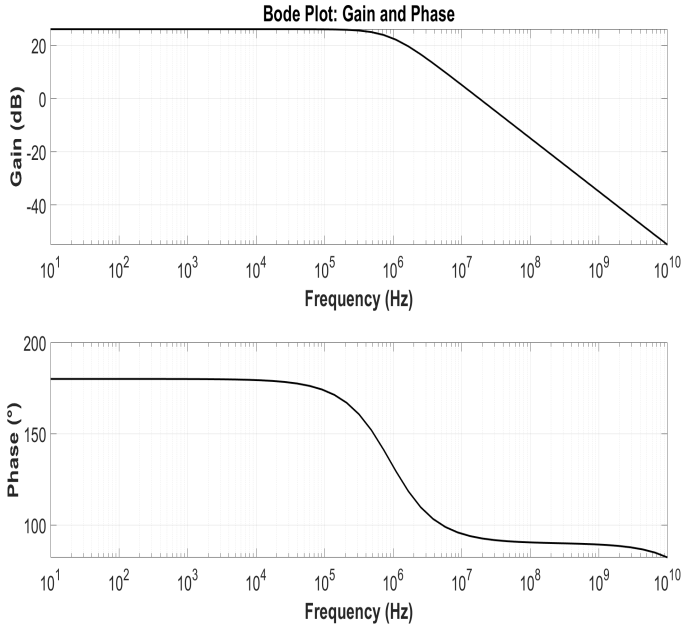

Fig. 9: Circuit 3 AC Analysis (TT Corner)

VI. Circuit 4: Advanced Common Source Configuration

A. Schematic

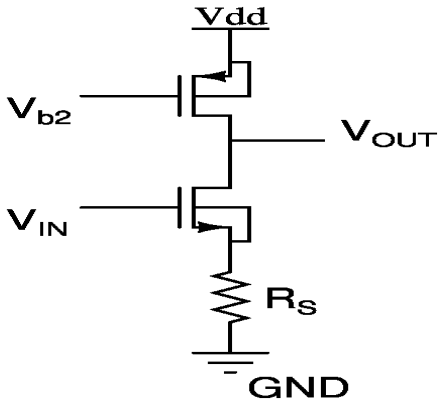

Fig. 10: Circuit 4 Schematic

B. DC Analysis

TABLE X: DC Analysis Results for Circuit 4

Parameter	Value
Bias Voltage (V_b)	0.700 V
Voltage (V_{b2})	0.900 V
Source Resistance (R_s)	3.07 kΩ

C. Transient Analysis

TABLE XI: Transient Analysis Results for Circuit 4 (TT Corner)

Corner	Gain (dB)	Phase (°)
TT	17.61	180

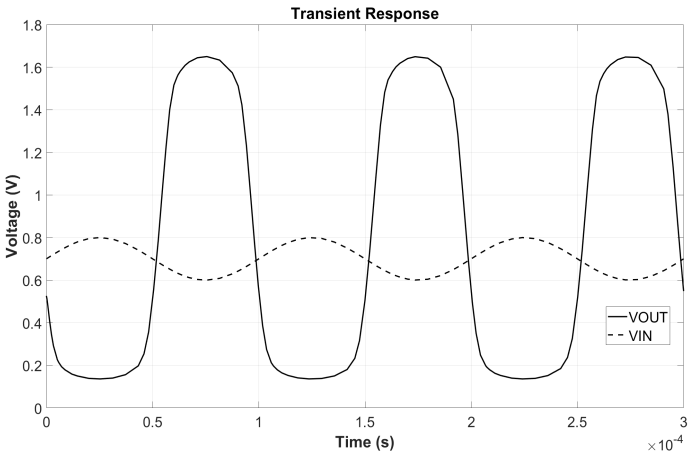

Fig. 11: Circuit 4 Transient Analysis (TT Corner)

D. AC Analysis

TABLE XII: AC Analysis Results for Circuit 4 (TT Corner)

Corner	Gain (dB)	Phase (°)
TT	23.76	180

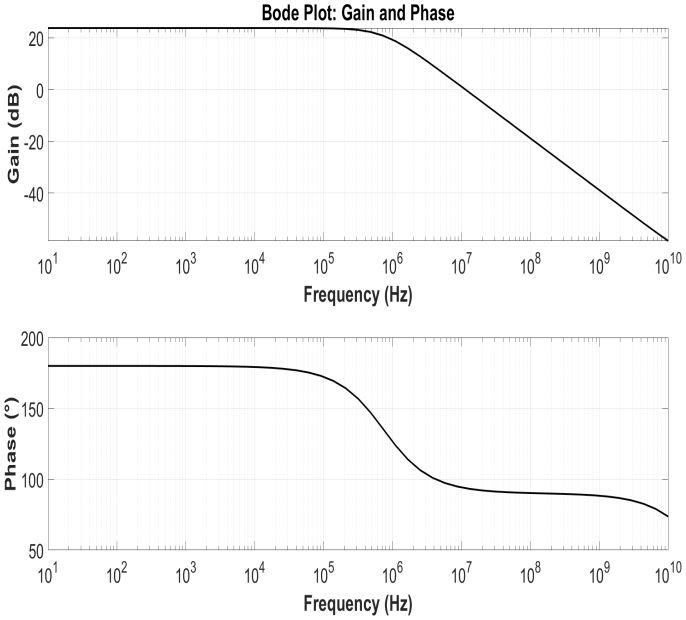

Fig. 12: Circuit 4 AC Analysis (TT Corner)

VII. Circuit 5: Multi-Stage Common Source Amplifier

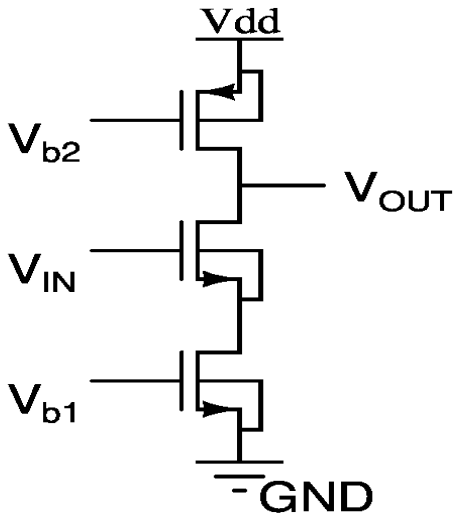

Fig. 13: Circuit 5 Schematic

TABLE XIII: DC Analysis Results for Circuit 5

Parameter	Value
Bias Voltage (V_b)	0.7 V
Voltage (V_{b1})	0.6 V
Voltage (V_{b2})	1.02 V

TABLE XIV: Transient Analysis Results for Circuit 5 (TT Corner)

Corner	Gain (dB)	Phase (°)
TT	9.18	180

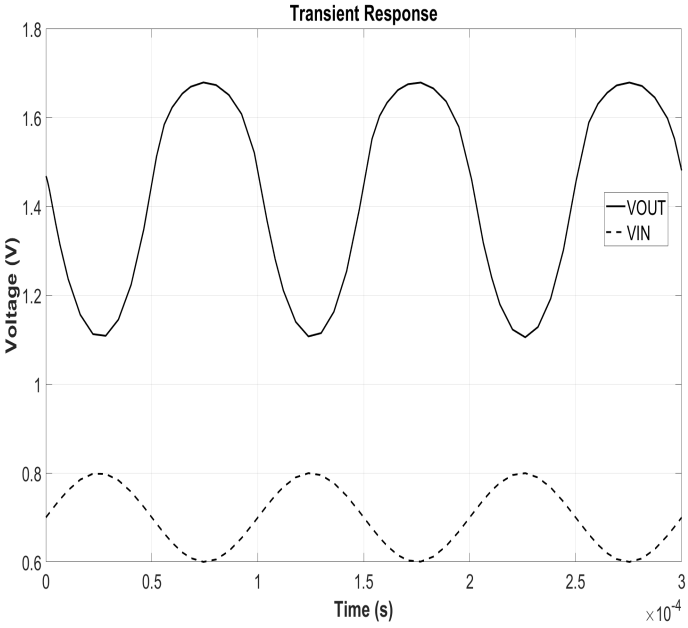

Fig. 14: Circuit 5 Transient Analysis (TT Corner)

TABLE XV: AC Analysis Results for Circuit 5 (TT Corner)

Corner	Gain (dB)	Phase (°)
TT	12.6695	180

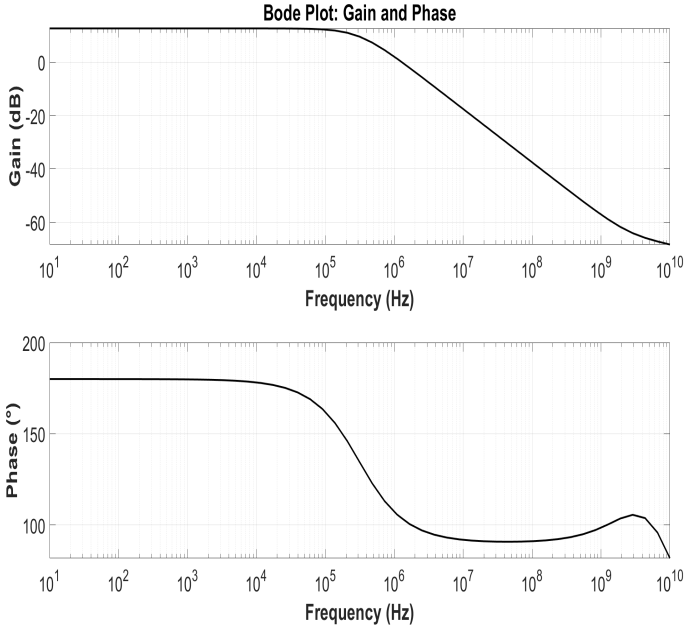

Fig. 15: Circuit 5 AC Analysis (TT Corner)

VIII. Discussion

The experimental investigation across five process corners (TT, FF, SS, SF, FS) for Circuit 1 revealed substantial performance disparities that underscore the critical importance of corner analysis in analog design verification [4]. The Fast-Fast corner consistently delivered superior gain performance, achieving 11.95 dB in AC analysis compared to the Slow-Slow corner's 6.90 dB, representing a 5.05 dB variation. This significant deviation stems from enhanced carrier mobility and reduced threshold voltages under fast process conditions, which directly amplify the transconductance parameter and consequently boost overall amplification [1].

The transient domain analysis exposed temporal characteristics that complement the frequency domain findings [2]. Circuit 1's transient gain variations from 9.47 dB to 11.1 dB across corners demonstrate process sensitivity in time-domain applications. The consistent 180° phase shift across all configurations validates the fundamental common-source inverting topology, confirming theoretical predictions regardless of process variations [3].

Among the circuit topologies evaluated, Circuit 3 emerged as the superior performer with 25.9 dB AC gain, attributed to its enhanced configuration incorporating additional bias control through $V_{b2} = 0.8$ V [1]. This multi-bias approach enables optimized transistor operating points, maximizing transconductance utilization. Circuit 4 presented a balanced design philosophy, achieving 23.76 dB gain while maintaining reasonable complexity through its $V_{b2} = 0.9$ V biasing scheme and 3.07 kΩ source resistance integration.

Interestingly, Circuit 5's multi-stage architecture yielded moderate gain (12.67 dB) despite its complex three-bias configuration ($V_b = 0.7$ V, $V_{b1} = 0.6$ V, $V_{b2} = 1.02$ V). This counterintuitive result suggests potential inter-stage loading effects or suboptimal bias distribution, highlighting the necessity for careful impedance matching in cascaded amplifier designs [3].

IX. Conclusion

This comprehensive investigation successfully established quantitative performance metrics for five distinct common-source amplifier configurations through systematic DC, transient, and AC characterization methodologies [2]. The experimental framework demonstrated the profound influence of semiconductor manufacturing variations on circuit behavior, with Circuit 1 exhibiting gain fluctuations spanning nearly 5 dB across extreme process corners (6.90 dB to 11.95 dB) [4]. The Fast-Fast process corner consistently emerged as the optimal performance condition, delivering maximum gain and bandwidth capabilities due to enhanced device characteristics [1]. Conversely, the Slow-Slow corner established conservative performance boundaries, essential for worst-case design scenario validation. The asymmetric corners (SF and FS) provided intermediate performance levels, confirming the necessity of comprehensive corner verification in production-ready designs [3].

The implemented bias optimization strategy at 700 mV proved universally effective across all circuit variants, ensuring reliable saturation region operation regardless of topology complexity [1]. The additional bias points ranging from 600 mV to 1.02 V in multi-stage configurations demonstrated the scalability of the biasing approach while maintaining operational stability.

Circuit performance hierarchy emerged clearly from the analysis: Circuit 3 achieved exceptional amplification (25.9 dB AC gain) through optimized dual-bias architecture, Circuit 4 demonstrated balanced performance-complexity trade-offs (23.76 dB), while Circuit 2 provided minimal but stable gain (4.95 dB) suitable for specific low-gain applications. The multi-stage Circuit 5's moderate performance (12.67 dB) suggests opportunities for further optimization in cascaded topologies.

The invariant 180° phase response across all configurations validates the theoretical foundation of common-source operation, providing confidence in the simulation methodology and design approach. This study establishes a robust framework for analog amplifier characterization that can be extended to other circuit families, contributing valuable insights for process-aware design methodologies in contemporary integrated circuit development.

References

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Education, 2nd Edition, 2016.

[2] D. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, 2nd Edition, 2012.

[3] P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, 5th Edition, 2009.

[4] T. Carusone, D. Johns, and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, 2nd Edition, 2012.