Technische Hochschule Rosenheim
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CA 5 – Processor 1

The lecture is based on the work and the documents of Prof. Dr. Theodor Tempelmeier

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Overview

What are the properties of a processor?

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Processor properties

- Processor architecture
- Exception and interrupt handling
- Instruction set architecture
- Memory model (part of memory lectures)
- Endianness
- Registers
- Addressing modes
- Advanced concepts
  - Instruction scheduling
  - Pipelines
  - Superscalarity
  - VLIW
  - Out-of-order memory access

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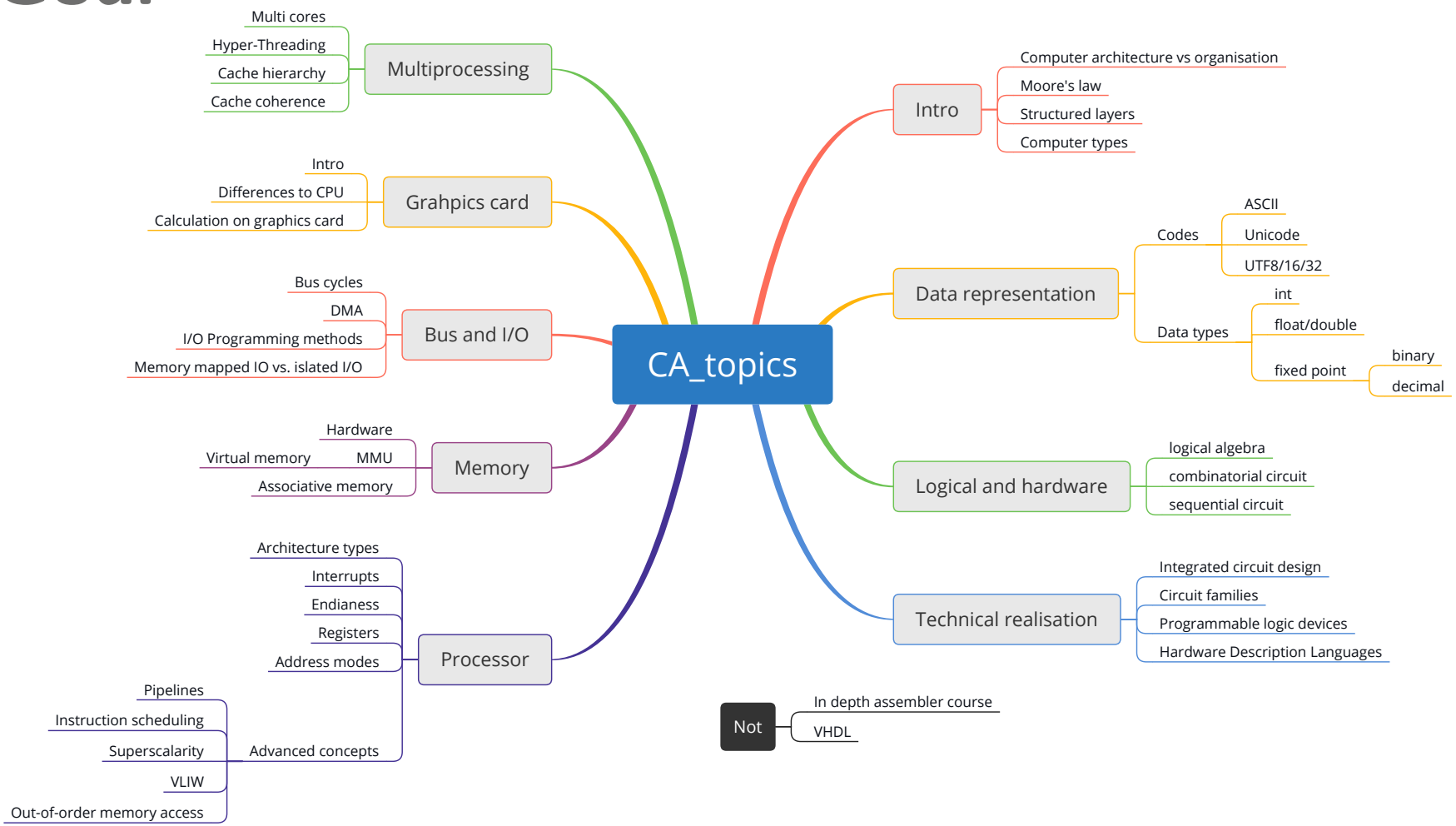
Goal



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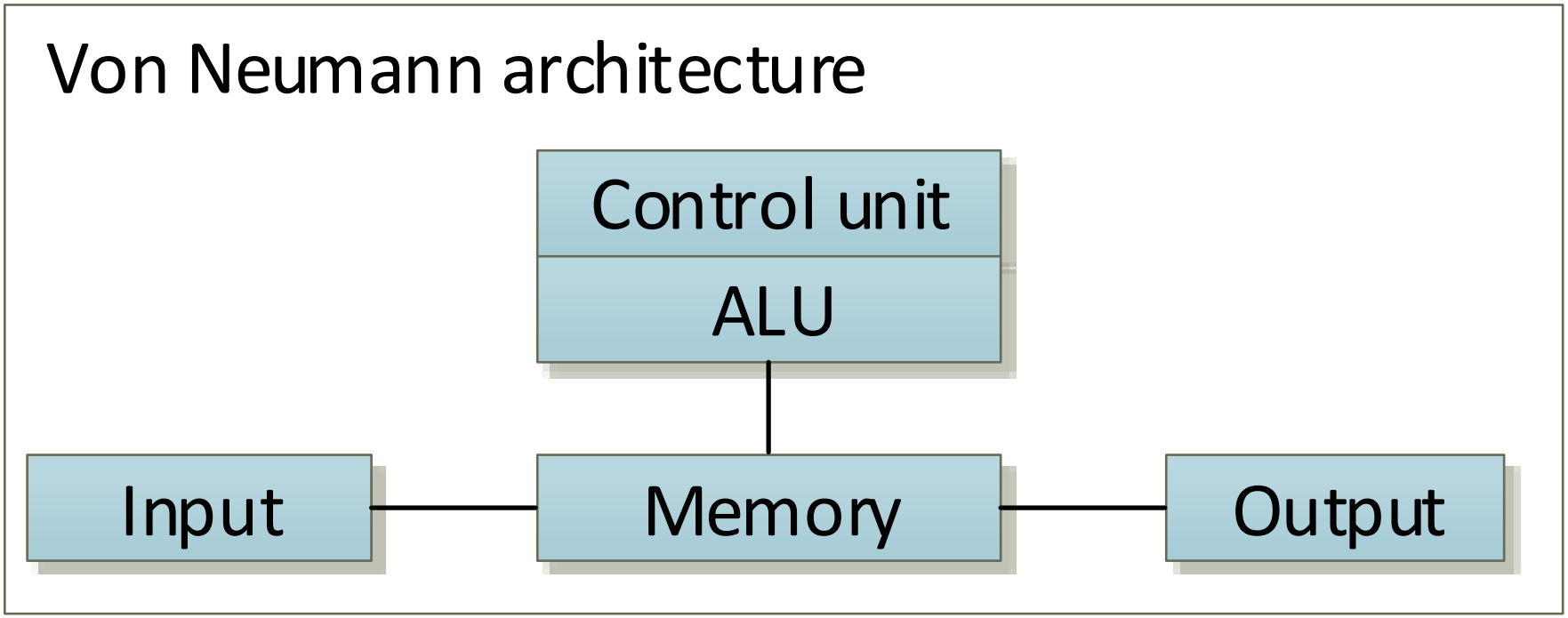
Goal

CA::Processor 1

- Processor architecture
- Exception and interrupt handling
- Instruction set architecture
- Endianness

Von Neumann architecture



[schematic, simplified view]

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Von Neumann architecture

Properties:

- **Instructions and data** are located in the **same memory** or address space
- Von Neumann – **bottleneck**:
  Command execution time $<$ **Memory access time**

Is the Von Neumann bottleneck still relevant?

In order to avoid and mitigate such problems, various strategies have been developed (e.g. cache memory)–but its still there!

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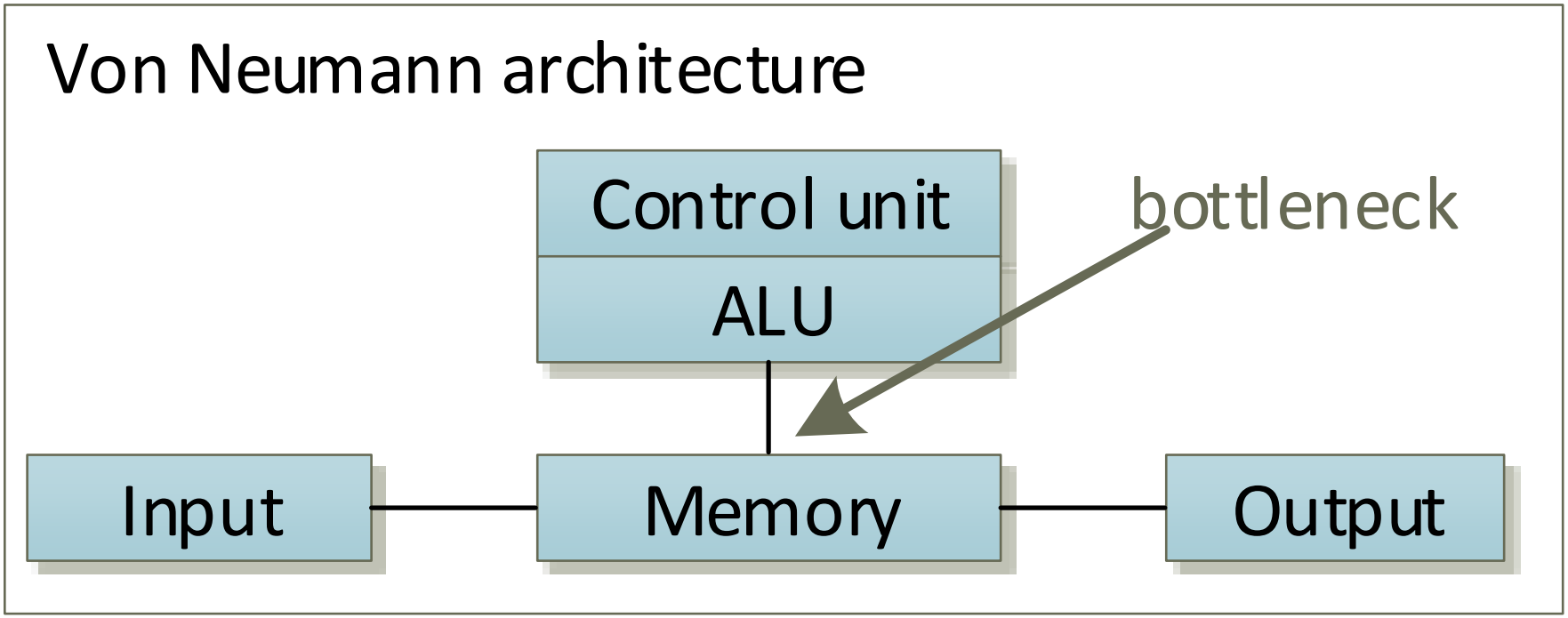
Von Neumann architecture – bottleneck



[schematic, simplified view]

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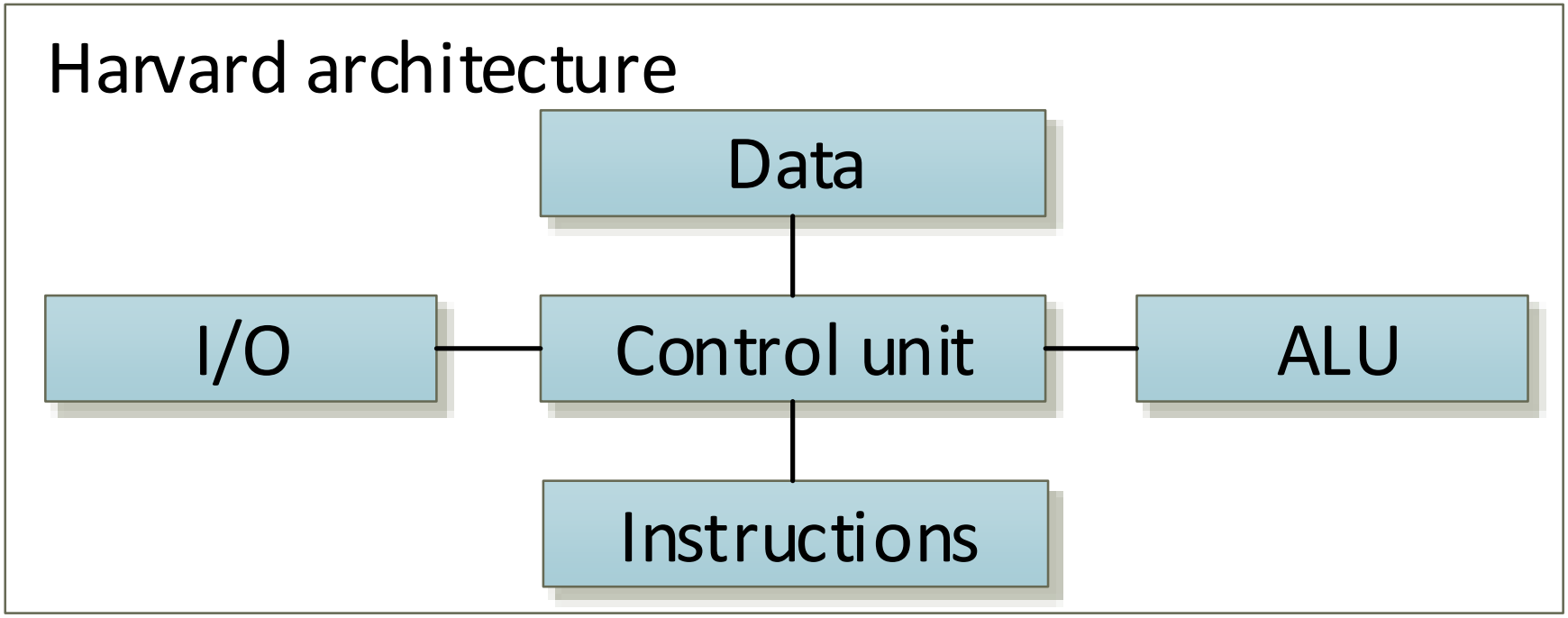
Harvard architecture



[schematic, simplified view]

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Harvard architecture

Properties:

- **Separate memory** for **data** and **instructions**
- **Data** memory is usually **read- and writeable**
- **Instruction** memory is usually **read-only**. Can't be modified through runtime

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Processor architecture

Discussion

Von Neumann vs. Harvard architecture: Does it play a role nowadays?

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Questions?

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Control unit

Pseudo C code of control unit inside the CPU:

```
while(true){
    fetch_next_command();
    decode_command();
    execute_command();
    if(interrupt_is_requested()) {
        save_PC_and_SR();
        load_new_PC();
    }
}
```

Instruction cycle: in principle, it's an **endless loop**

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Interrupts

What is an **interrupt**?

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Interrupt handling

An **interrupt request (IRQ)** causes the processor to **stop the current workflow** and to **process with a predefined interrupt service routine (ISR)**.

- **IRQ** -> **Interrupt request**
- **ISR** -> **Interrupt service routine**
- An ISR is a **function** that is called when an interrupt occurs
- It's just a **memory address** where the function (ISR) starts
- There exist **different types** of interrupts
- The ISR addresses are managed within the CPU with the **interrupt vector table**
- The **interrupt vector table** can be **manipulated** (e.g. in supervisor mode by the OS kernel)

Interrupt types

Name	Usual name	Reason, cause	Arrival	Comment
Reset	Reset	external	asynchronous	reset potentially at any point in an instruction
Interrupt	Real interrupt, IRQ	external (e.g. I/O)	asynchronous	is usually handled at the end of a command
Exception	Internal interrupt	internal (e.g. command error)	synchronous	is usually cancelled and may be repeated later
System call	SVC, supervisor call, Trap, Software interrupt	internal	synchronous	SVC n (n is the number of the SVC)
Timer	Timer, SysTick, Watchdog	external (clock)	asynchronous	is usually handled at the end of a command

...

[for example: ARM Cortex-M Exception handlers]

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Exceptions

Examples for exceptions:

- Division by zero
- Illegal command code
- Load or store to an unaligned address.
- Unauthorized memory access

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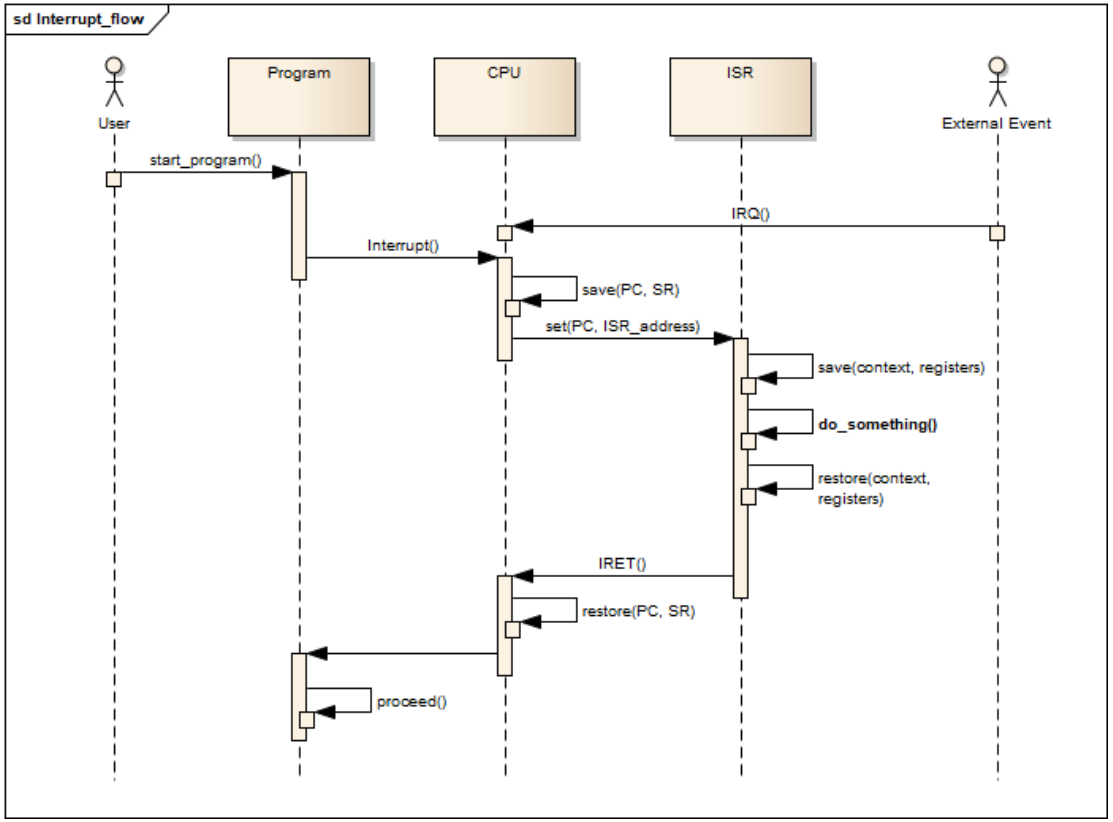
Interrupt flow



Sequence in the control unit

1. Save the old
   - PC (program counter) and
   - SR (status register)

   (e.g. on the stack)
2. Assign new values to
   - PC (program counter) and
   - SR (status register)

   from a fixed address ("interrupt vector")

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Interrupt vector table

Exception number	IRQ number	Vector	Offset
16+n	n	IRQn	0x40+4n
. . .		. . .	. . .
18	2	IRQ2	0x48
17	1	IRQ1	0x44
16	0	IRQ0	0x40
15	-1	SysTick, if implemented	0x3C
14	-2	PendSV	0x38
13		Reserved	
12			
11	-5	SVCall	0x2C
10		Reserved	
9			
8			
7			
6			
5			
4			
3	-13	HardFault	0x10
2	-14	NMI	0x0C
1		Reset	0x08
		Initial SP value	0x04
			0x00

- Example: **Cortex M0**
- Interrupt request (IRQ)
- For each IRQ one entry
- Each entry contains the address of an ISR

[source: Cortex-M0 Generic User Guide (2009), p. 2-22]

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Interrupt details

Who saves the registers?

- The CPU saves and restores PC and SR
- The ISR has to save the other registers at the beginning
- The ISR has to restore the other registers at the end
- Usually, the operating system does this (if you have one) in advance

Interruption in the middle of a command?

- Usually at the end of a CPU command
- But: exceptions can interrupt a running CPU command

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ISA - instruction set architecture

Do you know some common ISAs?

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ISA - instruction set architecture

The interface for low-level programming, very close to the hardware.

Degrees of freedom in instruction set architecture (ISA) design

Operations:	How many? Which? How complex?
Data types:	Which data types can the operations handle?
Command format:	Command length in bits? Number of addresses? Size of the address fields?
Register:	How many? Usable in which way?
Addressing:	Addressing types for the operands? Can be combined with the operations arbitrary ("orthogonal") or restricted?

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ISA - instruction set architecture

Command formats:

Command address	Example	Operands
Zero-address	`ADD`	Operands and result on stack!
One-address	`ADD X`	`A = A + X (A = "accu")`
Two-addresses	`ADD X, Y`	`X = X + Y or Y = X + Y`
Three-addresses	`ADD X, Y, Z`	`X = Y + Z or ...`

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ISA - special commands

Synchronization commands:

- TAS (test and set) or similar
- Tests a memory cell ($? = 0$) and sets it to one, if the test was successful.
- In the hardware single, atomic (i.e., non-interruptible) operation
- Uses a read-modify-write memory cycle that completes the operation without interruption.

Synchronisation area:

Area	Protection through
Critical area in a process	P and V operation
P-Operation in the operating system	TAS instruction (or similar)

In other architectures, partly different, more efficient, much more complicated solutions. Similar: Compare_and_Swap, keyword "Lock-free Programming".

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ISA - special commands: TAS

TAS example for Freescale ColdFire architecture

```
1  byte LOCK = 0; // =0 -> lock is free; !=0 -> locked
2
3  __asm { ;Inline assembly block with assembler instructions
4    GetLock:
5      TAS.B LOCK    ;Sets the N- or Z-Bit depending on LOCK and
6                    ;always sets LOCK = 0x80
7      BNE GetLock   ;If was LOCK != 0 then try it again (loop)
8                    ;(BNE, branch not equal)
9
10     ;Now we have the LOCK and we are inside the critical section
11     ;...
12
13   ReleaseLock:
14     CLR.B LOCK     // Sets LOCK = 0
15 }
```

ISA - CISC vs. RISC

CISC - complex instruction set computer

- Commands should be as close as possible to the high-level languages
- Can take a lot of internal CPU cycles for a command
- Support for a lot of addressing modes
- Allows compact encoding of programs (one command does a lot)

RISC - reduced instruction set computer

- Less, simple commands
- One commands should only take a few internal CPU cycles
- Supports only simple addressing modes (load/store necessary)
- Usually fixed length of opcodes

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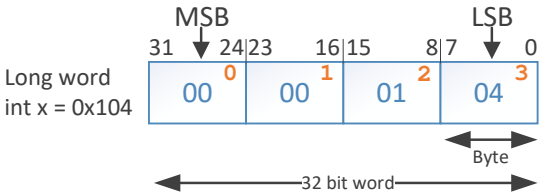
Endianness

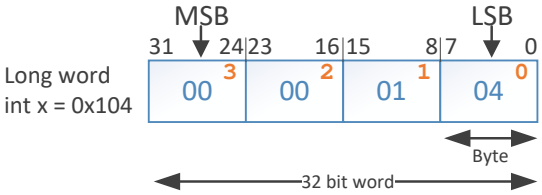
Endianness: The definition of the **byte order** within a **long word**.

Register view of a 32bit architecture:

Big Endian



Little Endian



- MSB - Most significant byte
- LSB - Least significant byte

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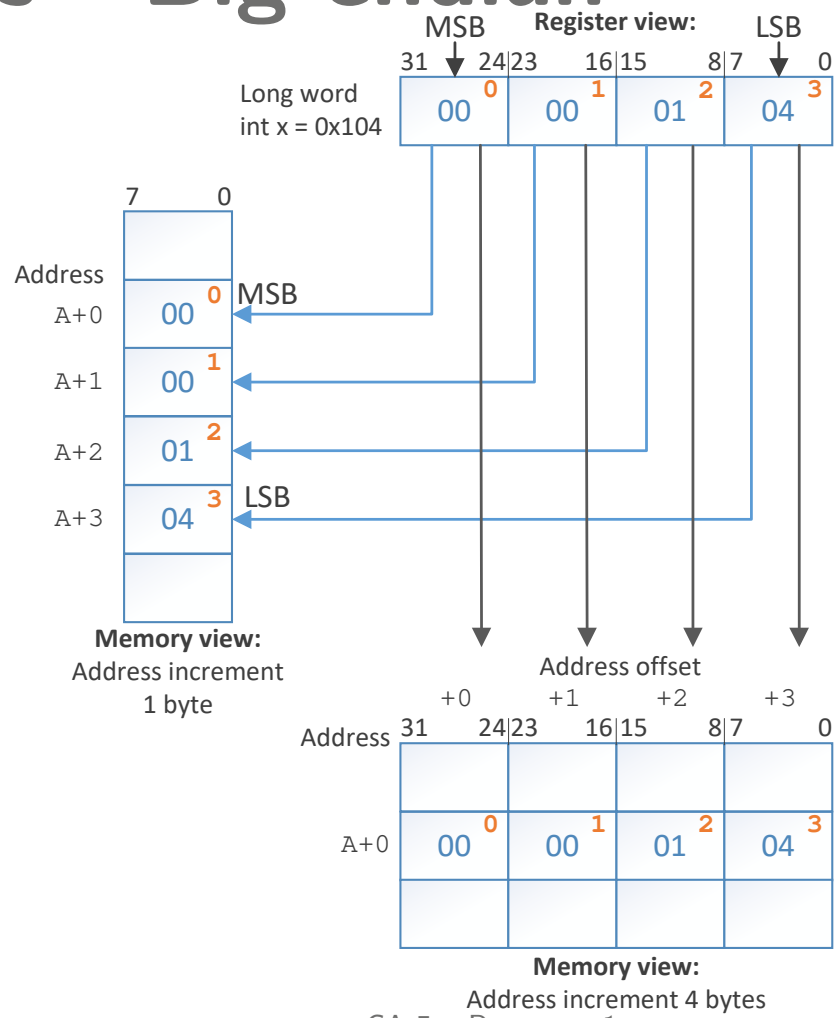
Endianness - Big endian



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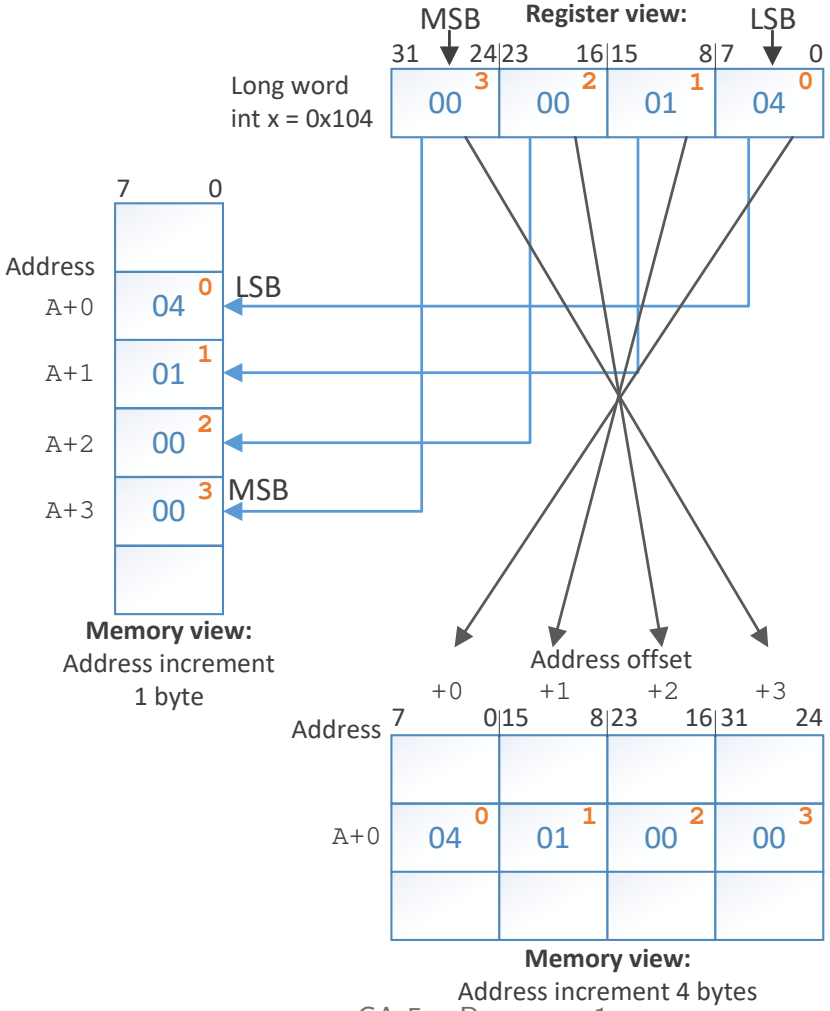
Endianness - Little endian



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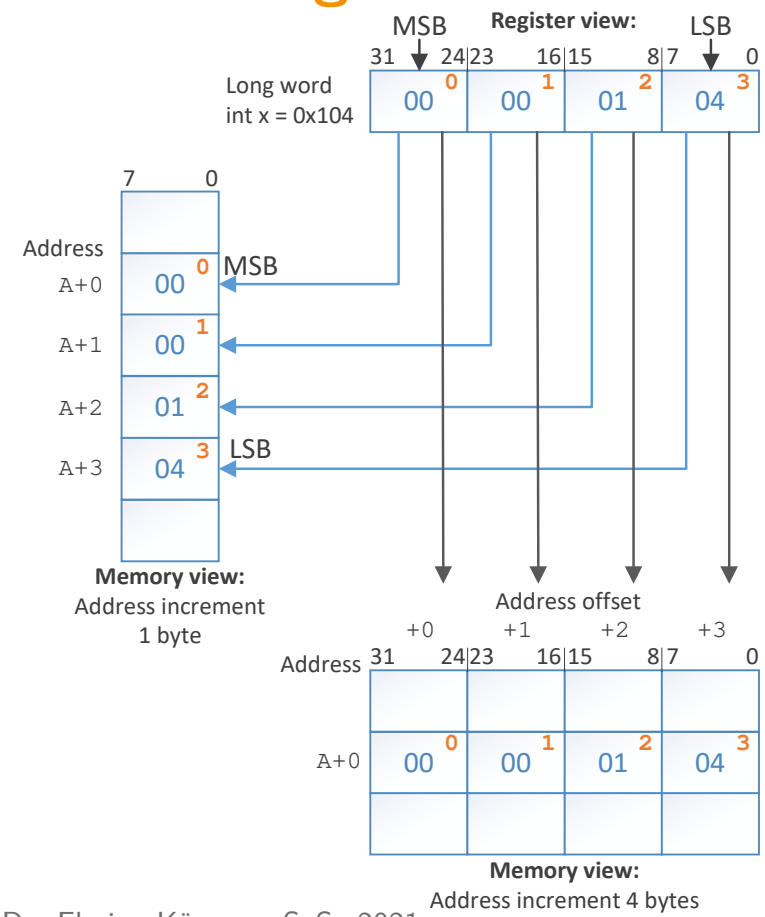
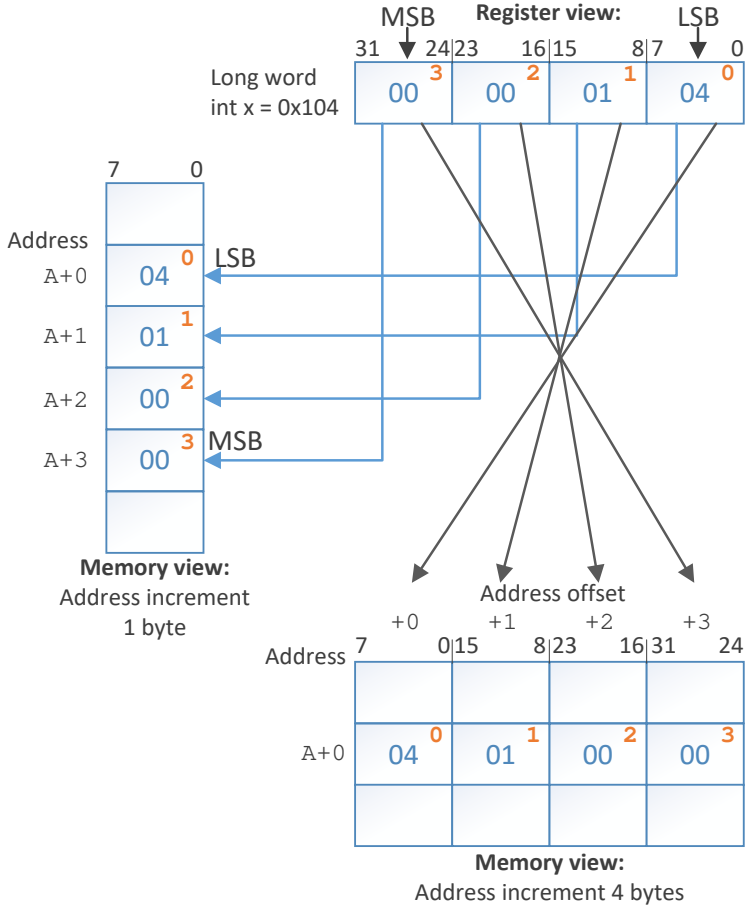
Endianness - BE/LE

Big endian



Little endian



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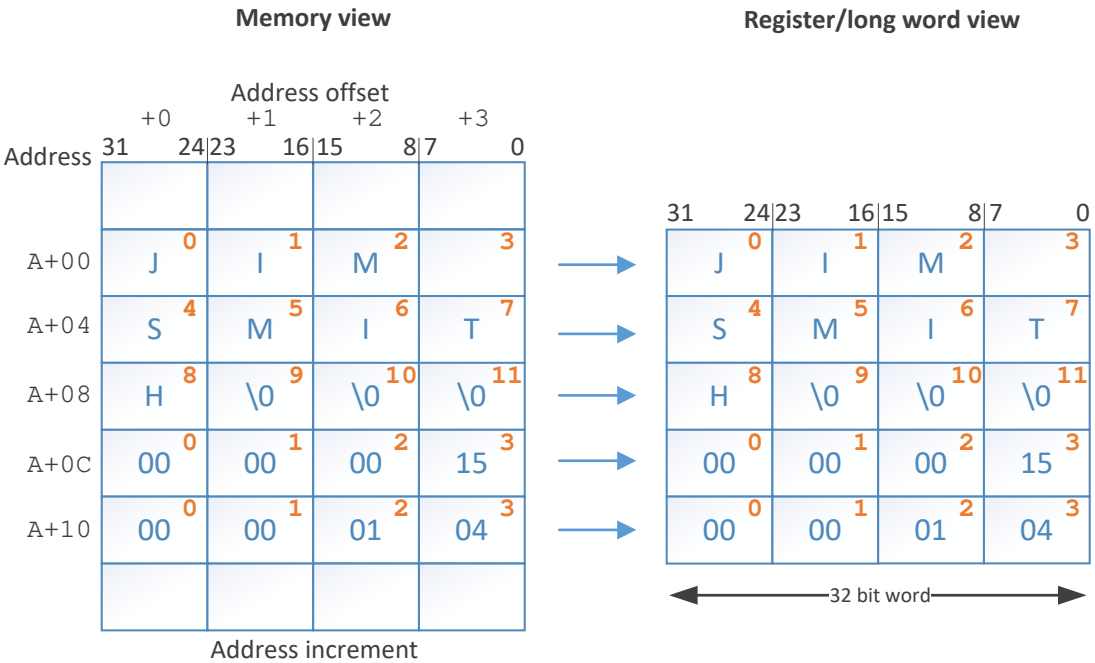
Endianness - example BE

```
1  #include <stdlib.h>
2  #include <stdint.h>
3
4  int main()
5  {
6      struct employee {
7          char     name[12];
8          uint32_t age;
9          uint32_t dept_nr;
10     };
11
12     struct employee smith = {
13         .name    = "JIM SMITH",
14         .age     = 21,    //0x15
15         .dept_nr = 0x104 //260
16     };
17
18     return EXIT_SUCCESS;
19 }
```

Big endian memory -> Register



[cmp: [1, p. 95-96]]]

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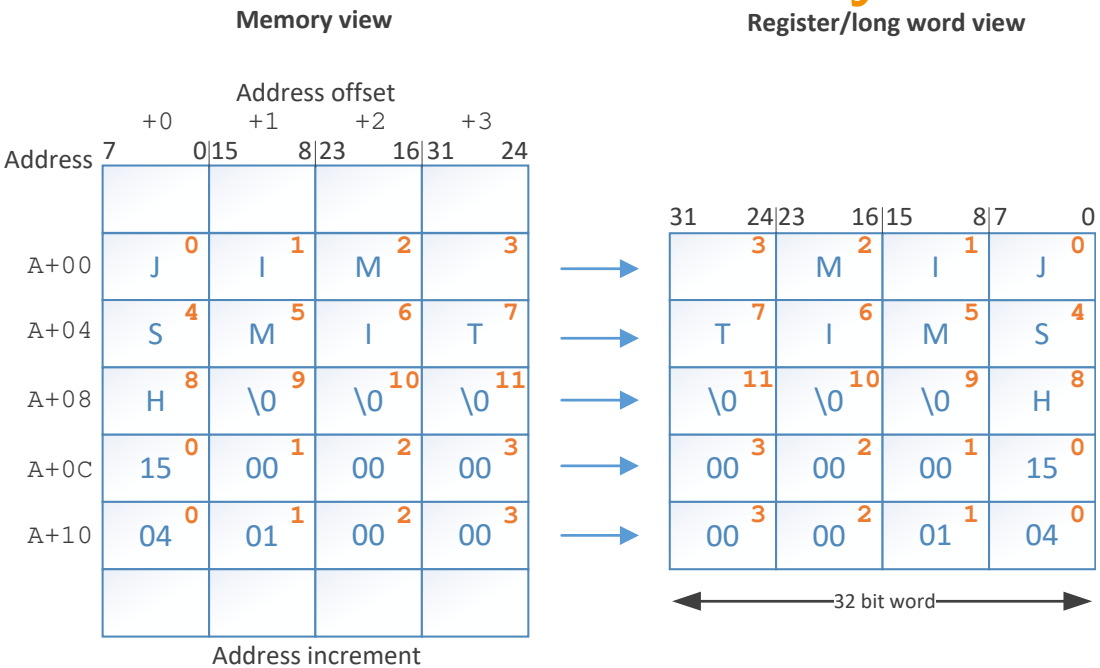
Endianness - example LE

```
1  #include <stdlib.h>
2  #include <stdint.h>
3
4  int main()
5  {
6      struct employee {
7          char     name[12];
8          uint32_t age;
9          uint32_t dept_nr;
10     };
11
12     struct employee smith = {
13         .name    = "JIM SMITH",
14         .age     = 21,    //0x15
15         .dept_nr = 0x104 //260
16     };
17
18     return EXIT_SUCCESS;
19 }
```

[cmp: [1, p. 95-96]]]

Little endian memory



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Endianness - example BE/LE

Big endian memory

Address offset

Address	+0 (31 … 24)	+1 (23 … 16)	+2 (15 … 8)	+3 (7 … 0)
A+00	J 0	I 1	M 2	3
A+04	S 4	M 5	I 6	T 7
A+08	H 8	\0 9	\0 10	\0 11
A+0C	00 0	00 1	00 2	15 3
A+10	00 0	00 1	01 2	04 3

Address increment
4 bytes

Little endian memory

Address offset

Address	+0 (7 … 0)	+1 (15 … 8)	+2 (23 … 16)	+3 (31 … 24)
A+00	J 0	I 1	M 2	3
A+04	S 4	M 5	I 6	T 7
A+08	H 8	\0 9	\0 10	\0 11
A+0C	15 0	00 1	00 2	00 3
A+10	04 0	01 1	00 2	00 3

Address increment
4 bytes

[cmp: [1, p. 95-96]]]

Endianness - usage

Big endian

- IBM Mainframe
- Freescale ColdFire
- Atmel AVR/AVR32
- ARM Thumb and ARM64 (also Apple M1)

Little endian

- Intel x86
- x86-64 (AMD64, Intel 64)
- RISC-V
- Qualcomm Hexagon

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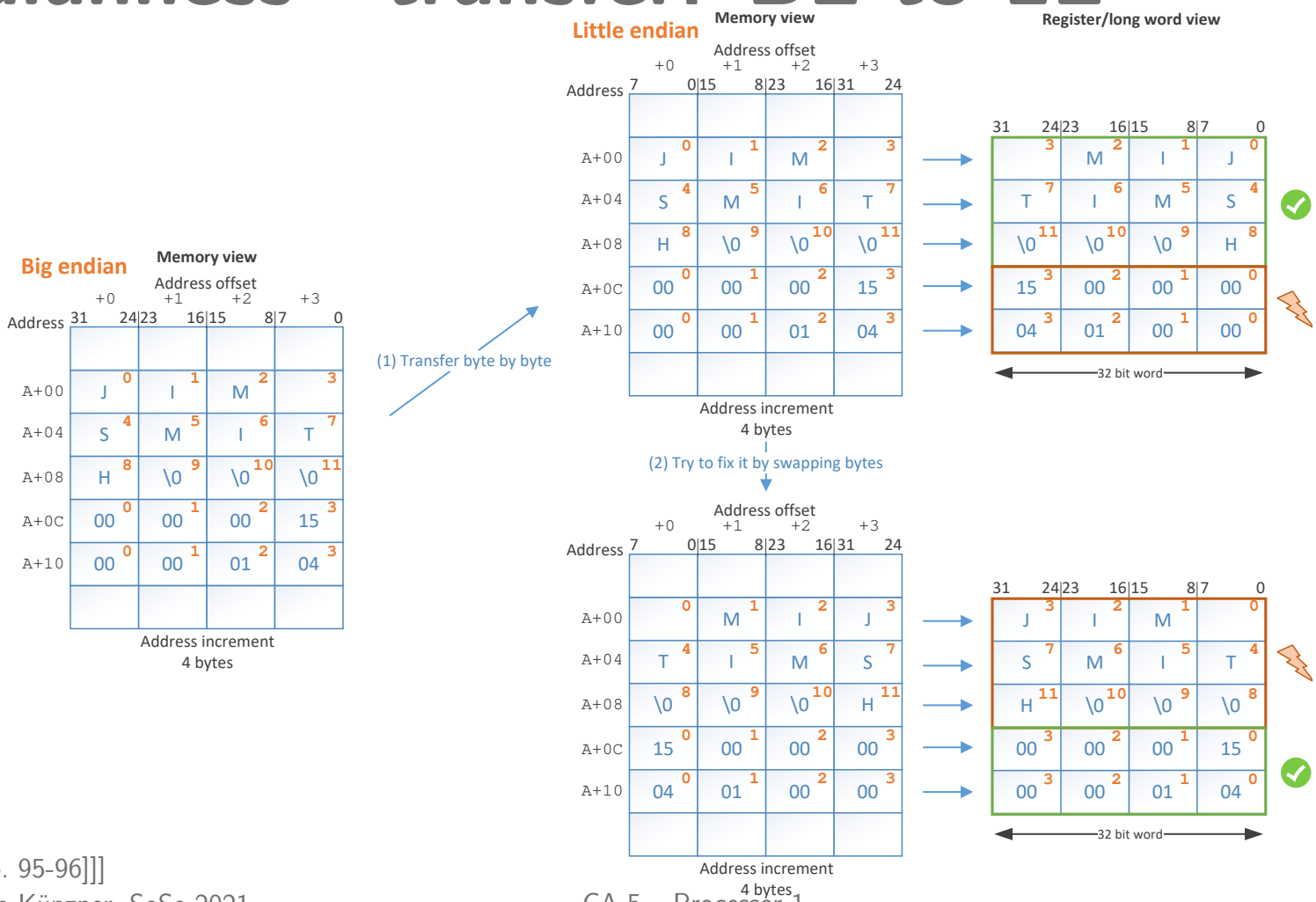
Endianness - transfer: BE to LE



[cmp: [1, p. 95-96]]]

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Endianness - problem

Problem can occur if

- Different data types are mixed: numbers, strings, or other data types
- Data type consists of more than one byte (multi byte, ≥ 2)
- Data are transferred between BE/LE systems

No problem occurs if

- Single byte data is transferred byte by byte (e.g. ASCII)
- Data is transferred within same endianness (LE -> LE, BE -> BE)

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Endianness - conclusion

Without the knowledge about the data types and the alignment, a transfer between BE/LE systems is not feasible.

Tanenbaum: „*There is no easy solution to this*“ [1, p. 96]

Endianness - possible solutions

Possible solution

- **Know** the endianness (e.g. **meta data!**)
- **Transfer** byte by byte (no problem for single byte data)
- If endianness is different and a long word ist transferred: additionally **swap** the bytes

Some examples:

- Network order: always BE
- Java: always BE; for transfer with others, `ByteOrder` can be set
- Unicode UTF-16/32: uses a BOM (byte order mark)
- TIF files: BE/LE identifier in header
- RPC (remote procedure call): marshalling (data as byte stream) solves the problem by using meta data

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Summary and outlook

Summary

- Processor architecture
- Exception and interrupt handling
- Instruction set architecture
- Endianness

Outlook

- Processor registers
- Processor examples
- Addressing modes