Prof. Dr. Florian Künzner

Technical University of Applied Sciences Rosenheim, Computer Science

Start: 8:01

CA 7 – Processor 3

The lecture is based on the work and the documents of Prof. Dr. Theodor Tempelmeier

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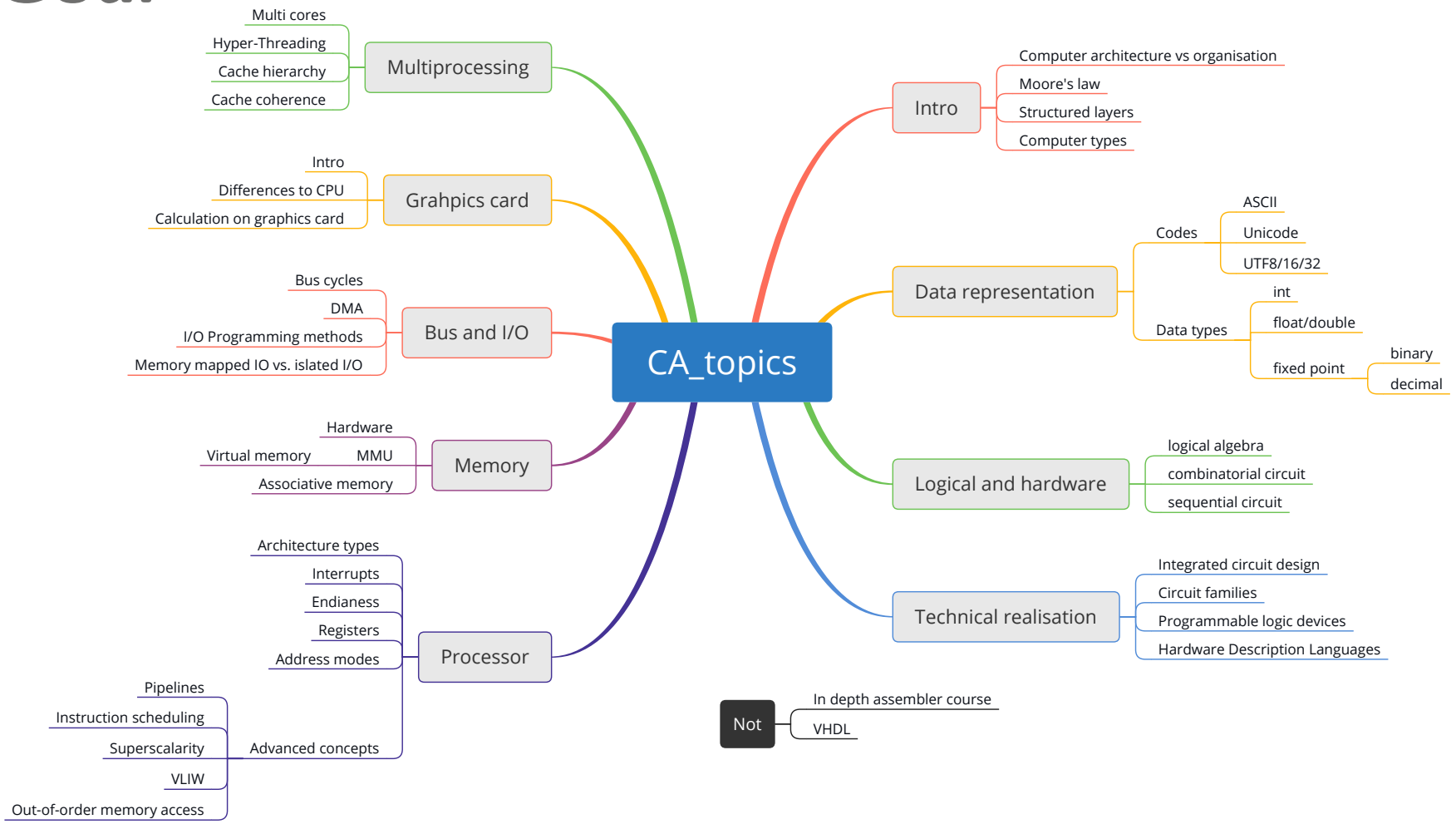
Goal



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Modern CPU techniques

Why are modern (single core) processors so fast nowadays?

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Goal

CA::Processor 3

- Pipelining
- Instruction scheduling
- Superscalar architecture
- VLIW
- Out-of-order memory access

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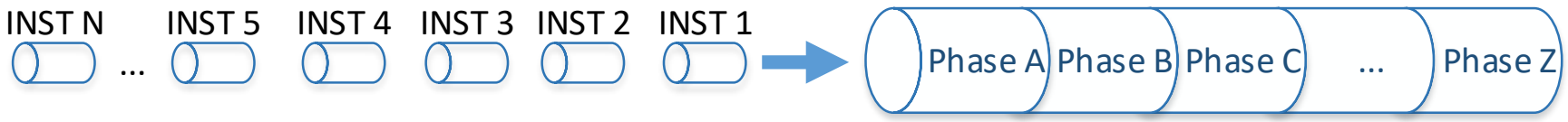
Pipelining



Idea of pipelining:

- Splitting an instruction processing cycle into individual phases
- Processing of these phases in subsequent stations
- Instructions run through the individual steps
- Each step does a partial processing of an instruction
- Time overlap of instruction processing!

Pipelining is done in hardware!

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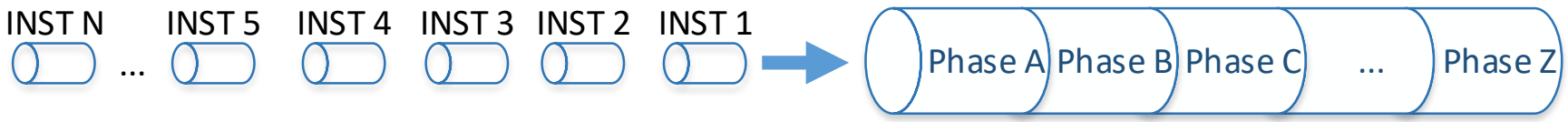

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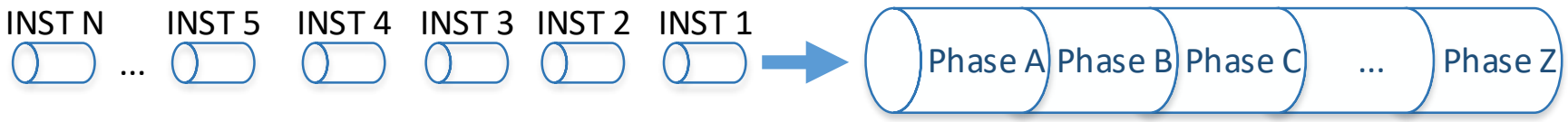

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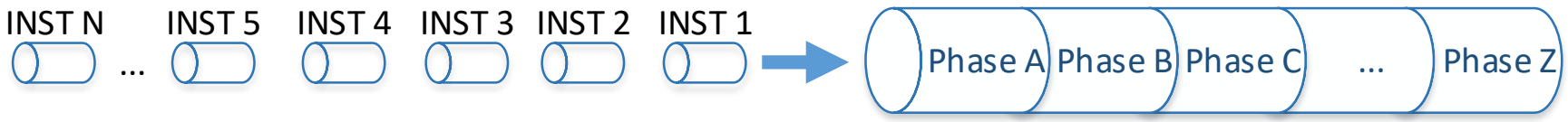

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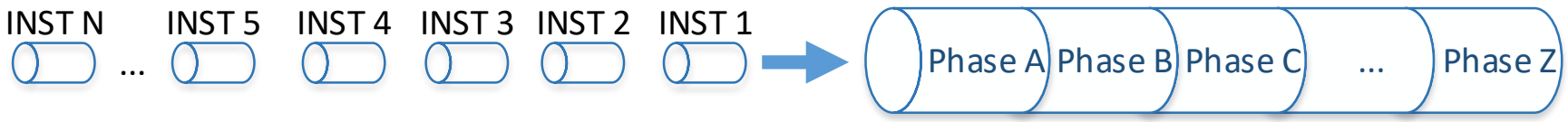

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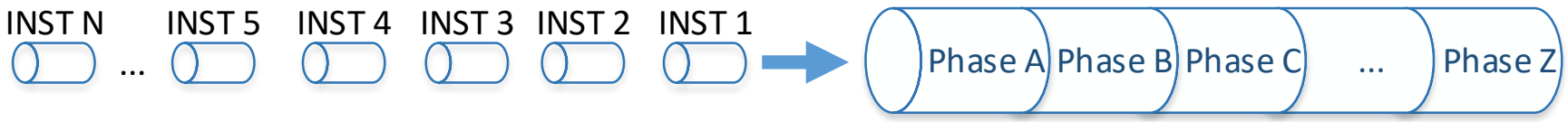

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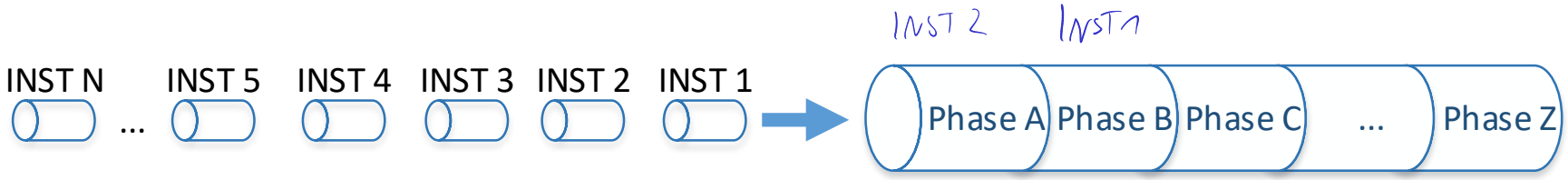

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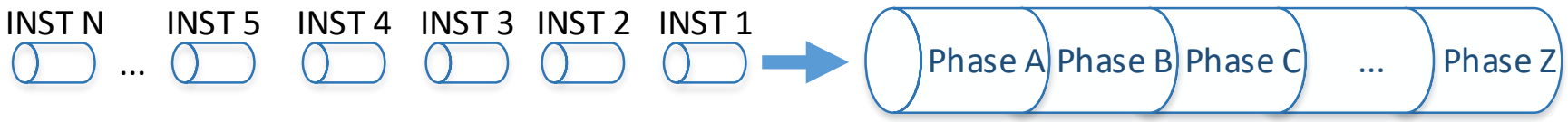

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Pipelining - example

This is a very simplified (classical RISC) pipeline, since modern processors contain many more pipeline phases.

1. Fetch instruction	2. Load operands	3. Execute instruction	4. Memory access	5. Save result into register	
INST 1					t_1
INST 2	INST 1				t_2
INST 3	INST 2	INST 1			t_3
INST 4	INST 3	INST 2	INST 1		t_4
INST 5	INST 4	INST 3	INST 2	INST 1	t_5
INST 6	INST 5	INST 4	INST 3	INST 2	t_6

time

Processing

- The processing of an instruction takes 5 clock cycles.
- On each clock cycle one instruction is started and one ends
- Without pipelining: Every 5 clock cycles, an instruction would be started and ended.

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Pipelining - Problems

The execution of instructions in a pipeline is disturbed by:

- Jump instructions
- Interrupts
- Data dependencies (the next instruction requires data from the previous)

Special hardware is often available for this purpose, in order to **minimize the disruption of the pipeline** as much as possible:

- On conditional jumps: Instructions for both alternatives are fetched and evaluated
- A kind of cache remembers which alternative from the past seems more likely (**branch prediction**)
- Try to avoid conditional jumps–instead use **conditional instructions** (e.g. `CMOV`, `MOVCC`)

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Questions?

All right? ⇒ 

Question? ⇒  and use **chat**

or

speak *after* I ask you to

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Instruction scheduling

Idea: **The Compiler changes the order of the instructions**

- Change the processing order of the instructions to **maximize** the **pipeline utilisation**
- Important: The **semantics** of the high-level language program **remains intact** (as-if rule).

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Instruction scheduling - Example

Unscheduled:

Nr	Opcode	Operand	Comment	C code

[source (with changes): Alsup: Motorola's 88000 Family Architecture, IEEE Micro, June 1990]

Pipeline (with 4 phases):

Fetch	Load	Execute	Save	
				t_1
				t_2
				t_3
				t_4
				t_5
				t_6
				t_7
				t_8
				t_9
				t_{10}
				t_{11}
				t_{12}
				t_{13}
				t_{14}
				t_{15}
				t_{16}
				t_{17}
				t_{18}
				t_{19}
				t_{20}
				t_{21}
				t_{22}

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Instruction scheduling - Example

Unscheduled:

Nr	Opcode	Operand	Comment	C code
1	LOAD	R7, (R30)	R7 = (R30)	
2	ADD	R7, R7, 1	R7 = R7+1	x++;
3	STORE	R7, (R30)	(R30) = R7	

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4	LOAD	R8, (R31)	R8 = (R31)	
5	ADD	R8, R8, 4	R8 = R8+4	y += 4;
6	STORE	R8, (R31)	(R31) = R8	

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7	CMP	R10, R6, R2	R10 = R6 < R2	if(R6 < R2)
8	BLT	R10, M	GOTO M if R10 < 0	GOTO M;

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Pipeline (with 4 phases):

Fetch	Load	Execute	Save	
1				t_1
2	1			t_2
2	–	1		t_3
2	–	–	1	t_4
3	2	–	–	t_5
3	–	2	–	t_6
3	–	–	2	t_7
4	3	–	–	t_8
5	4	3	–	t_9
5	–	4	3	t_{10}
5	–	–	4	t_{11}
6	5	–	–	t_{12}
6	–	5	–	t_{13}
6	–	–	5	t_{14}
7	6	–	–	t_{15}
8	7	6	–	t_{16}
8	–	7	6	t_{17}
8	–	–	7	t_{18}
–	8	–	–	t_{19}
–	–	8	–	t_{20}
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-	-	2	-	t_6
-	-	-	2	t_7
4	3	-	-	t_8
5	4	3	-	t_9
-	-	4	3	t_{10}
-	-	-	4	t_{11}
6	5	-	-	t_{12}
-	-	5	-	t_{13}
-	-	-	5	t_{14}
7	6	-	-	t_{15}
8	7	6	-	t_{16}
-	-	7	6	t_{17}
-	-	-	7	t_{18}
-	8	-	-	t_{19}
-	-	8	-	t_{20}
-	-	-	8	t_{21}
M				t_{22}

Total clock cycles: **21**

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Instruction scheduling - Example

Scheduled:

Nr	Opcode	Operand	Old order
1	LOAD	R7, (R30)	1
2	CMP	R10, R6, R2	7
3	LOAD	R8, (R31)	4
4	ADD	R7, R7, 1	2
5	ADD	R8, R8, 4	5
6	STORE	R7, (R30)	3
7	BLT	R10, M	8
8	STORE	R8, (R31)	6

[source (with changes): Alsup: Motorola's 88000 Family Architecture, IEEE Micro, June 1990]

Pipeline (with 4 phases):

Fetch	Load	Execute	Save	
1				t_1
2	1			t_2
3	2	1		t_3
4	3	2	1	t_4
5	4	3	2	t_5
5	–	4	3	t_6
6	5	–	4	t_7
7	6	5	–	t_8
8	7	6	5	t_9
–	8	7	6	t_{10}
–	–	8	7	t_{11}
–	–	–	8	t_{12}
M				t_{13}

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8	7	6	5	t_9
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-	-	8	7	t_{11}
-	-	-	8	t_{12}
M				t_{13}

Total clock cycles: **12**

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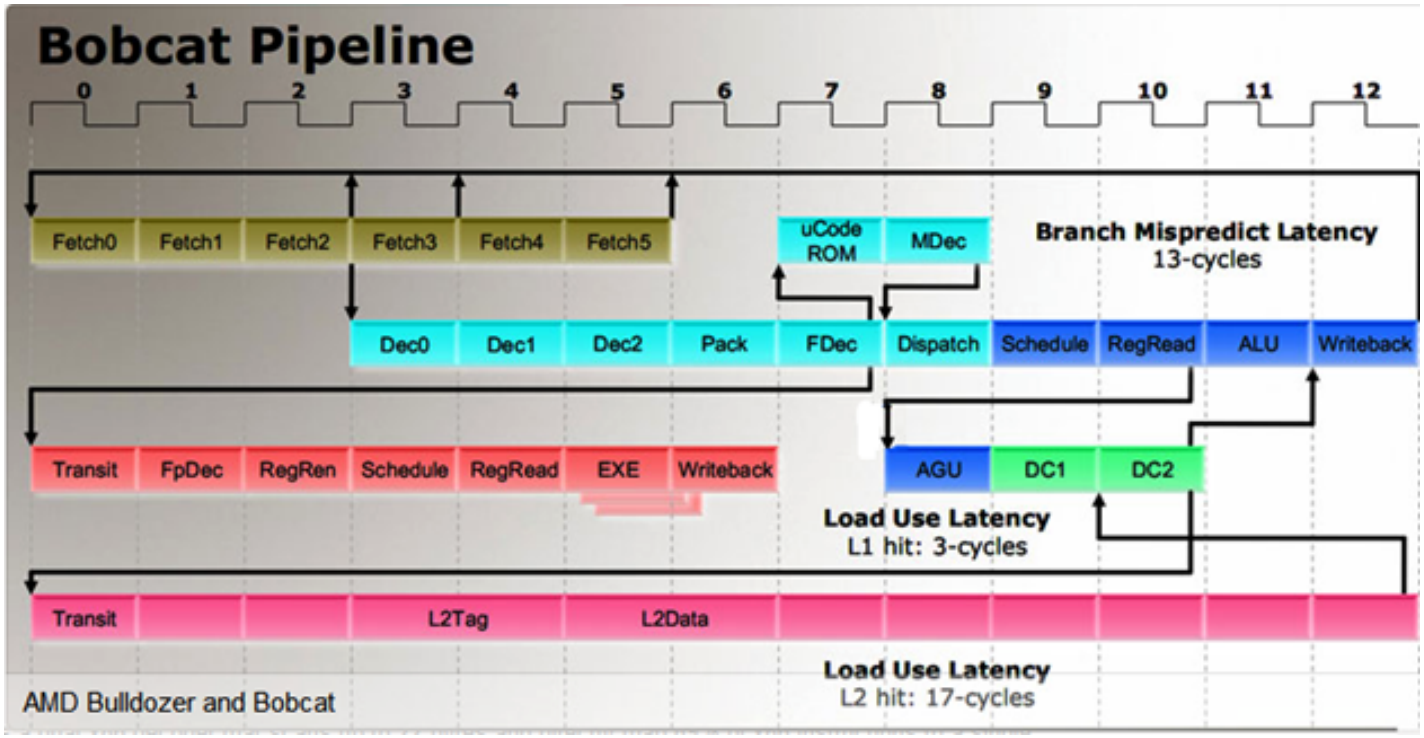
Example: AMD Bobcat pipelining



[Source: AMD Bobcat & Bulldozer Hot Chips Presentations 2011, available on youtube, last access 6.3.2015; Presentation: AMD Bobcat]

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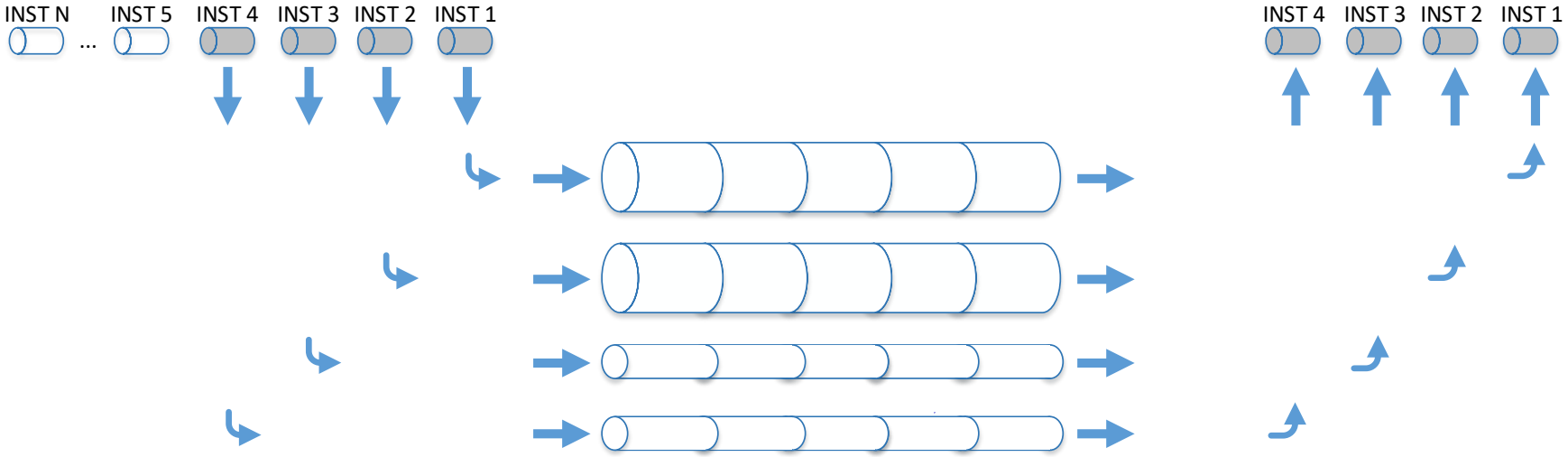
Superscalar architecture



Superscalar architecture:

- The CPU provides **several pipelines**
- The pipelines may be specialised for integer or floating point operations
- The CPU loads **multiple instructions** at each clock cycle
- Everything is done automatically inside the CPU: **programming model stays unchanged.**

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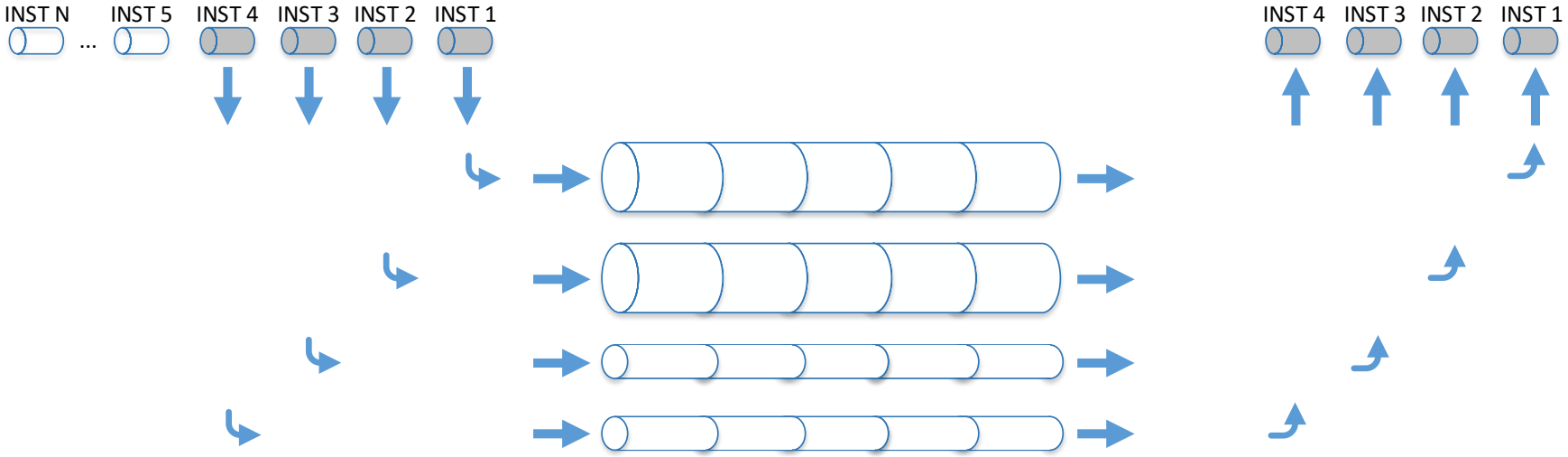

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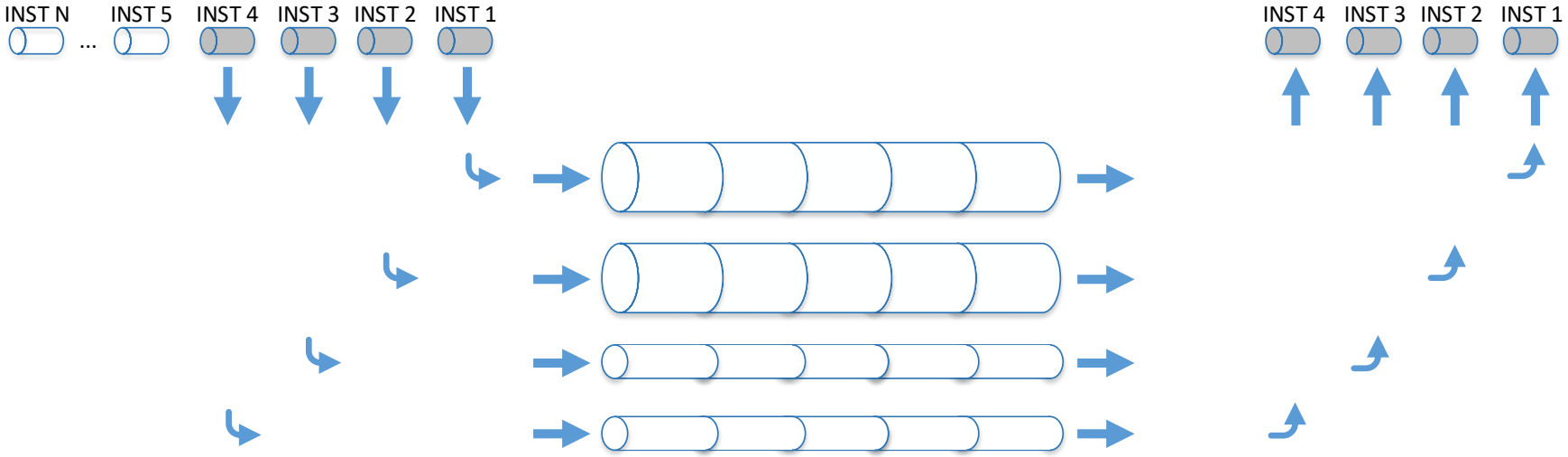

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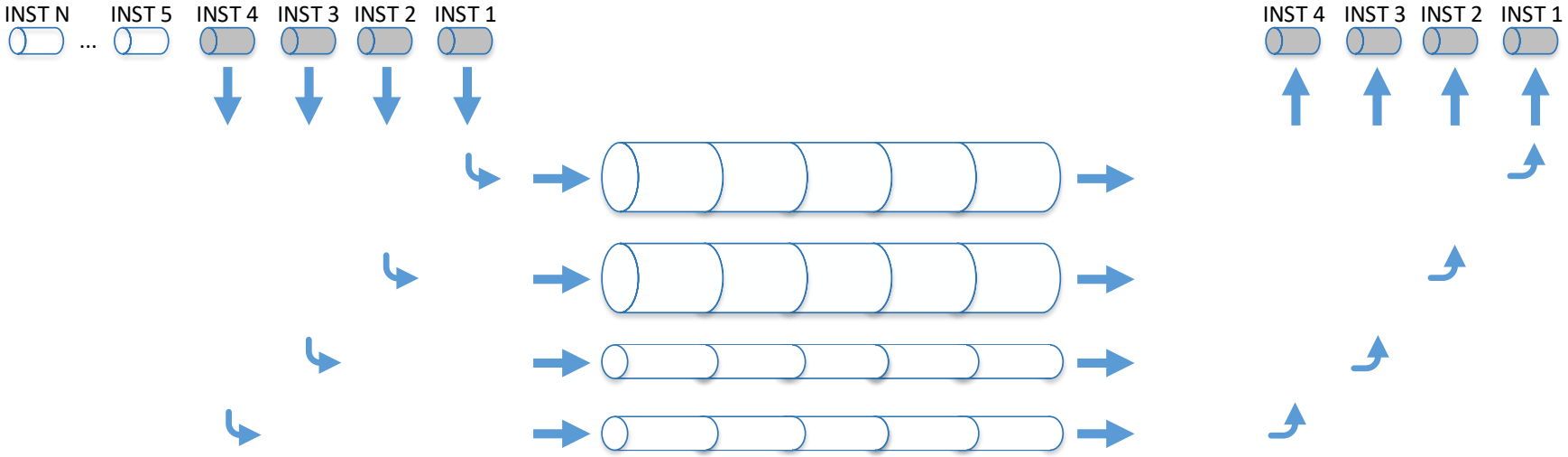

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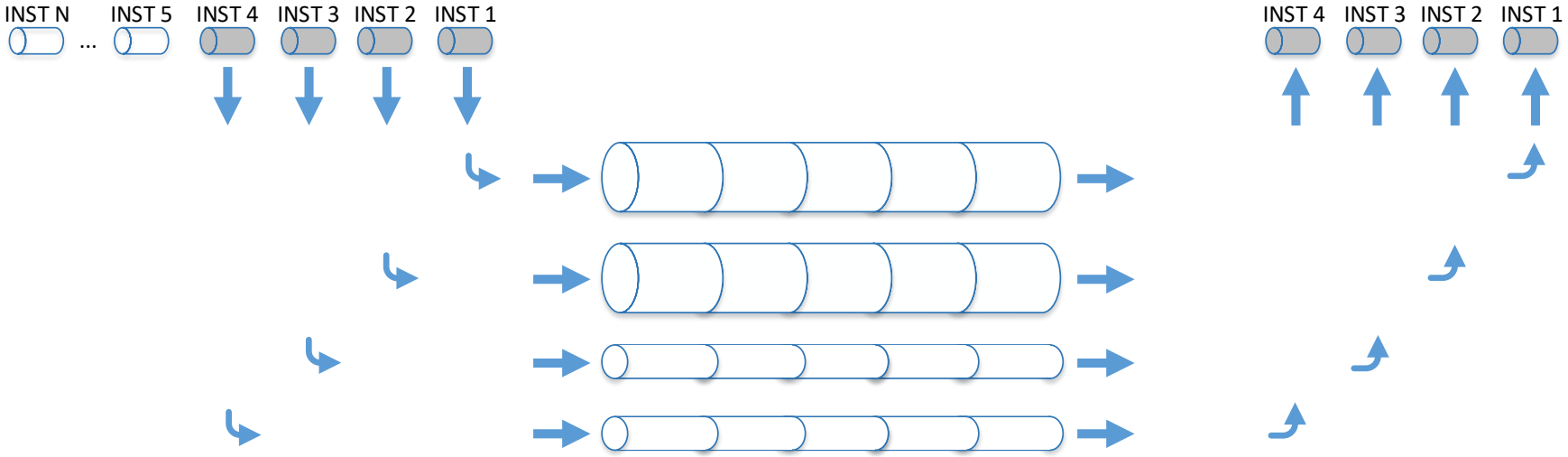

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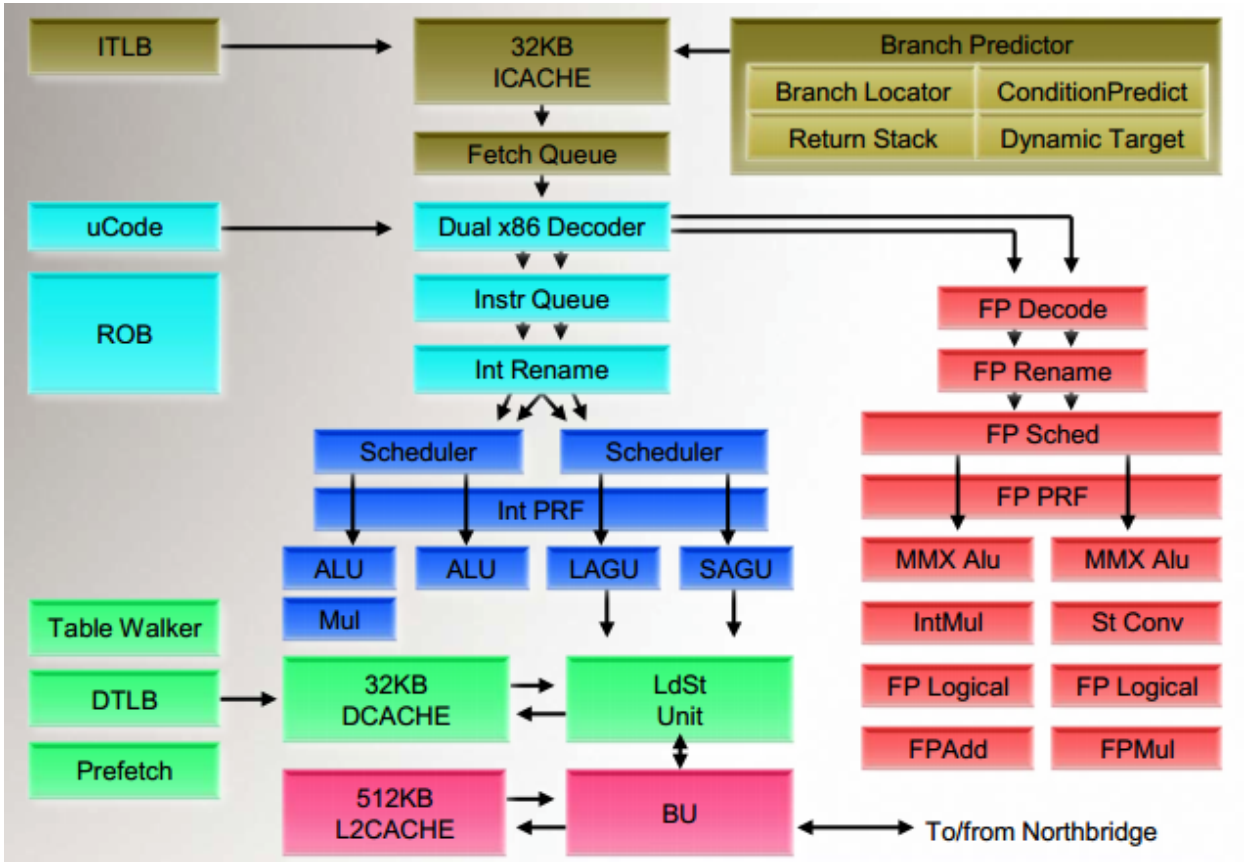
Example: AMD Bobcat superscalarity



[Source: AMD Bobcat & Bulldozer Hot Chips Presentations 2011, available on youtube, last access 6.3.2015]
Notice: AGU = address generation units, LAGU = AGU for loading operations, SAGU = AGU for storage operations

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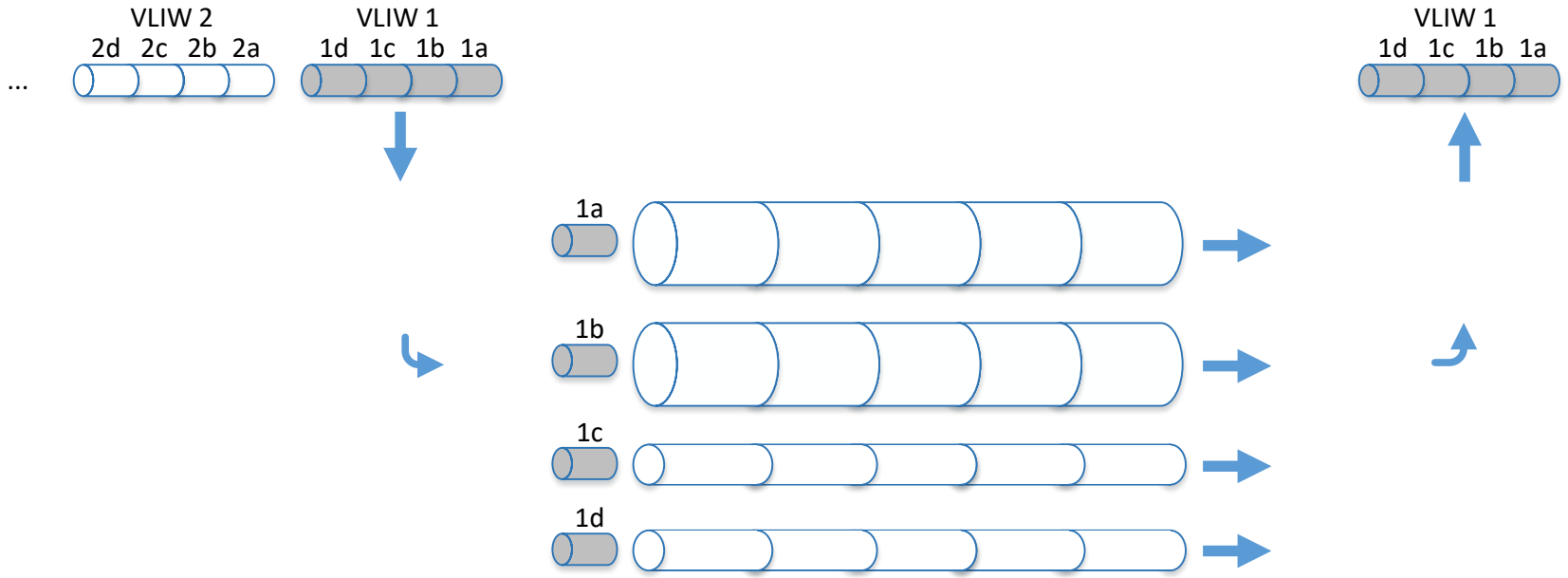
VLIW - Very Long Instruction Word



VLIW architecture:

- Parallel **operations are packed** into a very long instruction
- Packing is done by the **compiler at compile time**: **programming model changed!**
- The partial instructions of a VLIW must correspond to the functional units of the hardware.
- Its used by the **Intel Itanium** architecture (EPIC - Explicitly parallel instruction computer)

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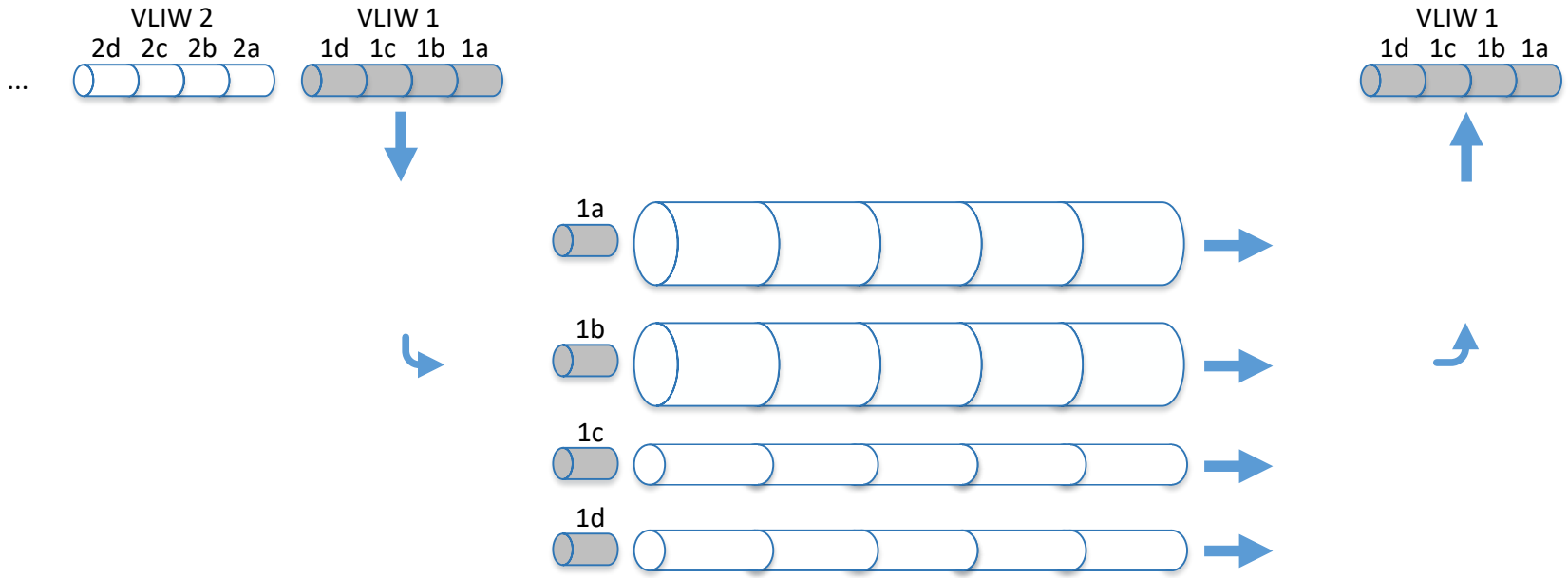

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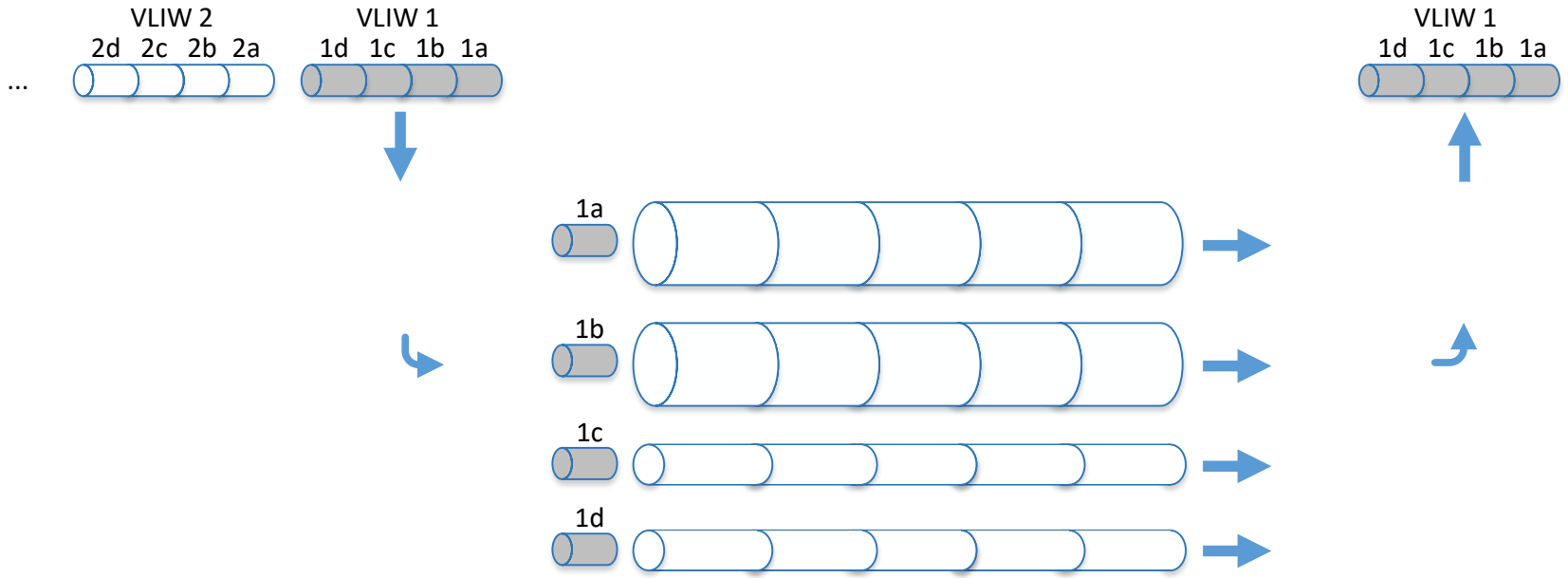

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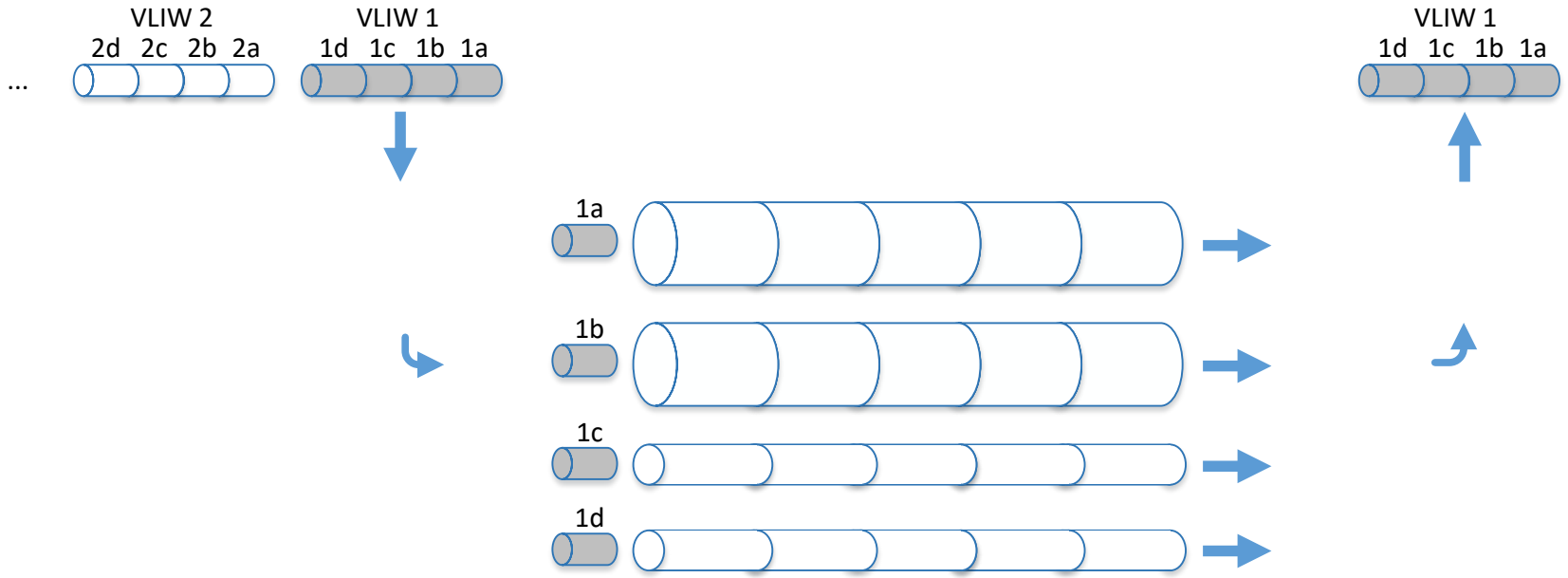

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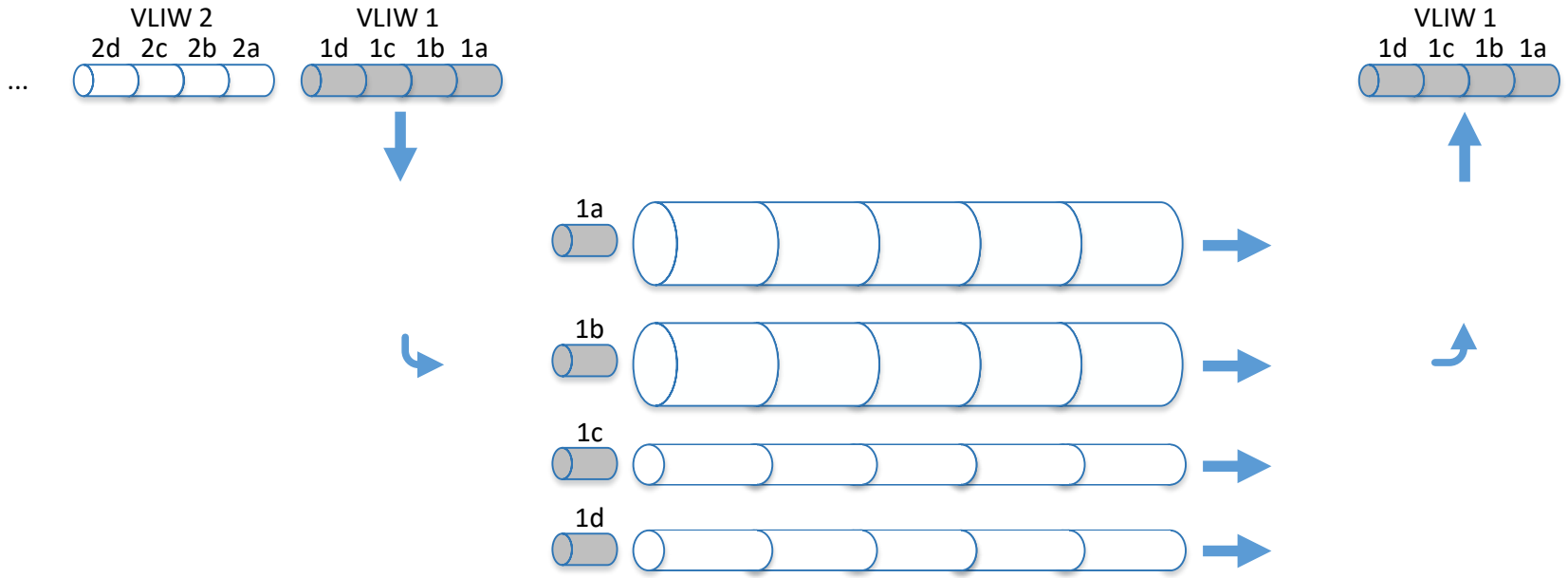

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Out-of-order memory access

Idea: The **hardware (CPU) changes the order of the instructions**: with the goal to better utilise the hardware

Details:

- Memory access (instruction) is **not** done in the specified order
- Some accesses are "**too early**" (e.g. speculative load)
- Some accesses are "**too late**" (e.g. posted writes)
- Attention: The **semantics must be guaranteed**!

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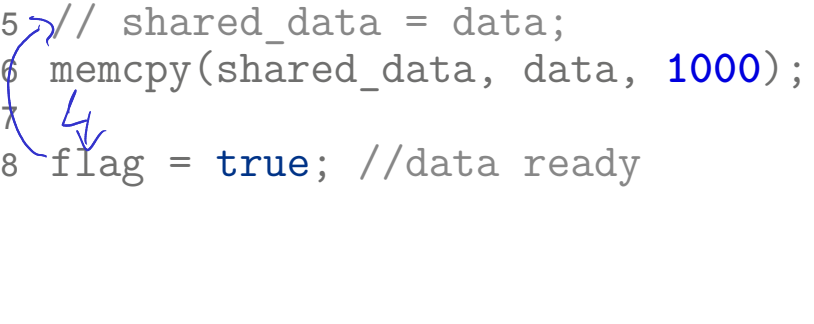
Out-of-order memory access - Example

Core 1: (producer)

```
1 byte data[1000];
2 byte shared_data[1000];
3 bool flag = false;
4
5 // shared_data = data;
6 memcpy(shared_data, data, 1000);
7
8 flag = true; //data ready
```

Core 2: (consumer)

```
1  byte data_copy[1000];
2  byte* shared_data; //attach
3  bool* flag;        //attach
4
5
6
7
8
9  while (flag != true) {} //busy wait
10
11 // data_copy = shared_data;
12 memcpy(data_copy, shared_data, 1000);
```



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Out-of-order memory access - Problem

Problem: Through **asynchronous execution** units (threads, processes, interrupts, ...), the out-of-order memory access can cause **unpredictable behaviour** in (concurrent programs, device drivers).

Prevent hardware from reordering

- Use of a **memory barrier**: a special hardware instruction (`memory_barrier`, `FENCE`)
- Forces the completion of all outstanding (instructions) memory accesses

Prevent compiler from reordering (instruction scheduling)

- Use of the `volatile` keyword in C
- Forces the compiler to
  - not omit reads from and writes to variable memory locations
  - not change reads/writes relative to other reads or writes to the same volatile location
- Notice: The `volatile` keyword does not prevent the hardware to reorder instructions

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Out-of-order memory access - Problem

Problem: Through **asynchronous execution** units (threads, processes, interrupts, ...), the out-of-order memory access can cause **unpredictable behaviour** in (concurrent programs, device drivers).

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Out-of-order memory access - Example

Core 1: (producer)

```
1  byte data[1000];
2  volatile byte shared_data[1000];
3  volatile bool flag = false;
4
5  // shared_data = data;
6  memcpy(shared_data, data, 1000);
7  __asm { memory_barrier }
8  flag = true; //data ready
```

Core 2: (consumer)

```
1  byte data_copy[1000];
2  volatile byte* shared_data;  //attach
3  volatile bool* flag;         //attach
4
5
6
7
8
9  while (flag != true) {} //busy wait
10 __asm { memory_barrier }
11 // data_copy = shared_data;
12 memcpy(data_copy, shared_data, 1000);
```

- The use of `__asm { memory_barrier }` and `volatile` should fix the problem.
- **Best solution**: use of a **semaphore** or a monitor, then all this is already solved for you (by OS software).

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Overview

Technique	How	Unit	Time

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Overview

Technique	How	Unit	Time
Pipelining	parallelisation of parts of an instruction	hardware	runtime

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Technique	How	Unit	Time
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Superscalarity	parallelisation on instruction level	hardware	runtime

Overview

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Pipelining	parallelisation of parts of an instruction	hardware	runtime
Instruction scheduling	reordering of instructions	compiler	compile time
Superscalarity	parallelisation on instruction level	hardware	runtime
VLIW	parallelisation on instruction level	compiler	compile time

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Technique	How	Unit	Time
Pipelining	parallelisation of parts of an instruction	hardware	runtime
Instruction scheduling	reordering of instructions	compiler	compile time
Superscalarity	parallelisation on instruction level	hardware	runtime
VLIW	parallelisation on instruction level	compiler	compile time
Out-of-order memory access	reordering of instructions	hardware	runtime

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Summary and outlook

Summary

- Pipelining
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- Superscalar architecture
- VLIW
- Out-of-order memory access

Outlook

- Memory

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