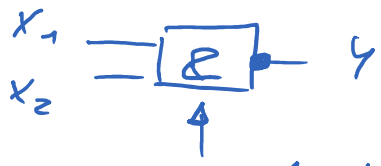
Bausteine der Digitaltechnik

Dienstag, 21. Mai 2019 09:31

Bisher:



$y = \overline{x_1 \cdot x_2}$

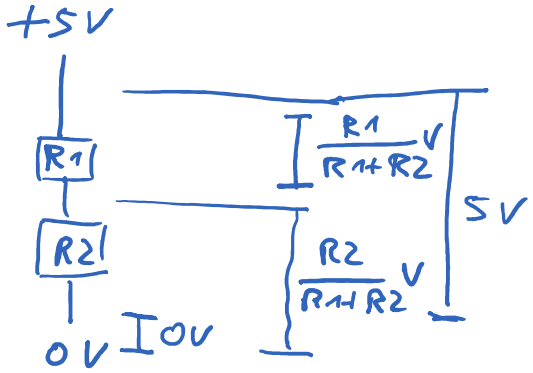
Wie wird das realisiert?

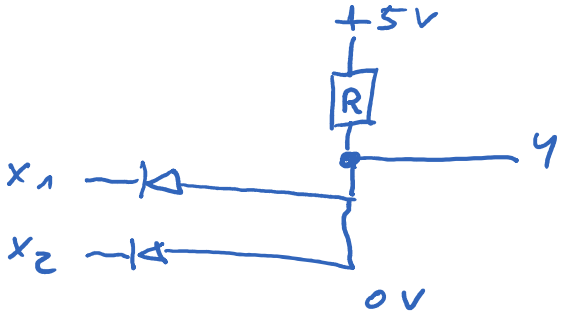
Verwende: . Widerstand — $U = R \cdot I$
. Diode
. Transistor

Diodenlogik:

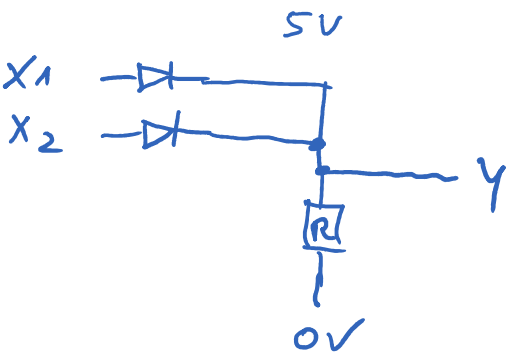
+	−	leitet
−	+	sperrt

x_1	x_2	$y = x_1 \cdot x_2$
0	0	0
0	1	0
1	0	0
1	1	1





ODER Gatter:



x_1	x_2	y
0	0	0
0	1	1
1	0	1
1	1	1

Transistoren: Halbleiter – MOS

Metal Oxide Semiconductor

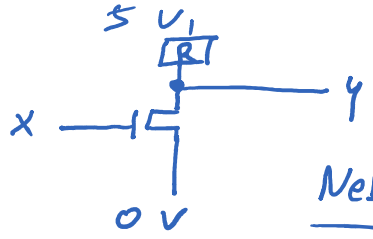
2 Typen von Transistoren

	p-Kanal	n-Kanal
sperrt	1	0
leitet	0	1

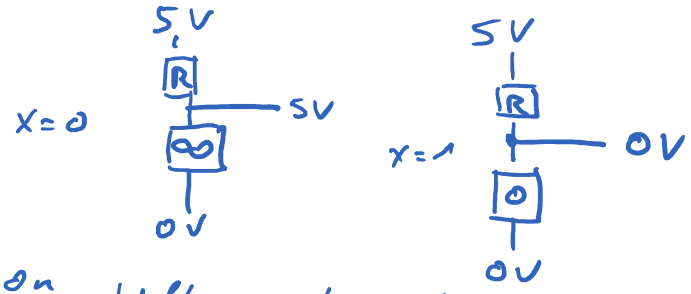
Nur p-Kanal → PMOS
n-Kanal → NMOS
beides → CMOS (complementary)

Bsp.: NMOS → Negation / Inverter

X	Y
0	1
1	0 ✓

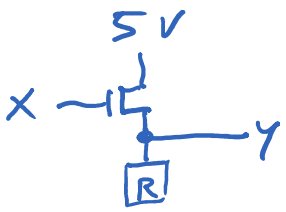


Nebenbetrachtung:



P-MOS – Negation

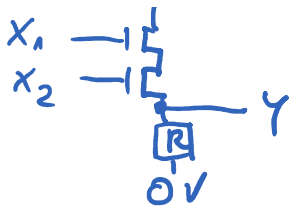
Wdh. p-Kanal Transistor leitet bei 0 am Gate, sperrt sonst.

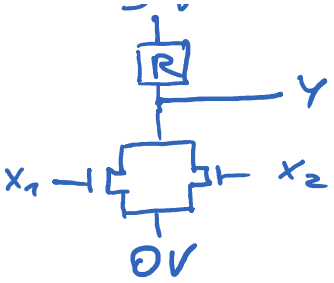


Was berechnet mit

p-Kanal

N-Kanal

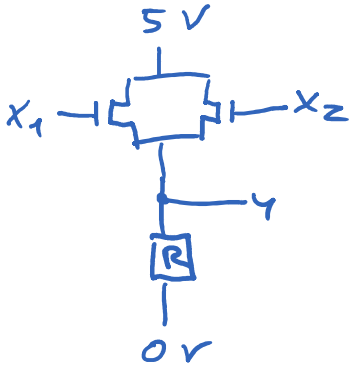




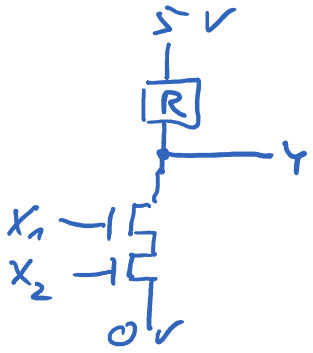
X_1	X_2	$Y = \overline{X_1 + X_2}$
0	0	1
0	1	0
1	0	0
1	1	0

NAND:

p-Kanal



N-Kanal

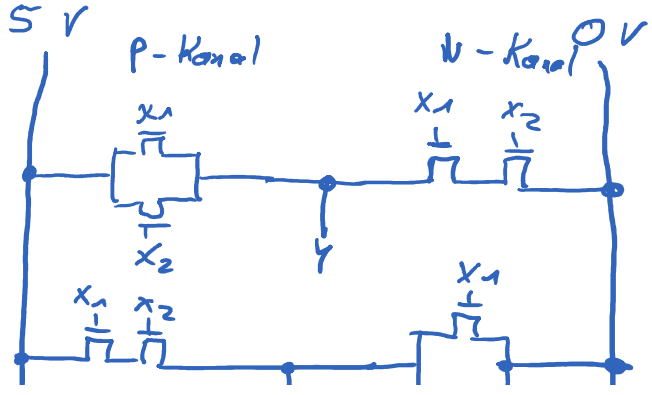


$X_1 = 0$ v $X_2 = 0$:

Vorteil: nur p-Kanal (PMOS) oder
nur N-Kanal (NMOS):
geringere Anzahl Produktionsschritten

Nachteil: Strom fließt immer

Kombination PMOS + NMOS → CMOS

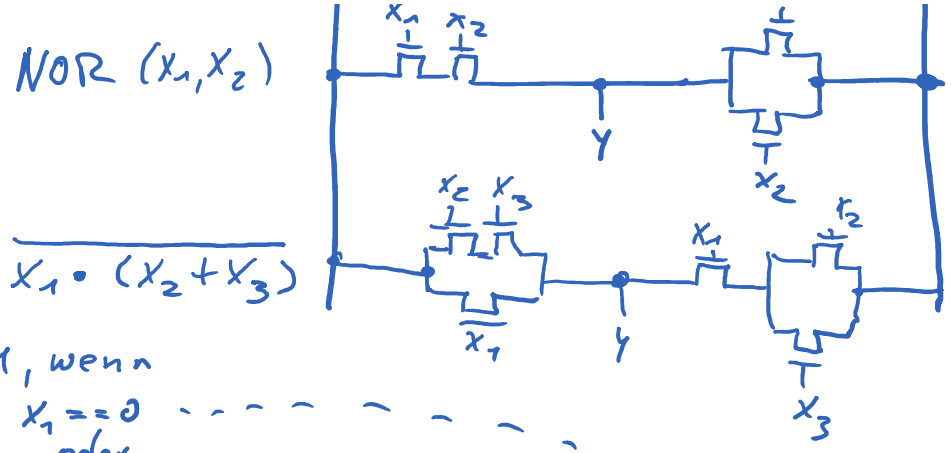


$\overline{X_1 \cdot X_2}$ NAND (X_1, X_2)

$\overline{X_1 + X_2}$ NOR (X_1, X_2)

NOR (x_1, x_2)

$\overline{x_1 \cdot (x_2 + x_3)}$



= 1, wenn
$x_1 == 0$
oder
$(x_2 + x_3) == 0$

= 0, wenn
$x_1 == 1$
und
$(x_2 + x_3) == 1$

x_1	x_2	x_3	$\overline{x_1 \cdot (x_2 + x_3)}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

$(x_1 + x_2) \cdot (x_3 + x_4)$