Exercise sheet 8 – Memory hardware

Goals:

- Memory hardware
- Memory capacity

Hint: consider the lecture about the orders of magnitudes for bits and bytes (decimal and binary)

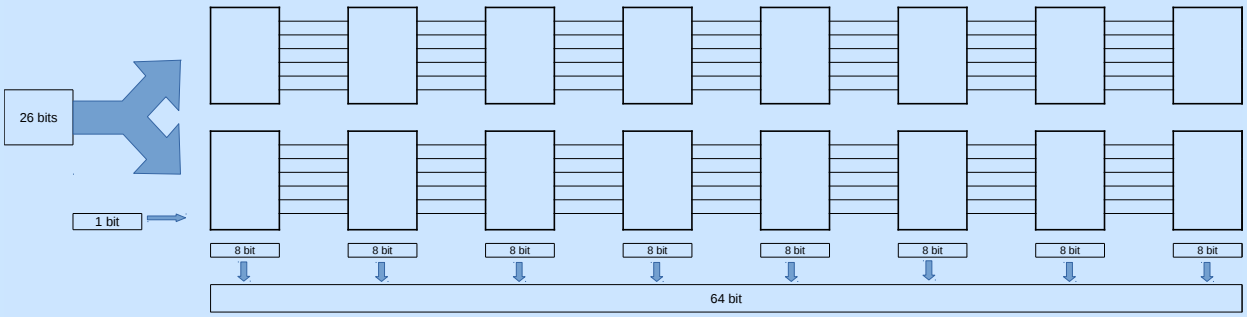
Exercise 8.1: Interconnection of memory chips

(a) State the layout (and the address lanes) for the following memory modules by drawing a scheme:

- Chip type 1: 1 GiB, databus: 64 bits, available memory chips: 64M x 8
- Chip type 2: 1 GiB, databus: 64 bits, available memory chips: 128M x 4

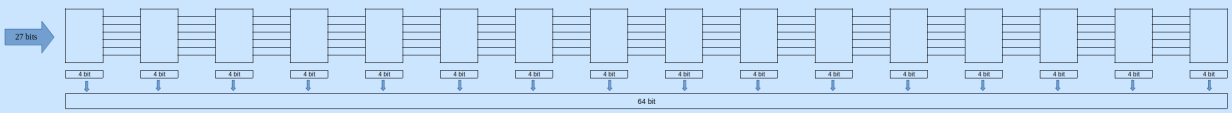
Proposal for solution:

Chip type 1: 64M x 8




```
Address calc according to lecture:
(1) log2(1 GiB)   = 30 bits
(2) log2(2)       = 1 lane/bits
(3) log2(64Mi)    = 26 lanes/bits
(4) log2(8 bytes) = 3 bits
=> 26 + 1 = 27 address lanes required
```

Chip type 2: 128M x 4




```
Address calc according to lecture:
(1) log2(1 GiB)   = 30 bits
(2) log2(1)       = 0 lane/bits
(3) log2(128Mi)   = 27 lanes/bits
(4) log2(8 bytes) = 3 bits
=> 27 + 0 = 27 address lanes required
```

(b) Which of those single chips can store more data? *Hint: Calculate the capacity for every chip-type.*

Proposal for solution: Both chips have the same capacity of 64 MiB:

```
Chip type 1:  64M * 8 = 512 Mibit (512 Mibit/8 = 64 MiB)
Chip type 2: 128M * 4 = 512 Mibit (512 Mibit/8 = 64 MiB)
```

Only their module layout differ, because both need to fill the 64 bit bus.

(c) Can you realise a total memory of 512 MiB with the second chip type?

Proposal for solution: Because of the data bus width of 64 bit, it is not possible to realise a memory module with less than 1 GiB. You need 16 chips in a row to fill the 64 bit bus. (Maybe yes with some strange tricks in interconnection …, but that is not discussed in this lecture)

(d) Where are two following 64-bit-words stored in chip type 1 if you use the most significant bit (= bit 26 of the address lanes) for chip (row) selection in the address lanes?

Proposal for solution: Following 64-bit-words are stored on the same chips (row).

```
Examination:

Memory addresses:      Bit representation:
                      MSB     LSB
0x0000000000000000 -> 0 ... 0 0|000
0x0000000000000008 -> 0 ... 0 1|000
0x0000000000000010 -> 0 ... 1 0|000
0x0000000000000018 -> 0 ... 1 1|000
...
```

The most right 3 bits are only for selecting the byte inside the 64 bit word. In the MSB of the address lanes, nothing changes in the consecutive addresses, but the LSB changes every time.

(e) Where are two following 64-bit-words stored in chip type 1 if you use the least significant bit (= bit 0 of the address lanes) for chip (row) selection in the address lanes?

Proposal for solution: Following 64-bit-words are stored alternating in the chips (row). This is called „*memory interleaving*“ and improves the performance.

Exercise 8.2: Memory module calculations

Consider two memory modules: (1) DDR5-5600 and (2) DDR5-5200 on a 64 bit system.

(a) Calculate the bandwidth of both modules. Which one is faster?

Proposal for solution:

(1):

$$\texttt{bandwidth} = 5600 \times 8 = 44800\ \texttt{MB/s} \Rightarrow 44.8\ \texttt{GB/s}$$

(2):

$$\texttt{bandwidth} = 5200 \times 8 = 41600\ \texttt{MB/s} \Rightarrow 41.6\ \texttt{GB/s}$$

Module (1) is faster than (2).

(b) Calculate the access time t_a of both modules. Which one is faster?

Proposal for solution:
(1):

$$t_a \geq \frac{2 \times (36 + 36)}{\texttt{5600 (MT/s)} = 0.000000026(s)} = 26 \texttt{ ns}$$

(2):

$$t_a \geq \frac{2 \times (40 + 40)}{\texttt{5200 (MT/s)} = 0.000000031(s)} = 30.77 \texttt{ ns}$$

Module (1) is faster than (2).

(c) Checkout the current prices for both modules. Which one would you buy? Please justify your decision.

Exercise 8.3: Memory module and chip analysis

(a) Update the `CA_exercises` repository with `git pull`.

(b) Open the dual channel picture `CA_exercises/sheet_08_memory/dual_channel.jpg` and search for some information about the type of the memory module on the right side.

taken from Von Smial - Own Work, FAL, https://commons.wikimedia.org/w/index.php?curid=2999544

Proposal for solution:
The data sheet can be found here: `https://datasheetspdf.com/pdf/616533/ElpidaMemory/E5108AGBG/1`

- Type: ELPIDA EDE5108AGBG, 64M × 8
- Generation: DDR2 *(Double Data Rate Synchronous Dynamic Random-Access Memory)*
- Clock-Rate: 667 MHz (for comparison latest available DDR4 SDRAM can clock up to 4600 MHz and higher)

(c) You can only see half of the module in the picture. How many memory chips may this module contain in total? Draw a sketch of the module to visualise the situation and try to state something about the data bus width and the capacity.

Proposal for solution: We can assume, that the memory module has 8 chips on one side.

```
Chip capacity: 64MiB

For SIMM: 64MiB * 8 chips = 512 MiB module capacity.
For DIMM: 64MiB * 8 chips * 2 sides = 1024 MiB = 1 GiB module capacity
```

(For comparison: some manufactures have 256 GiB modules announced for 2018/2019 to hit the market)