Exercise sheet 10 – Associative memory

Goals:

- Associative memory (Cache, TLB)
- Virtual memory on a 64 bit system

Exercise 10.1: Cache (theoretical)

Consider an architecture with the following details:

- 16 bit architecture
- Memory address: 0x00014494
- Data: 0xAFFE

(a) State the cache entry, considering a data size of a *word. Hint: Check out the size of a word.*

(b) State the cache entry, considering a cache line size of *256 bytes.*

(c) Exactly state the position of the value (0xAFFE) inside the 256 byte data entry.

(d) What is happening if the cache is empty and we try to access the cache line?

Exercise 10.2: TLB 1

Consider an architecture for page addressing similar to the 1 level page table in the lecture about the VM/MMU, but with a 32 bit architecture.

- The TLB *(translation lookaside buffer)* contains the following entry:

Key	Value
0x00009	0x00002

- The page table contains the following entries:

Page table offset	Value
...	
0x0000A	0x00003
0x00009	0x00002
0x00008	0x00001
...	

(a) Is the page table and the TLB consistent?

(b) State the virtual address, which is mapped to the 32 bit real address 0x00002AAA.

Exercise 10.3: TLB 2

Consider an architecture for page addressing similar to the 2 level page table in the lecture for a 32 bit architecture.
Given:

- Virtual address: 0x1202F494

- Real address: 0x00014494

(a) State the entry in the TLB for the given addresses.

(b) What is happening if the TLB is empty and we try to access the page?