Prof. Dr. Florian Künzner

Technical University of Applied Sciences Rosenheim, Computer Science

CA 4 – Technical realisation

The lecture is based on the work and the documents of Prof. Dr. Theodor Tempelmeier

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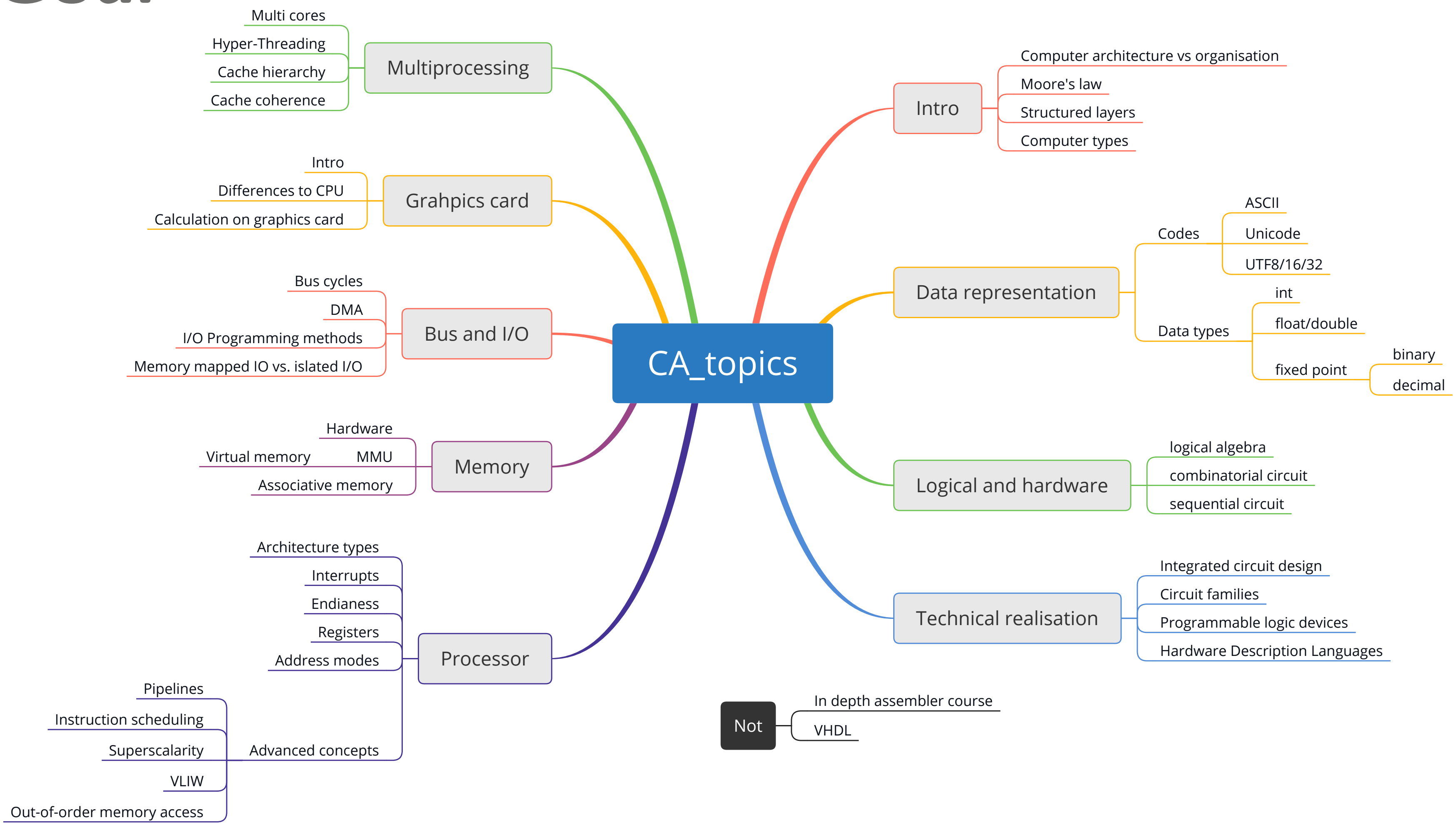
Goal



- CA_topics
  - Intro
    - Computer architecture vs organisation
    - Moore's law
    - Structured layers
    - Computer types
  - Data representation
    - Codes
      - ASCII
      - Unicode
      - UTF8/16/32
    - Data types
      - int
      - float/double
      - fixed point
        - binary
        - decimal
  - Logical and hardware
    - logical algebra
    - combinatorial circuit
    - sequential circuit
  - Technical realisation
    - Integrated circuit design
    - Circuit families
    - Programmable logic devices
    - Hardware Description Languages
  - Processor
    - Architecture types
    - Interrupts
    - Endianess
    - Registers
    - Address modes
    - Advanced concepts
      - Pipelines
      - Instruction scheduling
      - Superscalarity
      - VLIW
      - Out-of-order memory access
  - Memory
    - Hardware
    - Virtual memory
      - MMU
    - Associative memory
  - Bus and I/O
    - Bus cycles
    - DMA
    - I/O Programming methods
    - Memory mapped IO vs. islated I/O
  - Grahpics card
    - Intro
    - Differences to CPU
    - Calculation on graphics card
  - Multiprocessing
    - Multi cores
    - Hyper-Threading
    - Cache hierarchy
    - Cache coherence
- Not
  - In depth assembler course
  - VHDL

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Goal

CA::Technical realisation

- Development of integrated circuits
- Circuit families
- Programmable Logic Devices

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Logical functionality

...and it’s technical realisation

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Development of integrated circuits (ICs)

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Description with „(HDL) hardware description language“ (simulation)

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y = a * b
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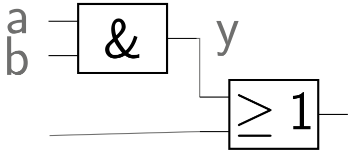
Logic (CAD, simulation)



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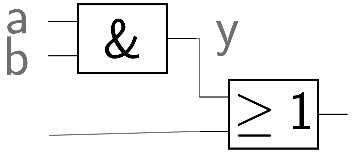
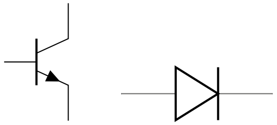


Technical – principle (CAD, simulation)



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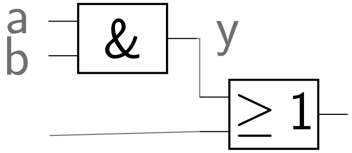

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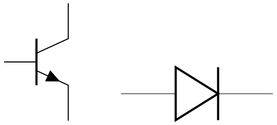
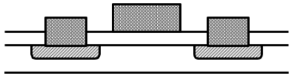


Technical – layout and layers on a chip (CAD, simulation)



Circuit families

Bipolar

Transistor transistor logic (TTL)
Emitter coupled logic (ECL)

- + fast
- – high power dissipation (Verlustleistung)
- – low integration density

Unipolar

Metal oxide semiconductor (MOS)
Field effect transistor (FET)

- – not that fast
- + low power dissipation
- + high integration density

Use in microprocessors and memory devices.

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Programmable logic devices

Types of IC's (integrated circuits):

1. Standard IC (the whole logic is predefined)
2. Full custom - IC

   Chip with customer logic (may be expensive and time consuming until production finished)
3. Gate arrays

   - Chip with a lot of logic elements (1. production step is the same for everyone)

   - Connection of the gates according to customer specifications (2. production step with mask according to customer specifications)
4. Field programmable logic modules
   (PLA, FPLA, PAL, EPLD, EEPLD, **GAL**, ..., **FPGA**)
   - "On site" with PC and programming device or even in soldered in state "programmable" - Programming means put user-specific logic into the IC.

Terminology:

The ICs under the numbers 2 and 3 (sometimes also 4) are called ASICs.
ASIC = application specific IC

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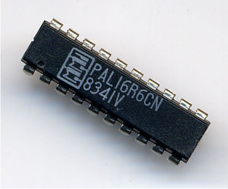
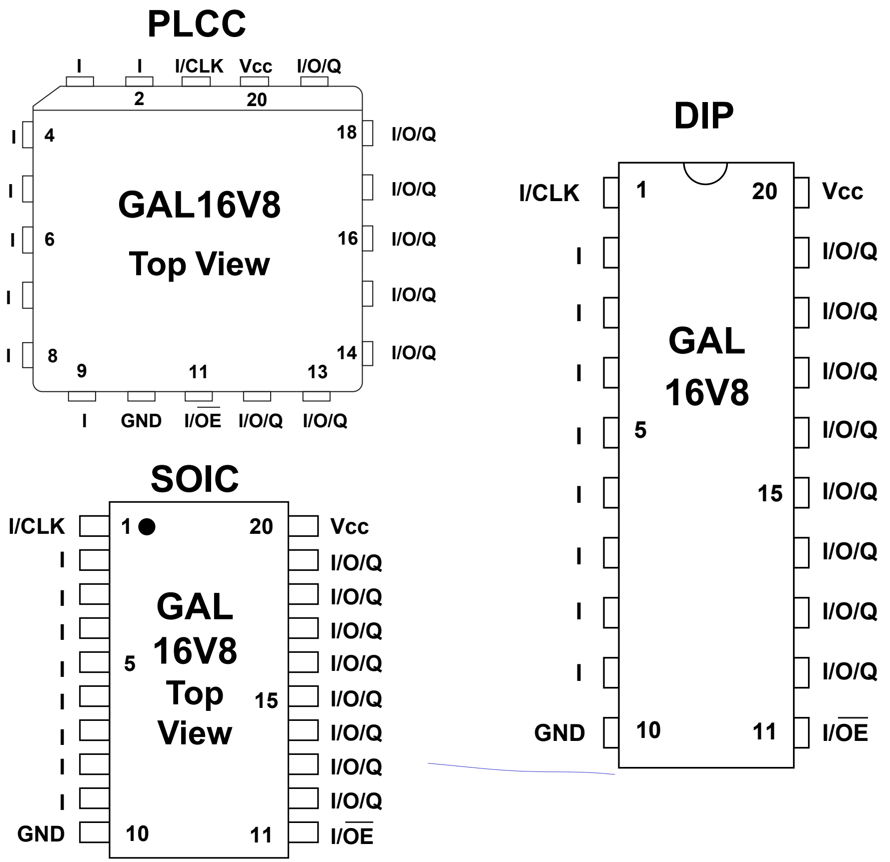
Example: Field programmable logic modules

PAL	Programmable array logic	
GAL	Generic array logic	
FPGA	Field programmable gate array	

[Image sources: wikipedia.org]

Example: GAL (generic array logic)

- Type: GAL16V8
- Company: Lattice
- Programmable AND array
- 20 year data retention



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Questions?

All right? ⇒ ✓

Question? ⇒ ✋ and use **chat**

or

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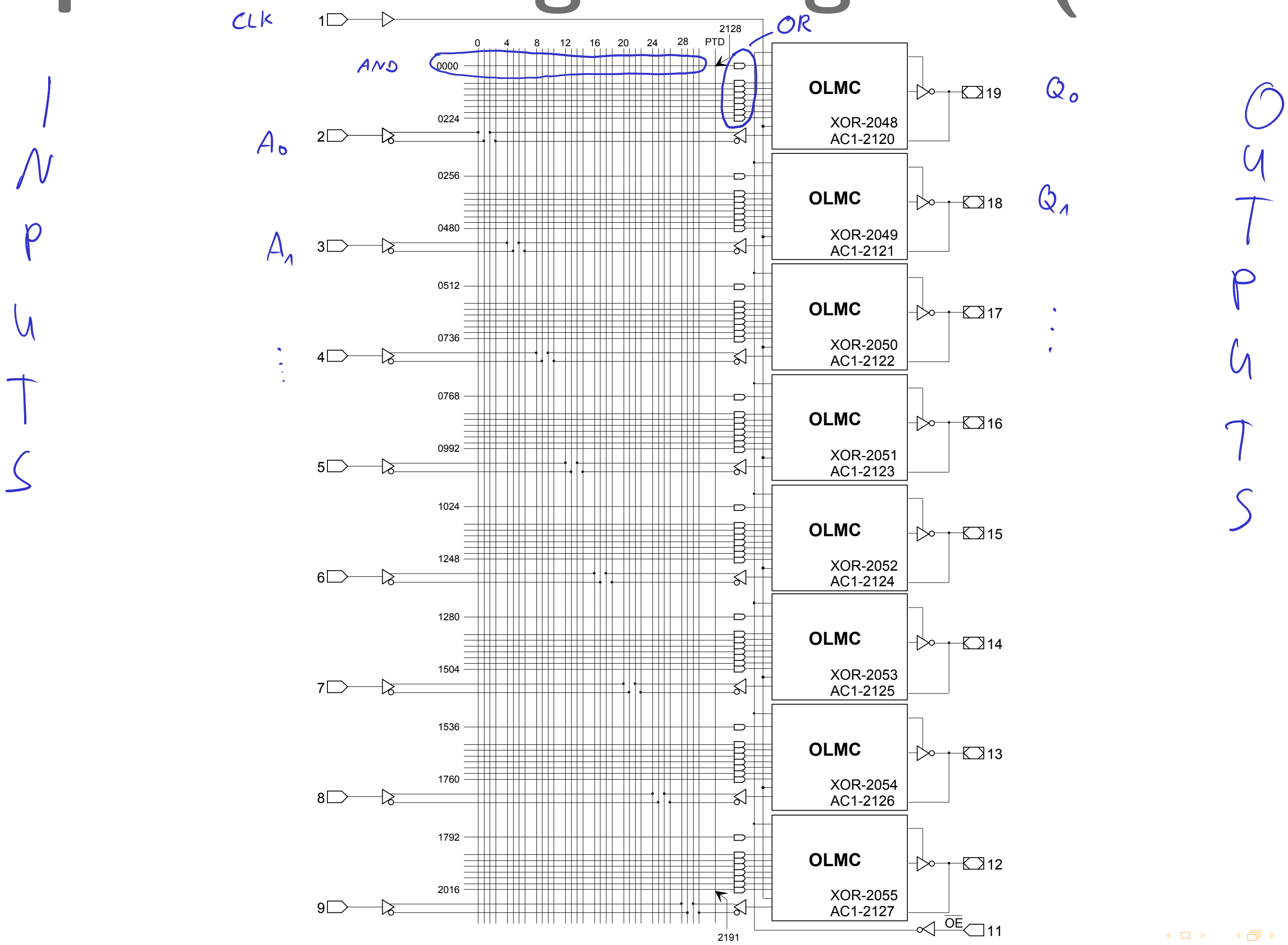
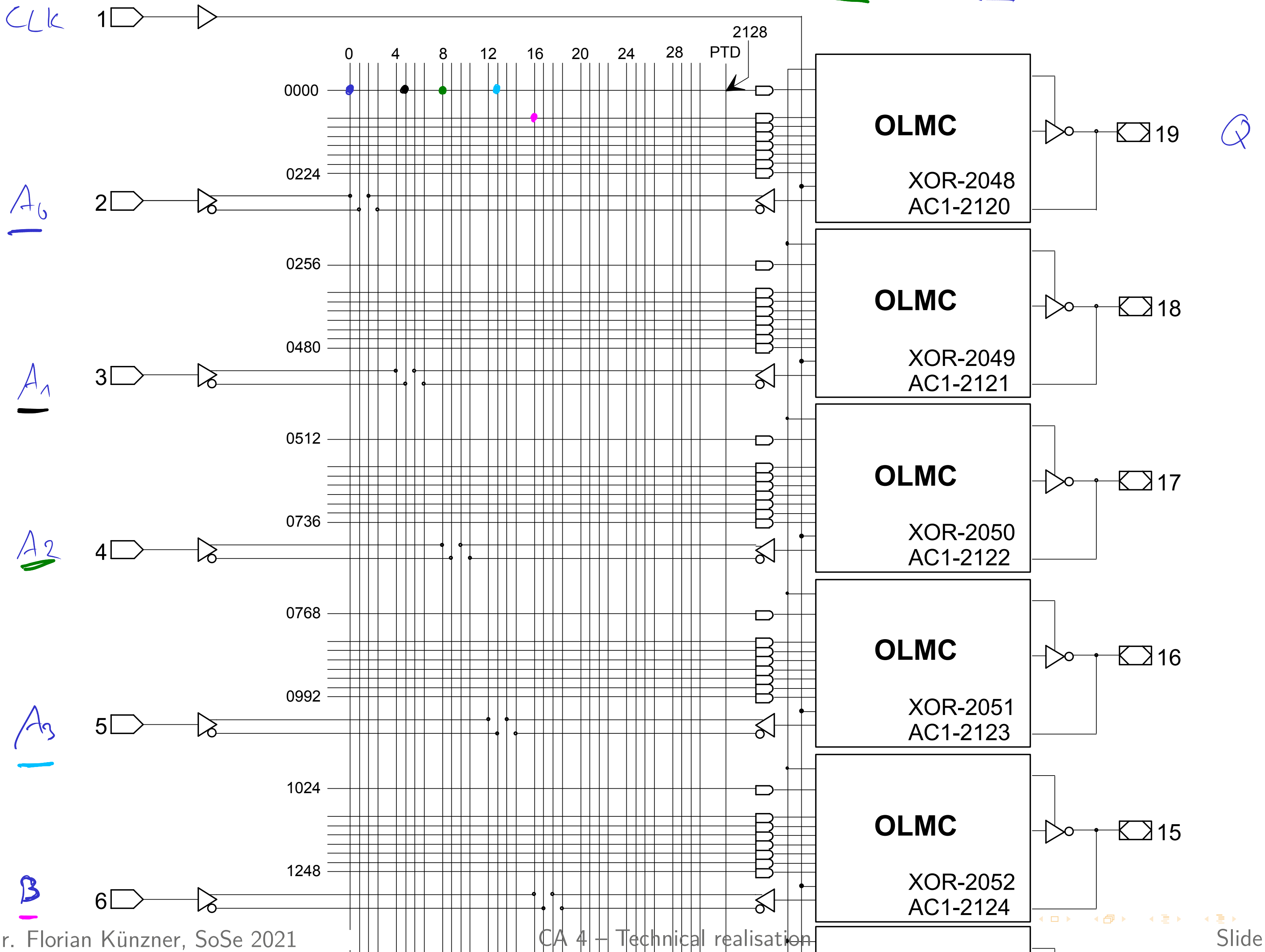
Example: GAL logic diagram (GAL16V8)



Example: GAL programming: $Q = \bar{A}_3 \cdot A_2 \cdot \bar{A}_1 \cdot A_0 + B$



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Tango-PLD

A language to describe the logic.

```
Logic(in A0, A1, A2, A3, B; out Q){
    Q = !A3 & A2 & !A1 & A0 | B;
    putpart("g16v8", "Logic",
            -,A0,A1,A2,A3,B,-,-,-,GND,
            -,-,-,-,-,-,-,-,Q,VCC);
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- The Tango-PLD compiler automatically creates the contact pattern (JEDEC file, zeros and ones)
- JEDEC file (Joint Electron Device Engineering Council):
  File format between data preperation system and PLD programmer
- Tango-PLD is outdated, because it's too simple for modern FPGAs.

[PLD file formats]

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Hardware description languages

VHDL – Very high speed integrated circuit hardware description language

⇒ **Programming of FPGAs!**

- A precise, formal description of an electronic circuit
- Allows automated analysis and simulation of an electronic circuit
- HDL != Programming language
  (HDL explicitly consider the notion of time and is therefore more complex)
- The syntax of VHDL is very similar to the programming language Ada.

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Summary and outlook

Summary

- Development of integrated circuits
- Circuit families
- Programmable Logic Devices

Outlook

- Processor architecture

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