



#### Prof. Dr. Florian Künzner

Technical University of Applied Sciences Rosenheim, Computer Science

### CA 8 – Memory 1

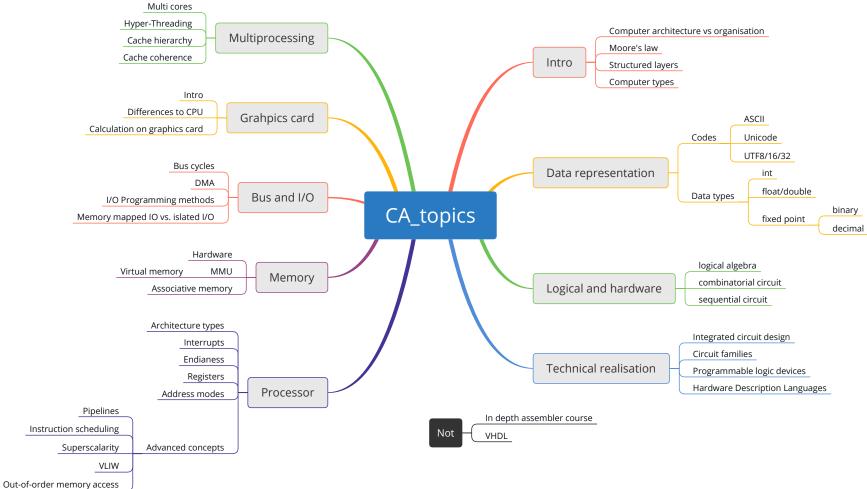
The lecture is based on the work and the documents of Prof. Dr. Theodor Tempelmeier

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### Goal

Goal



Summary





### CA::Memory 1 - Hardware

- Memory types
- Memory chips
- Memory modules
- Modern memory modules

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Summary

# Memory types

### RAM vs ROM

#### **RAM** - Random access memory



# Memory types

### RAM vs ROM

#### **RAM** - Random access memory

- For **read and write** access

- For **read only** memory access



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# Memory types

### RAM vs ROM

#### RAM - Random access memory

- For **read and write** access
- Usage: **programs and data**
- It is (usually) a volatile memory (data are lost when power is switched off)
- Very fast access time
- High power consumption
- Expensive

#### ROM - Read only memory

- For **read only** memory access
- Usage: **firmware** (BIOS, UEFI)
- It is a non-volatile memory (remembers the data even if power is switched off)
- Usually slower than RAM
- Low power consumption
- Cheaper than RAM
- Example: EPROM, EEPROM



Summary



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Memory modules

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Goal Memory types Bits and bytes Memory chips Memory modules Summary

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# Memory types

### It's all about RAM!

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# Memory types

### SRAM vs DRAM

**Property** 

SRAM - Static RAM



# Memory types

### SRAM vs DRAM

**Property** 

Construction

**SRAM** - Static RAM

Complex

**DRAM** - Dynamic RAM

+ Simple



Summary

# Memory types

### SRAM vs DRAM

**Property** 

Construction

Realisation of a bit - 4..6 transistors

SRAM - Static RAM

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# Memory types

### SRAM vs DRAM

Memory modules

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Size (capacity)

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### SRAM vs DRAM

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**Cache memory** 

#### **DRAM** - Dynamic RAM

- + Simple
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Main memory

### SRAM vs DRAM

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+ Highly dense





### **SRAM** vs **DRAM**

#### **Property**

Construction

Realisation of a bit

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Size (capacity)

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Charge leakage

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- + Not present

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- Present: refresh required



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Power consumption + Low

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- + Simple
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#### Main memory

- + Highly dense
- Present: refresh required
- High

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# Orders of magnitudes for bits and bytes

**Bits:** 

Bits (decimal)					
Symbol	Power	Num bits	Name		
1 kbit	10 <sup>3</sup>	1.000	kilobit		
1 Mbit	10 <sup>6</sup>	1.000.000	megabit		
1 Gbit	10 <sup>9</sup>	1.000.000.000	gigabit		
1 Tbit	$10^{12}$	1.000.000.000.000	terabit		

Bits (binary)					
Symbol	Power	Num bits	Name		
1 Kibit	$2^{10}$	1.024	kibibit		
1 Mibit	$2^{20}$	1.048.576	mebibit		
1 Gibit	$2^{30}$	1.073.741.824	gibibit		
1 Tibit	$2^{40}$	1.099.511.627.776	tebibit		

Bytes:

				1 KiB			
				1 GiB			
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Summary

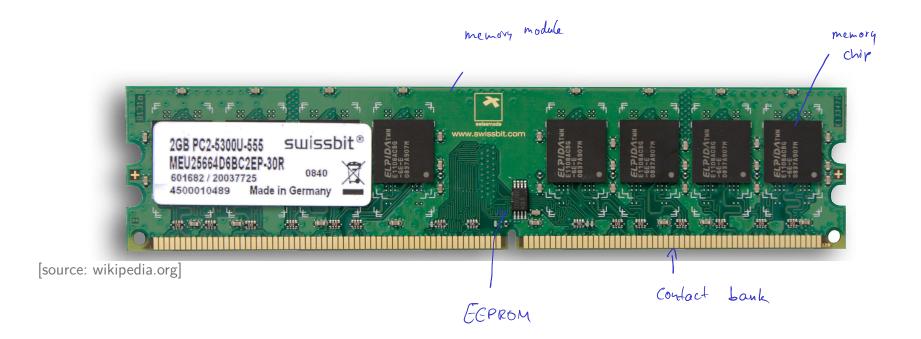
Memory types Bits and bytes Memory chips Memory modules Summary

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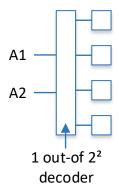
# Memory modules and chips - overview



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# Memory chips

Arrangement of memory cells: (within a memory chip) Linear Arrangement:



- To address 1-out-of-2<sup>n</sup> memory cells, *n* address lanes are required.
- Problem: Address lanes are expensive (takes place on the chip)



Memory modules

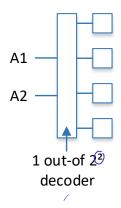
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Bits and bytes

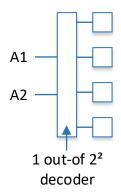


- To address 1-out-of- $2^n$  memory cells, naddress lanes are required.



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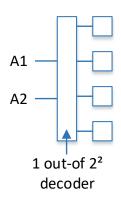




# Memory chips

**Arrangement of memory cells:** (within a memory chip)

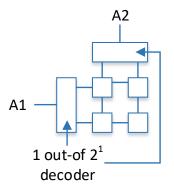
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Memory modules



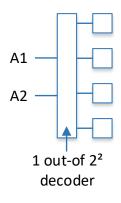
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# Memory chips

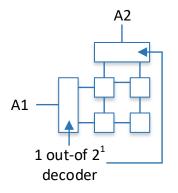
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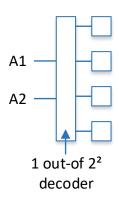
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# Memory chips

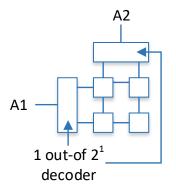
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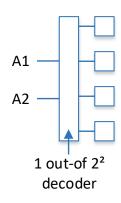
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# Memory chips

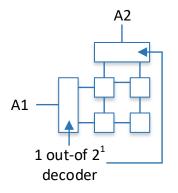
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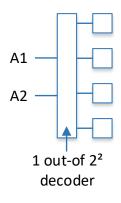
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# Memory chips

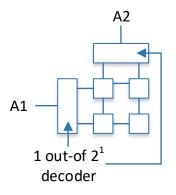
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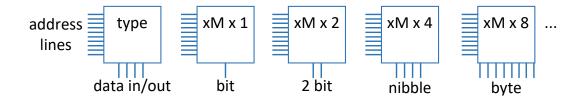
Summary



Summary

### Memory chips

#### **Chip types:**



# Terminology: Description

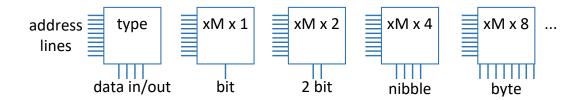
Type Unit

Memory modules



# Memory chips

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### **Terminology:**

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Type Unit

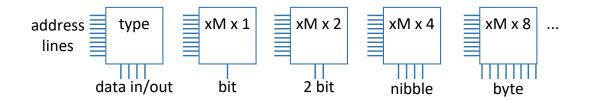
Chip with x mega that provides 1 bit per address  $\times M \times 1$  bit





# Memory chips

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Description

Type Unit

Chip with x mega that provides 1 bit per address  $xM \times 1$  bit Chip with x mega that provides 2 bit per address  $xM \times 2$  2 bit

Type

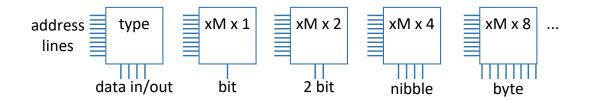
Unit

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## Memory chips

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**Description** 

Chip with x mega that provides 1 bit per address  $\times M \times 1$  bit

Chip with x mega that provides 2 bit per address  $xM \times 2$  2 bit

Chip with x mega that provides 4 bit per address  $\times M \times 4$  nibble

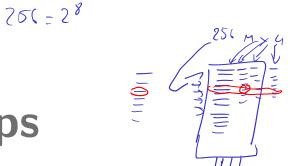
256 41 . 4 = 1024 MI 61 + B = 128 MB

Unit

Type

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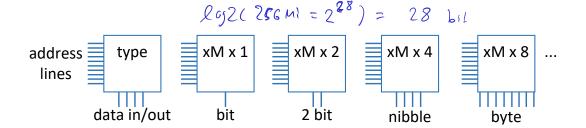
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## Memory chips

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## Memory chips

## **Chip capacity:**

On these chips: K means Ki, M means Mi, G means Gi, ... xK/xM/xG denotes the number of chip cell rows inside the chip

## Chip capacity = xM x number of bits per chip

- 16M x 1: 16Mi x 1 = 16 Mibit => 16Mi/8 = 2 MiB
- 16M x 2: 16Mi x 2 = 32 Mibit => 32Mi/8 = 4 MiB
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Memory modules

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## Questions?

All right?  $\Rightarrow$ 



Question?  $\Rightarrow$ 



and use chat

speak after | ask you to



## Memory modules

The memory chips on a memory module are usually arranged in a matrix layout.



[image source: samsung.com]

Memory address is divided into:

- Chip select address
- Chip address (inside the chip)



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Memory modules

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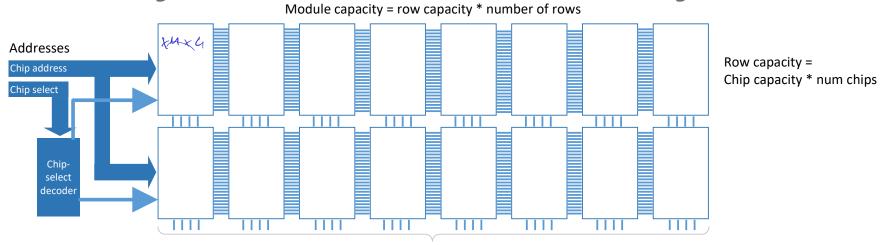
Goal Memory types Bits and bytes Memory chips Memory modules Summary

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## Memory modules - hardware layout



Data bus width = bits per chip \* num chips pw rou

**Address calculations:** 

Nr. Descriptions Calc Results

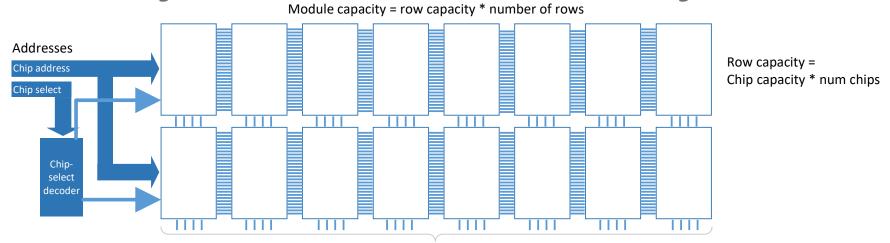
Memory types Bits and bytes Memory chips Memory modules Summary

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## Memory modules - hardware layout



Data bus width = bits per chip \* num chips

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(1) Number of bits to address the module capacatiy

Calc

log<sub>2</sub> (module capacity)

Results

number of bits

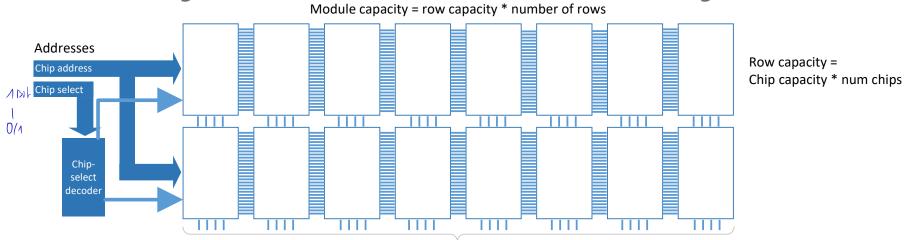
Memory types Bits and bytes Memory chips Memory modules Summary

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## Memory modules - hardware layout



Data bus width = bits per chip \* num chips

#### Address calculations:

#### Nr. Descriptions

- (1) Number of bits to address the module capacativ
- (2) Number of address lanes/bits for chip select

#### Calc

log<sub>2</sub>(module capacity)
log<sub>2</sub>(num. rows)

#### Results

number of bits number of bits/address lanes

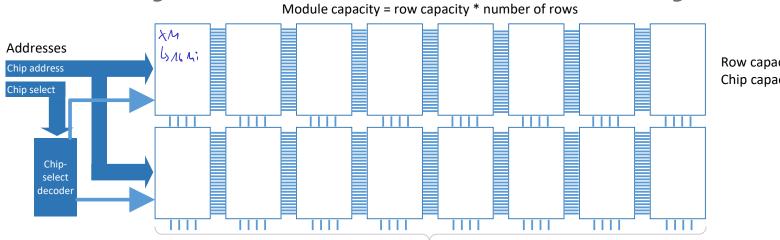
Memory types Bits and bytes Memory chips Memory modules Summary

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## Memory modules - hardware layout



Row capacity = Chip capacity \* num chips

Data bus width = bits per chip \* num chips

#### Address calculations:

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- (1) Number of bits to address the module capacativ
- (2) Number of address lanes/bits for chip select
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#### Calc

log<sub>2</sub>(module capacity) log<sub>2</sub>(num. rows) log<sub>2</sub>(num. chip cell rows)

#### Results

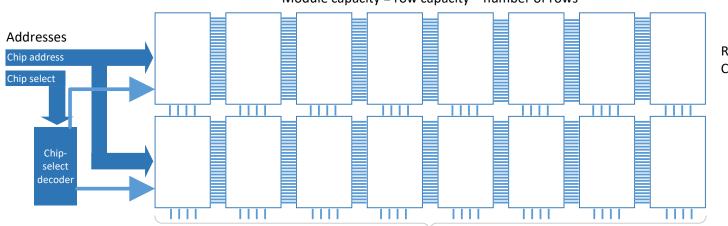
number of bits/address lanes number of bits/address lanes Memory types Bits and bytes Memory chips Memory modules Modern memory modules

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## Memory modules - hardware layout Module capacity = row capacity \* number of rows



Row capacity = Chip capacity \* num chips

Summary

Data bus width = bits per chip \* num chips

#### Address calculations:

#### Nr. Descriptions

- (1) Number of bits to address the module capacativ
- (2) Number of address lanes/bits for chip select
- (3) Number of address lanes/bits for chip address
- (4) Number of bits to address the bytes inside the word

#### Calc

log<sub>2</sub>(module capacity)

 $log_2(num. rows)$ 

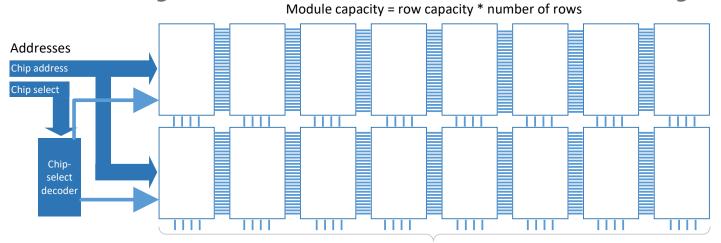
log<sub>2</sub>(num. chip cell rows)

log<sub>2</sub>(num. bytes per word)

#### Results

number of bits/address lanes number of bits/address lanes number of bits

## Memory modules - hardware layout



Row capacity = Chip capacity \* num chips

Data bus width = bits per chip \* num chips

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- (2) Number of address lanes/bits for chip select
- (3) Number of address lanes/bits for chip address
- (4) Number of bits to address the bytes inside the word

#### Calc

log<sub>2</sub>(module capacity)

log<sub>2</sub>(num. rows)

log<sub>2</sub>(num. chip cell rows)

 $log_2(num. bytes per word)$ 

#### Results

number of bits/address lanes number of bits/address lanes number of bits

#### Address calculation relationship:

Number of bits to address the module capacatiy:  $(1) = \sum_{i=2}^{4} (i) = (2) + (3) + (4)$ 

Prof. Dr. Florian Künzner, SoSe 2021

CA 8 – Memory 1

Slide 14 of 26



## Memory modules - example

#### **Example:**

28 67

Mbil

Design a memory module with: 2 GiB capacity and a 32 bit data bus

Data bus width = 4.8 =

Use chips of type 256M x 4 Module capacity =  $10^{10} \cdot 2 = 20^{10}$ Addresses 256M x 4 178 MIS Chip 256M x 4 select decoder

Row capacity =

128 MiD. 8 = 1024 MB = 1 Gil

#### **Address calculations:**

#### Nr. Descriptions

- (1) Number of bits to address the module capacativ
- (2) Number of address lanes/bits for chip select
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32 517

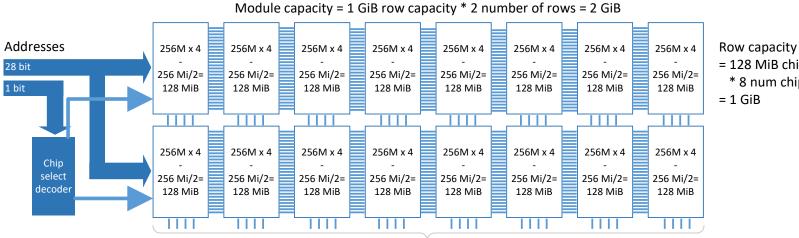
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## Memory modules - example (solution)

#### **Example:**

- Design a memory module with: 2 GiB capacity and a 32 bit data bus
- Use chips of type 256M x 4



= 128 MiB chip capacity

\* 8 num chips

= 1 GiB

Data bus width = 4 bits per chip \* 8 num chips = 32 bit (4 byte)

#### **Address calculations:**

#### **Descriptions**

- (1)Number of bits to address the module capacativ
- (2)Number of address lanes/bits for chip select
- (3)Number of address lanes/bits for chip address
- Number of bits to address the bytes inside the word

#### Calc

$$log_2(2 GiB = 2^{31})$$

$$log_2(2)$$

$$log_2(256 Mi = 2^{28})$$

#### log<sub>2</sub>(4bytes)

#### Result

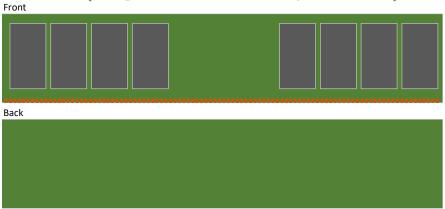
- 31 bits
- 1 lanes/bits
- 28 lanes/bits
- 2 bits

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## Memory modules - formats

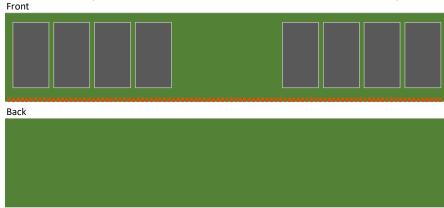
**SIMM** (single inline memory module):



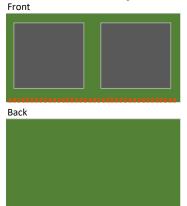


## Memory modules - formats

**SIMM** (single inline memory module):



#### **SO-SIMM** (small outline SIMM):



Modern memory modules Memory chips Memory modules Memory types Summary

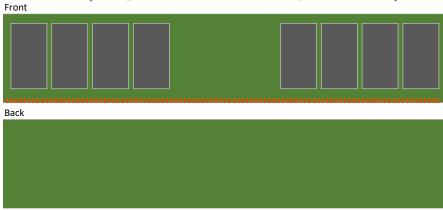
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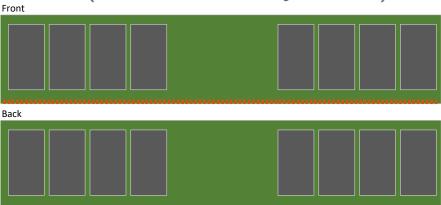


## Memory modules - formats

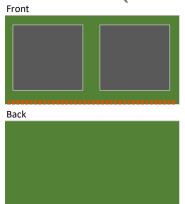
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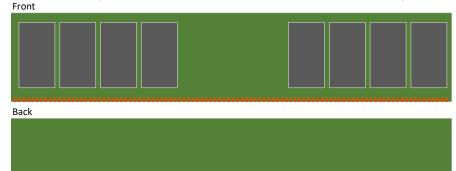


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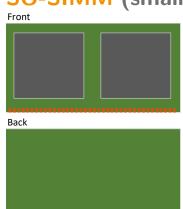


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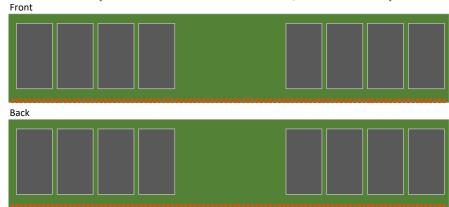
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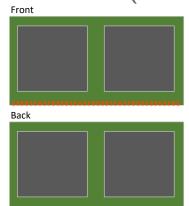




#### **DIMM** (dual inline memory module):



### **SO-DIMM** (small outline DIMM):



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## Memory modules - interleaving

### **Problem:**

After a **memory cell** is read in a DRAM, the cell **needs to be refreshed** and this takes some time.

### Idea:

Distribute consecutive addresses evenly across the chip rows.

- Reduces the problem of waiting until the refresh is complete
- Accelerates memory access in an effect similar to pipelining
- But due to the increased capacities of the individual chips, a memory module has only one or two chip rows. -> Solution:

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### **SDRAM**

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### **SDRAM**

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## Questions?

All right?  $\Rightarrow$ 



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## Modern memory modules

# Overview of various terms in the memory area

Memory modules

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## **SDRAM**

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## **SDRAM**

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Memory modules

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Memory modules



## **ECC**

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## **ECC**: error checking and correction

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## ECC: error checking and correction

- ECC memory can detect and correct the most common kinds of internal data corruption
- Allows the detection and correction of single bit errors
- Some do also detect double bit errors
- Application area: Scientific and financial computing applications which operate on sensitive data



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### DDR-SDRAM: double data rate SDRAM

- Transfers data at almost double the transfer rate
- Data is transferred on rising and falling edges.
- DDR4-RAM is state of the art for computers
- DDR5-RAM is approaching into the market in 2020/2021

Memory modules

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	DDR3	DDR4	DDR5
Data transfer rate	17 GiB/s	25,6 GiB/s	51,2 GiB/s
Max module capacity	16 GiB	64 GiB	128 GiB

Memory types Bits and bytes Memory chips Memory modules Modern memory modules Summary

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# Multi-channel memory architecture



- [source: wikipedia.com]
- Adds multiple channels from the memory to the controller
- Increase data transfer rate of DRAM memory modules with the memory controller
- Dual/Triple/Quad-channels are possible
- Dual-channel: theoretically doubles the data transfer rate
- New Intel processors (like Intel Core i7-9800X) supports quad-channel memory architecture

Memory types Bits and bytes Memory chips Memory modules Modern memory modules Summary

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Memory chips Modern memory modules Memory types Memory modules Summary

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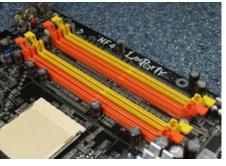
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# Summary and outlook

### **Summary**

- Memory types
- Memory chips
- Memory modules
- Modern memory modules

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# Summary and outlook

### **Summary**

- Memory types
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- Memory modules
- Modern memory modules

### Outlook

- MMU
- Virtual memory