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# Exercise sheet 14 – Multiprocessors

#### Goals:

- Cache coherency on multi core CPUs
- Exploration of a multi core CPU (Intel Core i9)

### Exercise 14.1: The MESI game (interactive team training)

- (a) We want to learn how a multi core CPU system handles the MESI-protocol with an interactive game. Build groups for
  - CPU 1
  - CPU 2
  - Cache 1
  - Cache 2
  - RAM

#### Assumptions:

- Multi-core CPU with 2 cores
- 32 bit architecture
- Cache line size: 32 byte
- Each cache has 2 cache lines

Both CPUs access the memory, so caches and RAM have to react appropriate. To keep it simple, we will work with only two address spaces (one for each cache line).

## Exercise 14.2: Information about the Intel Core i9-9980XE

Here, you can find some information about the CPU:

- https://en.wikichip.org/wiki/intel/core\_i9/i9-9980xe
- $\bullet \hspace{0.2cm} \texttt{https://www.anandtech.com/show/11550/the-intel-skylakex-review-core-i9-7900x-i7-7820x-and-i7-7800x-tested/500x-interled-skylakex-review-core-i9-7900x-i7-7820x-and-i7-7800x-tested/500x-interled-skylakex-review-core-i9-7900x-i7-7820x-and-i7-7800x-tested/500x-interled-skylakex-review-core-i9-7900x-i7-7820x-and-i7-7800x-tested/500x-interled-skylakex-review-core-i9-7900x-i7-7820x-and-i7-7800x-tested/500x-interled-skylakex-review-core-i9-7900x-i7-7820x-and-i7-7800x-tested/500x-interled-skylakex-review-core-i9-7900x-i7-7820x-and-i7-7800x-tested/500x-interled-skylakex-review-core-i9-7900x-i7-7820x-and-i7-7800x-tested/500x-interled-skylakex-review-core-i9-7900x-i7-7820x-and-i7-7800x-tested/500x-interled-skylakex-review-core-i9-7900x-i7-7820x-and-i7-7800x-tested/500x-interled-skylakex-review-core-i9-7900x-i7-7820x-and-i7-7800x-tested/500x-interled-skylakex-review-core-i9-7900x-i7-7820x-and-i7-7800x-interled-skylakex-review-core-i9-7900x-i7-7800x-i$
- (a) How many cores does this CPU have?
- (b) Does the CPU support Hyper-Threading? How many threads does the CPU have?
- (c) Describe the cache hierarchy of the CPU and visualise the situation.
- (d) How does the CPU guarantees the cache coherency?