Exercise sheet 8 – Memory hardware

Goals:

- Memory hardware
- Memory capacity

Hint: consider the lecture about the orders of magnitudes for bits and bytes (decimal and binary)

Exercise 8.1: Interconnection of memory chips

(a) State the layout (and the address lanes) for the following memory modules by drawing a scheme:
  - Chip type 1: 1 GiB, databus: 64 bits, available memory chips: 64M x 8
  - Chip type 2: 1 GiB, databus: 64 bits, available memory chips: 128M x 4

(b) Which of those single chips can store more data? *Hint: Calculate the capacity for every chip-type.*

(c) Can you realise a total memory of 512 MiB with the second chip type?

(d) Where are two following 64-bit-words stored in chip type 1 if you use the most significant bit (= bit 26 of the address lanes) for chip (row) selection in the address lanes?

(e) Where are two following 64-bit-words stored in chip type 1 if you use the least significant bit (= bit 0 of the address lanes) for chip (row) selection in the address lanes?

Exercise 8.2: Memory module calculations

Consider two memory modules: (1) DDR5-5600 and (2) DDR5-5200 on a 64 bit system.

(a) Calculate the bandwidth of both modules. Which one is faster?

(b) Calculate the access time t_a of both modules. Which one is faster?

(c) Checkout the current prices for both modules. Which one would you buy? Please justify your decision.

Exercise 8.3: Memory module and chip analysis 1

(a) Update the `CA_exercises` repository with `git pull`.

(b) Open the dual channel picture `CA_exercises/sheet_08_memory/dual_channel.jpg` and search for some information about the type of the memory module on the right side.

taken from Von Smial - Own Work, FAL, https://commons.wikimedia.org/w/index.php?curid=2999544

(c) You can only see half of the module in the picture. How many memory chips may this module contain in total? Draw a sketch of the module to visualise the situation and try to state something about the data bus width and the capacity.