Technische
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Exercise sheet 8 – Memory hardware

Goals:

- Memory hardware
- Memory capacity

*Hint: consider the lecture about the orders of magnitudes for bits and bytes (decimal and binary)*

Exercise 8.1: Interconnection of memory chips

(a) State the layout (and the address lanes) for the following memory modules by drawing a scheme:

- Chip type 1: 1 GiB, databus: 64 bits, available memory chips: 64M x 8
- Chip type 2: 1 GiB, databus: 64 bits, available memory chips: 128M x 4

Proposal for solution:

Chip type 1: 64M x 8
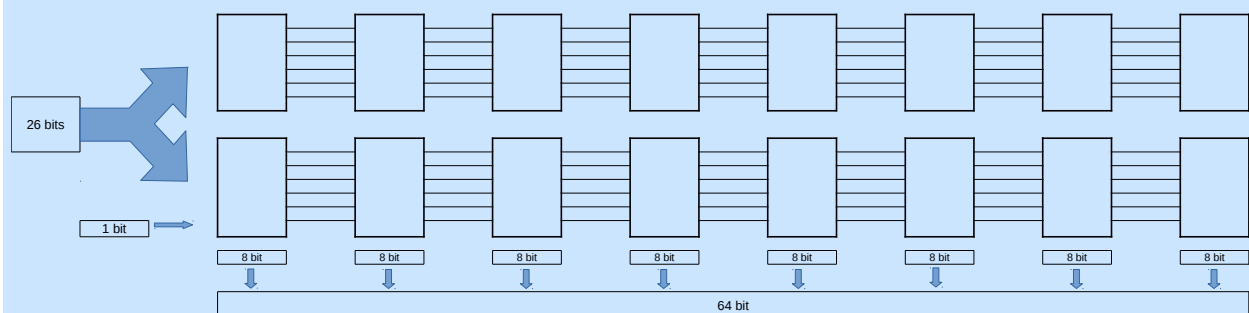

```
1  Address calc according to lecture:
2  (1) log2(1 GiB)   = 30 bits
3  (2) log2(2)       = 1 lane/bits
4  (3) log2(64Mi)    = 26 lanes/bits
5  (4) log2(8 bytes) = 3 bits
6  => 26 + 1 = 27 address lanes required
```
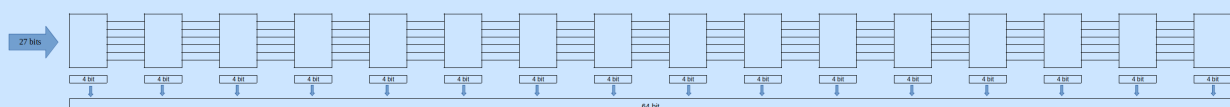
Chip type 2: 128M x 4


```
1  Address calc according to lecture:
2  (1) log2(1 GiB)   = 30 bits
3  (2) log2(1)       = 0 lane/bits
4  (3) log2(128Mi)   = 27 lanes/bits
5  (4) log2(8 bytes) = 3 bits
6  => 27 + 0 = 27 address lanes required
```

(b) Which of those single chips can store more data? *Hint: Calculate the capacity for every chip-type.*

> **Proposal for solution:** Both chips have the same capacity of 64 MiB:
>
> ```
> 1  Chip type 1:  64M * 8 = 512 Mibit (512 Mibit/8 = 64 MiB)
> 2  Chip type 2: 128M * 4 = 512 Mibit (512 Mibit/8 = 64 MiB)
> ```
>
> Only their module layout differ, because both need to fill the 64 bit bus.

(c) Can you realise a total memory of 512 MiB with the second chip type?

> **Proposal for solution:** Because of the data bus width of 64 bit, it is not possible to realise a memory module with less than 1 GiB. You need 16 chips in a row to fill the 64 bit bus. (Maybe yes with some strange tricks in interconnection …, but that is not discussed in this lecture)

(d) Where are two following 64-bit-words stored in chip type 1 if you use the most significant bit (= bit 26 of the address lanes) for chip (row) selection in the address lanes?

> **Proposal for solution:** Following 64-bit-words are stored on the same chips (row).
>
> ```
> 1  Examination:
> 2
> 3  Memory addresses:      Bit representation:
> 4                     MSB       LSB
> 5  0x0000000000000000 -> 0 ... 0 0|000
> 6  0x0000000000000008 -> 0 ... 0 1|000
> 7  0x0000000000000010 -> 0 ... 1 0|000
> 8  0x0000000000000018 -> 0 ... 1 1|000
> 9  ...
> ```
>
> The most right 3 bits are only for selecting the byte inside the 64 bit word. In the MSB of the address lanes, nothing changes in the consecutive addresses, but the LSB changes every time.

(e) Where are two following 64-bit-words stored in chip type 1 if you use the least significant bit (= bit 0 of the address lanes) for chip (row) selection in the address lanes?

> **Proposal for solution:** Following 64-bit-words are stored alternating in the chips (row). This is called „*memory interleaving*" and improves the performance.

Exercise 8.2: Memory module and chip analysis 1

(a) Update the `RA_exercises` repository with `git pull`.

(b) Open the dual channel picture `RA_exercises/sheet_08/dual_channel.jpg`
and search for some information about the type of the memory module on the right side.

taken from Von Smial - Own Work, FAL, https://commons.wikimedia.org/w/index.php?curid=2999544

> **Proposal for solution:**
>
> The data sheet can be found here: `https://datasheetspdf.com/pdf/616533/ElpidaMemory/E5108AGBG/1`
>
> - Type: ELPIDA EDE5108AGBG, 64M × 8

- Generation: DDR2 *(Double Data Rate Synchronous Dynamic Random-Access Memory)*

- Clock-Rate: 667 MHz (for comparison latest available DDR4 SDRAM can clock up to 4600 MHz and higher)

(c) You can only see half of the module in the picture. How many memory chips may this module contain in total? Draw a sketch of the module to visualise the situation and try to state something about the data bus width and the capacity.

Proposal for solution: We can assume, that the memory module has 8 chips on one side.

```
1  Chip capacity: 64MiB
2
3  For SIMM: 64MiB * 8 chips = 512 MiB module capacity.
4  For DIMM: 64MiB * 8 chips * 2 sides = 1024 MiB = 1 GiB module capacity
```

(For comparison: some manufactures have 256 GiB modules announced for 2018/2019 to hit the market)

Exercise 8.3: Memory module and chip analysis 2

Check out the following pictures and interpret the label:

RA_exercises/sheet_08/TRS 1 GB pc2-5300CL5 667Mhz-0.jpg

RA_exercises/sheet_08/TRS 1 GB pc2-5300CL5 667Mhz-2.jpg

Hint: The label is for the whole memory module, not for a single chip.

(a) What does the label 1GB 128Mx64 stand for?

Proposal for solution: The label describes the whole memory module (not a single chip): 1 GiB total capacity, with a 64 bit bus.

(b) Can you make assumptions about the used single chips of the module?

Proposal for solution: According to the label, one chip could have 128Mi–but we don't now how much pins one chip has.

(c) Try to draw a sketch of the chip arrangement on the memory module.

Proposal for solution:

Here https://www.reusbetter.de/trs-2x1gb-trsdd2001g64u-667cl5bzx-16-pc2-5300. html is a hint that the module is a DIMM, which means chips on both sides. Because there is no additional information readable, we are not able to definitely make a statement. We are only able to assume there are 8 modules on one side.

```
1  Number of chips: 8 chips on one side * 2 sides = 16 chips in total
2
3  -> Chip capacity: 1 GiB module capacity / 16 chips = 64 MiB per chip
4  -> Pins per chip: 64 MiB * 8 Bit (1 byte has 8 bit) / 128 Mi = 4 pins per chip
5  -> Number of chips per row: 64 Bit data bus width / 4 pins per chip = 16 chips
```

With that information, we can assume that the 16 chips are arranged as one row (8 chips on the front and 8 chips of the back side), which looks very similar to *exercise 8.1 chip type 2.*