Exercise sheet 8 – Memory hardware

Goals:

- Memory hardware
- Memory capacity

Hint: consider the lecture about the orders of magnitudes for bits and bytes (decimal and binary)

Exercise 8.1: Interconnection of memory chips

(a) State the layout (and the address lanes) for the following memory modules by drawing a scheme:
  - Chip type 1: 1 GiB, databus: 64 bits, available memory chips: 64M x 8
  - Chip type 2: 1 GiB, databus: 64 bits, available memory chips: 128M x 4

(b) Which of those single chips can store more data? *Hint: Calculate the capacity for every chip-type.*

(c) Can you realise a total memory of 512 MiB with the second chip type?

(d) Where are two following 64-bit-words stored in chip type 1 if you use the most significant bit (= bit 26) for chip (row) selection in the address lanes?

(e) Where are two following 64-bit-words stored in chip type 1 if you use the least significant bit (= bit 0) for chip (row) selection in the address lanes?

Exercise 8.2: Memory module and chip analysis 1

(a) Update the `RA_exercises` repository with `git pull`.

(b) Open the dual channel picture `RA_exercises/sheet_08/dual_channel.jpg` and search for some information about the type of the memory module on the right side.

taken from Von Smial - Own Work, FAL, https://commons.wikimedia.org/w/index.php?curid=2999544

(c) You can only see half of the module in the picture. How many memory chips may this module contain in total? Draw a sketch of the module to visualise the situation and try to state something about the data bus width and the capacity.

Exercise 8.3: Memory module and chip analysis 2

Check out the following pictures and interpret the label:
`RA_exercises/sheet_08/TRS 1 GB pc2-5300CL5 667Mhz-0.jpg`
`RA_exercises/sheet_08/TRS 1 GB pc2-5300CL5 667Mhz-2.jpg`
Hint: The label is for the whole memory module, not for a single chip.

(a) What does the label 1GB 128Mx64 stand for?

(b) Can you make assumptions about the used single chips of the module?

(c) Try to draw a sketch of the chip arrangement on the memory module.