



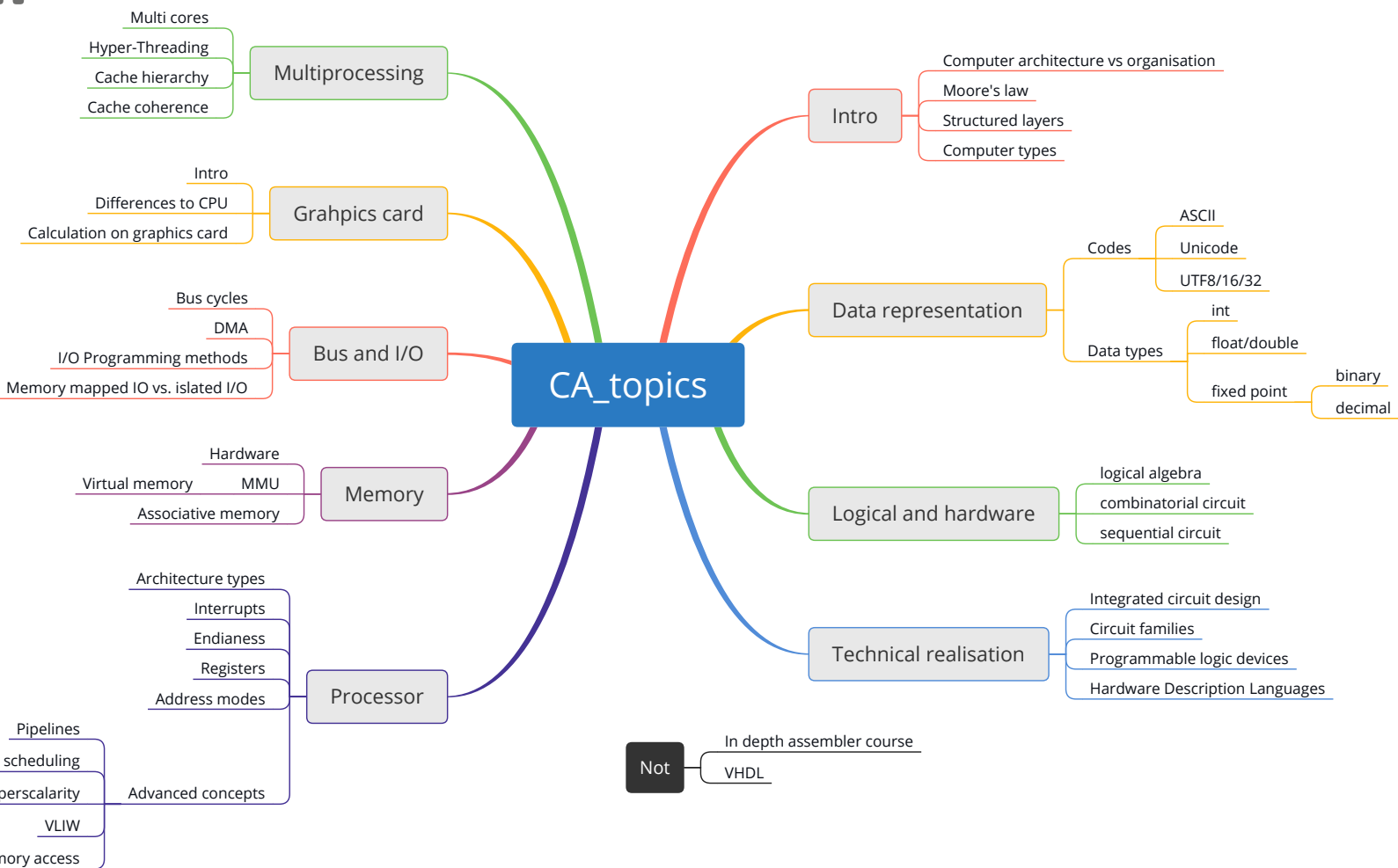
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CA 8 – Memory 1

The lecture is based on the work and the documents of Prof. Dr. Theodor Tempelmeier

Goal



Goal

CA::Memory 1 - Hardware

- Memory types
- Memory chips
- Memory modules
- Modern memory modules

Memory types

RAM vs ROM

RAM - Random access memory

- For **read and write** access
- Usage: **programs and data**
- It is (usually) a **volatile** memory (data are lost when power is switched off)
- **Very fast** access time
- **High power** consumption
- **Expensive**

ROM - Read only memory

- For **read only** memory access
- Usage: **firmware** (BIOS, UEFI)
- It is a **non-volatile** memory (remembers the data even if power is switched off)
- Usually **slower than RAM**
- **Low power** consumption
- **Cheaper** than RAM
- Example: EPROM, EEPROM

Memory types

It's all about **RAM!**

Memory types

SRAM vs DRAM

Property	SRAM - Static RAM	DRAM - Dynamic RAM
Construction	- Complex	+ Simple
Realisation of a bit	- 4..6 transistors	+ 1 transistor + 1 capacitor
Speed	+ Faster	- Slower
Size (capacity)	- Small	+ Large
Cost	- Expensive	+ Cheap
Used for	Cache memory	Main memory
Density	- Less dense	+ Highly dense
Charge leakage	+ Not present	- Present: refresh required
Power consumption	+ Low	- High

Orders of magnitudes for bits and bytes

Bits:

Bits (decimal)			
Symbol	Power	Num bits	Name
1 kbit	10 ³	1.000	kilobit
1 Mbit	10 ⁶	1.000.000	megabit
1 Gbit	10 ⁹	1.000.000.000	gigabit
1 Tbit	10 ¹²	1.000.000.000.000	terabit
...			

Bits (binary)			
Symbol	Power	Num bits	Name
1 Kibit	2 ¹⁰	1.024	kibibit
1 Mibit	2 ²⁰	1.048.576	mebibit
1 Gibit	2 ³⁰	1.073.741.824	gibibit
1 Tibit	2 ⁴⁰	1.099.511.627.776	tebibit
...			

Bytes:

Bytes (decimal)			
Symbol	Power	Num bytes	Name
1 kB	10 ³	1.000	Kilobyte
1 MB	10 ⁶	1.000.000	Megabyte
1 GB	10 ⁹	1.000.000.000	Gigabyte
1 TB	10 ¹²	1.000.000.000.000	Terabyte
...			

Bytes (binary)			
Symbol	Power	Num bytes	Name
1 KiB	2 ¹⁰	1.024	Kibibyte
1 MiB	2 ²⁰	1.048.576	Mebibyte
1 GiB	2 ³⁰	1.073.741.824	Gibibyte
1 TiB	2 ⁴⁰	1.099.511.627.776	Tebibyte
...			

Memory modules and chips - overview

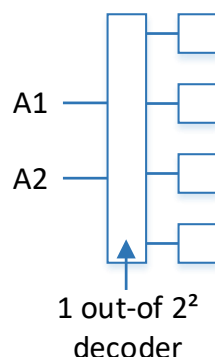


[source: wikipedia.org]

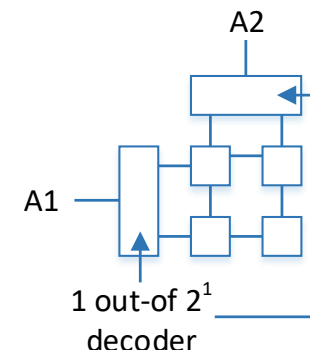
Memory chips

Arrangement of memory cells: (within a memory chip)

Linear Arrangement:



Matrix Arrangement:

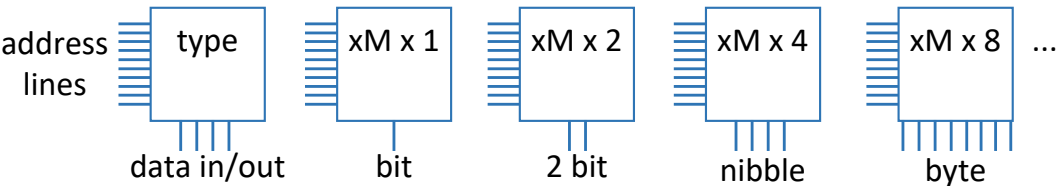


- To address 1-out-of- 2^n memory cells, n address lanes are required.
- Problem: Address lanes are expensive (takes place on the chip)

- To address 1-out-of- 2^n memory cells, only $n/2$ address lanes are required.
- The address is usually transferred in two steps:
 - 1: Row address
 - 2: Column address
- Only half the address lanes are required

Memory chips

Chip types:



Terminology:

Description	Type	Unit
Chip with x mega that provides 1 bit per address	xM x 1	bit
Chip with x mega that provides 2 bit per address	xM x 2	2 bit
Chip with x mega that provides 4 bit per address	xM x 4	nibble
Chip with x mega that provides 8 bit per address	xM x 8	byte

Memory chips

Chip capacity:

On these chips: K means Ki, M means Mi, G means Gi, ...

xK/xM/xG denotes the number of chip cell rows inside the chip

Chip capacity = xM x number of bits per chip

Examples:

■ 16M x 1: 16Mi x 1 = 16 Mibit $\Rightarrow 16\text{Mi}/8 = 2 \text{ MiB}$

■ 16M x 2: 16Mi x 2 = 32 Mibit $\Rightarrow 32\text{Mi}/8 = 4 \text{ MiB}$

■ 1G x 4: 1Gi x 4 = 4 Gibit $\Rightarrow 4\text{Gi}/8 = 512 \text{ MiB}$

■ 1G x 8: 1Gi x 8 = 8 Gibit $\Rightarrow 8\text{Gi}/8 = 1 \text{ GiB}$

Questions?

All right? \Rightarrow 

Question? \Rightarrow  and use **chat**

or

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Memory modules

The memory chips on a memory module are usually arranged in a matrix layout.



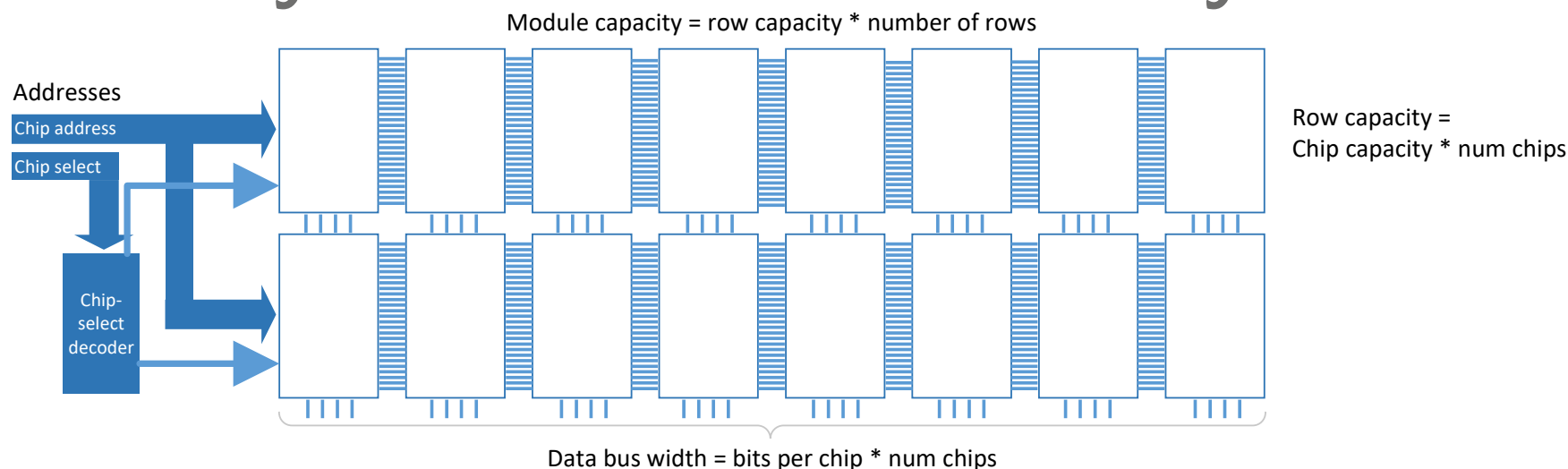
[image source: samsung.com]

Memory address is divided into:

- Chip select address
- Chip address (inside the chip)



Memory modules - hardware layout



Address calculations:

Nr. Descriptions

- (1) Number of bits to address the module capacity
- (2) Number of address lanes/bits for chip select
- (3) Number of address lanes/bits for chip address
- (4) Number of bits to address the bytes inside the word

Calc

- $$\log_2(\text{module capacity})$$
- $$\log_2(\text{num. rows})$$
- $$\log_2(\text{num. chip cell rows})$$
- $$\log_2(\text{num. bytes per word})$$

Results

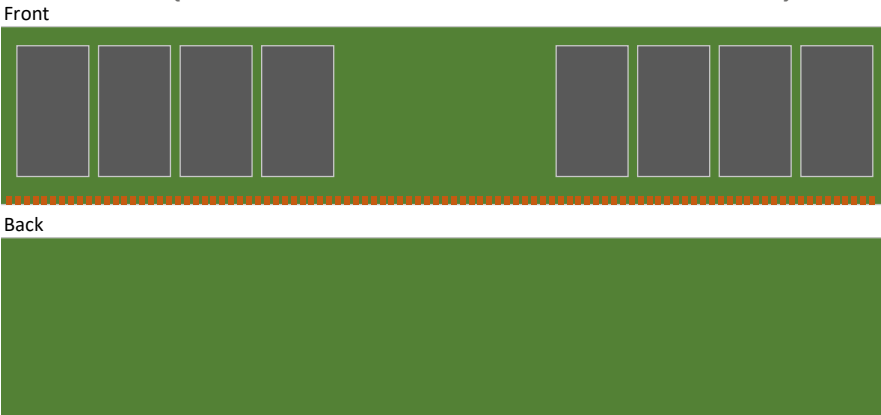
- number of bits
- number of bits/address lanes
- number of bits/address lanes
- number of bits

Address calculation relationship:

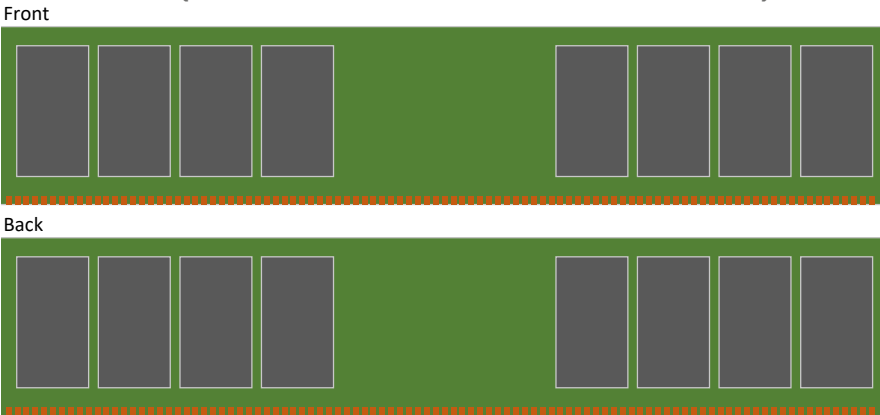
Number of bits to address the module capacity: $(1) = \sum_{i=2}^4 (i) = (2) + (3) + (4)$

Memory modules - formats

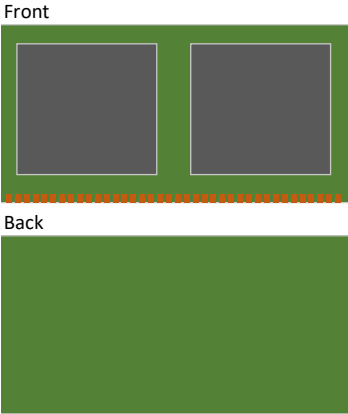
SIMM (single inline memory module):



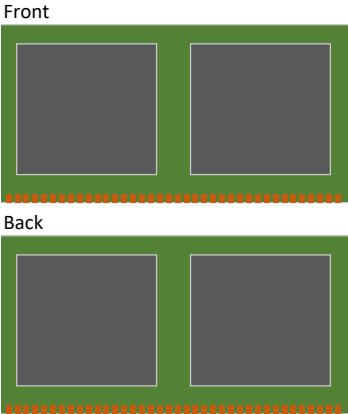
DIMM (dual inline memory module):



SO-SIMM (small outline SIMM):



SO-DIMM (small outline DIMM):



Memory modules - interleaving

Problem:

After a **memory cell** is read in a DRAM, the cell **needs to be refreshed** and this takes some time.

Idea:

Distribute consecutive addresses evenly across the chip rows.

- **Reduces** the problem of **waiting** until the refresh is complete
- **Accelerates memory access** in an effect similar to pipelining
- But due to the increased capacities of the individual chips, a memory module has only one or two chip rows. -> Solution:

SDRAM

Questions?

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Modern memory modules

Overview of various terms in the memory area

SDRAM

SDRAM: synchronous DRAM

- **Synchronous** means there as a **clock** pulse
- **Dynamic** means there is a **refresh necessary**
- **Memory is divided** into several equally sized and independent **banks**: allows **interleaving** within chips
- Chips can accept new commands before finishing the previous one (for another bank).

ECC

ECC: error checking and correction

- ECC memory can **detect and correct** the most common kinds of internal **data corruption**
- Allows the **detection** and **correction** of **single bit errors**
- Some do also **detect double bit errors**
- Application area: Scientific and financial computing applications which operate on sensitive data

DDR-SDRAM

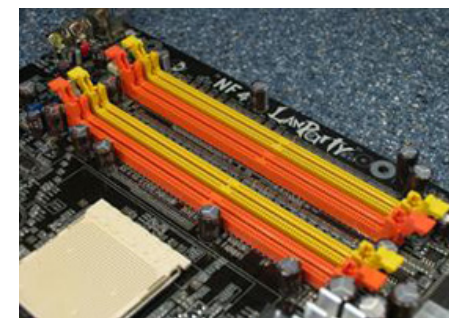
DDR-SDRAM: double data rate SDRAM

Idea:

- Transfers data at almost double the transfer rate
- **Data is transferred on rising and falling edges.**
- DDR4-RAM is state of the art for computers
- DDR5-RAM is approaching into the market in 2020/2021

	DDR3	DDR4	DDR5
Data transfer rate	17 GiB/s	25,6 GiB/s	51,2 GiB/s
Max module capacity	16 GiB	64 GiB	128 GiB

Multi-channel memory architecture



[source: wikipedia.com]

Idea:

- Adds **multiple channels** from the memory to the controller
- **Increase data transfer rate** of DRAM memory modules with the memory controller
- Dual/Triple/Quad-channels are possible
- **Dual-channel: theoretically doubles** the data transfer rate
- New Intel processors (like Intel Core i7-9800X) supports quad-channel memory architecture

Questions?

All right?



Question?



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Summary and outlook

Summary

- Memory types
- Memory chips
- Memory modules
- Modern memory modules

Outlook

- MMU
- Virtual memory