Exercise sheet 3 – Hardware

Goals:

- Basic knowledge about chip manufacturing
- Hardware circuits
- Interrupt handling

Exercise 3.1: Chip manufacturing?

We'll watch the *chip manufacturing* video from Infineon: `https://www.youtube.com/watch?v=_Kj58yQ67KI`

(a) What is the main commodity for computer chips.

Proposal for solution: Sand/Silicium.

(b) What is a transistor in the context of a microchip and how many pins does it have?

Proposal for solution: A transistor is the smallest switch unit on a microchip. Every transistor has 3 pins. It works like a switch.

(c) How are the chips designed/programmed/planned?

Proposal for solution: With computer aided design (CAD) and simulation programs.

(d) What kind of production environment is required to produce computer chips?

Proposal for solution: A special clean room (dust-free) is required.

(e) How many chips can be on produced on a wafer?

Proposal for solution: Some dozen up to several thousand, depending on the wafer size and the chip size.

(f) How many pins does each chip have?

Proposal for solution: More than 1000 pins are possible.

Exercise 3.2: Update RA repository

(a) `cd RA_exercises`
(b) `git pull`

Exercise 3.3: Hardware: combinatorial circuit vs. sequential circuit?

(a) Describe the difference between combinatorial circuits and sequential circuits.

Proposal for solution: sequential circuit = combinatorial circuit + time (clock) + register states

- sequential circuit = Schaltwerk
- combinatorial circuit = Schaltnetz

(b) The programmable logic device (PLD) *GAL 16v8* can be run in 'simple mode' without a clock entry or in 'registered mode' with clock entry (cf. `RA_exercises/sheet_03/lattice_gal16v8.pdf`). State the reference to the question 3.3a.

Exercise 3.4: Hardware: GAL Programming

For this exercise use the `RA_exercises/sheet_03/gal16v8_logic_diagram_registered_mode.pdf` file as a template for your drawings (programming). Program the GAL16V8 in **registered mode**. *Hint: You may print this or you use a PDF annotator like Xournal++.*

(a) Denote the clock input as: CLK.

(b) Denote the inputs as: $A_0, A_1, \ldots$

(c) Denote the outputs as: $Q_0, Q_1, \ldots$

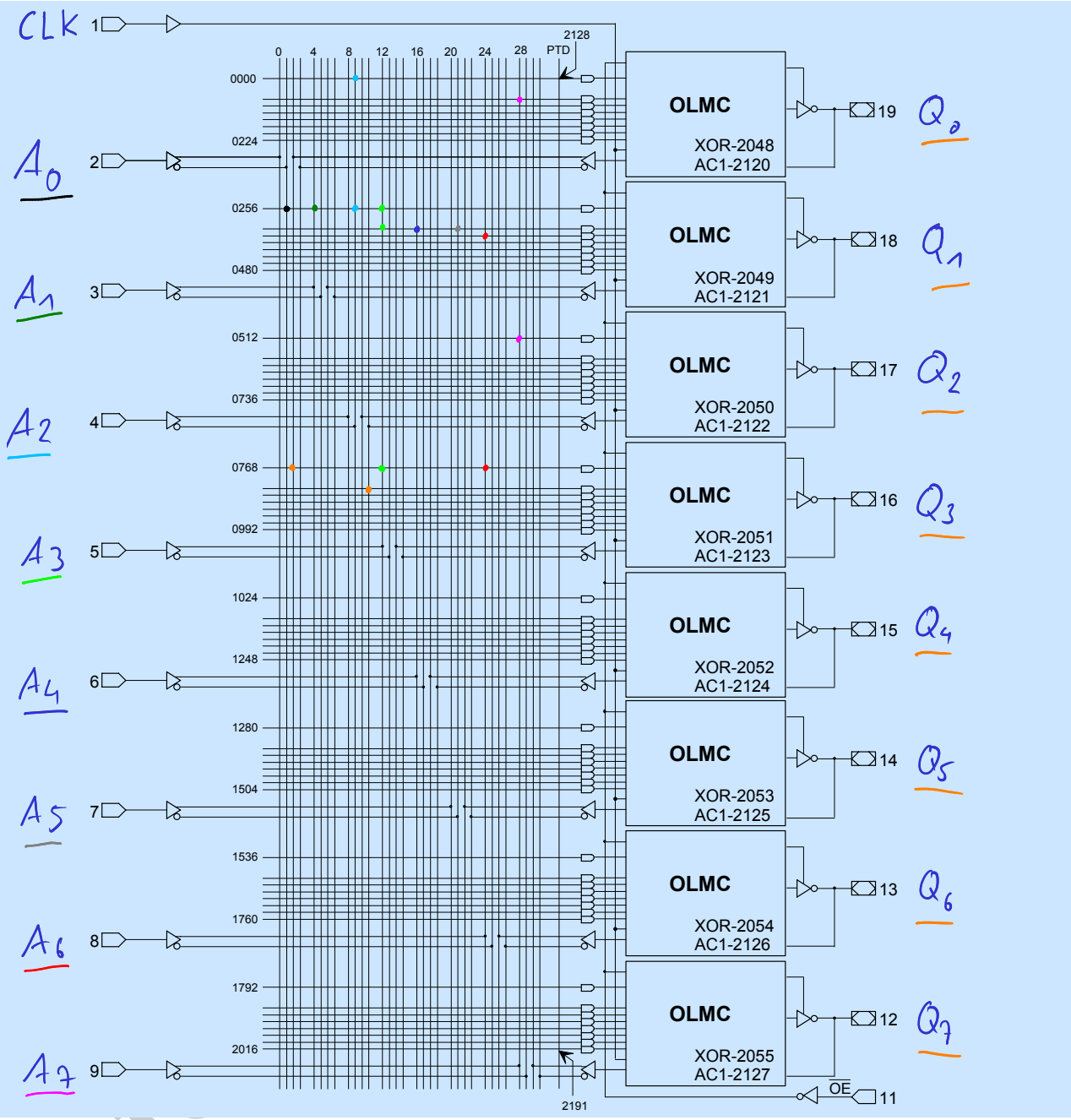
(d) Program $Q_0 = \bar{A}_2 + A_7$

(e) Program $Q_1 = A_3 \cdot \bar{A}_2 \cdot A_1 \cdot \bar{A}_0 + A_3 \cdot A_4 \cdot \bar{A}_5 + A_6$

(f) Program $Q_2 = A_7$

(g) Program $Q_3 = A_6 \cdot A_3 \cdot Q_0 + \bar{Q}_2$

Proposal for solution:



Exercise 3.5: Signal propagation time of the Lattice GAL16V8

(a) The Lattice GAL16V8 has a maximum signal propagation time of $t_{max} = 3.5$ ns. What is the supported theoretical maximum frequency F_{max} in MHz?

Proposal for solution: $F_{max} \approx 285$MHz. The GAL16V8 documentation states $F_{max} = 250$MHz, this is a bit slower than the theoretical maximum frequency which we calculated, due to some more detailled timing delays that has to be considered.