

## Exercise sheet 12 – I/O

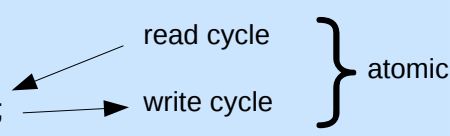
### Goals:

- Programmed I/O
- Interrupt driven I/O
- DMA

### Exercise 12.1: Synchronisation commands

- (a) Describe a machine instruction for synchronisation and its interaction with the application, OS (operating system), and bus level. *Hint: You may consider the TAS command and semaphores, learned in the Operating Systems (Betriebssysteme) lecture as well as in this lecture. Use some pseudo-code to describe your ideas.*

**Proposal for solution:** Remember the *TAS* (test and set) command from lecture the Operating Systems? We learned that the OS is using it to provide semaphores for synchronization.

<u>Application</u>	<u>OS</u>	<u>Bus</u>
P(s);	<pre> P_OP(s) {     do {         TAS_LOCK;     } while(!successful)     }                 </pre>	
// critical section	<pre> . . .                 </pre>	
V(s);	<pre> V_OP(s) {     LOCK = 0; // release     }                 </pre>	
Semaphore (P()/V() operation)	TAS instruction with (LOCK variable)	Atomic read/write bus cycle (LOCK bus signal)

### Exercise 12.2: Programmed I/O (single transfer) with busy wait (pseudo C code)

Consider a system with the *F-Bus serial interface* (FSI). You want to receive data (characters) from the FSI with the busy wait approach. Compare the lecture for that.

- (a) Update the RA\_exercises repository with `git pull`.

- (b) In

RA\_exercises/sheet\_12/io\_pc\_prog\_io\_busy\_wait/io\_pc\_prog\_io\_busy\_wait.c  
you will find a skeleton file.



- (c) Complete the skeleton with pseudo C to read 16 bytes (characters) from the *F-Bus serial interface* (FSI) into the memory buffer.

**Proposal for solution:**

```
1  #include <stdlib.h>
2  #include <inttypes.h>
3
4  typedef volatile struct { //FSI interface
5      uint16_t CSR; //control and status register
6      uint16_t TBUF; //transmit buffer register
7      uint16_t RBUF; //receive buffer register
8      uint16_t CFR; //configuration register
9  } FsiStruct;
10
11 //FSI: FsiStruct is mapped to the memory position 0xFF000000
12 #define FSI (*(FsiStruct*)(0xFF000000))
13
14 #define TRDY (0B1000000000000000) //Mask for TRDY (or: 0x8000)
15 #define TIE (0B0100000000000000) //Mask for TIE (or: 0x4000)
16 #define RRDY (0B0000000010000000) //Mask for RRDY (or: 0x0080)
17 #define RIE (0B0000000001000000) //Mask for RIE (or: 0x0040)
18 //more defines...
19
20 #define BUFFER_SIZE (16)
21 uint8_t buffer[BUFFER_SIZE] = {0}; //initialise all elements with 0
22
23 int main(void) {
24     for(int i = 0; i < BUFFER_SIZE; ++i) {
25         while((bool)(FSI.CSR & RRDY) == false) { //wait until FSI has provided next ch
26             //busy wait (do nothing)
27         }
28         buffer[i] = (uint8_t)FSI.RBUF;
29     }
30
31     return EXIT_SUCCESS;
32 }
```

**Exercise 12.3: Programmed I/O (single transfer) with polling (pseudo C code)**

Consider a system with the *F-Bus serial interface* (FSI). You want to receive data (characters) from the FSI with the polling approach. Compare the lecture for that.

- (a) In `RA_exercises/sheet_12/io_pc_prog_io_polling/io_pc_prog_io_polling.c` you will find a skeleton file.
- (b) Complete the skeleton with pseudo C to read 16 bytes (characters) from the *F-Bus serial interface* (FSI) into the memory buffer.

**Proposal for solution:**

```
1  #include <stdlib.h>
2  #include <inttypes.h>
3  #include <stdbool.h> //bool
4
5  typedef volatile struct { //FSI interface
6      uint16_t CSR; //control and status register
7      uint16_t TBUF; //transmit buffer register
8      uint16_t RBUF; //receive buffer register
```



```
9     uint16_t CFR; //configuration register
10 } FsiStruct;
11
12 //FSI: FsiStruct is mapped to the memory position 0xFF000000
13 #define FSI (*((FsiStruct*)(0xFF000000))
14
15 #define TRDY (0B1000000000000000) //Mask for TRDY (or: 0x8000)
16 #define TIE (0B0100000000000000) //Mask for TIE (or: 0x4000)
17 #define RRDY (0B0000000001000000) //Mask for RRDY (or: 0x0080)
18 #define RIE (0B0000000000100000) //Mask for RIE (or: 0x0040)
19 //more defines...
20
21 #define BUFFER_SIZE (16)
22 uint8_t buffer[BUFFER_SIZE] = {0}; //initialise all elements with 0
23
24 int main(void) {
25     for(int i = 0; i < BUFFER_SIZE; ++i) {
26
27         while(true) {
28             if((bool)(FSI.CSR & RRDY) == true) { //if the FSI has provided next character
29                 buffer[i] = (uint8_t)FSI.RBUF; //copy the received character
30                 break; //proceed with next character
31             } else {
32                 //do something else...
33             }
34         }
35     }
36
37     return EXIT_SUCCESS;
38 }
```

#### Exercise 12.4: Interrupt driven I/O (single transfer) (pseudo C code)

Consider a system with the *F-Bus serial interface* (FSI). You want to receive data (characters) from the FSI with the interrupt control approach. Compare the lecture for that.

- (a) In `RA_exercises/sheet_12/io_pc_interrupt_io/io_pc_interrupt_io.c` you will find a skeleton file.
- (b) Complete the skeleton with pseudo C to read 16 bytes (characters) from the *F-Bus serial interface* (FSI) into the memory buffer.

#### Proposal for solution:

```
1 #include <stdlib.h>
2 #include <inttypes.h>
3
4 typedef volatile struct { //FSI interface
5     uint16_t CSR; //control and status register
6     uint16_t TBUF; //transmit buffer register
7     uint16_t RBUF; //receive buffer register
8     uint16_t CFR; //configuration register
9 } FsiStruct;
10
11 //FSI: FsiStruct is mapped to the memory position 0xFF000000
12 #define FSI (*((FsiStruct*)(0xFF000000))
13
14 #define TRDY (0B1000000000000000) //Mask for TRDY (or: 0x8000)
15 #define TIE (0B0100000000000000) //Mask for TIE (or: 0x4000)
```



```
16 #define RRDY (0B0000000010000000) //Mask for RRDY (or: 0x0080)
17 #define RIE (0B0000000001000000) //Mask for RIE (or: 0x0040)
18 //more defines...
19
20 typedef void (*ISR_t)(void); //Function pointer for an ISR
21 //INTVECTOR: ISR_t is mapped to the memory position 0x000000C8
22 #define INTVECTOR (*(ISR_t*)(0x000000C8))
23
24 #define BUFFER_SIZE (16)
25 volatile uint8_t counter = 0;
26 volatile uint8_t buffer[BUFFER_SIZE] = {0}; //initialise all elements with 0
27
28 void ISR_serial_read(); //prototype
29
30 int main(void) {
31     //Start transfer
32     INTVECTOR = &ISR_serial_read; //set ISR for receive character
33     FSI.CSR |= RIE; //enable RIE flag
34
35     //do something else while transfer is in progress...
36
37     return EXIT_SUCCESS;
38 }
39
40 //an interrupt is triggered if
41 //the hardware has provided a new character
42 void ISR_serial_read() {
43     buffer[counter] = (uint8_t)FSI.RBUF;
44     counter++;
45     if (counter == BUFFER_SIZE){
46         FSI.CSR &= ~RIE; //delete the RIE flag to stop the transfer
47                          //~ is the bitwise inversion.
48
49         //buffer full -> inform outer world (somehow)
50     }
51 }
```

### Exercise 12.5: DMA programming (pseudo C code)

Consider a system with the *F-Bus DMA disk* (FDD). You want to write data (some words) from the memory with the DMA approach to the disk. Compare the lecture for that.

- (a) In `RA_exercises/sheet_12/io_pc_dma/io_pc_dma.c` you will find a skeleton file.
- (b) Complete the skeleton with pseudo C to write 16 words (4 bytes per word) from the memory to the *F-Bus DMA disk* (FDD).
- Source (memory) starting address: 0x400000
  - Target (disk) starting address: 0x4711

*Hint: Source, destination, how much, GO!*

#### Proposal for solution:

```
1 #include <stdlib.h>
2 #include <stdbool.h>
3 #include <inttypes.h>
4
```



```
5  typedef volatile struct { //FDD interface
6      uint32_t CSR; //control and status register
7      uint32_t DARH; //disk address register HI
8      uint32_t DARL; //disk address register LO
9      uint32_t BAR; //bus address register
10     uint32_t BCR; //byte count register
11 } FddStruct;
12
13 //FDD: FddStruct is mapped to the memory position 0xFF000010
14 #define FDD (*(FddStruct*)(0xFF000010))
15
16 #define GO      (0x01) //Mask for GO
17 #define IE      (0x40) //Mask for IE
18 #define WRITE   (0x02) //Mask for WRITE
19 //more defines...
20
21 typedef void (*ISR_t)(void); //Function pointer for an ISR
22 //INTVECTOR: ISR_t is mapped to the memory position 0x00000108
23 #define INTVECTOR (*(ISR_t*)(0x00000108))
24
25 void ISR() { //interrupt service routine for the end of the transfer
26     //notify application that everything is transferred
27 }
28
29 int main(void) {
30     //In principle: {source, destination, how much, GO}
31     INTVECTOR = &ISR; //ISR address is set to INTVECTOR (address 0x00000108)
32
33     //Configure DMA interface
34     FDD.BAR = 0x400000; //source memory address
35     FDD.DARH = 0x0; //destination LBA address (bit 32 to 47)
36     FDD.DARL = 0x4711; //destination LBA address (bit 0 to 31)
37     FDD.BCR = 0x40; //how much: number of bytes
38     FDD.CSR = IE | WRITE | GO; //0x43
39
40     //DMA transmits data now without CPU.
41     //At the end there is an interrupt!
42
43     return EXIT_SUCCESS;
44 }
```