Exercise sheet 9 – Memory

Goals:

- MMU
- Virtual memory

Exercise 9.1: Intel x86/32 bit 1 level page table

Consider an Intel x86/32 bit architecture with a 1 level page table, similar to the 1 level page table in the lecture.
Given are:

- 32 bit architecture
- 4 KiB page/frame size
- 1 level page table
- Virtual address: 0x1202F494
- Real address: 0x00014494

The virtual address is mapped to the real address.

(a) State the *offset* part of the given addresses.

(b) State the *page number* and the page base address.

(c) State the *frame number* and the frame base address.

(d) State the entry and its position in the page table for the given situation. *Hint: You may want to draw a scheme, similar to the lecture. Specify as much details as possible with explicit numbers.*

(e) How many pages are possible for the given 32 bit architecture?

(f) Estimate the size in bytes for the page table. *Hint: You may simplify the address calculation by only considering to use a full word (address word) for each entry.*

Exercise 9.2: Intel x86/32 bit 2 level page table

Now consider an Intel x86/32 bit architecture with a 2 level page table (without segmentation). Use the same addresses as given in exercise 9.1.

(a) Have a look on `CA_exercises/sheet_09_memory_mmu/AMD64 Architecture Programmer's Manual.pdf` file page 135 (PDF: 195).

(b) Draw a scheme with the situation. Use as much details as possible with explicit numbers (*you may calculate them and make certain assumptions*).

Exercise 9.3: Intel x86/64 bit architecture with 3 level page table

Hint: Use the »AMD64 Architecture Programmer's Manual Volume 2: System Programming« to answer that question.

Given is:

- Virtual address: 0x0000 FF00 1232 F494
- Real address: 0x0000 0078 0012 F494
- Long-Mode Page Translation
- Page size: 2 MiB
- Bytes used for sign extension: 2
- Maximum bits for real memory addresses: 52 bits
- 3 level page table: *Page-Map, Page-Directory-Pointer, Page-Directory*

(a) Have a look on `CA_exercises/sheet_09_memory_mmu/AMD64 Architecture Programmer's Manual.pdf` file page 146 (PDF: 206).

(b) How many bits are used for the offset? Show the offset in the given addresses.

(c) How many bits are used for each page table level?

(d) Draw a scheme for the page table situation. Use as much details as possible with explicit numbers (you may calculate them and make certain assumptions).

(e) Calculate the maximum addressable real memory.