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CA 5 – Processor 2

The lecture is based on the work and the documents of Prof. Dr. Theodor Tempelmeier

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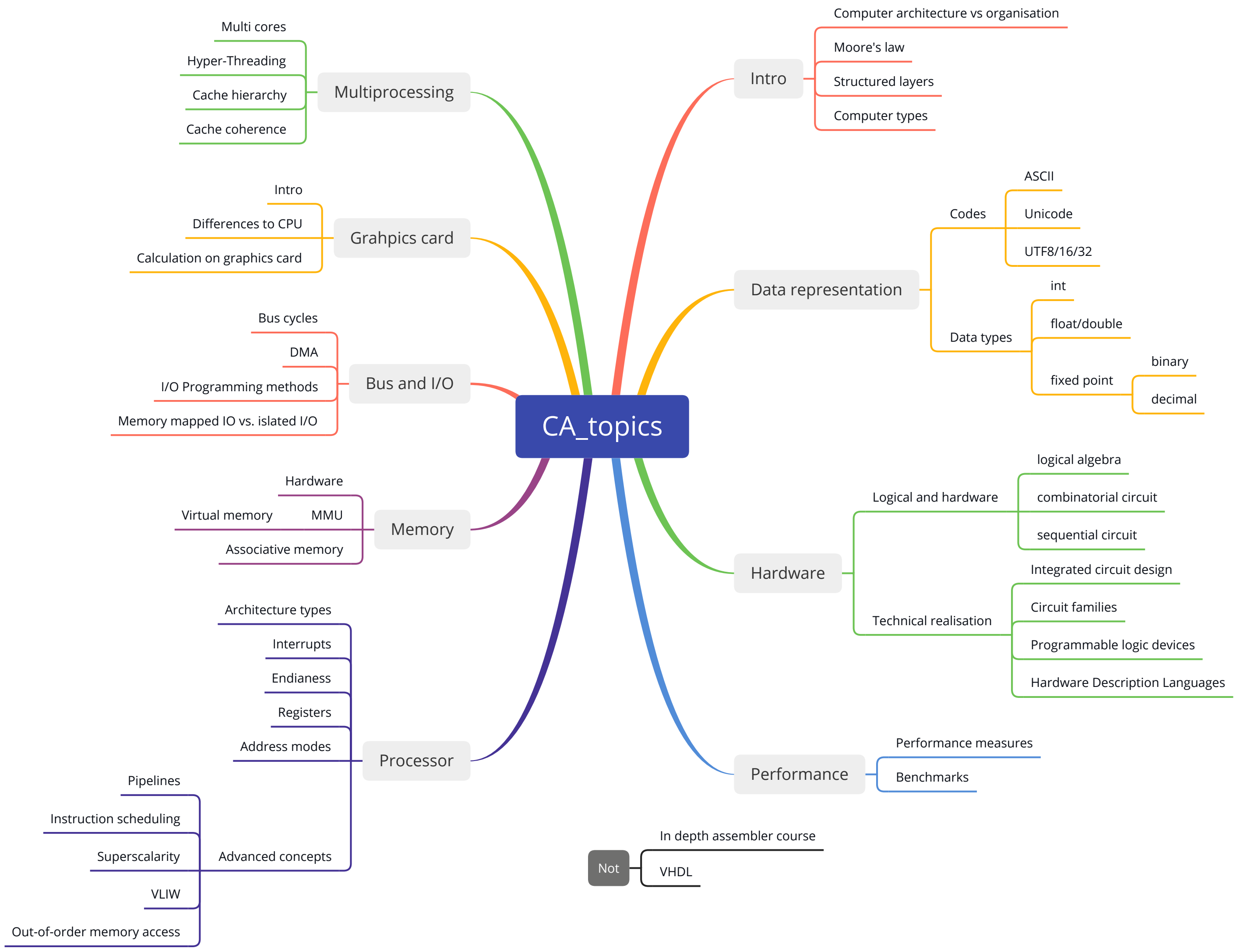
Goal



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Goal

CA::Processor 2

- Endianness
- Examples
- Usage
- Transfer
- Solutions

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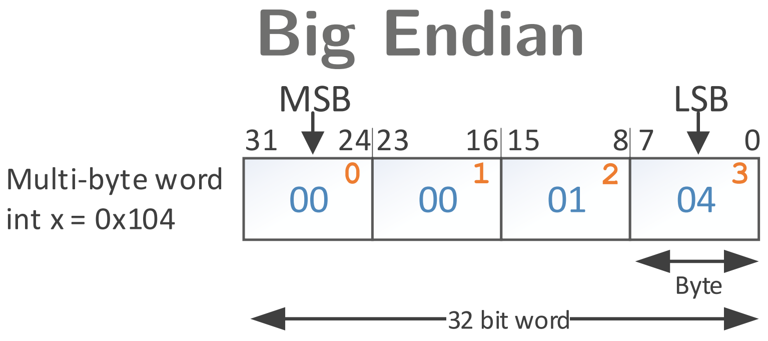
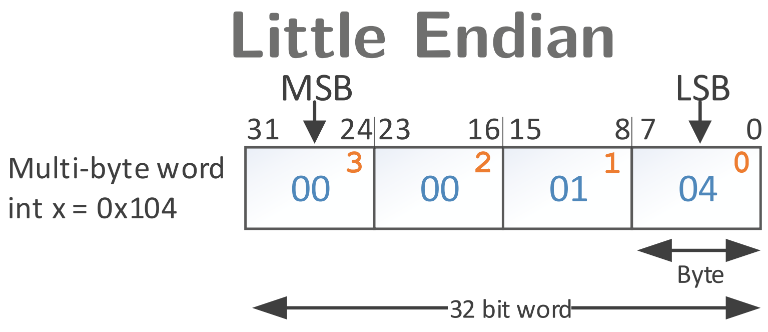
Endianness

Endianness: The definition of the **byte order** within a **multi-byte word**.

Register view of a 32bit architecture:





- MSB - Most significant byte
- LSB - Least significant byte

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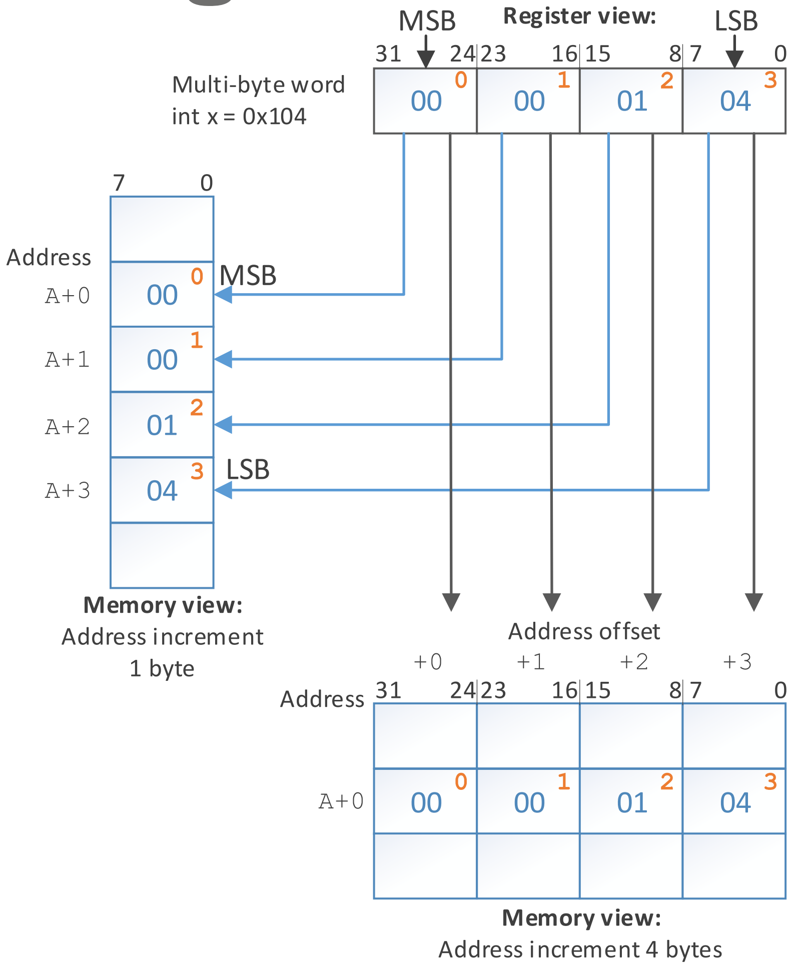
Endianness - Big endian



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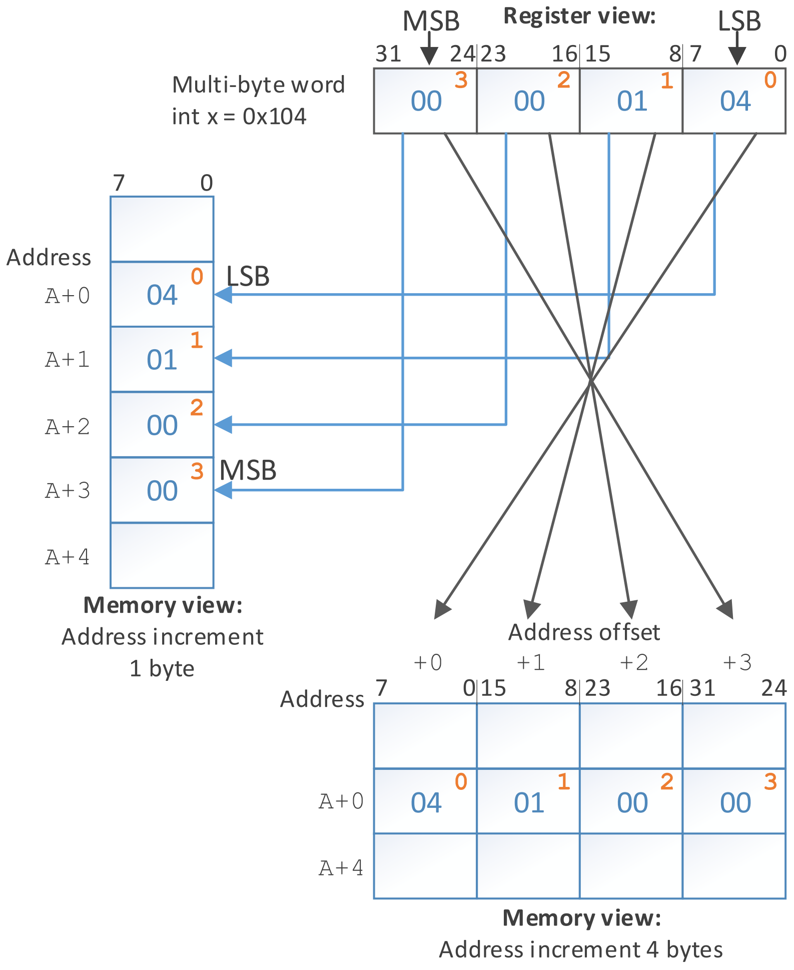
Endianness - Little endian



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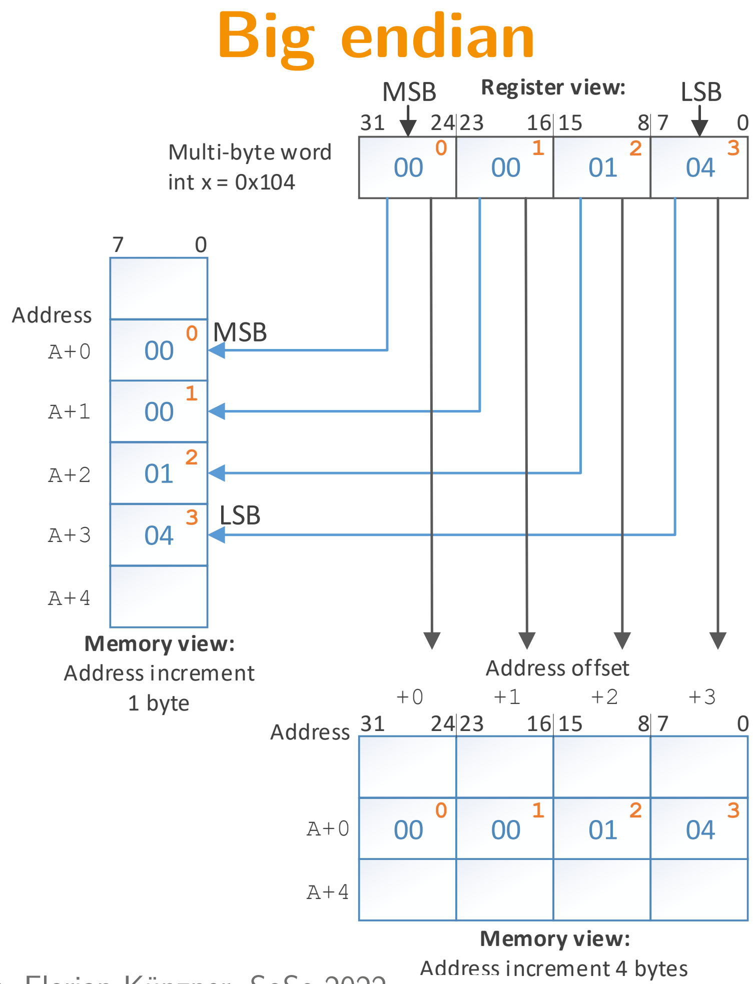
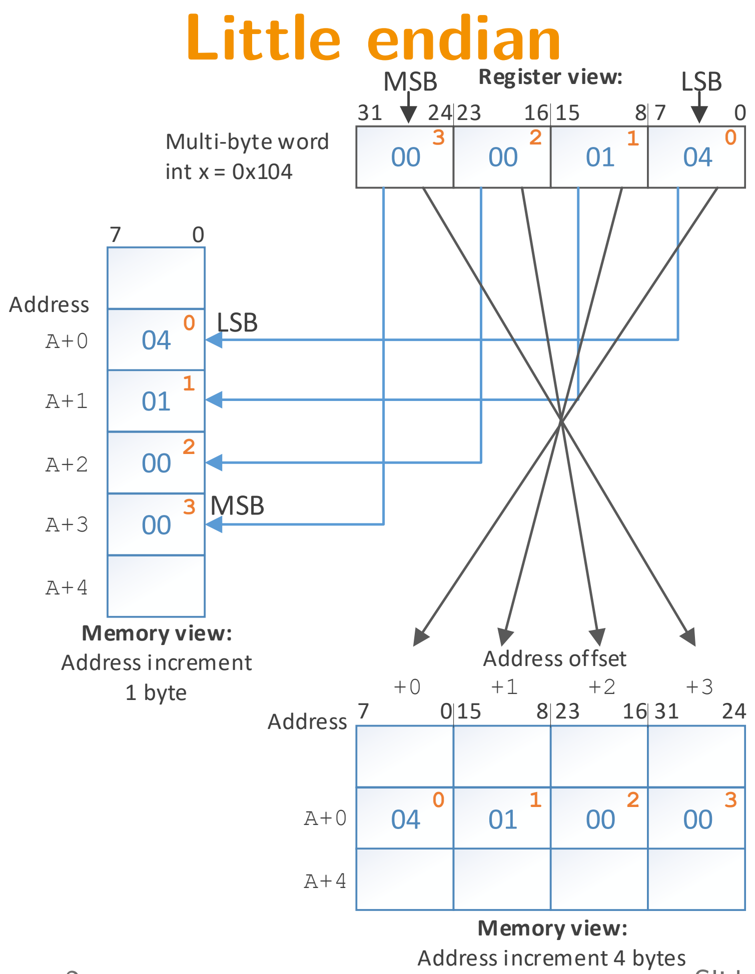
Endianness - BE/LE





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Endianness - example BE

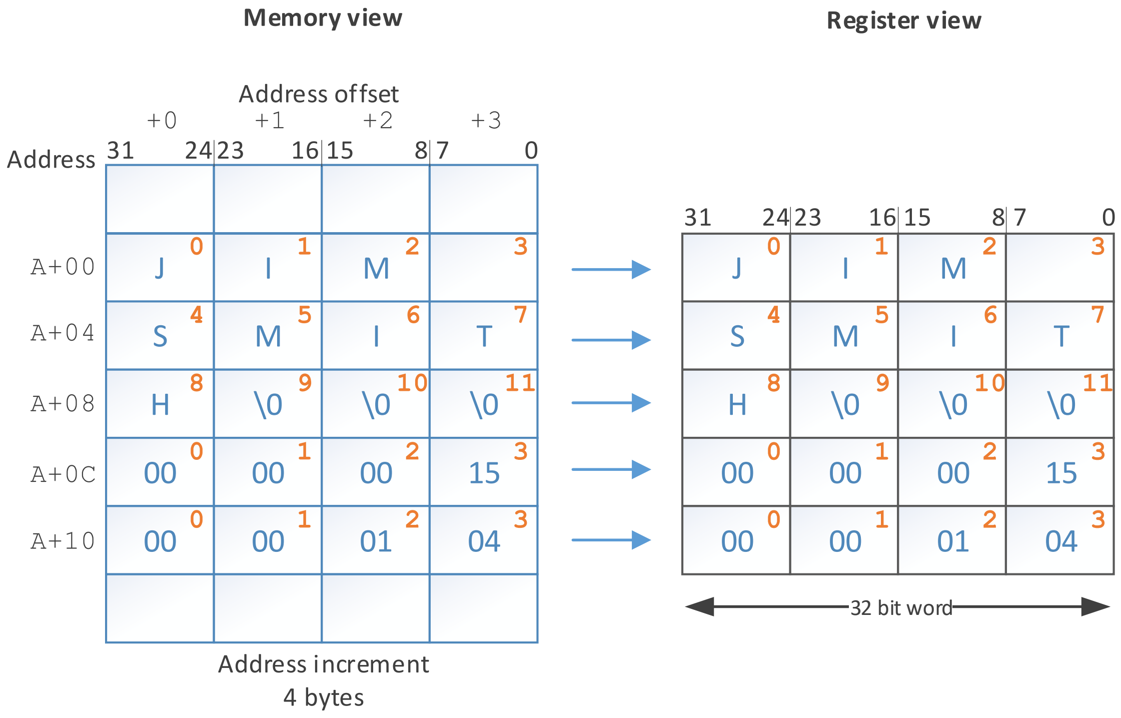
Big endian memory -> Register

```c
#include <stdlib.h>
#include <stdint.h>

int main()
{
    struct employee {
        char     name[12];
        uint32_t age;
        uint32_t dept_nr;
    };

    struct employee smith = {
        .name    = "JIM SMITH",
        .age     = 21,   //0x15
        .dept_nr = 0x104 //260
    };

    return EXIT_SUCCESS;
}
```



[cmp: [1, p. 95-96]]

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Endianness - example LE

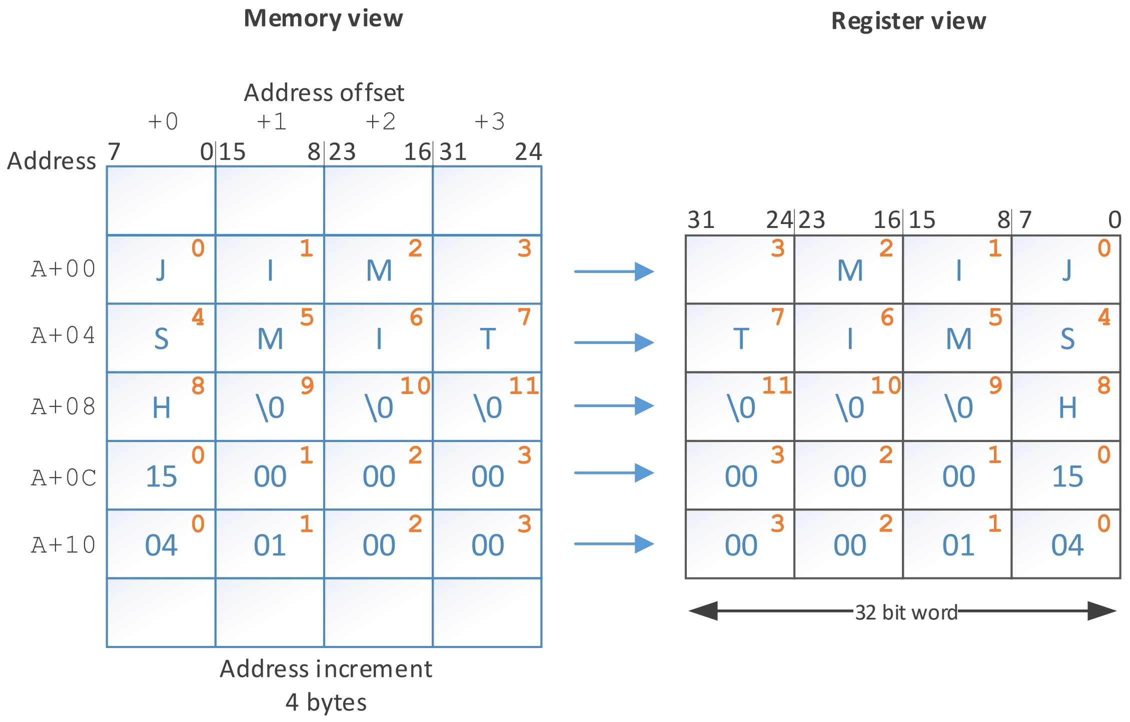
Little endian memory -> Register

```c
#include <stdlib.h>
#include <stdint.h>

int main()
{
    struct employee {
        char      name[12];
        uint32_t age;
        uint32_t dept_nr;
    };

    struct employee smith = {
        .name    = "JIM SMITH",
        .age     = 21,    //0x15
        .dept_nr = 0x104 //260
    };

    return EXIT_SUCCESS;
}
```



[cmp: [1, p. 95-96]]

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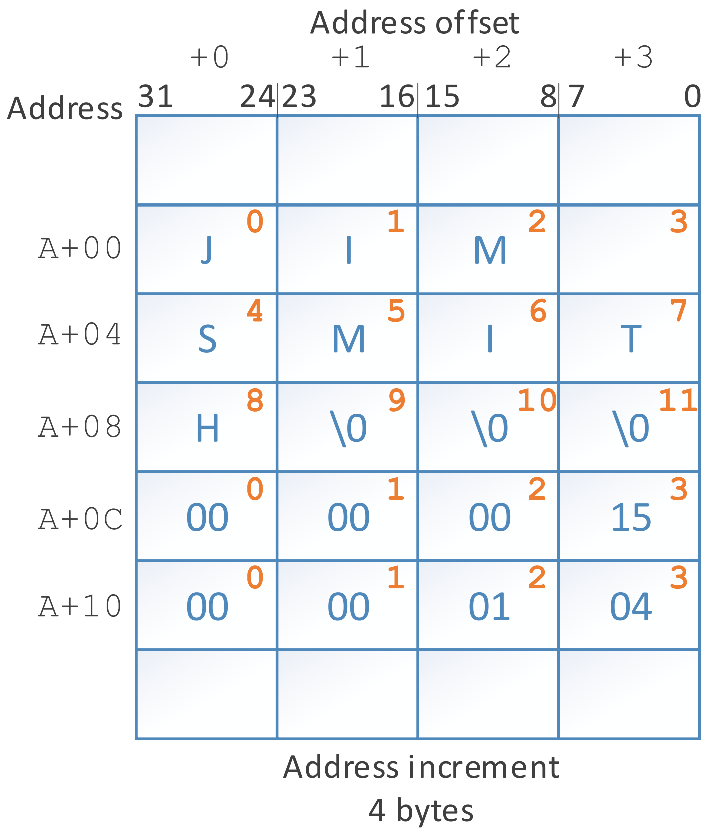
Endianness - example BE/LE

Big endian memory

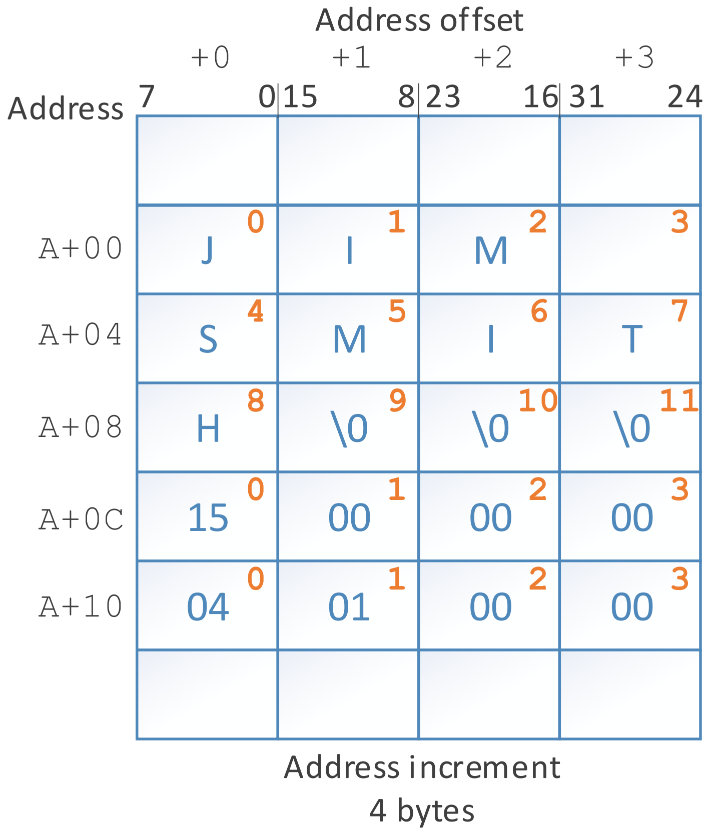


Address offset

Address	+0 (31 … 24)	+1 (23 … 16)	+2 (15 … 8)	+3 (7 … 0)
A+00	J 0	I 1	M 2	3
A+04	S 4	M 5	I 6	T 7
A+08	H 8	\0 9	\0 10	\0 11
A+0C	00 0	00 1	00 2	15 3
A+10	00 0	00 1	01 2	04 3

Address increment
4 bytes

Little endian memory



Address offset

Address	+0 (7 … 0)	+1 (15 … 8)	+2 (23 … 16)	+3 (31 … 24)
A+00	J 0	I 1	M 2	3
A+04	S 4	M 5	I 6	T 7
A+08	H 8	\0 9	\0 10	\0 11
A+0C	15 0	00 1	00 2	00 3
A+10	04 0	01 1	00 2	00 3

Address increment
4 bytes

[cmp: [1, p. 95-96]]

Endianness - usage

Big endian

- IBM Mainframe
- Freescale ColdFire
- Atmel AVR/AVR32
- ARM Thumb and ARM64 (also Apple M1)

Little endian

- Intel x86
- x86-64 (AMD64, Intel 64)
- RISC-V
- Qualcomm Hexagon

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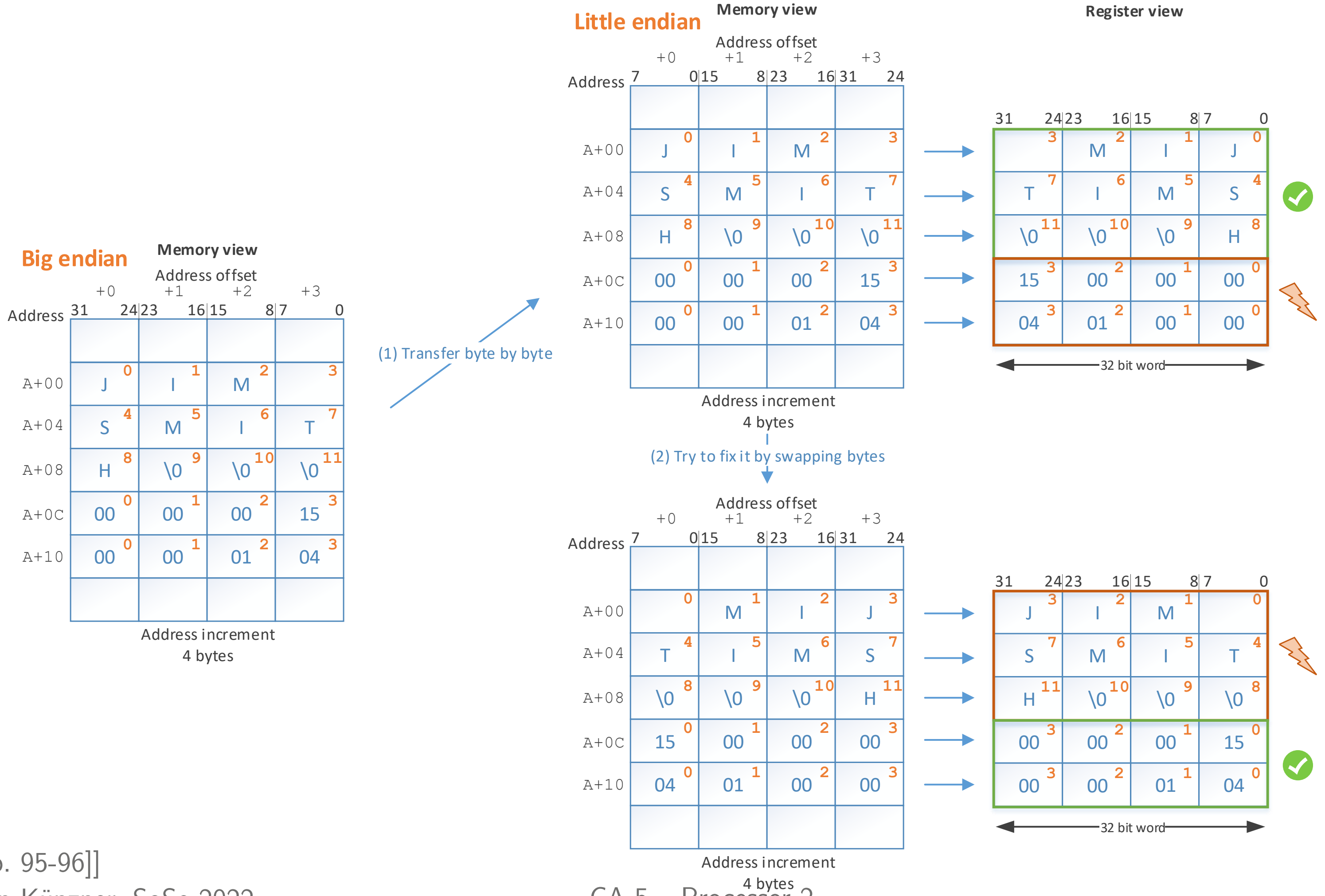
Endianness - transfer: BE to LE



[cmp: [1, p. 95-96]]

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Endianness - problem

Problem can occur if

- Different data types are mixed: numbers, strings, or other data types
- Data type consists of more than one byte (multi-byte word, ≥ 2)
- Data are transferred between BE/LE systems

No problem occurs if

- Single-byte data is transferred byte by byte (e.g. ASCII)
- Data is transferred within same endianness (LE -> LE, BE -> BE)

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Endianness - conclusion

Without the knowledge about the data types and the endianness, a transfer between BE/LE systems is not feasible.

Tanenbaum: „*There is no easy solution to this*“ [1, p. 96]

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Endianness - possible solutions

Possible solution

- **Know** the endianness (e.g. **meta data!**)
- **Transfer** byte by byte (no problem for single-byte data)
- If endianness is different and a multi-byte word is transferred: additionally **swap** the bytes

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Endianness - solutions

Some examples:

- Network order: always BE
- Java: always BE; for transfer with others, `ByteOrder` can be set
- Unicode UTF-16/32: uses a BOM (byte order mark)
- TIF files: BE/LE identifier in header
- RPC (remote procedure call): marshalling (data as byte stream) solves the problem by using meta data

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Summary and outlook

Summary

- Endianness
- Examples
- Usage
- Transfer
- Solutions

Outlook

- Processor registers
- Processor examples
- Addressing modes