Prof. Dr. Florian Künzner
Technical University of Applied Sciences Rosenheim, Computer Science

CA 4 – Processor 1

The lecture is based on the work and the documents of Prof. Dr. Theodor Tempelmeier

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Overview

What are the properties of a processor?

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Processor properties

- Processor architecture
- Exception and interrupt handling
- Instruction set architecture
- Memory model (part of memory lectures)
- Endianness
- Registers
- Addressing modes
- Advanced concepts
  - Instruction scheduling
  - Pipelines
  - Superscalarity
  - VLIW
  - Out-of-order memory access

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Goal

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CA::Processor 1

- Processor architecture
- Exception and interrupt handling
- Instruction set architecture

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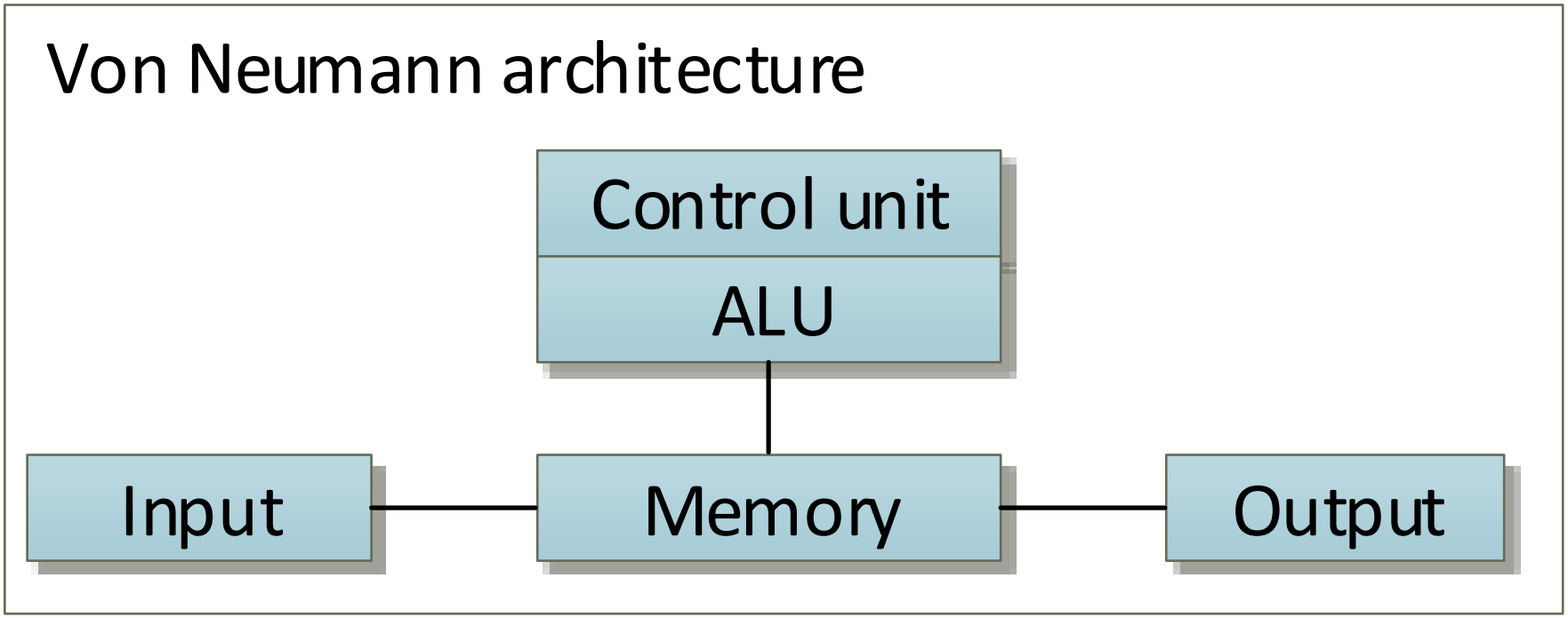
Von Neumann architecture



[schematic, simplified view]

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Von Neumann architecture

Properties:

- **Instructions and data** are located in the **same memory** or address space
- Von Neumann – **bottleneck**:
  Instruction execution time < Memory access time

Is the Von Neumann bottleneck still relevant?

In order to avoid and mitigate such problems, various strategies have been developed (e.g. cache memory)–but its still there!

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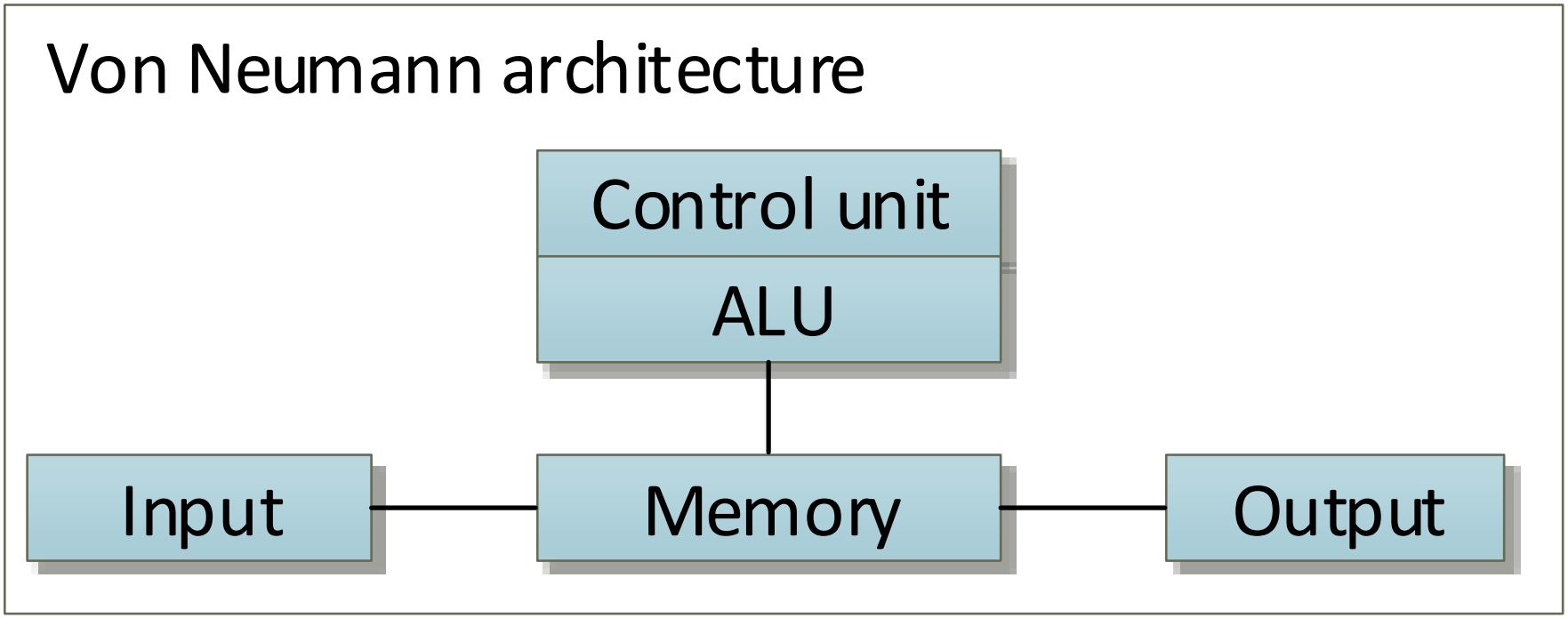
Von Neumann architecture – bottleneck



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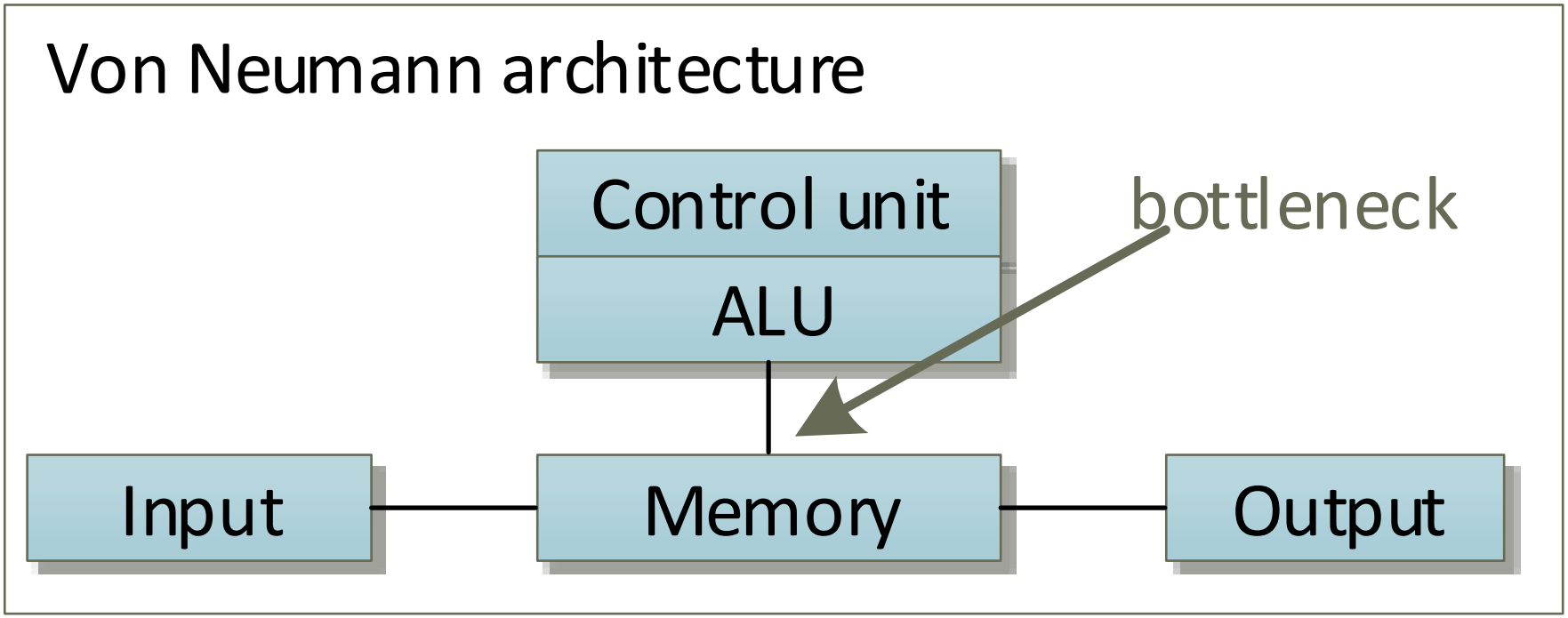

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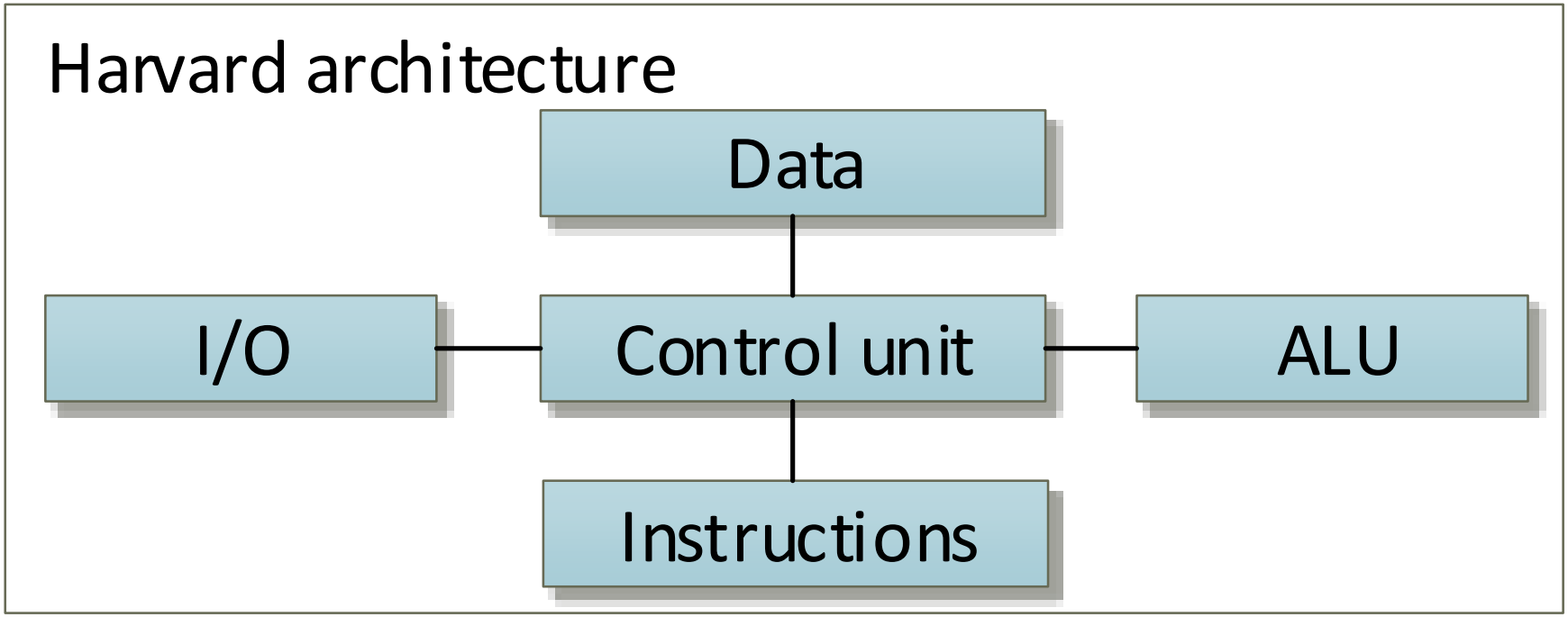
Harvard architecture



[schematic, simplified view]

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Harvard architecture

Properties:

- **Separate memory** for **data** and **instructions**
- **Data** memory is usually **read- and writeable**
- **Instruction** memory is usually **read-only**. Can't be modified through runtime

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Processor architecture

Discussion

Von Neumann vs Harvard architecture: Does it play a role nowadays?

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Control unit

Pseudo C code of control unit inside the CPU:

```
1 while(true){
2     fetch_next_instruction();
3     decode_instruction();
4     execute_instruction();
5     if(interrupt_is_requested()) {
6         save_PC_and_SR();
7         load_new_PC();
8     }
9 }
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Instruction cycle: in principle, it's an **endless loop**

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Interrupts

What is an interrupt?

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Interrupt handling

An **interrupt request (IRQ)** causes the processor to **stop the current workflow** and to **process with a predefined interrupt service routine (ISR)**.

- IRQ -> **Interrupt request**
- ISR -> **Interrupt service routine**
- An ISR is a **function** that is called when an interrupt occurs
- It's just a **memory address** where the function (ISR) starts
- There exist **different types** of interrupts
- The ISR addresses are managed within the CPU with the **interrupt vector table**
- The **interrupt vector table** can be **manipulated** (e.g. in supervisor mode by the OS kernel)

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[for example: ARM Cortex-M Exception handlers]

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Exceptions

Examples for exceptions:

- Division by zero
- Illegal instruction code
- Load or store to an unaligned address
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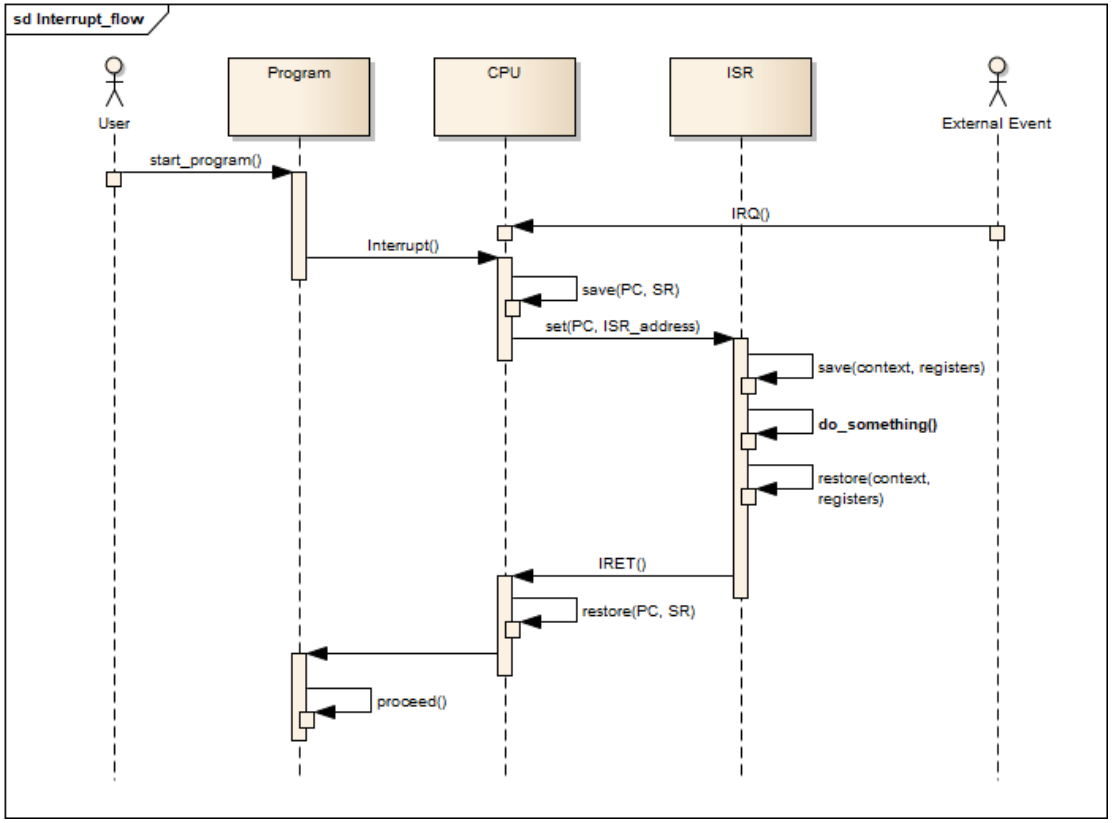
Interrupt flow



Sequence in the control unit

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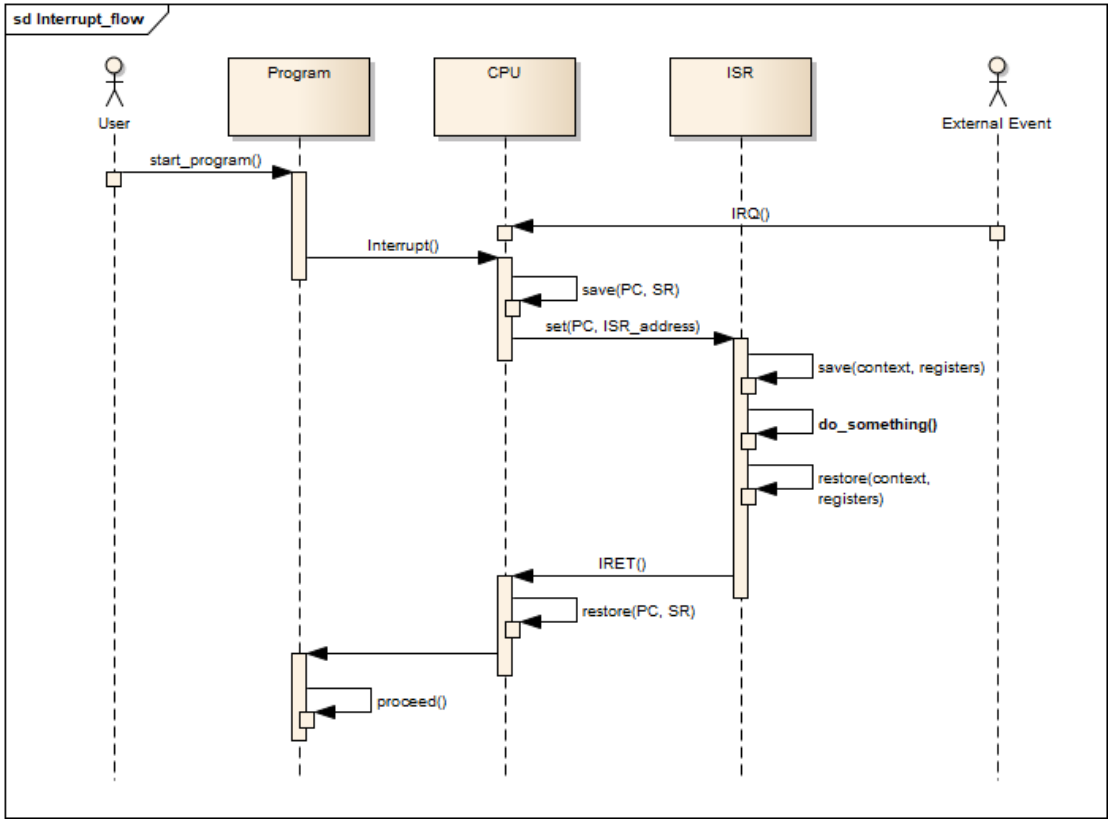
Interrupt flow



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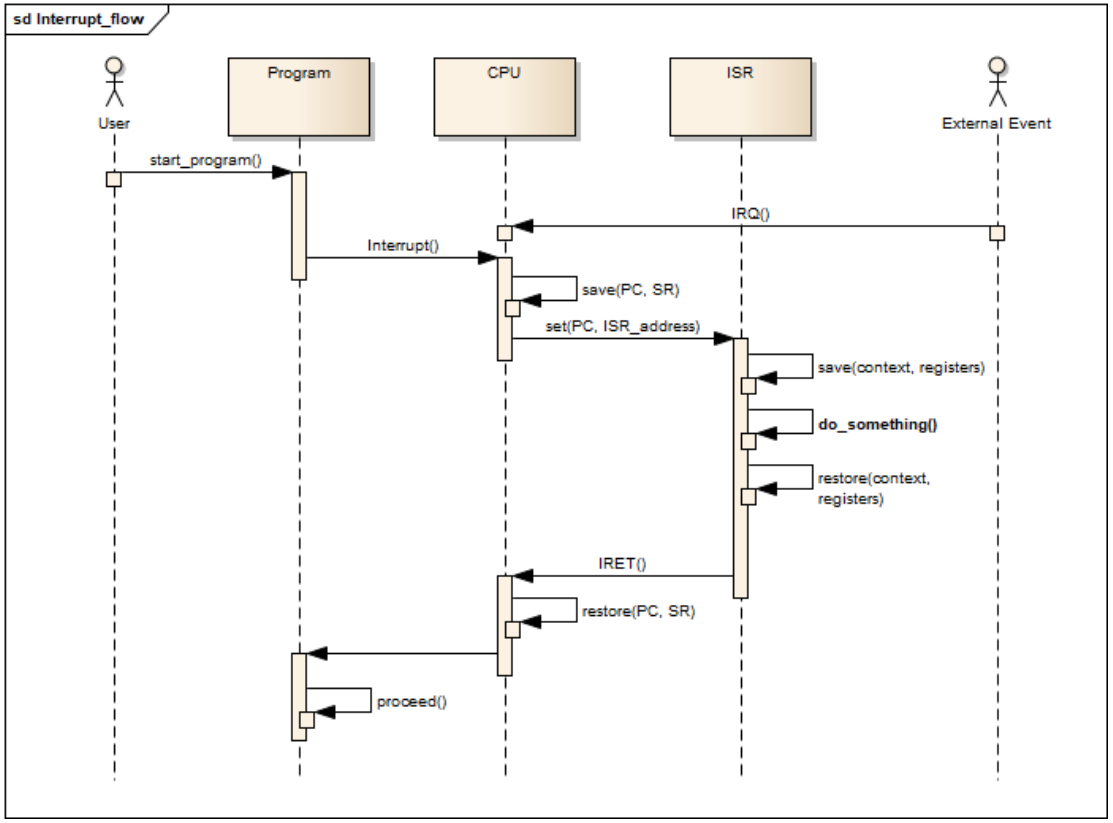

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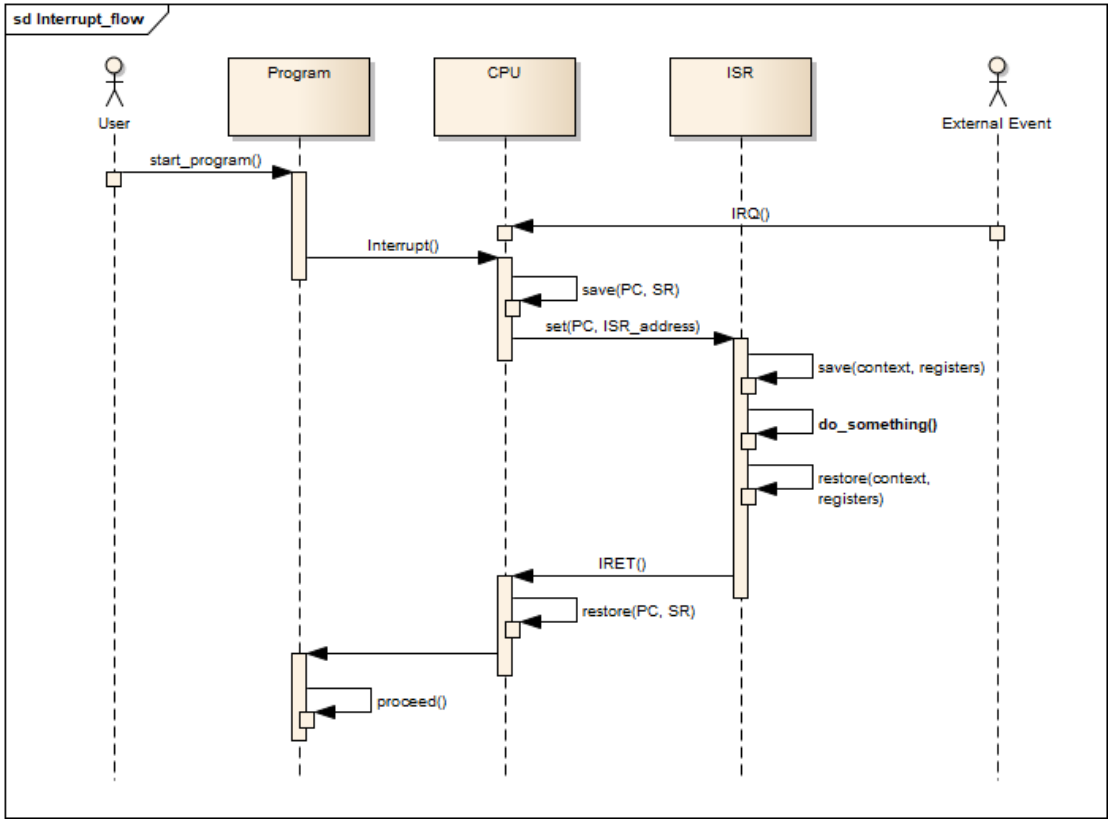

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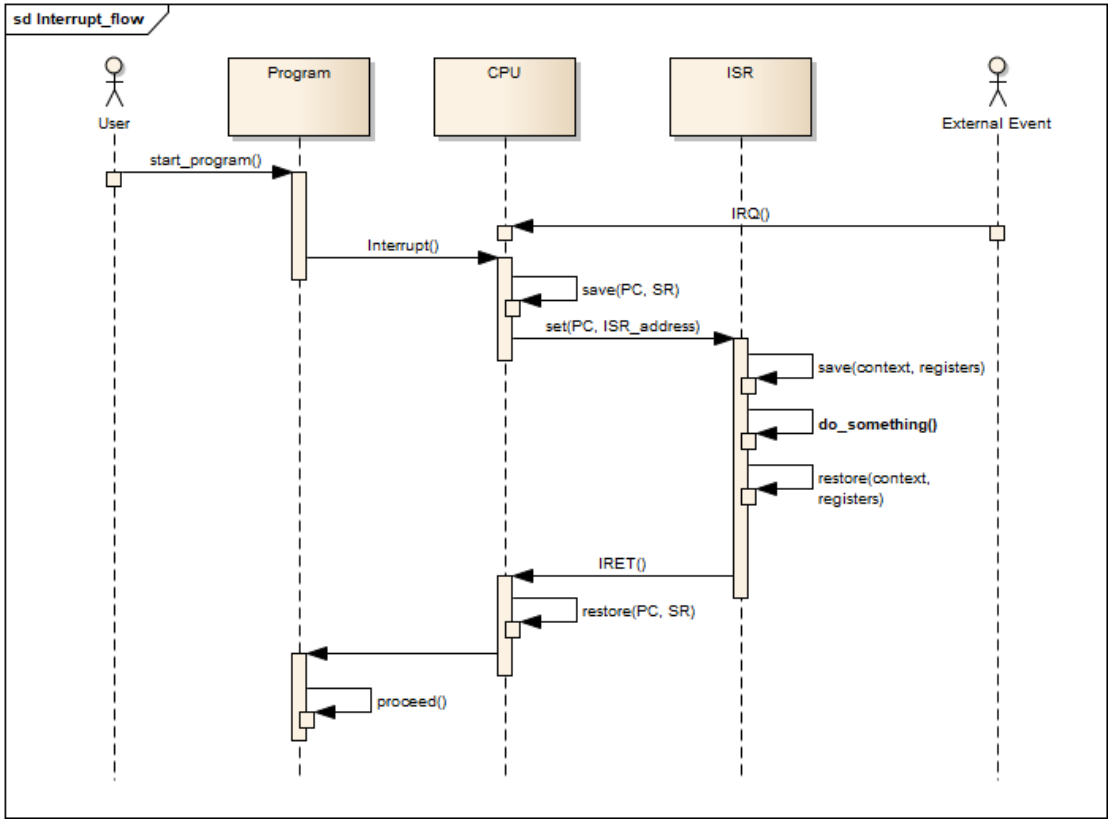

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2. Assign new values to

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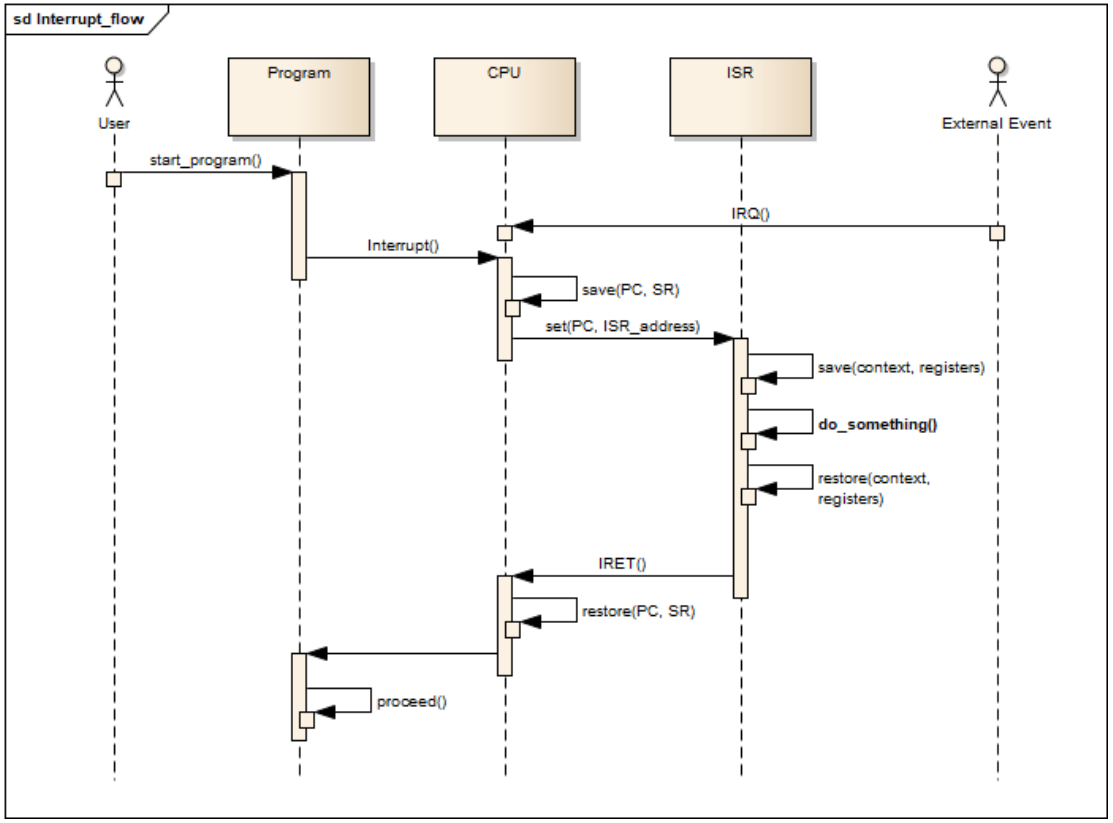

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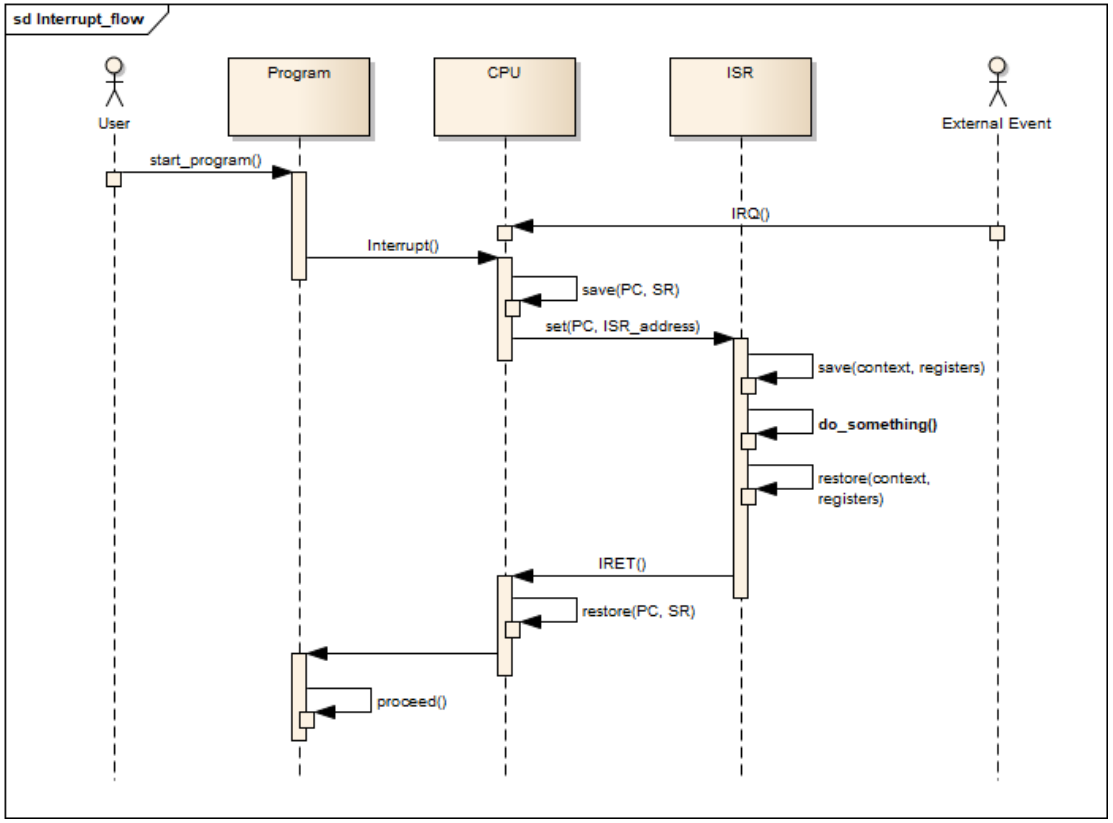

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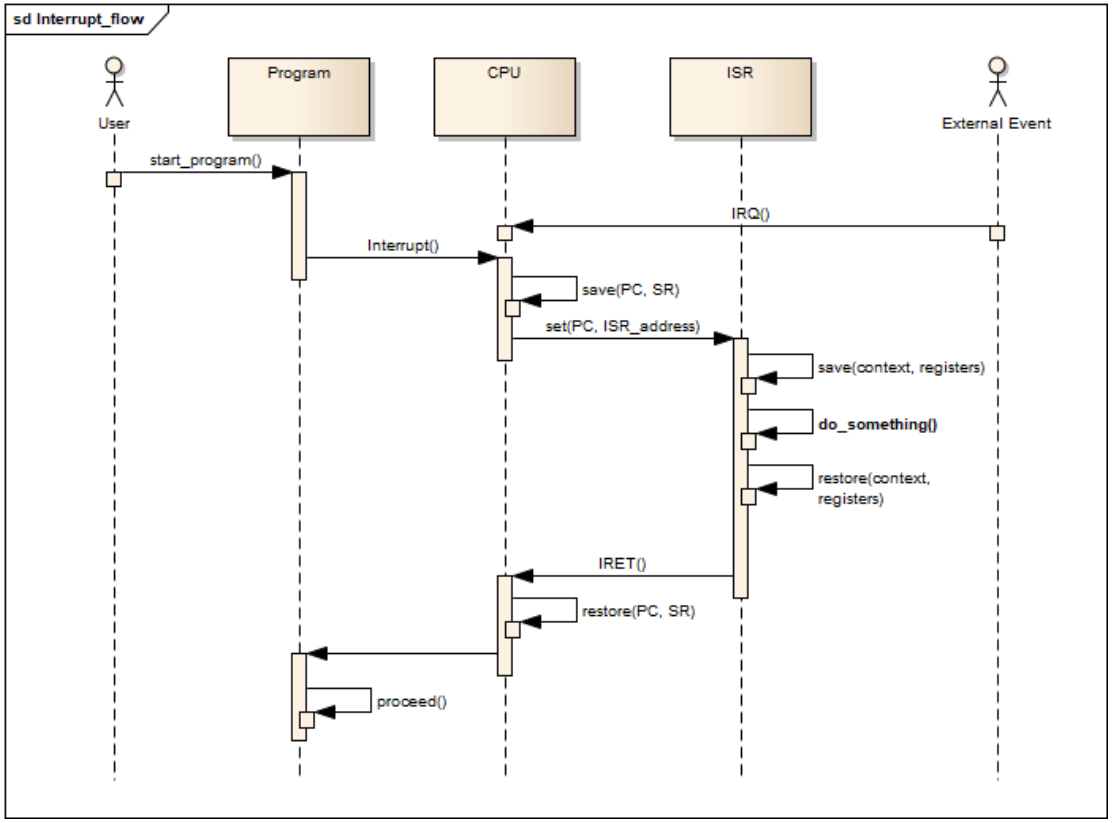

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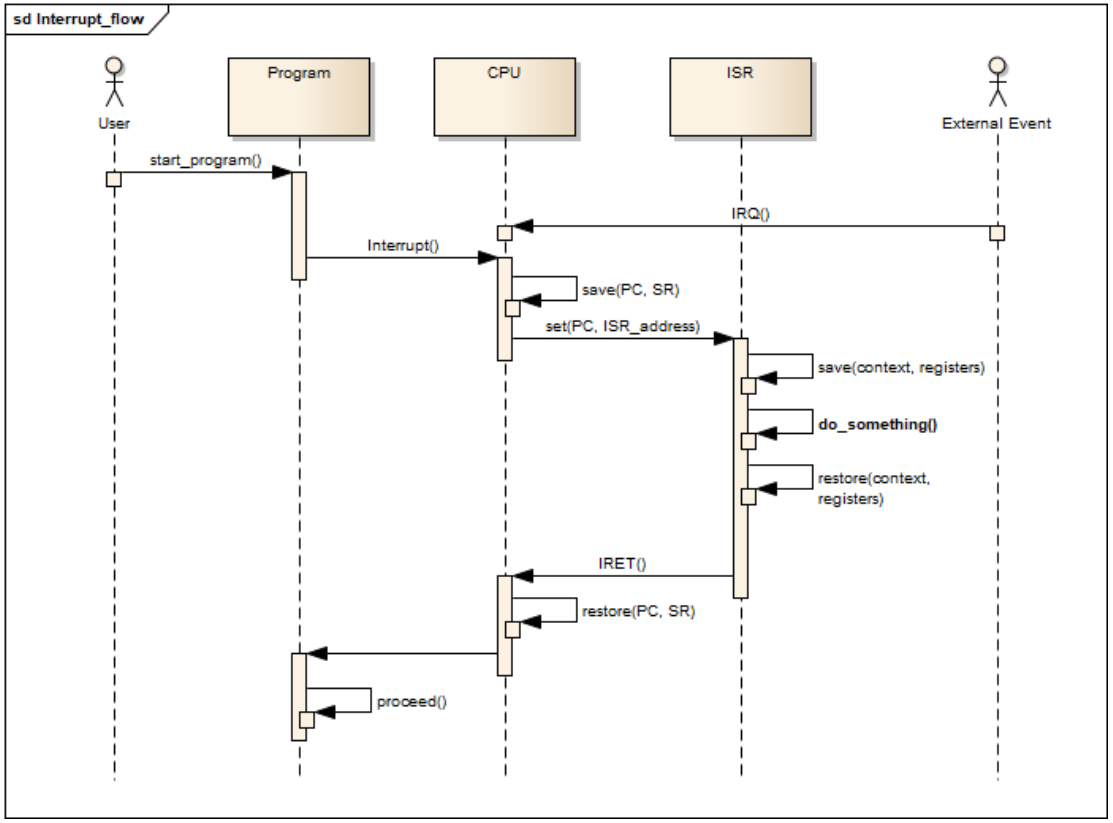

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Interrupt vector table

Exception number	IRQ number	Vector	Offset
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18	2	IRQ2	0x48
17	1	IRQ1	0x44
16	0	IRQ0	0x40
15	-1	SysTick, if implemented	0x3C
14	-2	PendSV	0x38
13		Reserved	
12			
11	-5	SVCall	0x2C
10		Reserved	
9			
8			
7			
6			
5			
4			
3	-13	HardFault	0x10
2	-14	NMI	0x0C
1		Reset	0x08
		Initial SP value	0x04
			0x00

- Example: **Cortex M0**
- Interrupt request (IRQ)
- For each IRQ one entry
- Each entry contains the address of an ISR

[source: Cortex-M0 Generic User Guide (2009), p. 2-22]

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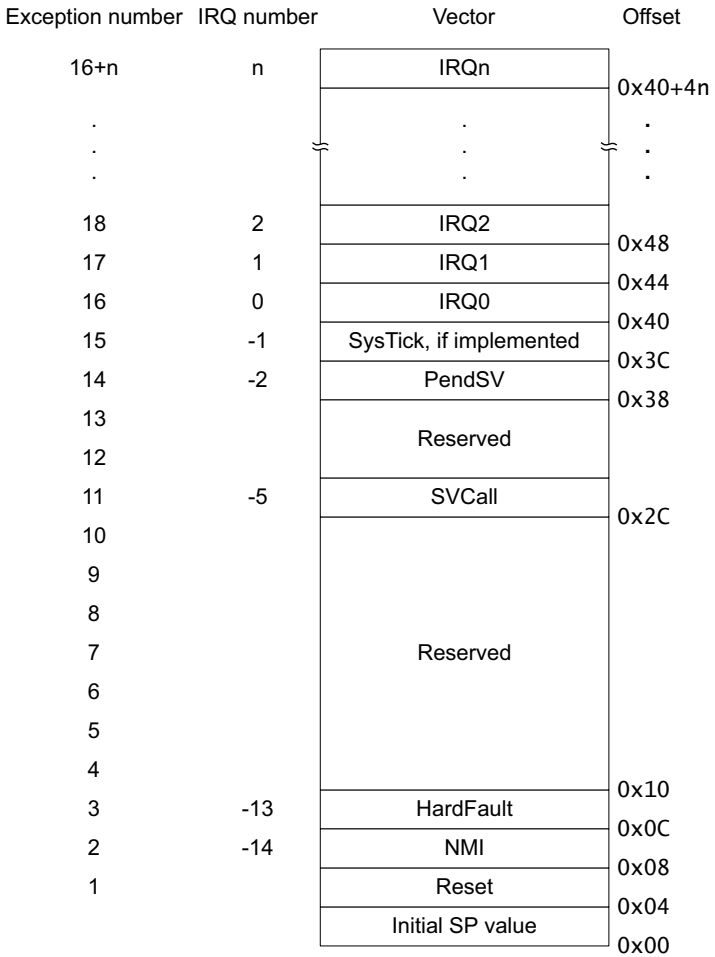

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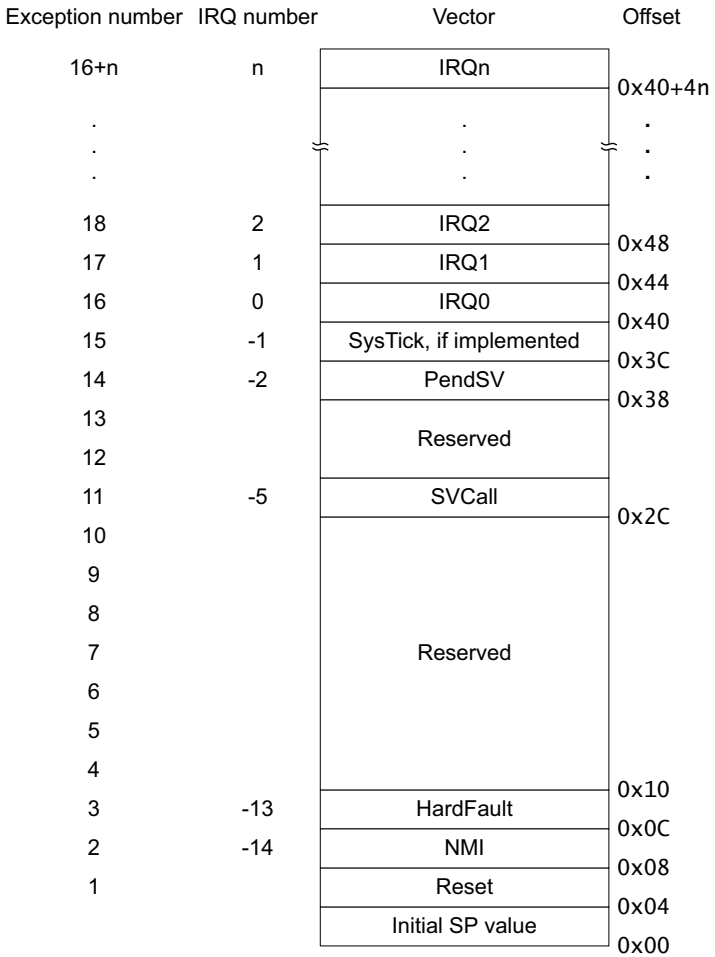
Interrupt vector table



- Example: **Cortex M0**
- Interrupt request (IRQ)
- For each IRQ one entry
- Each entry contains the address of an ISR

[source: Cortex-M0 Generic User Guide (2009), p. 2-22]

Interrupt details

Who saves the registers?

- The CPU saves and restores PC and SR
- The ISR has to save the other registers at the beginning
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- Usually, the operating system does this (if you have one) in advance

Interruption in the middle of an instruction?

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ISA - instruction set architecture

Do you know some common ISAs?

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ISA - instruction set architecture

The interface for low-level programming, very close to the hardware.

Degrees of freedom in instruction set architecture (ISA) design

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Register:	How many? Usable in which way?
Addressing:	Addressing types for the operands? Can be combined with the operations arbitrary ("orthogonal") or restricted?

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ISA - instruction set architecture

Instruction formats:

Instruction address Example Operands

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Three-addresses	`ADD X, Y, Z`	`X = Y + Z or ...`

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ISA - special instructions

Synchronisation instructions:

- TAS (test and set) or similar
- Tests a memory cell ($? = 0$) and sets it to one, if the test was successful.
- In the hardware single, atomic (i.e., non-interruptible) operation
- Uses a read-modify-write memory cycle that completes the operation without interruption.

Synchronisation area:

Area	Protection through
Critical area in a process	P and V operation
P-Operation in the operating system	TAS instruction (or similar)

In other architectures, partly different, more efficient, much more complicated solutions. Similar: Compare_and_Swap, keyword "Lock-free Programming".

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ISA - special instructions: TAS

TAS example for Freescale ColdFire architecture

```
1  byte LOCK = 0; // =0 -> lock is free; !=0 -> locked
2  //...
3  __asm { ;Inline assembly block with assembler instructions
4    GetLock:
5      TAS.B LOCK    ;Sets the N- or Z-Bit depending on LOCK and
6                    ;always sets LOCK = 0x80
7      BNE GetLock   ;If LOCK was != 0 then try it again (loop)
8                    ;(BNE, branch not equal)
9  }
10 // Now, we have the LOCK and we are inside the critical section
11 // ...
12 __asm { ;Inline assembly block with assembler instructions
13   ReleaseLock:
14     CLR.B LOCK     // Sets LOCK = 0
15 }
```

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ISA - CISC vs RISC

CISC - complex instruction set computer

- Instructions should be as close as possible to the high-level languages
- Can take a lot of internal CPU cycles for an instruction
- Support for a lot of addressing modes
- Allows compact encoding of programs (one instruction does a lot)

RISC - reduced instruction set computer

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ISA - CISC vs RISC

Discussion

CISC vs RISC: Does it play a role nowadays?

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Summary and outlook

Summary

- Processor architecture
- Exception and interrupt handling
- Instruction set architecture

Outlook

- Endianness

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