Start: 8:01

Technische Hochschule Rosenheim
Technical University of Applied Sciences

Prof. Dr. Florian Künzner

Technical University of Applied Sciences Rosenheim, Computer Science

CA 8 – Memory 1

The lecture is based on the work and the documents of Prof. Dr. Theodor Tempelmeier

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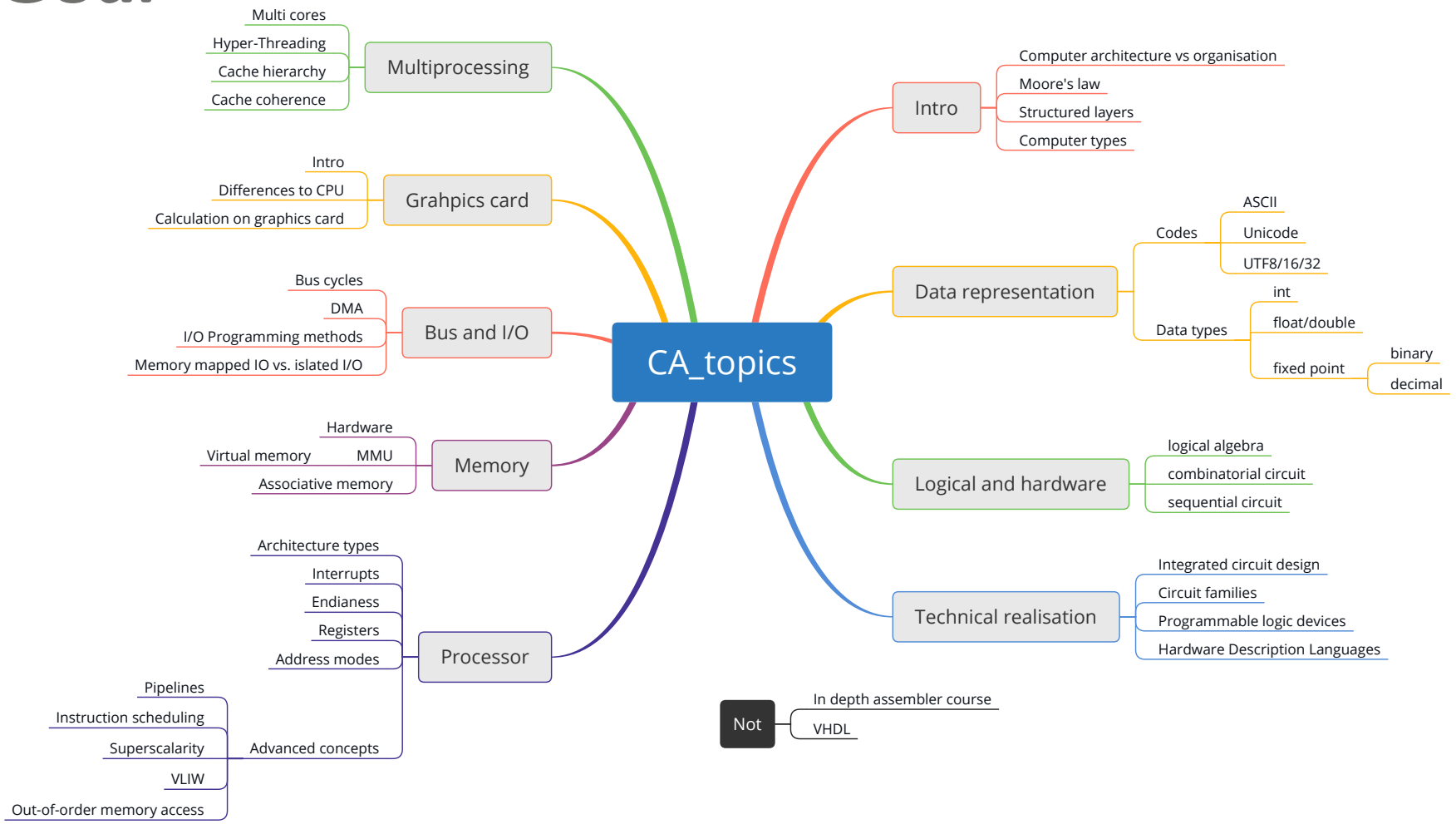
Goal



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Goal

CA::Memory 1 - Hardware

- Memory types
- Memory chips
- Memory modules
- Modern memory modules

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Memory types

RAM vs ROM

RAM - Random access memory

- For **read and write** access
- Usage: **programs and data**
- It is (usually) a **volatile** memory (data are lost when power is switched off)
- **Very fast** access time
- **High power** consumption
- **Expensive**

ROM - Read only memory

- For **read only** memory access
- Usage: **firmware** (BIOS, UEFI)
- It is a **non-volatile** memory (remembers the data even if power is switched off)
- Usually **slower than RAM**
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- Example: EPROM, EEPROM

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Memory types

It's all about RAM!

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Memory types

SRAM vs DRAM

Property	SRAM - Static RAM	DRAM - Dynamic RAM

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Memory types

SRAM vs DRAM

Property	SRAM - Static RAM	DRAM - Dynamic RAM
Construction	– Complex	+ Simple

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Density	– Less dense	+ Highly dense

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Charge leakage	+ Not present	– Present: refresh required

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Density	– Less dense	+ Highly dense
Charge leakage	+ Not present	– Present: refresh required
Power consumption	+ Low	– High

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Orders of magnitudes for bits and bytes

Bits:

Bits (decimal)			
Symbol	**Power**	**Num bits**	**Name**
1 kbit	10^3	1.000	kilobit
1 Mbit	10^6	1.000.000	megabit
1 Gbit	10^9	1.000.000.000	gigabit
1 Tbit	10^{12}	1.000.000.000.000	terabit
...			

Bits (**binary**)			
Symbol	**Power**	**Num bits**	**Name**
1 Kibit	2^{10}	1.024	kibibit
1 Mibit	2^{20}	1.048.576	mebibit
1 Gibit	2^{30}	1.073.741.824	gibibit
1 Tibit	2^{40}	1.099.511.627.776	tebibit
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Memory modules and chips - overview

[source: wikipedia.org]

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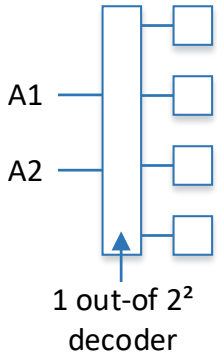
Memory chips

Arrangement of memory cells: (within a memory chip)

Linear Arrangement:



- To address 1-out-of-2^n memory cells, n address lanes are required.
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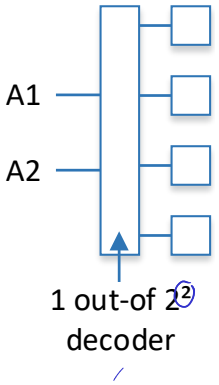

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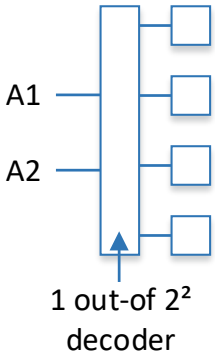

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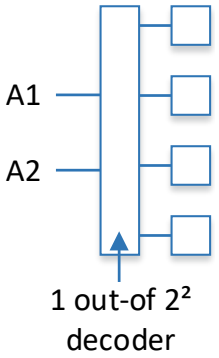

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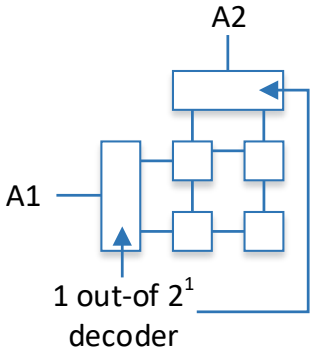

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- The address is usually transferred in two steps:
  - 1: Row address
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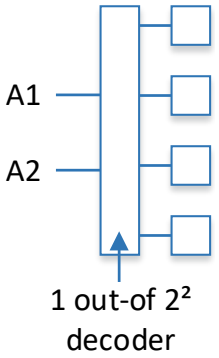

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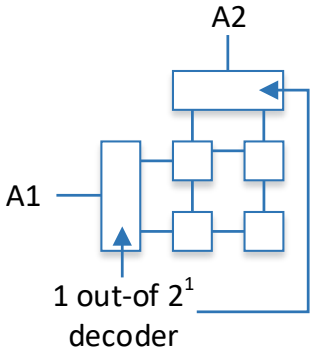

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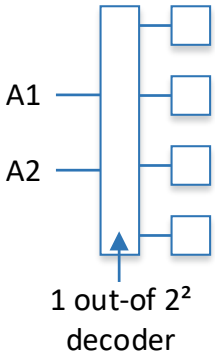

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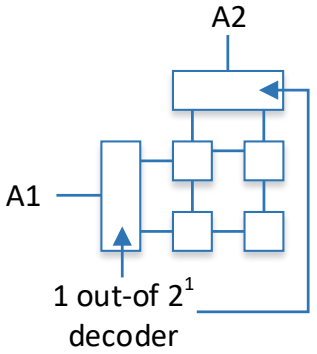

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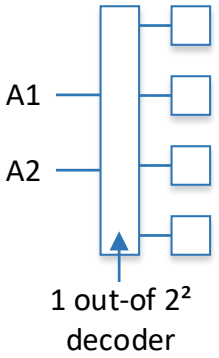

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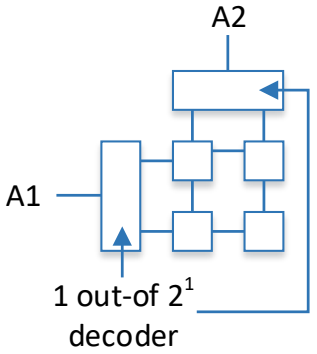

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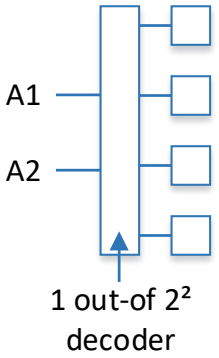

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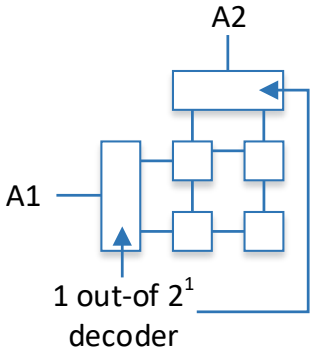

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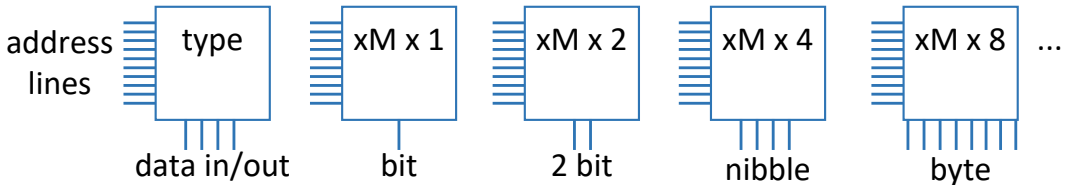

Terminology:

Description	Type	Unit

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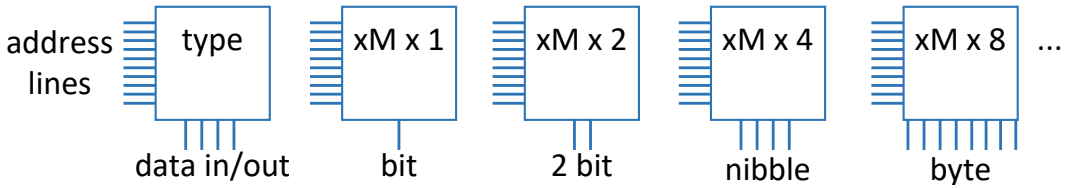

Terminology:

Description	Type	Unit
Chip with x mega that provides 1 bit per address	xM x 1	bit

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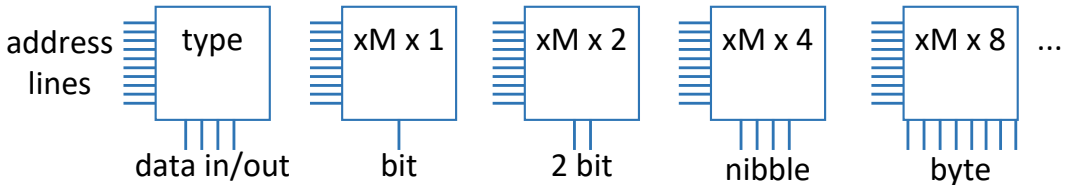

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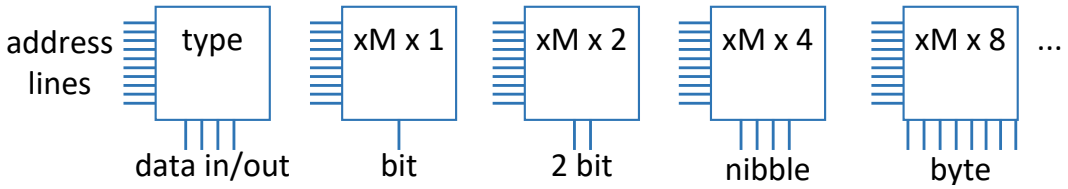

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Chip with x mega that provides 4 bit per address	xM x 4	nibble

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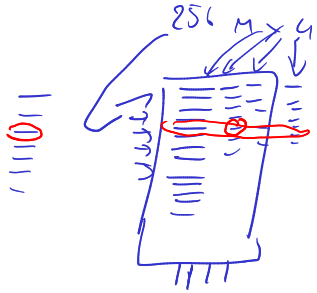

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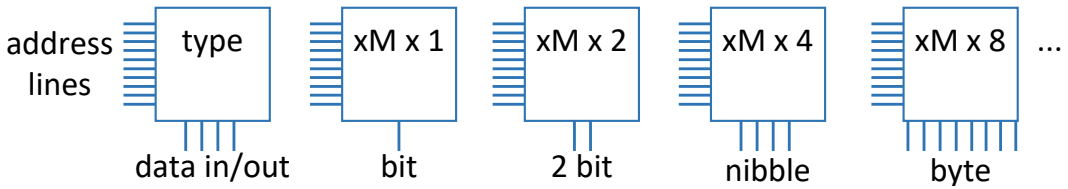
Memory chips

Chip types:



Terminology:

Description	Type	Unit
Chip with x mega that provides 1 bit per address	xM x 1	bit
Chip with x mega that provides 2 bit per address	xM x 2	2 bit
Chip with x mega that provides 4 bit per address	xM x 4	nibble
Chip with x mega that provides 8 bit per address	xM x 8	byte

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Memory chips

Chip capacity:

On these chips: K means Ki, M means Mi, G means Gi, ...
xK/xM/xG denotes the number of chip cell rows inside the chip

Chip capacity = xM x number of bits per chip

Examples:

- 16M x 1: 16Mi x 1 = 16 Mibit => 16Mi/8 = 2 MiB
- 16M x 2: 16Mi x 2 = 32 Mibit => 32Mi/8 = 4 MiB
- 1G x 4: 1Gi x 4 = 4 Gibit => 4Gi/8 = 512 MiB
- 1G x 8: 1Gi x 8 = 8 Gibit => 8Gi/8 = 1 GiB

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Memory modules

The memory chips on a memory module are usually arranged in a matrix layout.

[image source: samsung.com]

Memory address is divided into:

- Chip select address
- Chip address (inside the chip)

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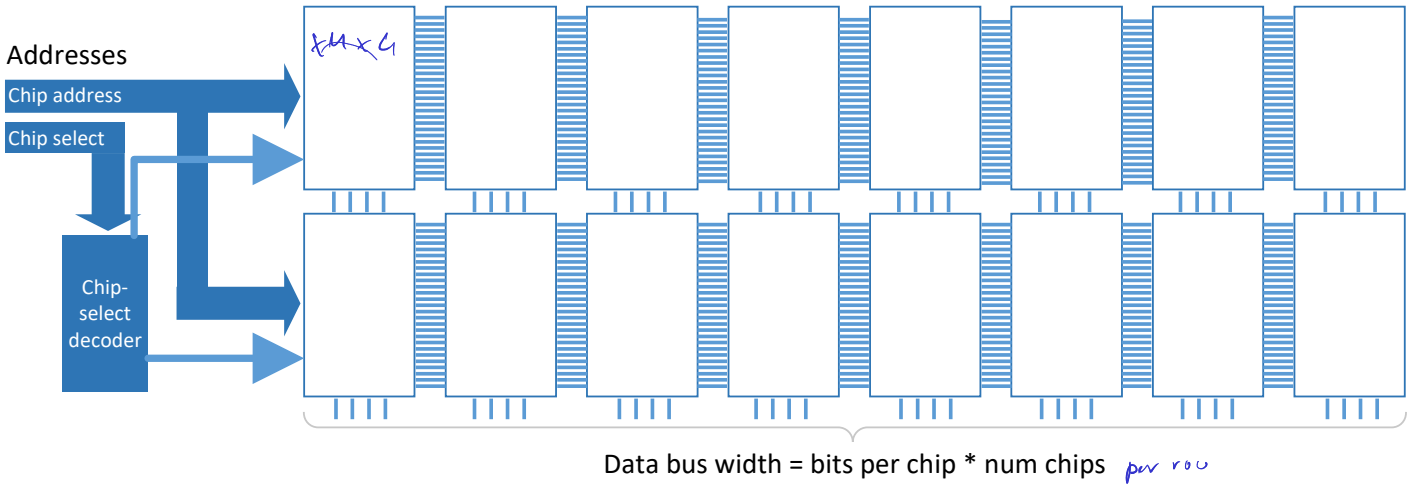
Memory modules - hardware layout

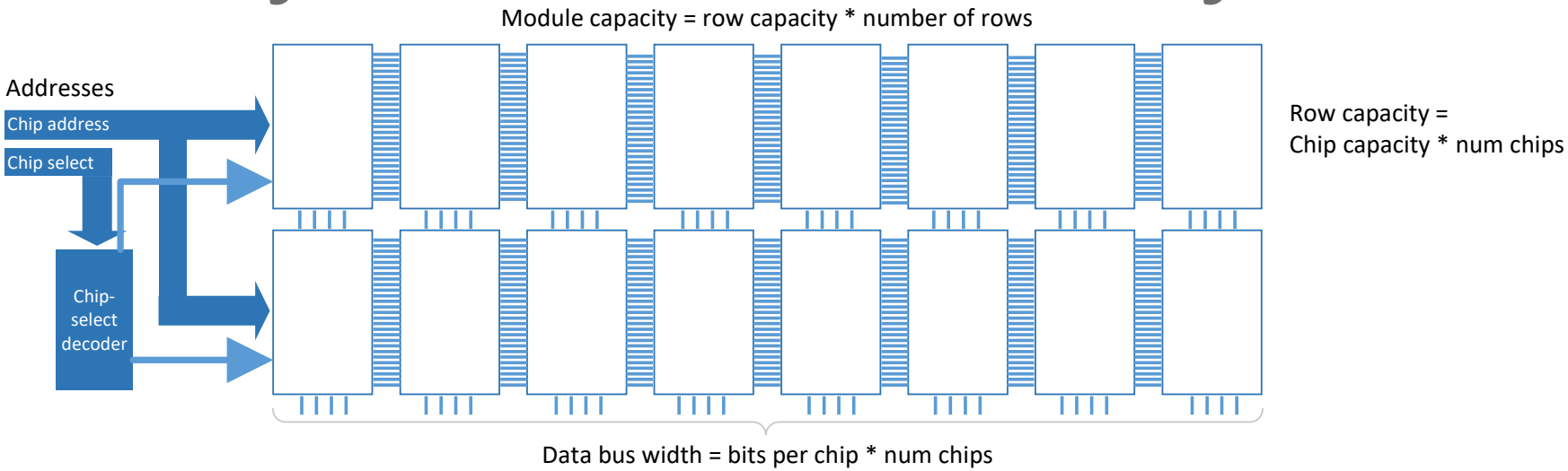
Module capacity = row capacity * number of rows



Address calculations:

Nr.	Descriptions	Calc	Results

Memory modules - hardware layout



Address calculations:

Nr.	Descriptions	Calc	Results
(1)	Number of bits to address the module capacatiy	$log_2(module\ capacity)$	number of bits

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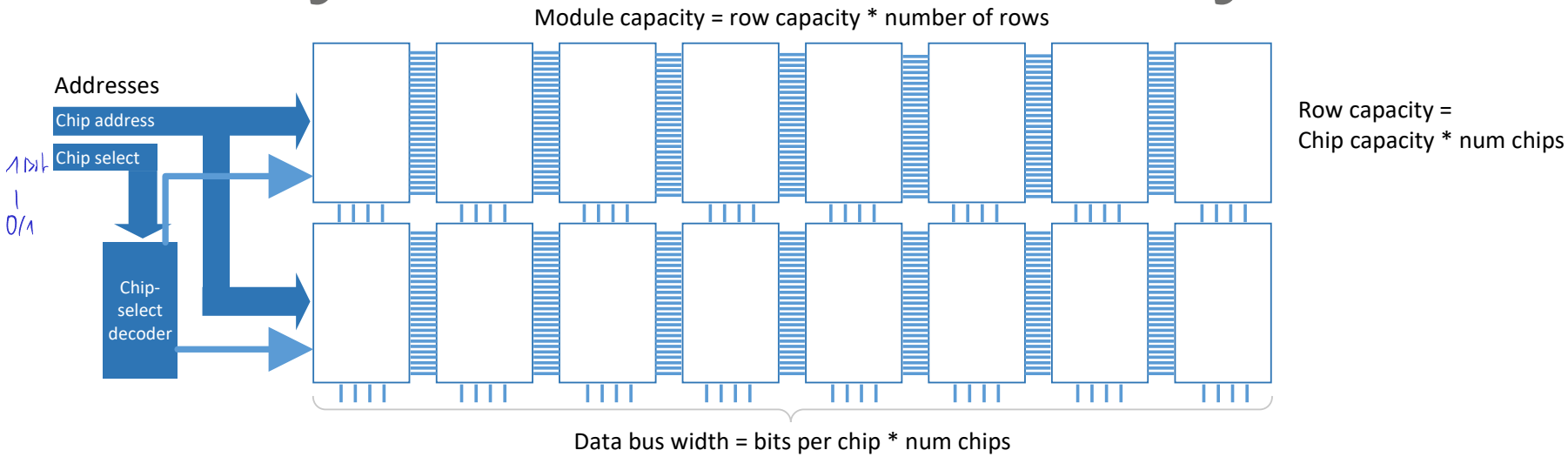
Memory modules - hardware layout



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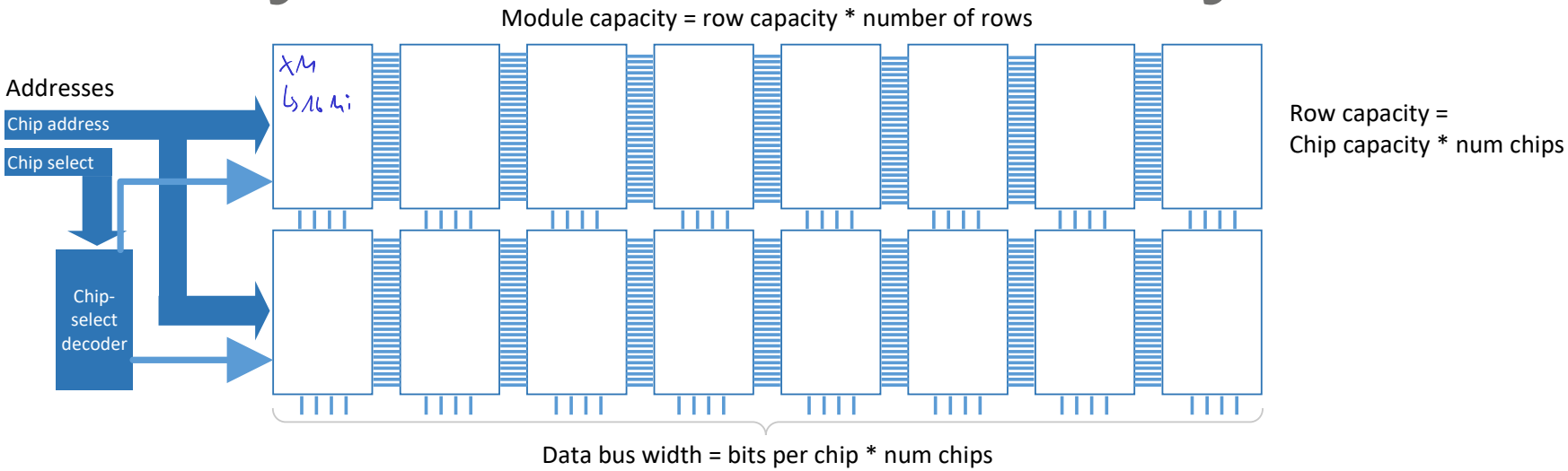

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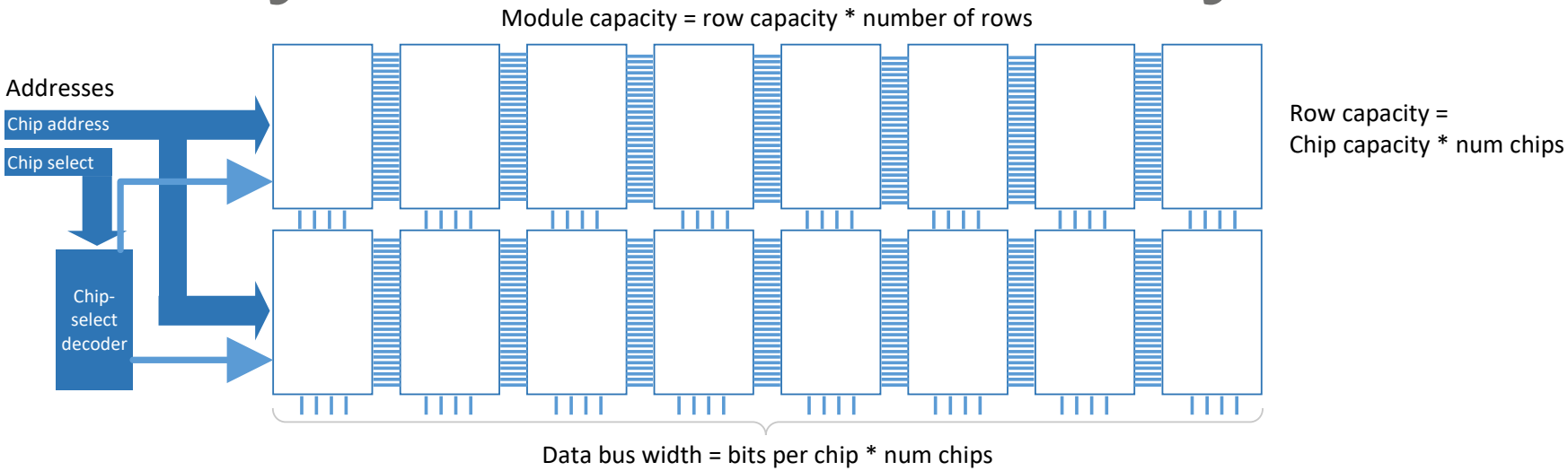
Memory modules - hardware layout



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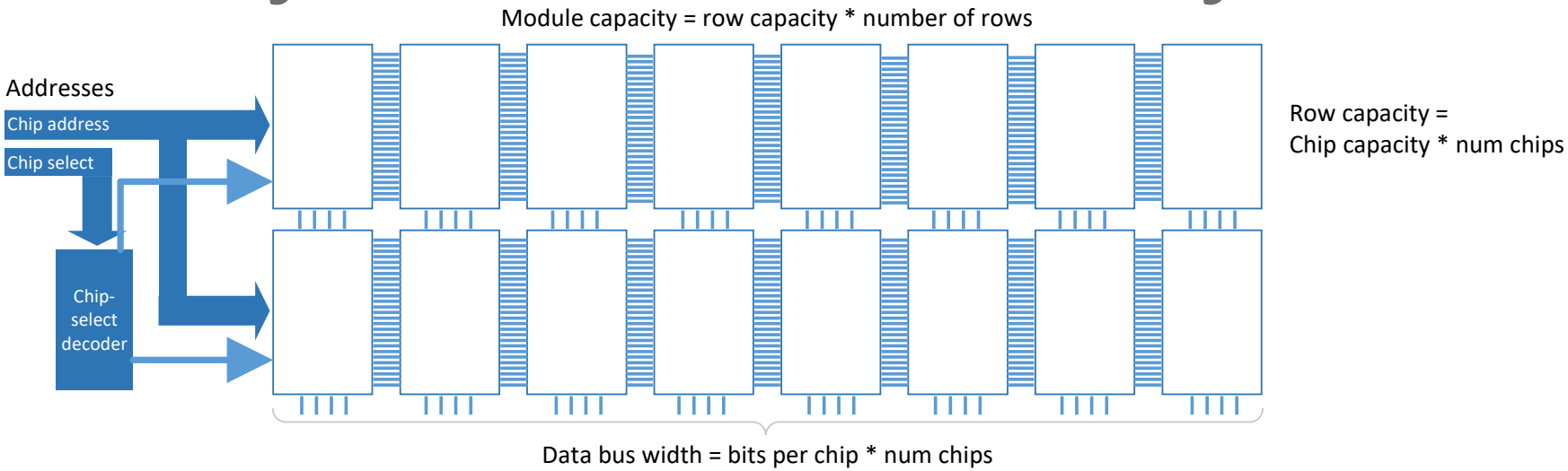

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Address calculation relationship:

Number of bits to address the module capacatiy: $(1) = \sum_{i=2}^{4}(i) = (2) + (3) + (4)$

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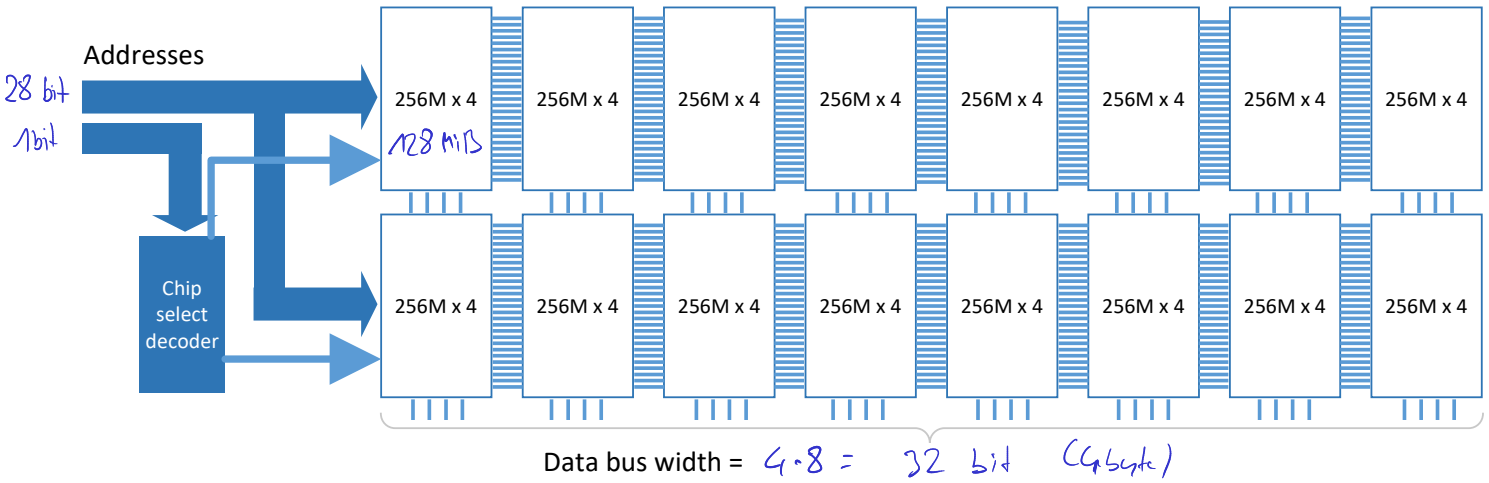
Memory modules - example

Example:

- Design a memory module with: 2 GiB capacity and a 32 bit data bus
- Use chips of type 256M x 4

Module capacity = 1 GiB · 2 = 2 GiB



Address calculations:

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(1)	Number of bits to address the module capacatiy	$\log_2(2\,\text{Gib} = 2^{31})$	31 bit
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(3)	Number of address lanes/bits for chip address	$\log_2(256\,\text{Mi} = 2^{28})$	28 bit
(4)	Number of bits to address the bytes inside the word	$\log_2(4 = 2^{2})$	2 bit

} 31 bit

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Memory modules - example (solution)

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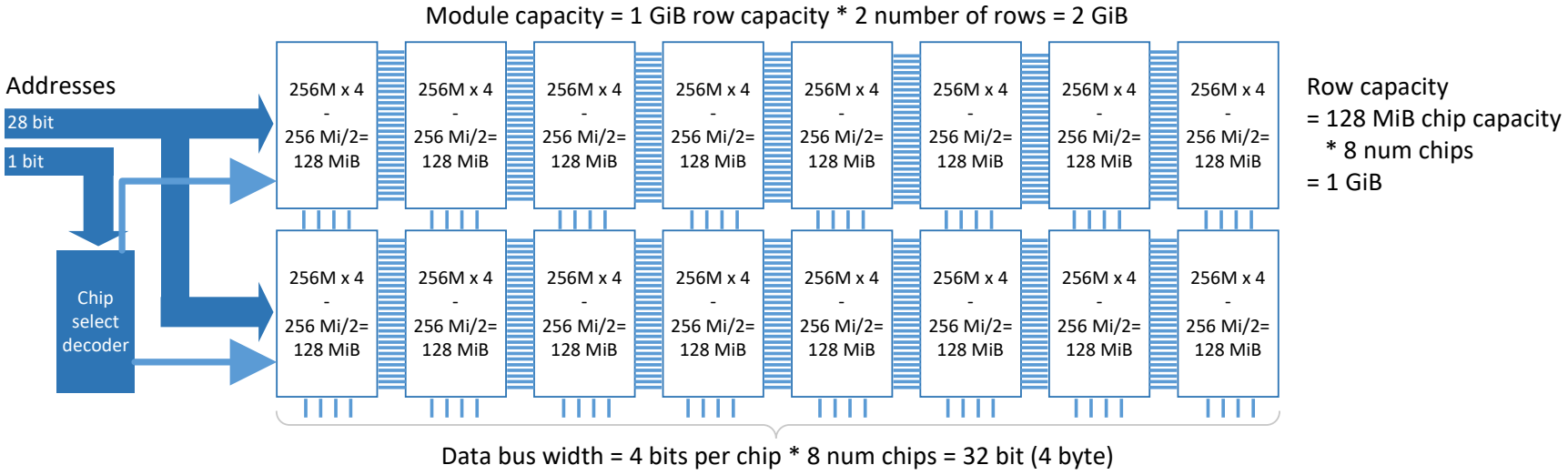

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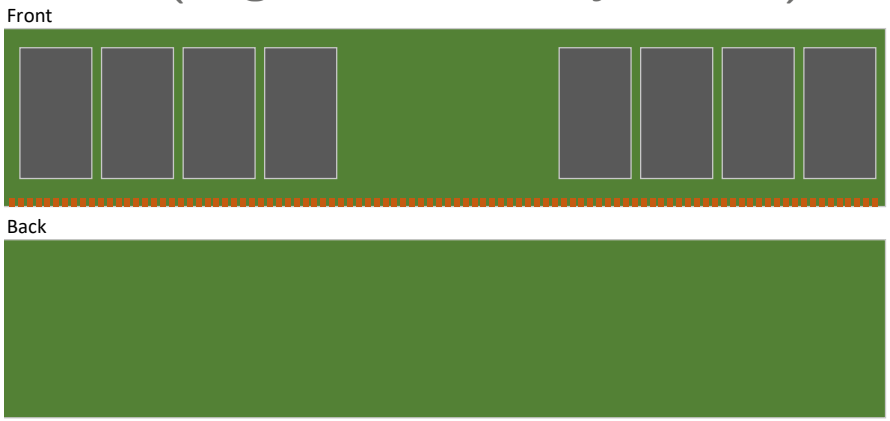
Memory modules - formats

SIMM (single inline memory module):



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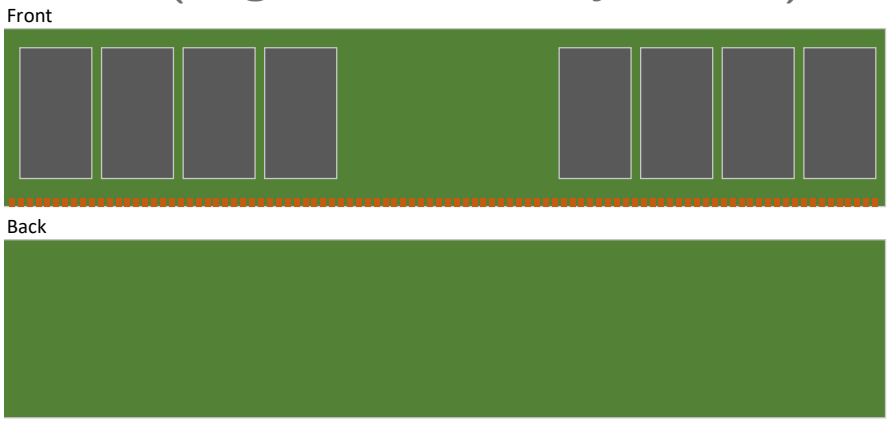
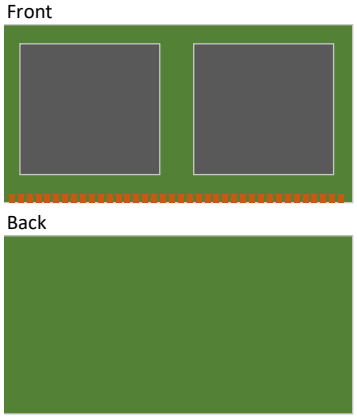


SO-SIMM (small outline SIMM):



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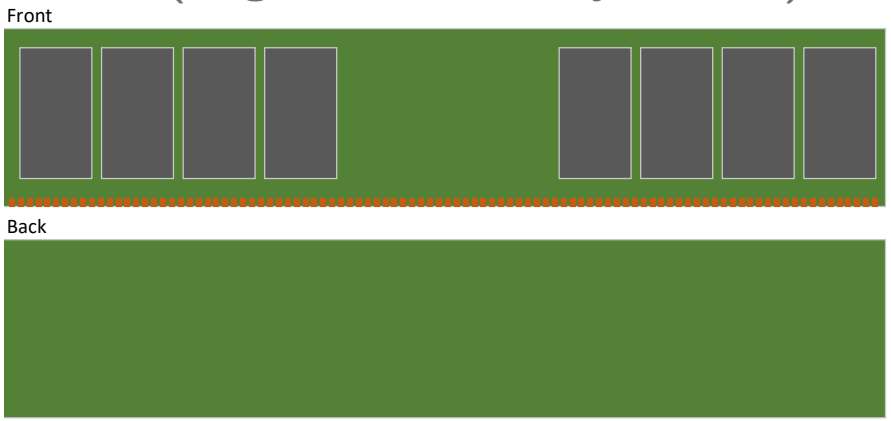

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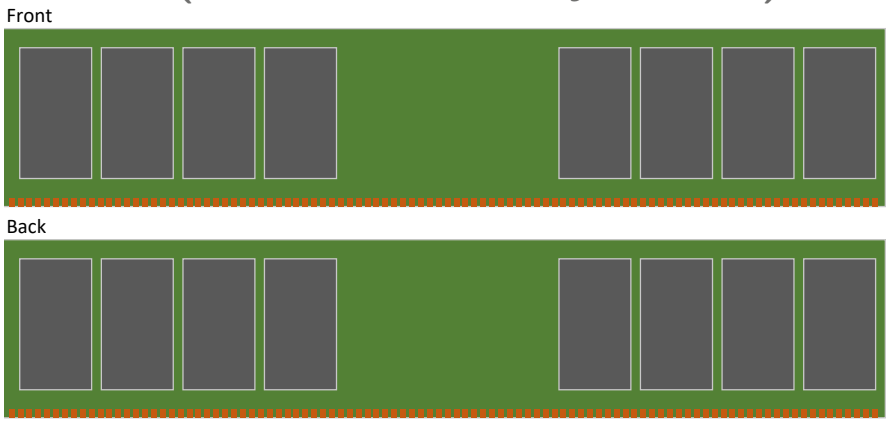

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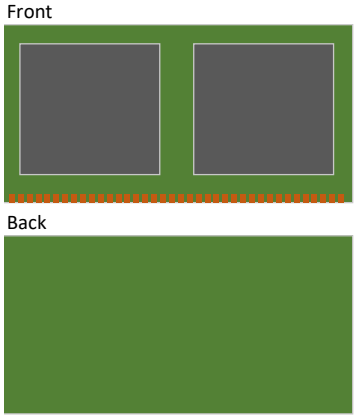

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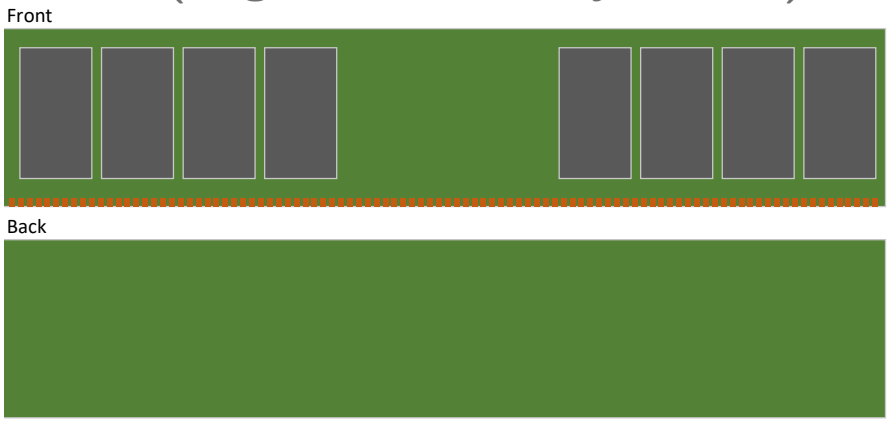

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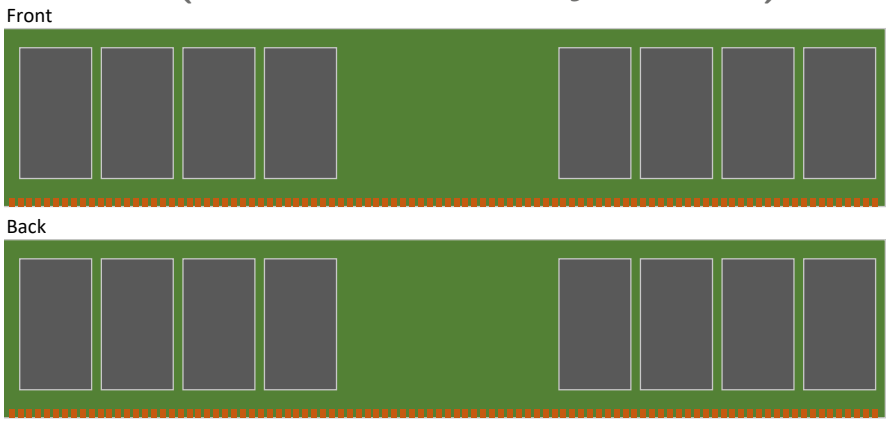

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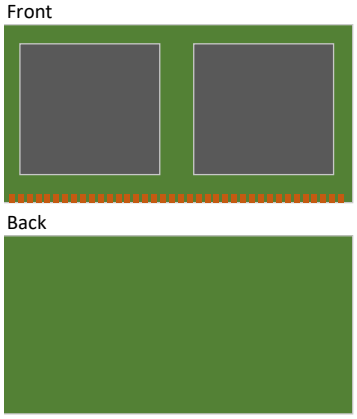

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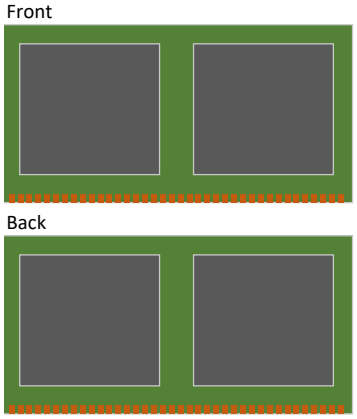

Memory modules - interleaving

Problem:

After a **memory cell** is read in a DRAM, the cell **needs to be refreshed** and this takes some time.

Idea:

Distribute consecutive addresses evenly across the chip rows.

- Reduces the problem of waiting until the refresh is complete
- Accelerates memory access in an effect similar to pipelining
- But due to the increased capacities of the individual chips, a memory module has only one or two chip rows. -> Solution: SDRAM

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Modern memory modules

Overview of various terms in the memory area

SDRAM

SDRAM: synchronous DRAM

- **Synchronous** means there as a **clock** pulse
- **Dynamic** means there is a **refresh necessary**
- **Memory is divided** into several equally sized and independent **banks**: allows **interleaving** within chips
- Chips can accept new commands before finishing the previous one (for another bank).

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ECC: error checking and correction

- ECC memory can **detect and correct** the most common kinds of internal **data corruption**
- Allows the **detection** and **correction** of **single bit errors**
- Some do also **detect double bit errors**
- Application area: Scientific and financial computing applications which operate on sensitive data

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DDR-SDRAM

DDR-SDRAM: double data rate SDRAM

Idea:

- Transfers data at almost double the transfer rate
- **Data is transferred on rising and falling edges.**
- DDR4-RAM is state of the art for computers
- DDR5-RAM is approaching into the market in 2020/2021

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	DDR3	DDR4	DDR5
Data transfer rate	17 GiB/s	25,6 GiB/s	51,2 GiB/s
Max module capacity	16 GiB	64 GiB	128 GiB

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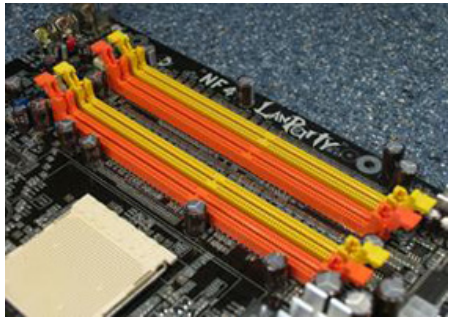
Multi-channel memory architecture



[source: wikipedia.com]

Idea:

- Adds **multiple channels** from the memory to the controller
- **Increase data transfer rate** of DRAM memory modules with the memory controller
- Dual/Triple/Quad-channels are possible
- **Dual-channel**: **theoretically doubles** the data transfer rate
- New Intel processors (like Intel Core i7-9800X) supports quad-channel memory architecture

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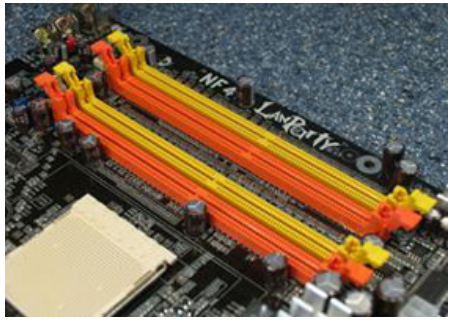
Multi-channel memory architecture



[source: wikipedia.com]

Idea:

- Adds **multiple channels** from the memory to the controller
- **Increase data transfer rate** of DRAM memory modules with the memory controller
- Dual/Triple/Quad-channels are possible
- **Dual-channel**: **theoretically doubles** the data transfer rate
- New Intel processors (like Intel Core i7-9800X) supports quad-channel memory architecture

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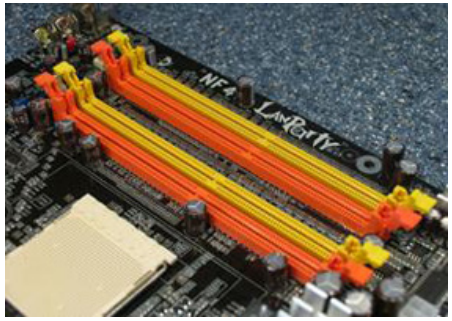

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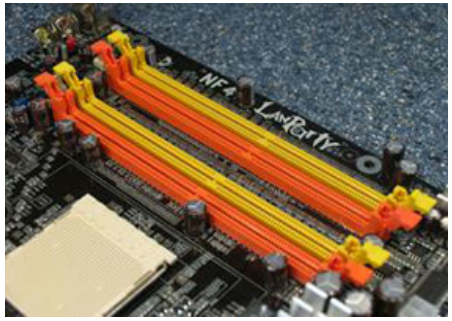

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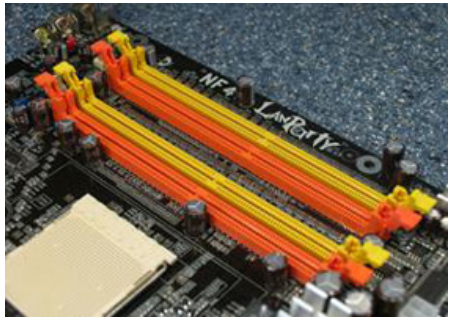

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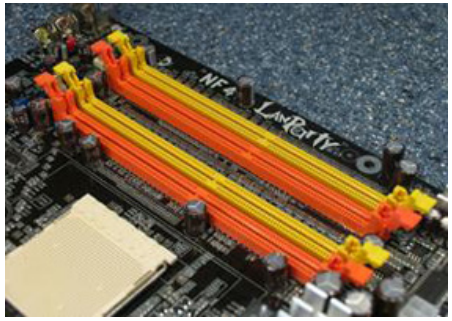

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Questions?

All right? ⇒ 

Question? ⇒  and use **chat**

or

speak *after* I ask you to

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Summary and outlook

Summary

- Memory types
- Memory chips
- Memory modules
- Modern memory modules

Outlook

- MMU
- Virtual memory

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