Technische Hochschule Rosenheim
Technical University of Applied Sciences

Prof. Dr. Florian Künzner
Technical University of Applied Sciences Rosenheim, Computer Science

Start: 8:01

CA 3 – Logical hardware

The lecture is based on the work and the documents of Prof. Dr. Theodor Tempelmeier

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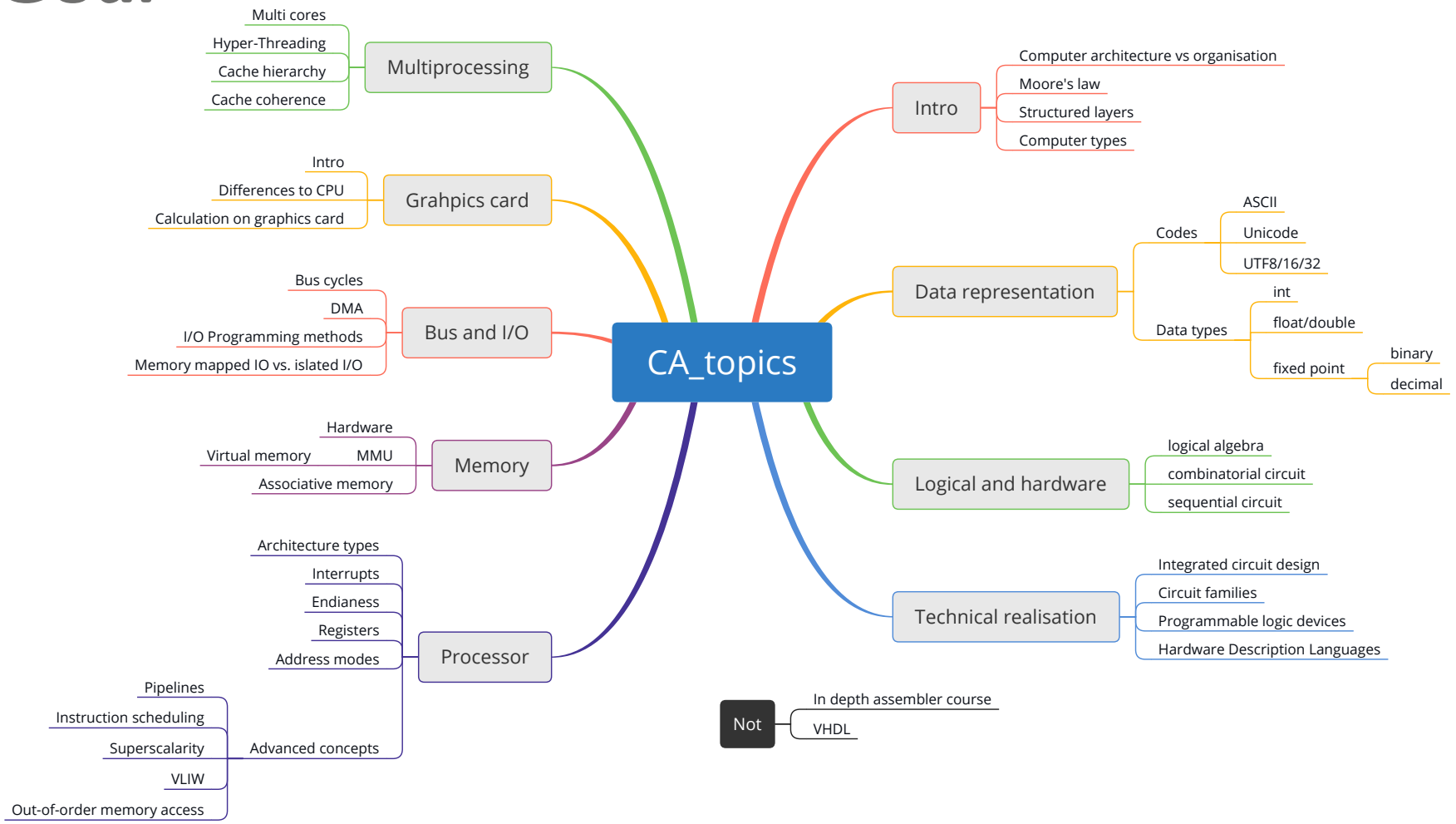
Goal



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Goal

CA::Logical hardware

- Logical algebra
- Logical elements
- Combinatorial circuits
- Sequential circuits

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Logical algebra

Notation:

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Logical algebra

Notation:

Operators $\vee, +, OR$ $\wedge, \cdot, AND$ $\neg, \bar{x}, NOT$

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Logical algebra

Notation:

Operators	$\vee, +, OR$	$\wedge, \cdot, AND$	$\neg, \bar{x}, NOT$
Operand	$\{0, 1\}$		

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Axiom	$a+b=b+a$	$a \cdot b = b \cdot a$	
	$(a+b)+c=a+(b+c)$	$(a \cdot b) \cdot c = a \cdot (b \cdot c)$	
	$a+(a \cdot b)=a$	$a \cdot (a+b) = a$	
	$a+0=a$	$a \cdot 1 = a$	
	$a \cdot (b+c) = (a \cdot b)+(a \cdot c)$	$a+(b \cdot c) = (a+b) \cdot (a+c)$	
	$a \cdot \neg a = 0$	$a + \neg a = 1$	

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De Morgan	$\neg(a \cdot b) = \neg a + \neg b$	$\neg(a+b) = \neg a \cdot \neg b$

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Logical elements

Type	New DIN norm	American norm

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Logical elements

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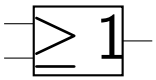
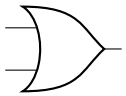
OR		

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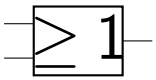
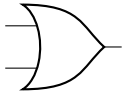
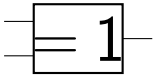
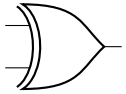
OR		
XOR		

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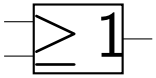
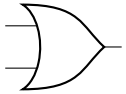
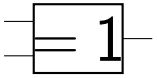
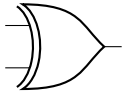
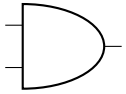
OR		
XOR		
AND		

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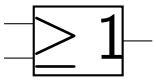
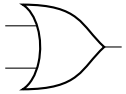
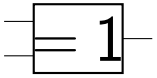
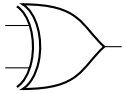
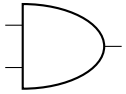
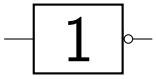
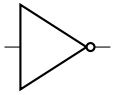
OR		
XOR		
AND		
Invert		

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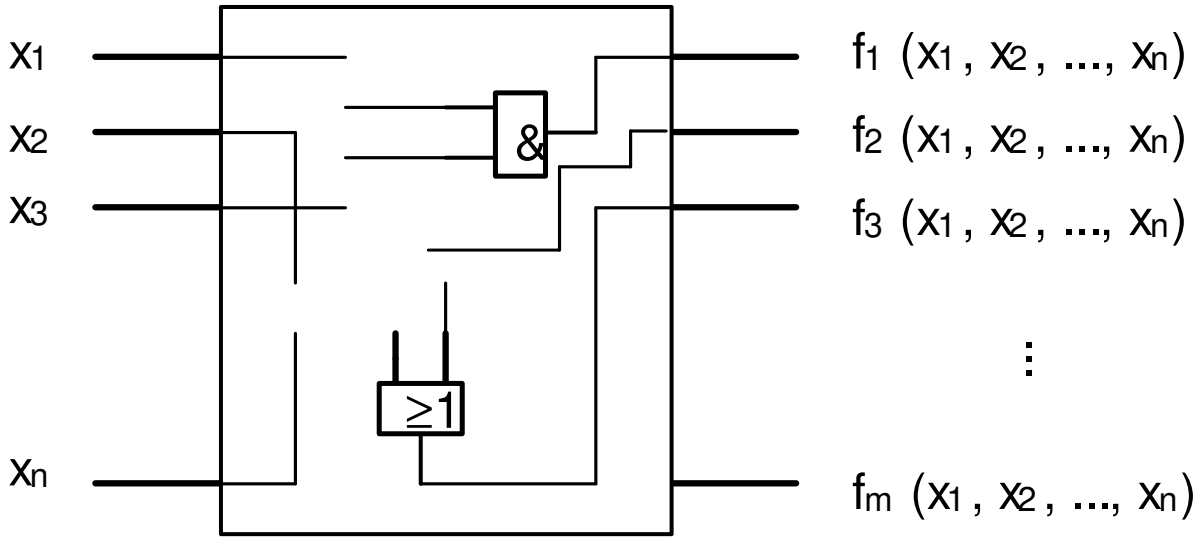
Combinatorial circuits

A combination of logical elements into a circuit.



- Switching function = logical combinations
- Representation by truth tables or boolean expressions

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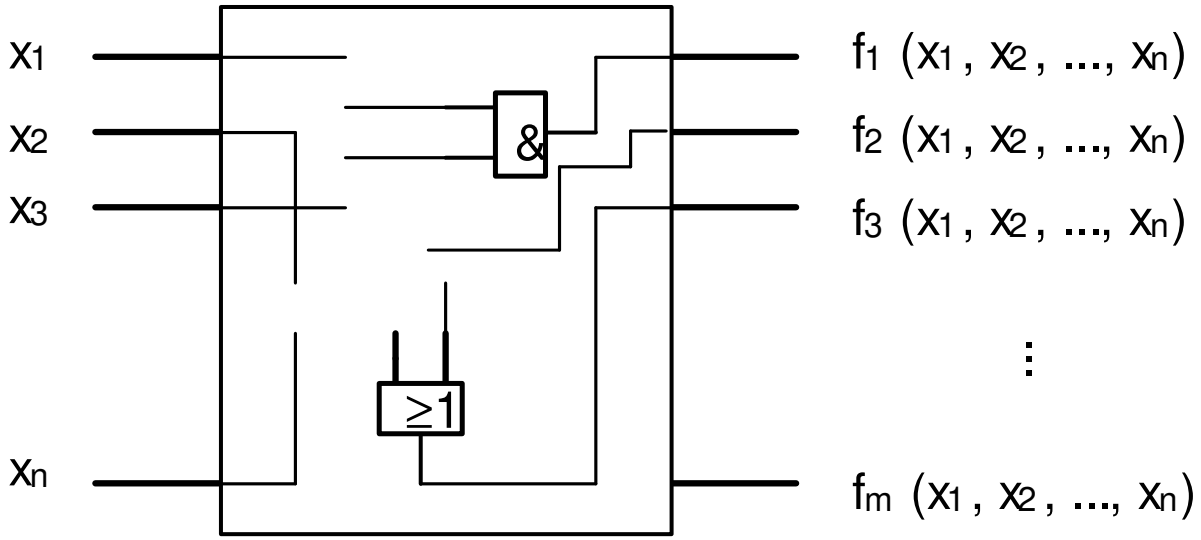

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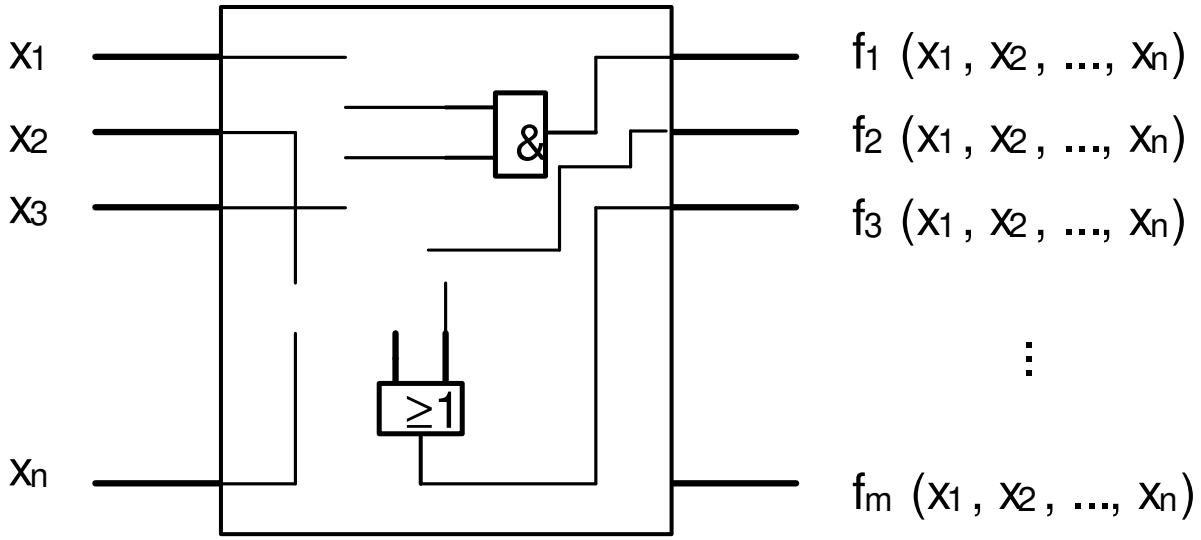

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Sequential circuits

Definition

Sequential circuits = combinational circuit + clock pulse + internal states

- Through the clock pulse it is a clocked (getaktete) operation mode
- Internal states (e.g. through flip-flop registers)

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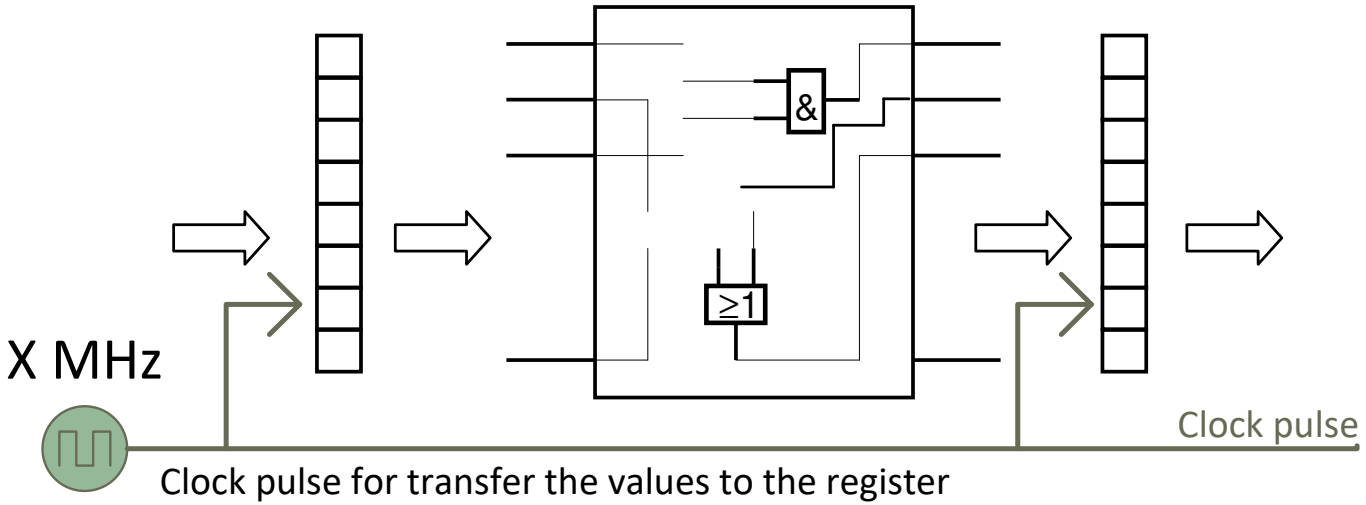

- Flip-flop registers at input and output (I/O registers)
- Clock pulse for transfer data at a defined time

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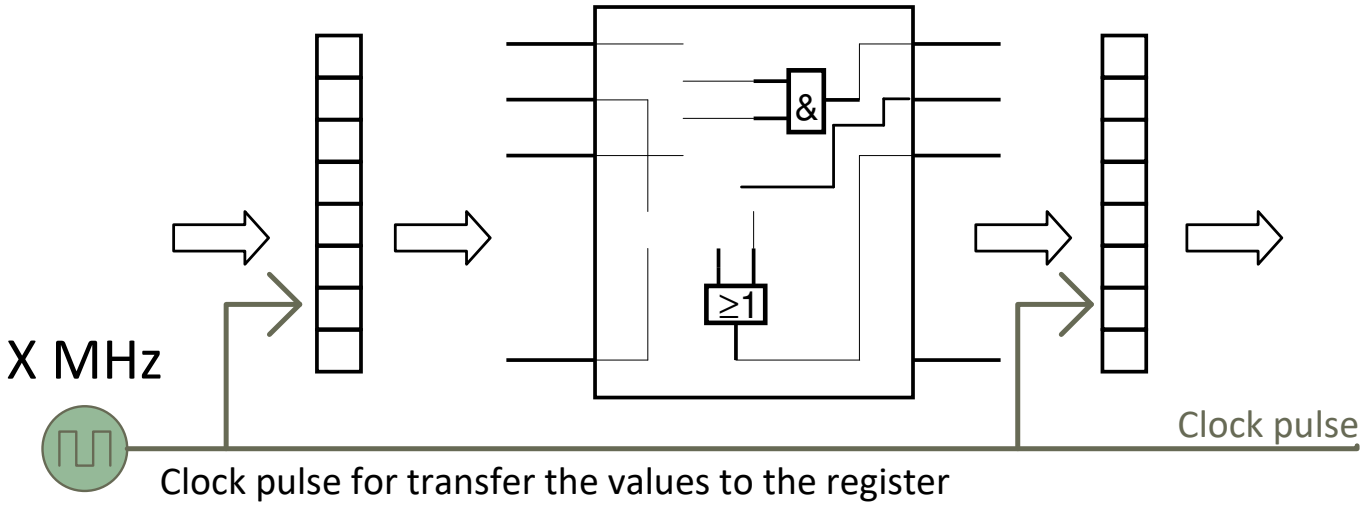

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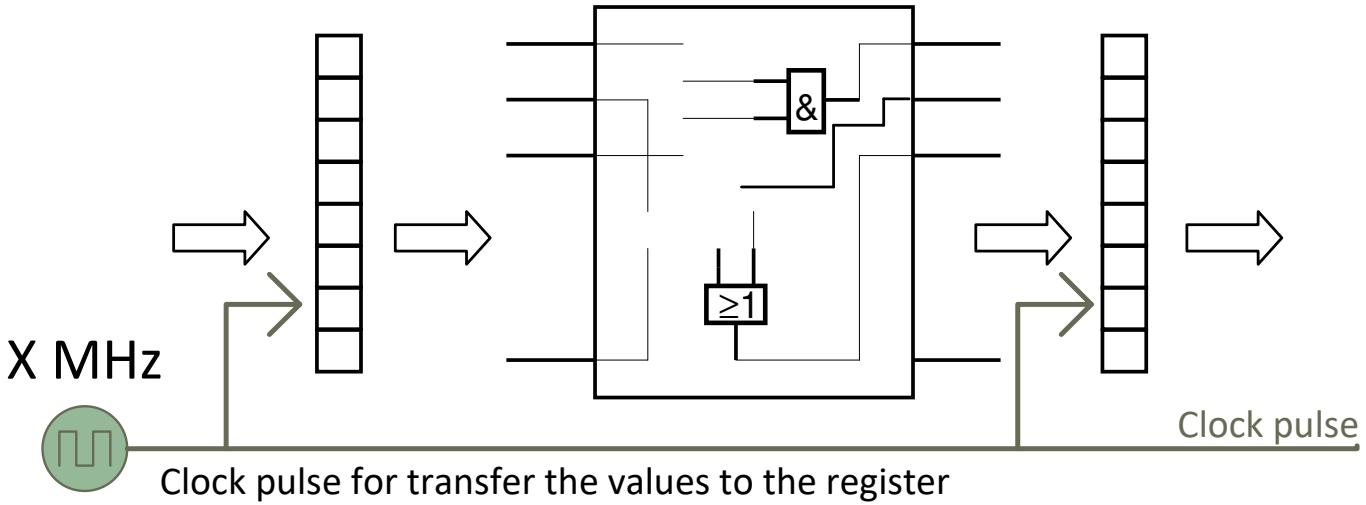

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Sequential circuits

Also called synchronous circuits:

- Theoretically divided into combinational circuit and memory elements (registers).
- It takes t_{max} time until all signals are through the network of logic elements.
- Signals are only transferred to memory elements (I/O registers) at defined clock times (clock pulse).

Condition

$$\frac{1}{\text{clock rate (frequency)}} > t_{max} \tag{1}$$

If you want higher clock rate $\Rightarrow$ t_{max} has to be reduced:

- Improvements in electrical engineering and solid state physics
- Redesign of circuit with less logic elements

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Questions?

All right? ⇒ 

Question? ⇒  and use **chat**

or

speak *after* I ask you to

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Summary and outlook

Summary

- Logical algebra
- Logical elements
- Combinatorial circuits
- Sequential circuits

Outlook

- Technical realisation

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