

The SOF file named “rc4.sof” is located in directory “*/rtl/output_files/rc4.sof”

State of the Lab: working functionalities include:

TOP LEVEL:

“*/rtl/ksa.sv”

Original written in VHDL, was translated to system Verilog. Additionally, all the other modules are written in system Verilog.

Algorithm part 1, Initialize memory S:

“*/rtl/mem_init.sv”

The memory is filled with content from 0 to 255. The writing to memory process requires a clock cycle of waiting after “write_enable” is set to on. The instantiation to memory S is included in the ksa.sv.

Algorithm part 2, swapping memory content:

“*/rtl/swap.sv”

This uses a state machine that first reads and stores the value of “S[i]”, then updates value of “j” according to secret key and reads & stores the value of S[j], and lastly swap them by writing them to the memory. Note that the reading from memory process also requires a clock cycle wait time.

Algorithm part 3, decryption:

“*/rtl/loop3.sv”

This state machine is very similar to the previous one (swapping) with additional interaction with the “check result” module. At the same time, it is more complicated than the swapping state machine since it has to interact with memory S, ROM, and the result memory K, this is implemented by the use of flags which indicate the mem/rom that the decryption module is working with (namely “rom_flag”, “s_flag”, and “k_falg”).

Check result:

“*/rtl/check_result.sv”

This state machine checks the decrypted byte every time when it is written to the memory K. If the decrypted byte is not a lower case character or spacebar, the state machine will tell module “mem_init”, “swap”, and “loop3” to restart, and ask “key_gen” to generate a new key to try. If all the bytes written to the memory K pass the check, then the state machine will see this as “secret key found” and light up LED[0].

Key generation:

“*/rtl/key_gen.sv”

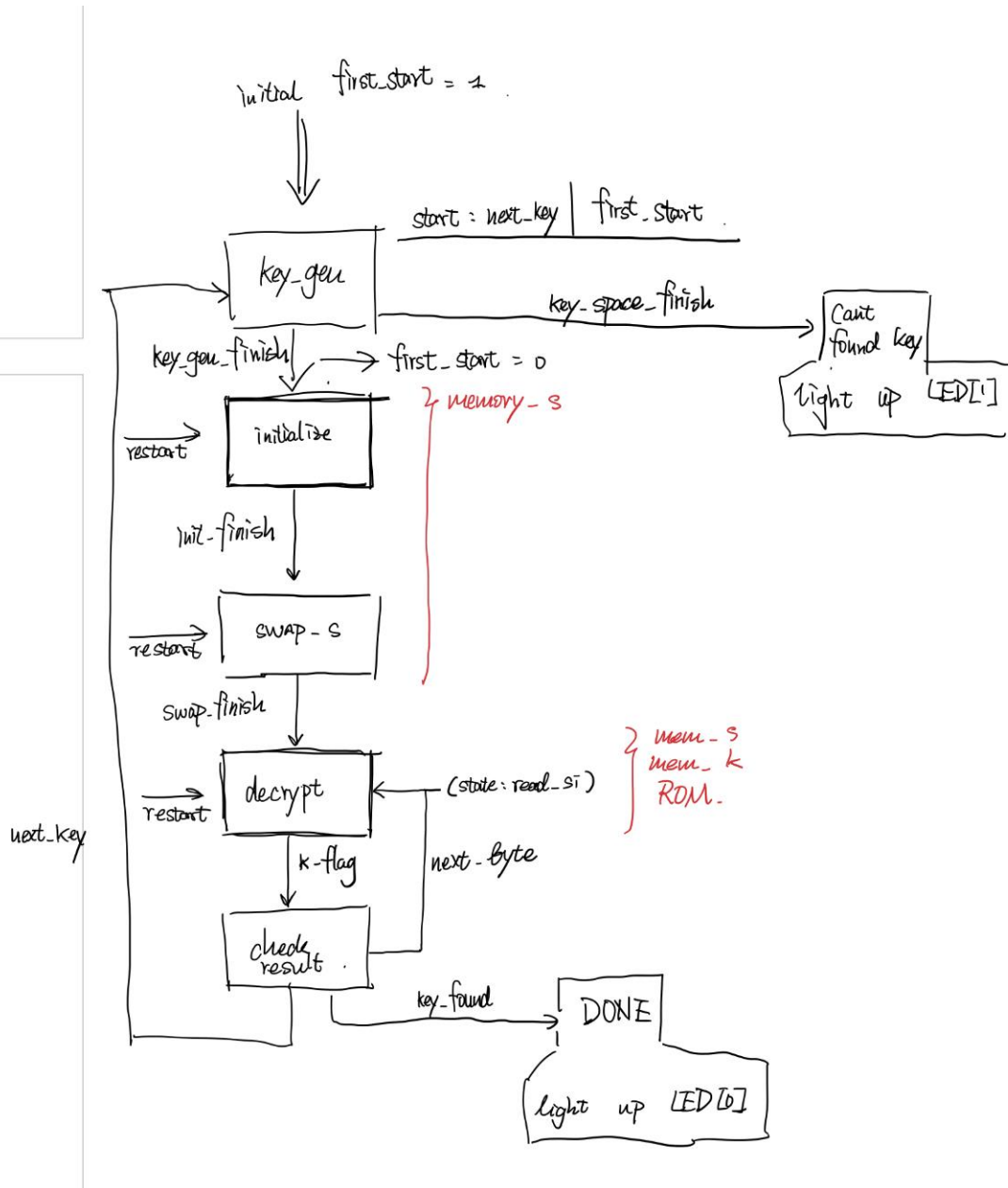
This state machine generates new key when the “check result” module ask. Besides, it generates key “24'b0” the first time the system starts without prompt from the “check result” module. If the counter in the module exceeds 22'h3FFFFFF (the initial 2 bits of key are zero), in another word, when the state machine finish searching the key space, it would regard the secret key is not found and light up LED[1].

NOTE that the multi-core hasn't been completed.

Simulations:

Operation & explanation of the simulation is written in the comment of every testbench code.

Flow chart:



Decryption result (for task 3):

Message 4:

The screenshot shows the 'In-System Memory Content Editor' interface. The top panel includes an 'Instance Manager' table and a 'JTAG Chain Configuration' section.

Instance Manager:

Index	Instance ID	Status	Width	Depth
0	S	Not running	8	256
1	ROM	Not running	8	256
2	K	Not running	8	256

JTAG Chain Configuration: JTAG ready

Hardware: DE-SoC [USB-1] Setup...
Device: @2: 5CSE(BA5)MA5/5CS1 Scan Chain
File: [Download icon] ...

Instance 0: S

Index	Value	Decrypted Data
000000	08 84 88 8F 2F FB EA BC 78 EF CB E8 58 B1 63 04 26 6E CD 95 5F	.../...x...X.c.&n..._
000015	CE 0D 4B B3 27 11 9E 52 C0 D1 9B 23 93 16 AC D8 2A C2 0B 6C F3	..K.'...R...#.....*..1.
00002a	90 1E 66 2D D6 B6 C8 46 13 AD 22 03 FC 74 B2 09 ED 44 15 54 7F	..f-...F...".t...D.T.
00003f	65 99 47 31 D4 4D 91 5C 20 D0 80 12 A7 19 67 4A 6D 76 81 DB 33	e.G1.M.\gUmv..3
000054	E6 9A A5 6B 9D 2E 57 87 05 43 73 BD 83 A8 E2 8B 3A 8C 64 5B 1C	..k..W..Cs.....:d[.
000069	F4 21 06 2B 02 3F B7 1D A0 69 AA 68 56 0E E7 7A EC 3B 00 F9 C3	..!+.?...i.hV...z;...
00007e	53 AF 14 F1 EE 6F 01 3E 92 CF 48 F6 E4 F5 35 1A BE CA 2C C7 37	S....o>..H...5....7
000093	BF 6A 7C 25 B5 9F 5E FF 18 30 F8 32 62 DD A3 E9 24 DE E5 B0 F7	..j %.^..0.2b...\$....
0000a8	40 A2 5D 71 29 97 C5 4F 0C 55 0A 34 FA 5A 86 59 D3 B9 60 D7 C4	@.]q)...O.U.4.Z.Y...'
0000bd	61 E0 C1 C9 7E 3C 72 DF 41 77 10 D2 F0 A4 50 70 FE B8 07 0F 82	a...~<r.Aw....Ep....
0000d2	94 BA 36 E3 DA 79 AE 42 B4 E1 75 7B 4E BB A1 A9 3D 51 AB 38 96	..6...y.B..u{N...=Q.8.
0000e7	D5 17 DC 89 EB 85 39 8E 49 8A A6 1F 8D 98 D9 1B 4C 9C C6 45 CC9.I.....L..E.
0000fc	7D F2 28 FD	}.(.

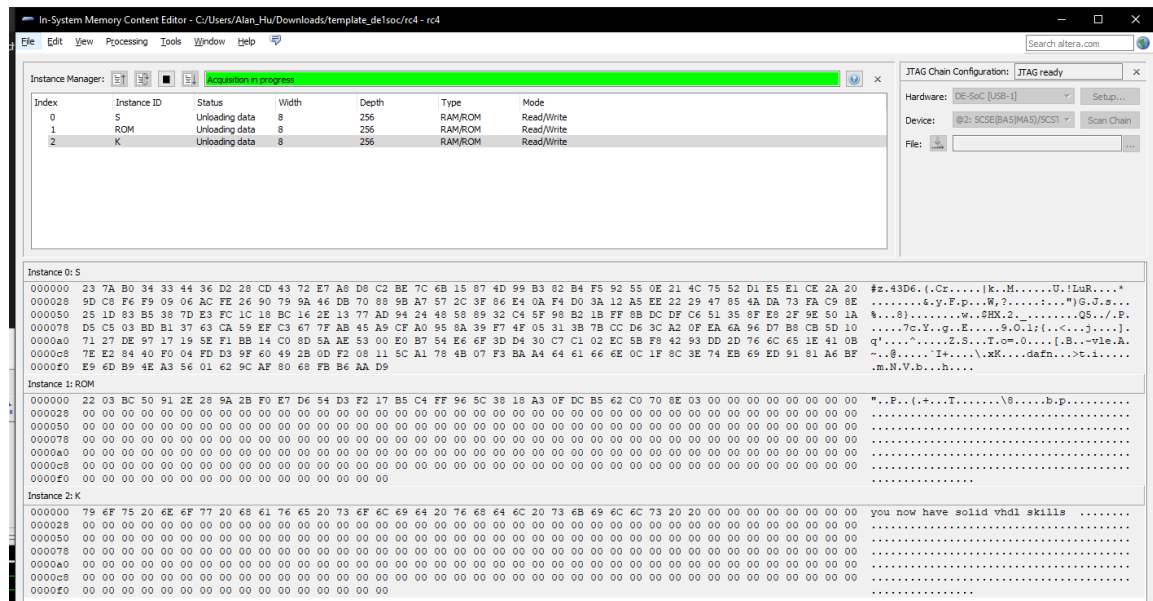
Instance 1: ROM

Index	Value	Decrypted Data
000000	C5 AF B0 4D 4E FD A5 58 2C 54 10 D6 4F D0 86 B8 05 57 42 10 1C	...MN...X,T..O....WB..
000015	E9 27 36 35 04 C6 E7 A7 1D C4 E8 00 00 00 00 00 00 00 00 00 00	.'65.....
00002a	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00003f	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
000054	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
000069	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00007e	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
000093	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0000a8	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0000bd	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0000d2	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0000e7	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0000fc	00 00 00 00

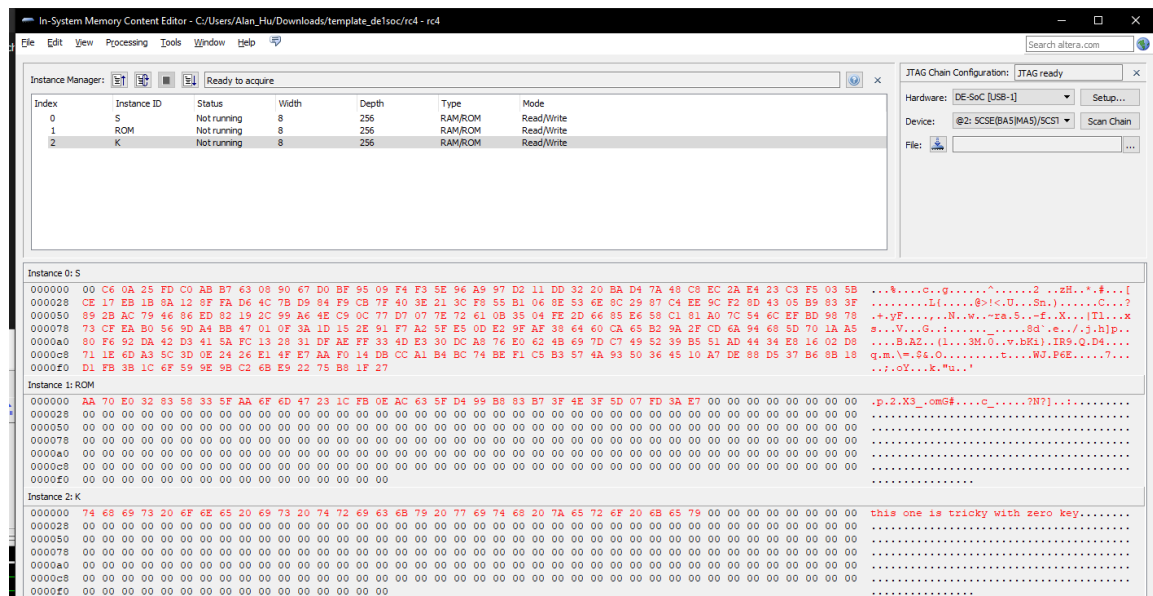
Instance 2: K

Index	Value	Decrypted Data
000000	72 63 20 66 6F 75 72 20 69 73 20 6E 6F 74 20 76 65 72 79 20 73	rc four is not very s
000015	65 63 75 72 65 20 20 20 20 20 20 00 00 00 00 00 00 00 00 00 00	ecure
00002a	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00003f	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
000054	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
000069	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00007e	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
000093	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0000a8	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0000bd	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0000d2	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0000e7	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0000fc	00 00 00 00

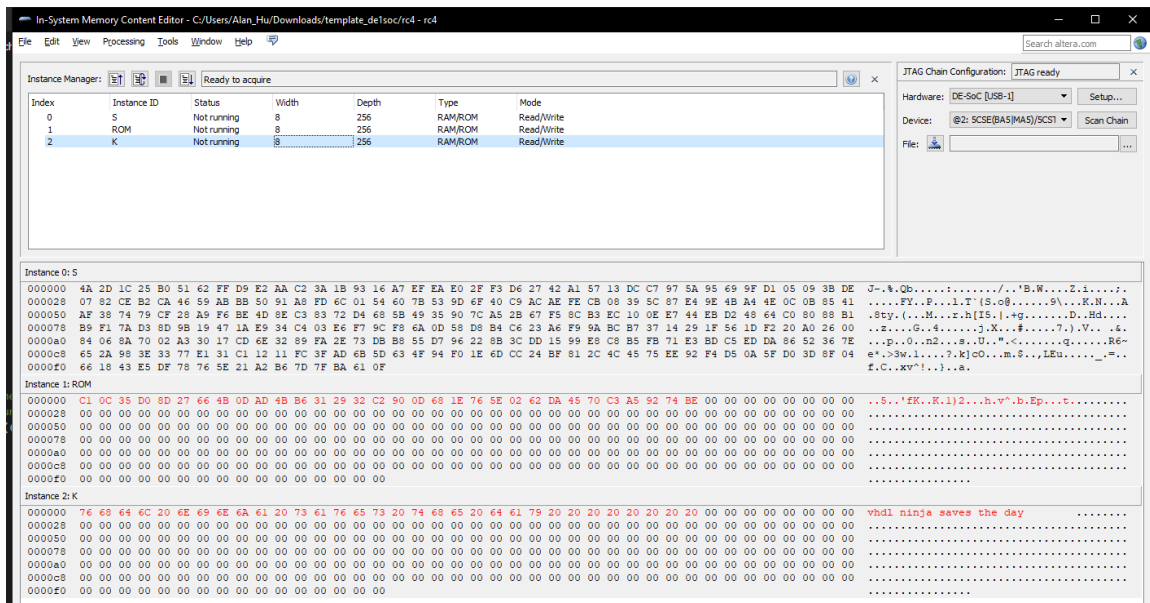
Message 5:



Message6



Message 7



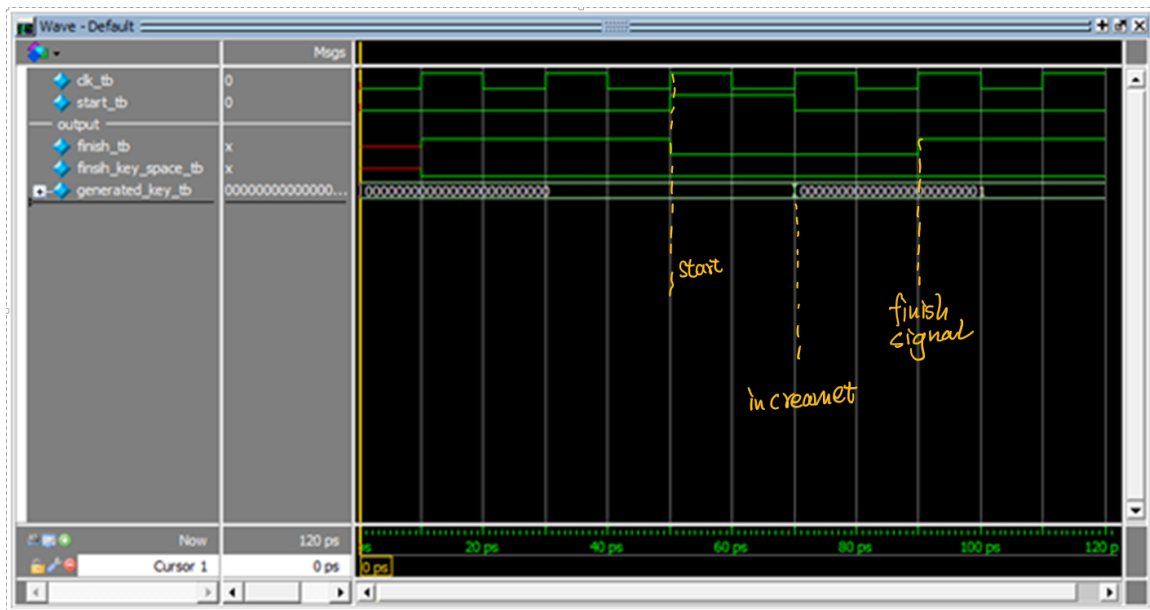
Message 8:

No key found

Test bench:

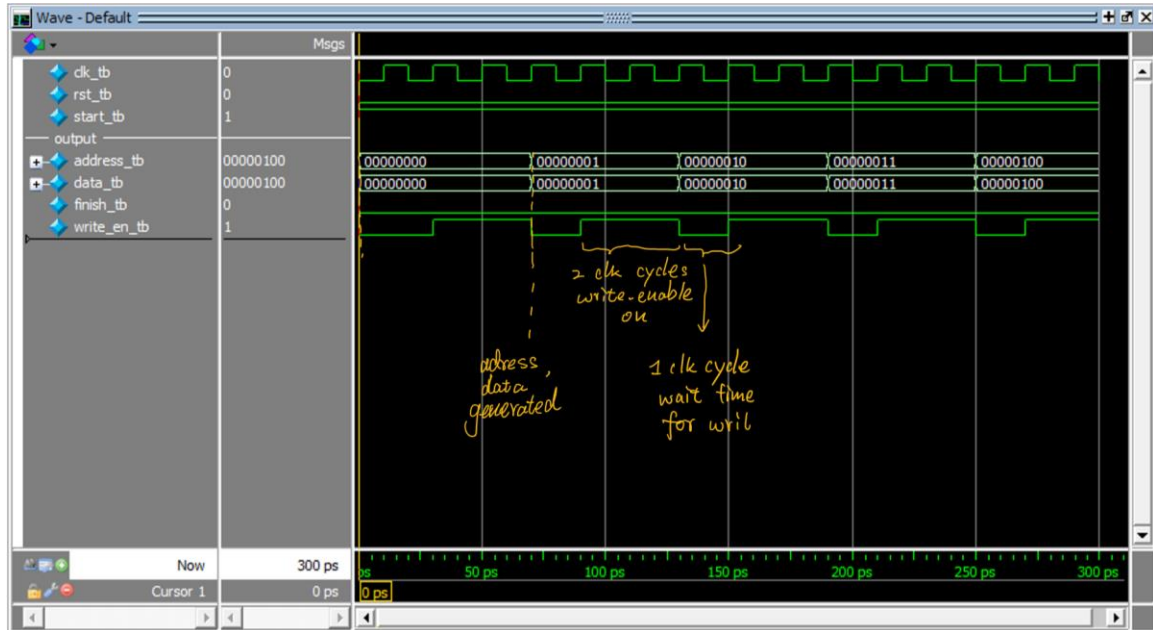
For Key generator:

File "*/rtl/key_gen_tb.sv" is the testbench for "key_gen.sv"



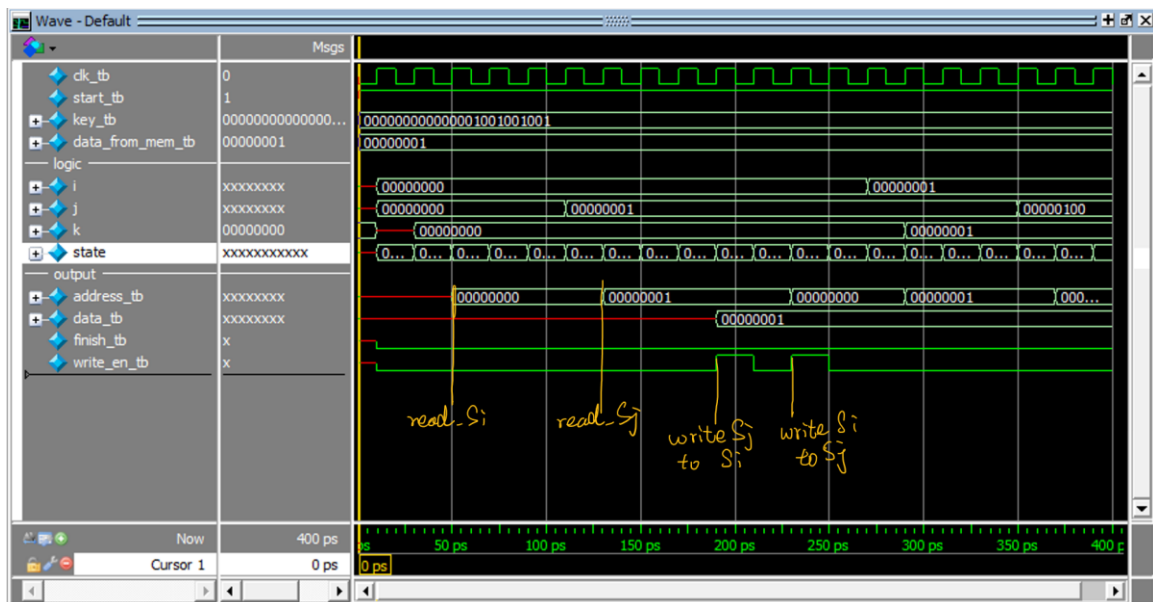
For initialize memory:

File "`*/rtl/mem_init_tb.sv`" is the testbench for "`mem_init.sv`".



For swap:

File "`*/rtl/swap_tb.sv`" is the testbench for "`swap.sv`".



For decryption & check result:

Since decryption is really similar to swap, a simulation is non-necessary.