The University of British Columbia

Assignment 4

ELEC 402 2021, Taught by Reza Molavi, Ivan Cheng

Result for Q1

Delay (avg of t_{pLH} and t_{pHL})	Layout Area	Delay X Layout area
12.065ps	0.238μm^2	5.742 μm^2 ps

Yuqian Hu, 64133713
11-14-2021

Q1.

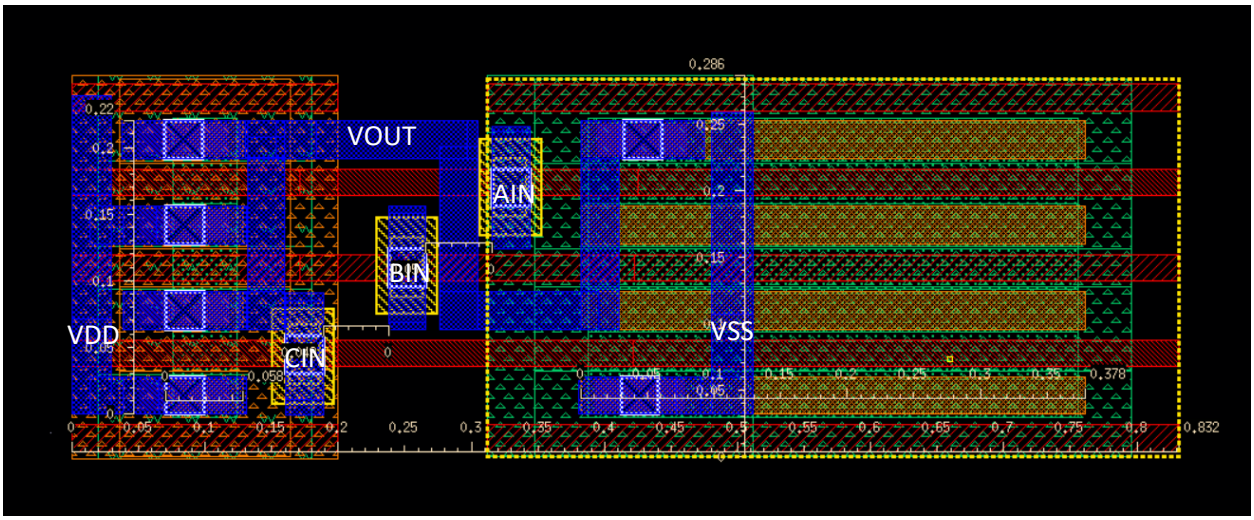


Figure 1.1 NAND3 gate layout, with labeled pins: AIN, BIN, CIN, VDD, VSS, and VOUT. The width of pmos is 58nm and the width for nmos is 378nm

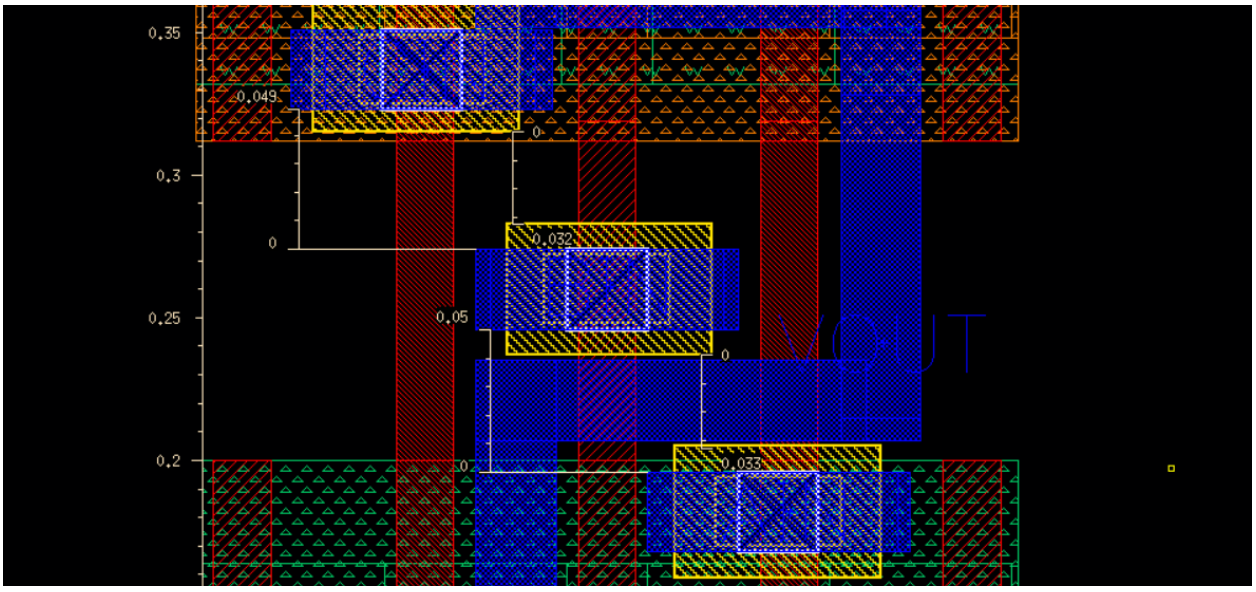


Figure 1.2 distance between shortest distanced pins AIN, BIN, and CIN

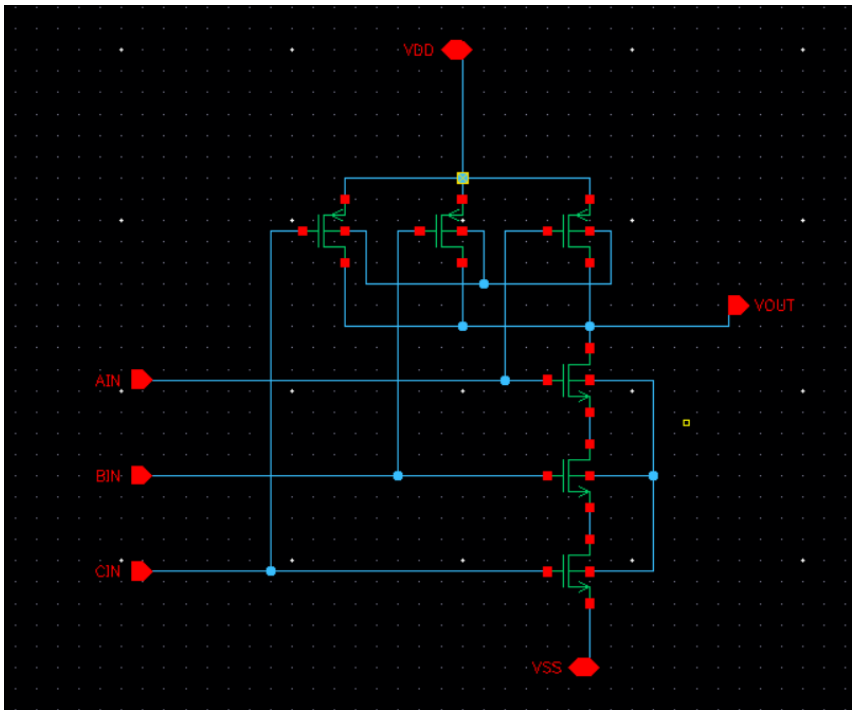


Figure 1.3 Schematic of the NAND3 gate

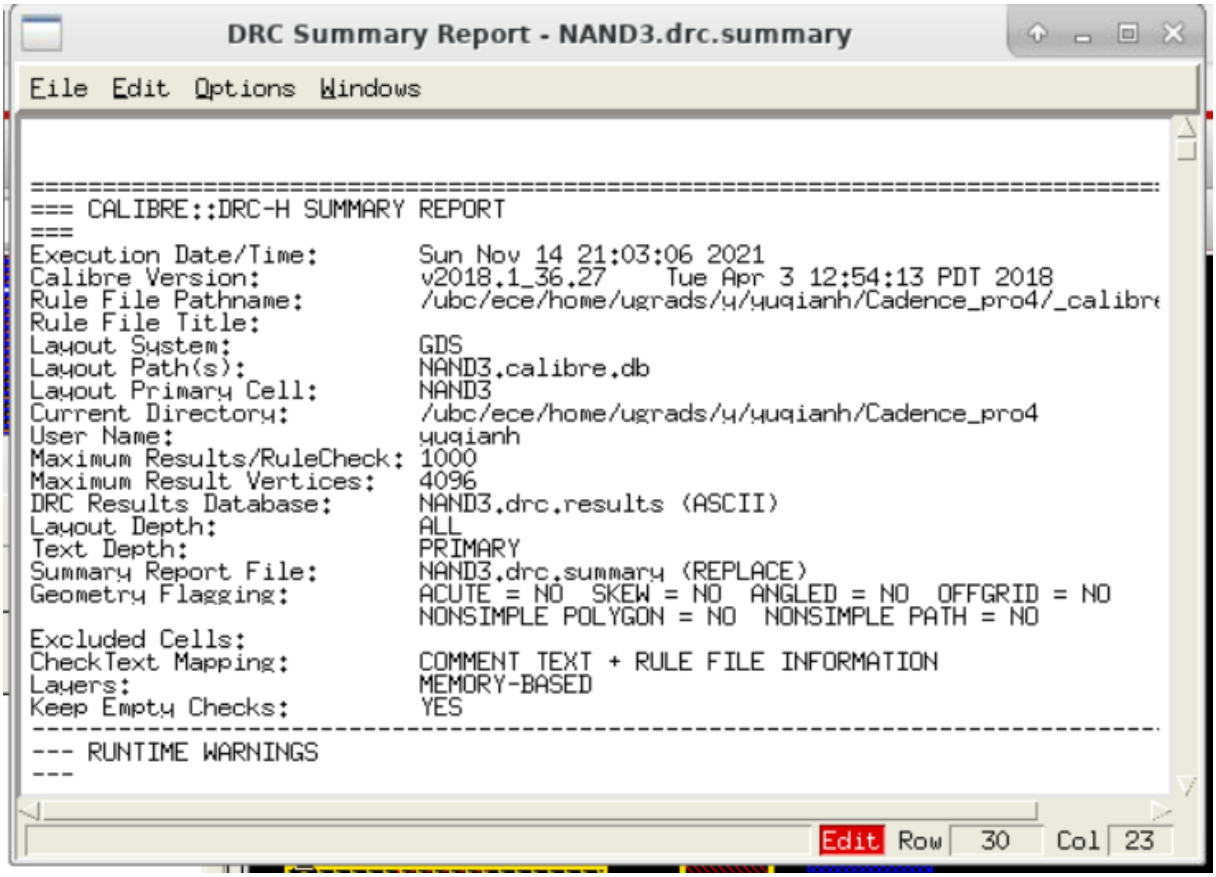


Figure 1.4 DRC summary of the NAND3 gate

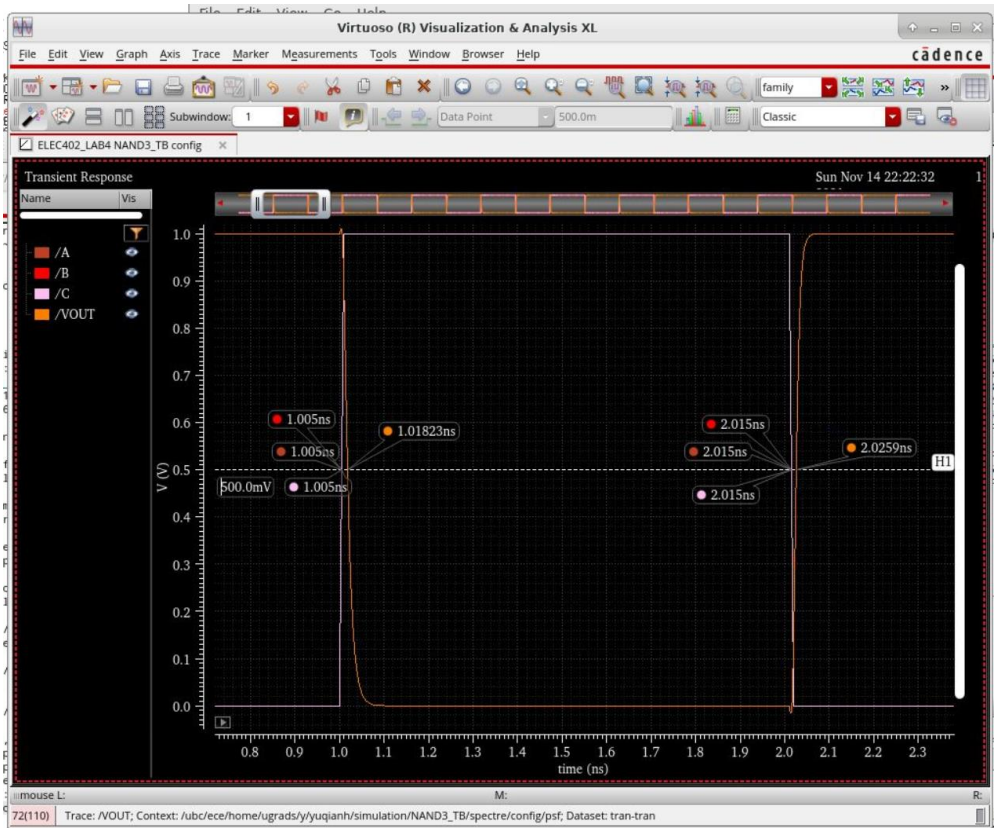


Figure 1.5 As shown the t_{pHL} = 1.01923ns – 1.005ns = 14.23ps, t_{pLH} = 2.0259ns – 2.015ns = 10.9ps, which is close to symmetrical. (Worst case situation)

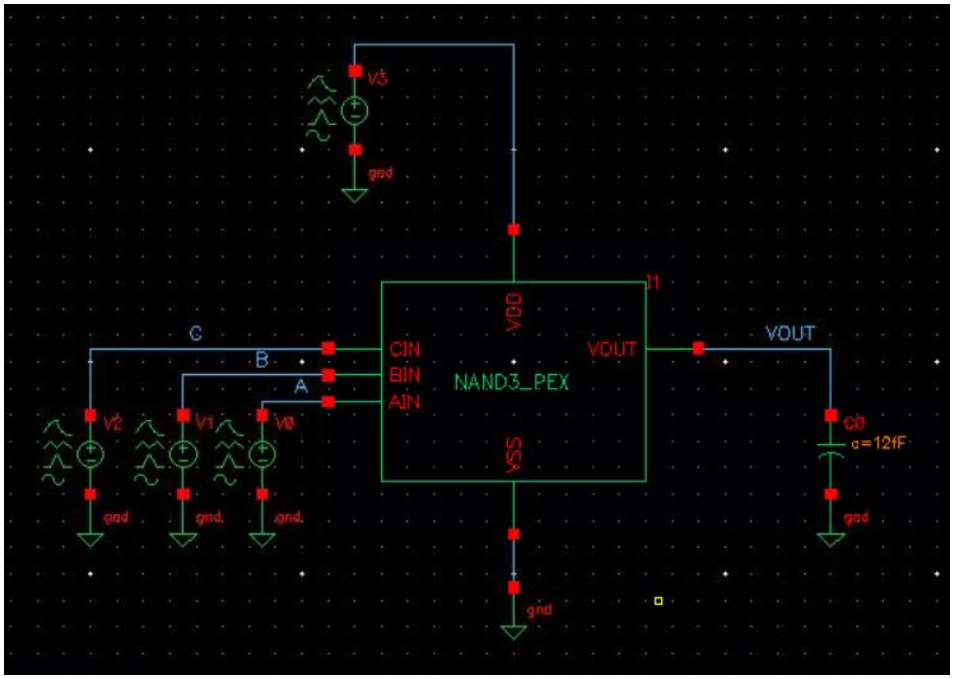


Figure 1.6 schematic of the testbench, the load capacitance is 12pF

Q2.

Logic expression extracted from the pull-down circuit: ~F = (A+B)CD

So, the logic function is **F = (~A~B)+~C+~D**

(a). Sizing:

Since we need to match inverter of NMOS W/L=4λ, PMOS W/L=8λ.

For pull-down circuit, the worst case is ACD/BCD in series. So, we make them 3W each to match 1W for an inverter. A = B = C = D = 3W = 12 λ

For pull-down circuit, the worst case is BA in series. So, we make both of AB 4W and both of CD 2W to match the pull-down resistance. (pmos has twice the resistance than the nmos). A = B = 4W = 16 λ, C = D = 2W = 8 λ.

(b). Worst case transition:

$\mathbf{t_{pHL}}$: When input ABCD is 1110, there are 5 mosfet charged up to VDD. In this case, when D goes from low to high (1111), 5 of the gates mosfet start discharging. (1110 -> 1111)

$\mathbf{t_{pLH}}$: When input ABCD is 0111, all of pull-down circuit discharge to GND. In this case, when B goes from high to low (0011), AB in the pull-down circuit start charging. (0111 -> 0011)

Simulation:

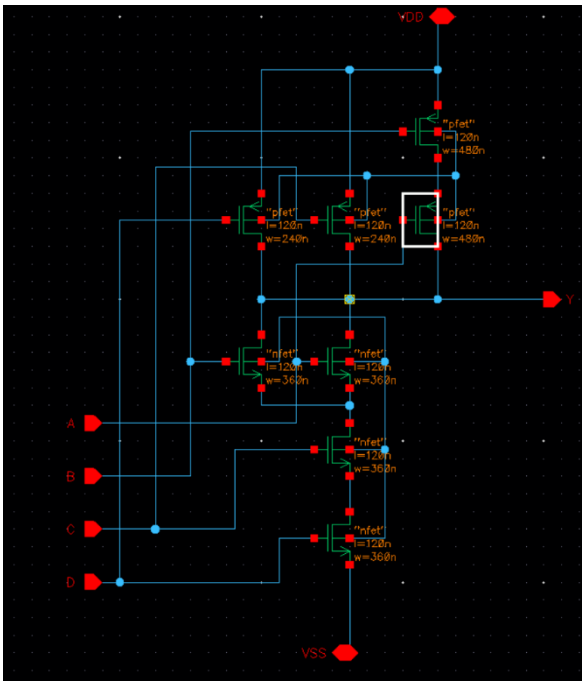
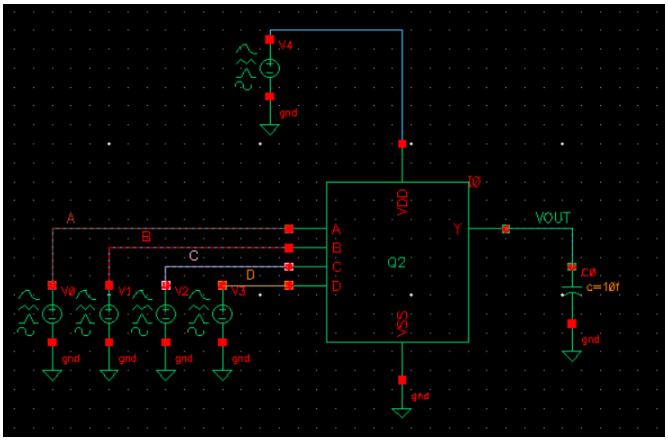


Figure 2.1 ← Schematic of the logic circuit.

Figure 2.2 ↓ Schematic of the testbench with a load of 12fF



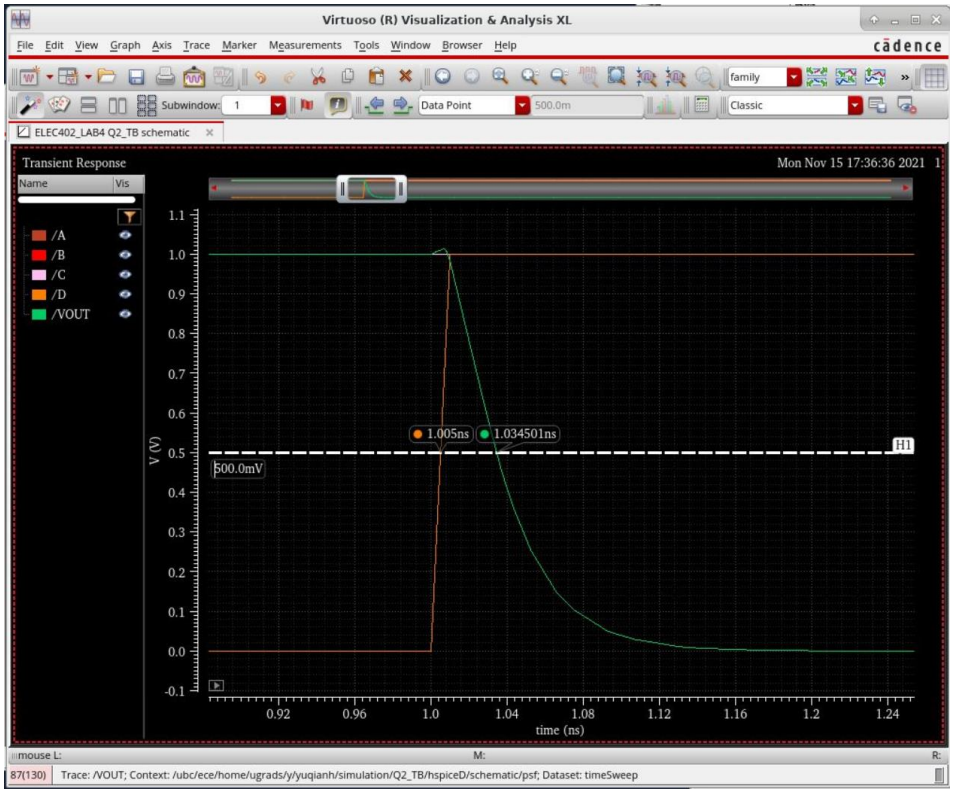


Figure 2.3 simulation result of (1110 -> 1111) t_{pHL} = 1.034501ns – 1.005ns = 29.51ps

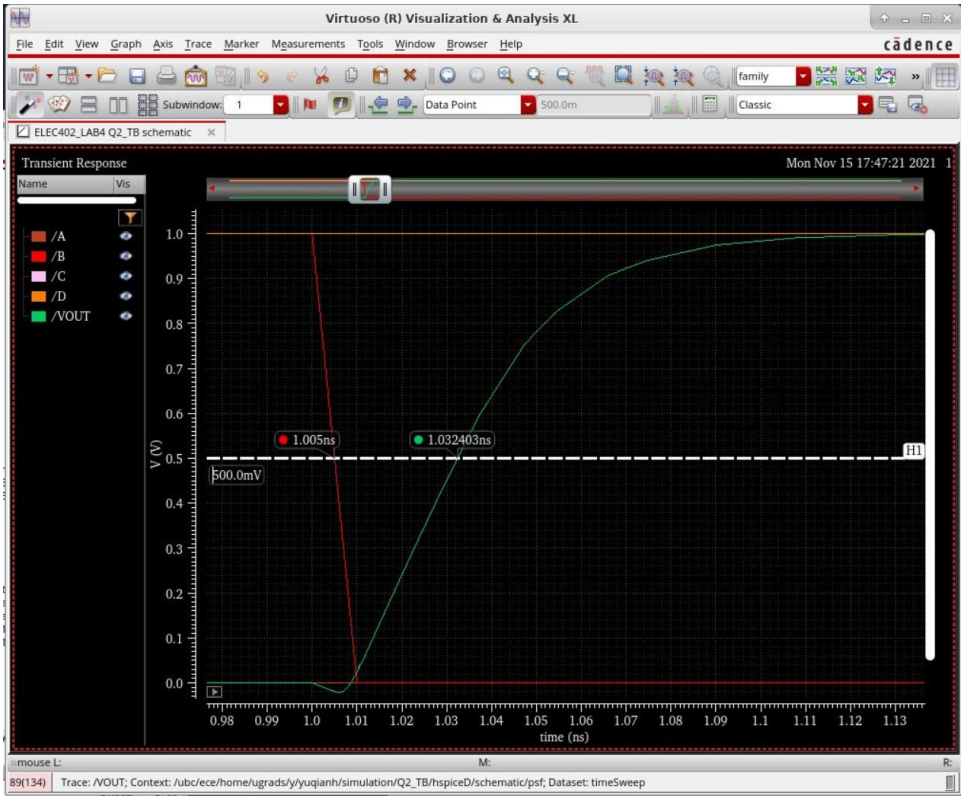


Figure 2.4 Simulation result of (0111 -> 0011) t_{pLH} = 1.032403ns – 1.005ns = 27.03ps

Q3.

(a). Logic function: OUT = ~C = ~((~A sel) + (~B selB)) = (A + sel)(B + selB)

(b). A to C:

Path from A to C goes through an inverter and a nmos (assuming sel is high). So the equivalent circuit can be modeled as following (assuming long channel since L = 100nm):

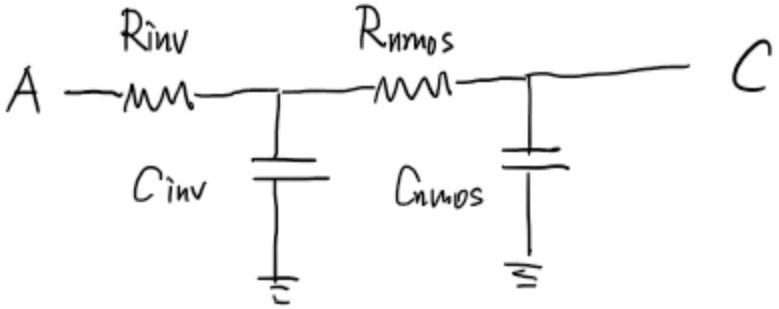


Figure 3.1 Equivalent circuit of A to C

$R_{inv} = R_{nmos} = R_{eq}(L/W) = 12.5\ k\Omega * (2\lambda/4\lambda) = 6.25\ k\Omega$

$C_{TG} = C_{eff} * 2*(4\ \lambda) + C_g * (4\ \lambda) = 1.0 * 2 * 4 * 0.1 + 2.0 * 4 * 0.1 = 1.6\ fF$

$C_{inv} = C_{eff} * (4\lambda + 8\lambda) + C_{TG} = 1.0\ * (12 * 0.1) + 1.6fF = 1.2fF + 1.6fF = 2.8fF$

$C_{nmos} = f * C_g * (4\lambda + 8\ \lambda) + C_{TG} = (2.4f + 1.6)\ fF$ (the output inverter is f times large than the input inverter)

(c).(d). A to C delay

So, the delay is $t_D = R_{inv} * C_{inv} + (R_{inv} + R_{nmos}) * C_{nmos} = (30 + 30f)\ ps$

(e). A to OUT:

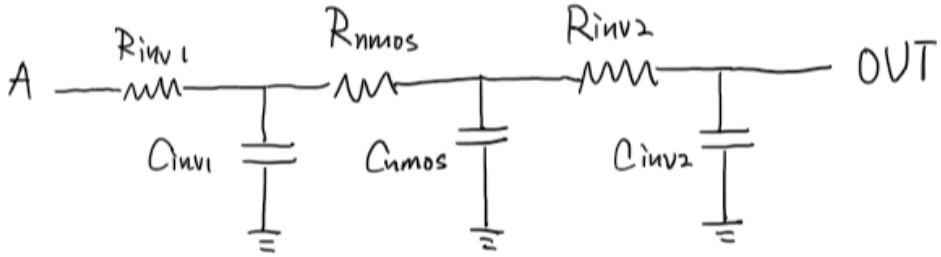


Figure 3.2 Equivalent circuit of A to OUT

$Rinv2 = R_{TG}/f = (6.25/f)k\Omega$

$C_{inv2} = f* C_{eff} * (4\lambda + 8\lambda) + C_{load} = f * 1 * 12 * 0.1 + 50 = (1.2f + 50)\ fF$

So, the delay is t_D = (30 + 30f) ps + (Rinv1 + Rnmos + Rinv2)*Cinv2 = ((30 + 30f) + (32.512f + 312.5/f + 6))ps = (42f + 312.5/f + 662.5) ps

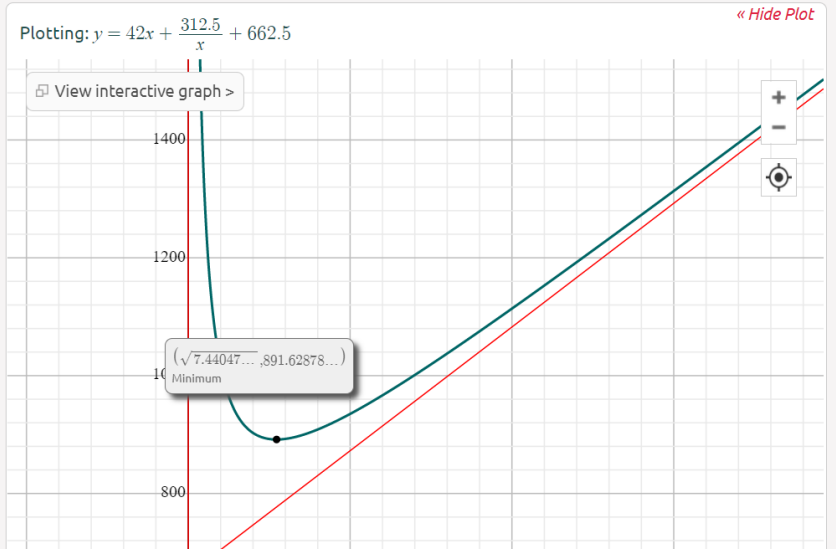


Figure 3.3 f for lowest delay

So when f = 2.7277, it has the lowest delay t_D = 891 ps.