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| The University of British Columbia |
| Assignment 4 |
| ELEC 402 2021, Taught by Reza Molavi, Ivan Cheng |

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| Delay (avg of tpLH and tpHL) | Layout Area | Delay X Layout area |
| 12.065ps | 0.238μm2 | 5.742 μm2 ps |

Result for Q1

**Q1.**

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VOUT

AIN

BIN

VSS

CIN

VDD

Figure 1.1 NAND3 gate layout, with labeled pins: AIN, BIN, CIN, VDD, VSS, and VOUT. The width of pmos is 58nm and the width for nmos is 378nm

A screenshot of a computer

Description automatically generated with medium confidenceFigure 1.2 distance between shortest distanced pins AIN, BIN, and CIN

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Description automatically generated

Figure 1.3 Schematic of the NAND3 gate

Graphical user interface, text, application

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Figure 1.4 DRC summary of the NAND3 gate

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Figure 1.5 As shown the tpHL = 1.01923ns – 1.005ns = 14.23ps, tpLH = 2.0259ns – 2.015ns = 10.9ps, which is close to symmetrical. (Worst case situation)

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Figure 1.6 schematic of the testbench, the load capacitance is 12pF

**Q2.**

Logic expression extracted from the pull-down circuit: ~F = (A+B)CD

So, the logic function is **F = (~A~B)+~C+~D**

**(a). Sizing:**

Since we need to match inverter of NMOS W/L=4λ, PMOS W/L=8λ.

For pull-down circuit, the worst case is ACD/BCD in series. So, we make them 3W each to match 1W for an inverter. A = B = C = D = 3W = 12 λ

For pull-down circuit, the worst case is BA in series. So, we make both of AB 4W and both of CD 2W to match the pull-down resistance. (pmos has twice the resistance than the nmos). A = B = 4W = 16 λ, C = D = 2W = 8 λ.

**(b). Worst case transition:**

**tpHL**: When input ABCD is 1110, there are 5 mosfet charged up to VDD. In this case, when D goes from low to high (1111), 5 of the gates mosfet start discharging. (1110 -> 1111)

**tpLH**: When input ABCD is 0111, all of pull-down circuit discharge to GND. In this case, when B goes from high to low (0011), AB in the pull-down circuit start charging. (0111 -> 0011)

Simulation:

A screenshot of a video game

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Description automatically generated with low confidenceFigure 2.1 ← Schematic of the logic circuit.

Figure 2.2 ↓Schematic of the testbench with a load of 12fF

Graphical user interface

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Figure 2.3 simulation result of (1110 -> 1111) tpHL = 1.034501ns – 1.005ns = 29.51ps

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Figure 2.4 Simulation result of (0111 -> 0011) tpLH = 1.032403ns – 1.005ns = 27.03ps

**Q3.**

(a). Logic function: OUT = ~C = ~((~A sel) + (~B selB)) = (A + sel)(B + selB)

(b). A to C:

Path from A to C goes through an inverter and a nmos (assuming sel is high). So the equivalent circuit can be modeled as following (assuming long channel since L = 100nm):

Diagram, schematic

Description automatically generated

Figure 3.1 Equivalent circuit of A to C

Rinv = Rnmos = Req(L/W) = 12.5 kΩ \* (2λ/4λ) = 6.25 kΩ

CTG = Ceff \* 2\*(4 λ) + Cg \* (4 λ) = 1.0 \* 2 \* 4 \* 0.1 + 2.0 \* 4 \* 0.1 = 1.6 fF

Cinv = Ceff \* (4λ +8λ) + CTG = 1.0 \* (12 \* 0.1) + 1.6fF = 1.2fF + 1.6fF = 2.8fF

Cnmos = f \* Cg \* (4λ + 8 λ) + CTG = (2.4f + 1.6) fF (the output inverter is f times large than the input inverter)

(c).(d). A to C delay

So, the delay is tD = Rinv \* Cinv + (Rinv + Rnmos) \* Cnmos = (30 + 30f) ps

(e). A to OUT:

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Figure 3.2 Equivalent circuit of A to OUT

Rinv2 = RTG/f = (6.25/f)kΩ

Cinv2 = f\* Ceff \* (4λ + 8λ) + Cload = f \* 1 \* 12 \* 0.1 + 50 = (1.2f + 50) fF

So, the delay is tD = (30 + 30f) ps + (Rinv1 + Rnmos + Rinv2)\*Cinv2 = ((30 + 30f) + (32.512f + 312.5/f + 6))ps = (42f + 312.5/f + 662.5) ps

Chart

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Figure 3.3 f for lowest delay

So when f = 2.7277, it has the lowest delay tD = 891 ps.