Spartan-6 FPGA
AX309
User Manual

ALINX

Document History

Revision	Date	Description
REV1.0	2017-6-16	First Release

Copyright reminder

Integrated Development Environment

AX309 DEVELOPMENT KIT uses Xilinx FPGA, user should download the software of ISE Design Suite 14.7 from Xilinx website(https://www.xilinx.com). or download it from Baidu cloud plate which we provided.

Link：http://pan.baidu.com/s/1bpnedbh password：2jy7

Getting Help

Here are the addresses where you can get help if you encounter any problems:

Official Site: Http://www.alinx.com.cn

FPGA forum: http://www.heijin.org

Taobao Shop: http://oshcn.taobao.com

Email : avic@alinx.com.cn

TEL：+86-021-67676997

We will continually provide interesting examples and labs on our forum. Please visit http://www.heijin.org for more information.

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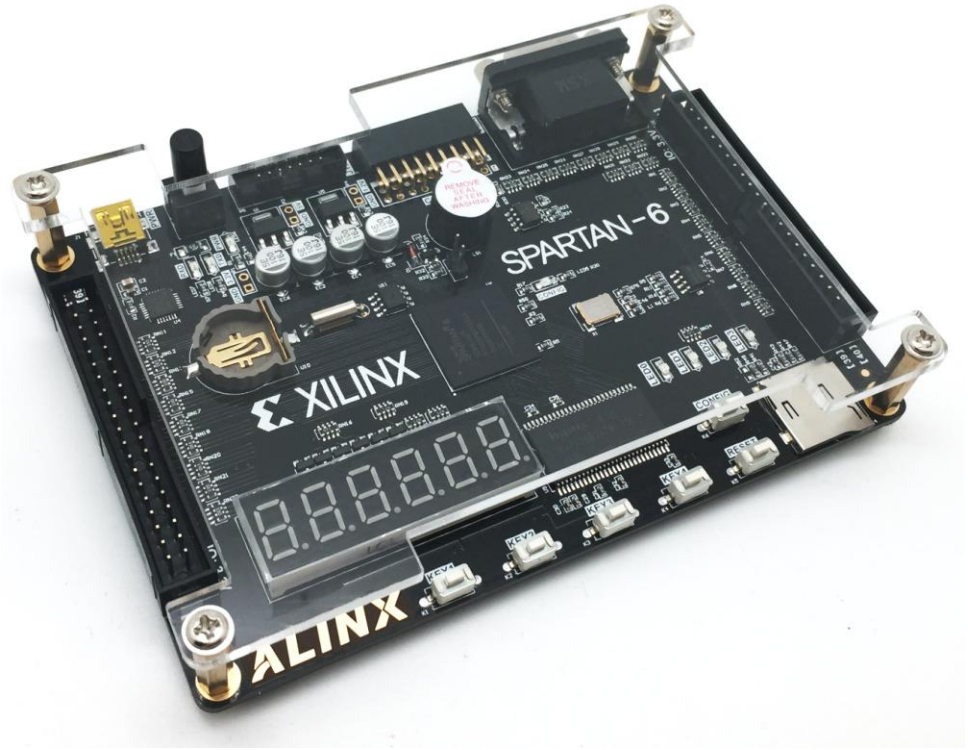
The FPGA development board (AX309) provides everything you need to develop FPGA applications using Xilinx SPARTAN6 FPGA. It has many features that allow users to implement a wide range of designed. The kit contains complete reference designs and source code for each interface and function on board. it is a good choice and easy to use for students or FPGA engineers to learn FPGA and do evaluation. This document provides users of key information about the kit. following Figure shows a photograph of the whole FPGA board.



1. Overview

This board is the evaluation board with Xilinx FPGA Spartan6 used for a complete and powerful system processing. The FPGA chipset is Xilinx Spartan6 XC6SLX9 device in FBGA256 package, the feature summary of this FPGA device is listed as following:

Device	Logic Cells(1)	Configurable Logic Blocks (CLBs)			DSP48A1 Slices(3)	Block RAM Blocks		CMTs(5)	Memory Controller Blocks (Max)(6)	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices(2)	Flip-Flops	Max Distributed RAM (Kb)		18 Kb(4)	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	132
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,758	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358

The main resources and features are listed below:

Parameter	Value

Logic Cells	9152
DSP48 Slices （18 x 18 multiplier, an adder, and accumulator）	16
Configurable Logic Blocks(CLBs)	90Kb
Block RAM Blocks	576Kb
CMTs	2
MAX User I/O	200
Core Power Supply	1.15V-1.25V(suggest is 1.2V);
Operation Temperature	0-85℃

Figure 1-1 provides a quick overview of AX309 board, it depicts the layout of the board and indicates the location of the connector and key components.

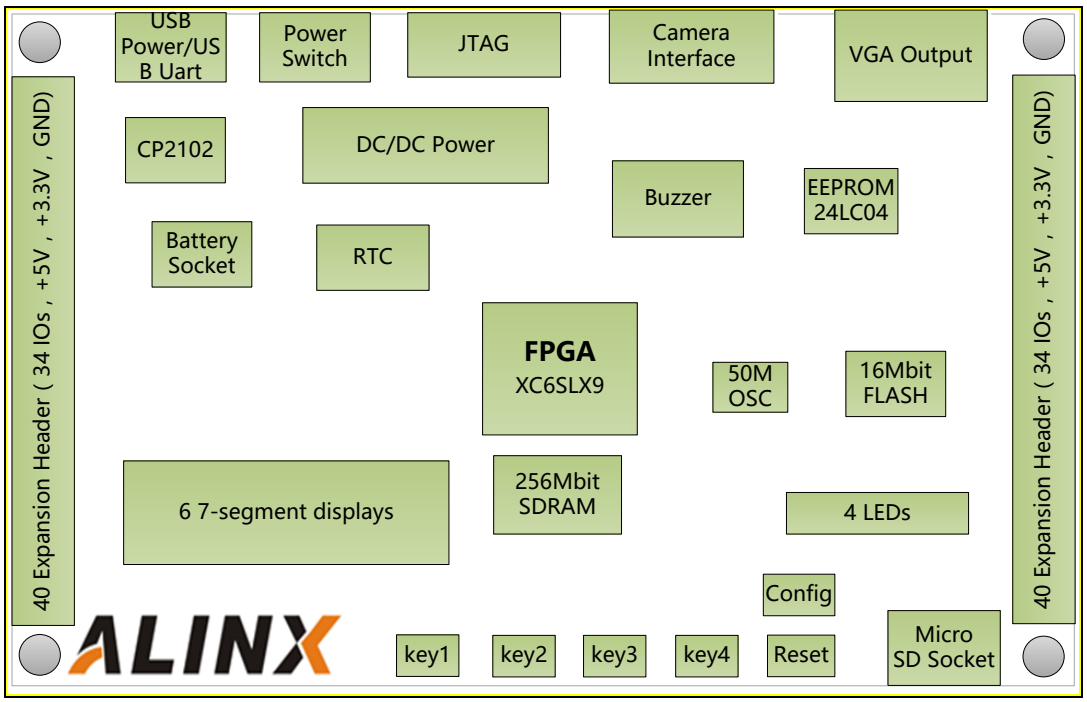


Figure 1-1 Block diagram of AX309 board

The following hardware resources and features are provided on the board:

FPGA Device

- Xilinx Spartan6 XC6SLX9;
- 9152 Logic Cells;
- 16 DSP48 Slices include 18 x 18 multiplier, an adder, and accumulator;
- 576Kb Block RAM Blocks;
- 90Kb Configurable Logic Blocks(CLBs);

- FBGA256 package;

Configuration and Debug

- 16Mbit serial configuration device(SPI FLASH);
- 14pin XILINX standard 2.0mm JTAG connector;

Memory Device

- 256Mbit SDRAM(4Bank x 4M x 16bits);

Communication

- One port of USB-to-serial;
- Real-Time Clock;
- EEPROM with IIC interface;
- Micro SD Socket with SPI interface;
- One buzzer;

Connectors

- Two 40pin expansion headers(use to connect 4.3' LCD module, ADDA module, Audio module etc.);
- One 18pin CMOS header(It can connect ALINX CMOS image sensor);

Display

- One port of VGA output;

Buttons and Indicators

- 4 user LEDs;
- 4 user Buttons;
- Six 7-segment displays

Power

- 5V Power Supply;

2. Power

AX309 board is powered from MINI USB port from PC. When the board and PC computer is connected with USB cable, the AX309 board will power on if the power switch is pushed down. The block diagram of power design is showed as Figure 2-1:

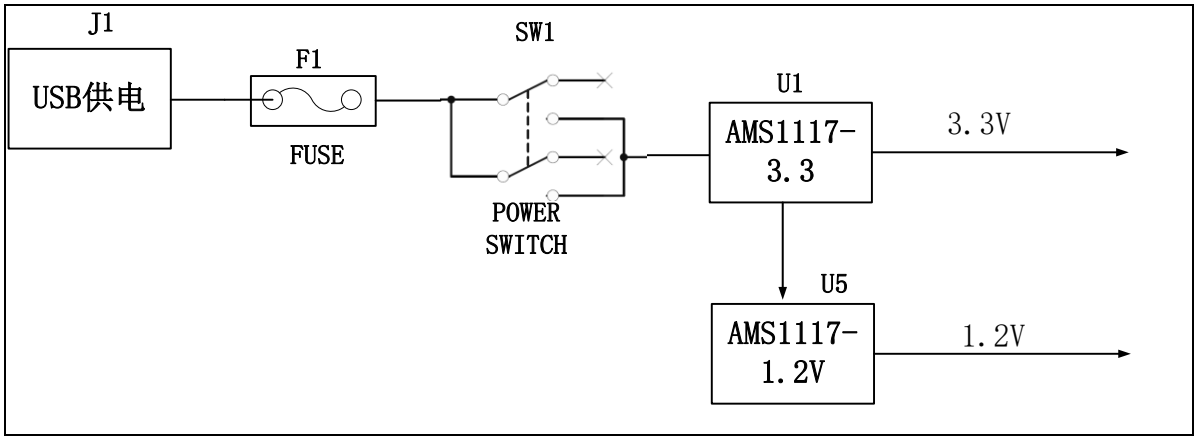


Figure 2-1 Block Diagram Of Power Design

+5V power supply is coming from MINI USB port, it will generate two powers of +3.3V and +1.2V through the LDO voltage regulators AMS1117. +3.3V power is used for FPGA BANK supply voltage, and the +1.2V is used for FPGA core supply voltage.

In AX309 PCB design, it use 4-layers and keep one layer for whole ground layer. so the high-speed signals on PCB has whole ground layer to reference, it will improve the signal integrity for high-speed signal on board.

there are test points for each power supply on board for user to test and check.

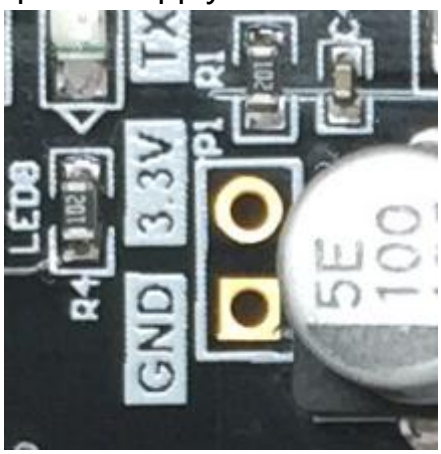


Figure 2-1 The Test Point of Power Voltage

3. FPGA

As mentioned before, AX309 board uses Xilinx Spartan6 FPGA device, the detail part number is XC6SLX9-2FTG256C. The Spartan-6 FPGA ordering information shown in Figure 3-1.

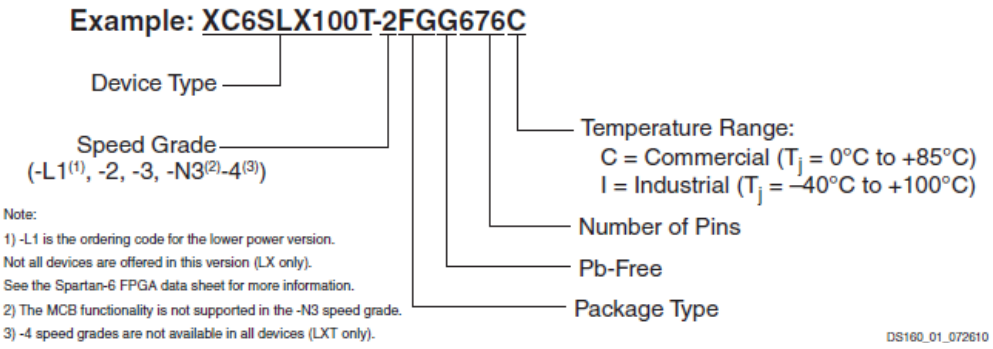


Figure 3-1 Spartan-6 Ordering Information

Figure 3-2 shows the FPGA chipset on AX309 board.

Figure 3-2 FPGA Chipset

1) JTAG Interface

FPGA JTAG interface is connected to a single 14pins connector. When connect a Platform USB cable to the JTAG connector, users can configure and debug the FPGA logic or program SPI FLASH. If programming FPGA using bit file, the configuration file in FPGA will lost after board power is off, but if program the SPI FLASH with MCS file, the configuration of FPGA will not lost even board power is off, FPGA can read the configuration data from SPI FLASH again when power is on.

The hardware design of JTAG connector is showed as Figure 3-3, JTAG interface includes four signals(TCK,TDO,TMS,TDI). these four signals connects between FPGA device and JTAG connector with 33ohm resistors, the 33ohm resistors will protect FPGA device to avoid damage。

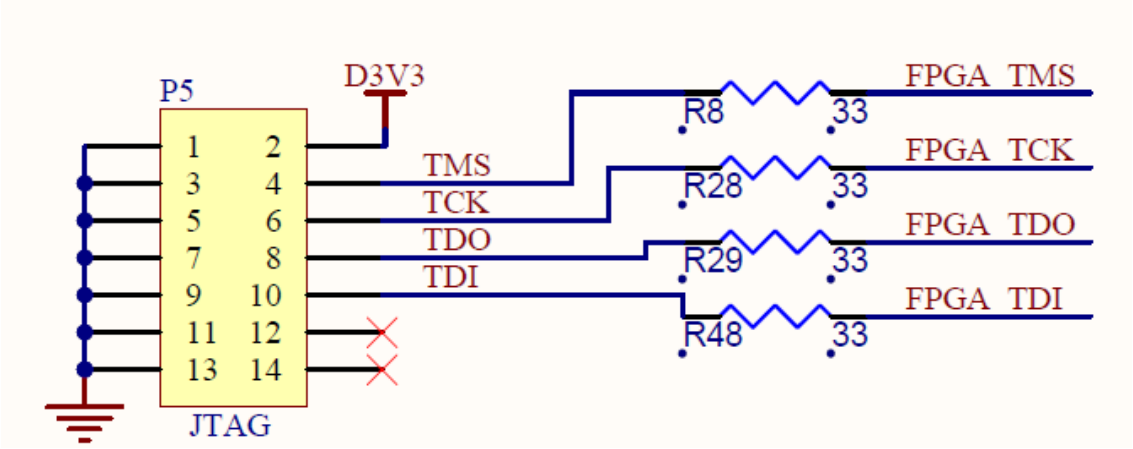


Figure 3-3 Hardware Design Of JTAG Connector

JTAG connector is 14pin connector, the pin pitch is 2.0mm. Figure 3-4 shows the onboard JTAG connector .

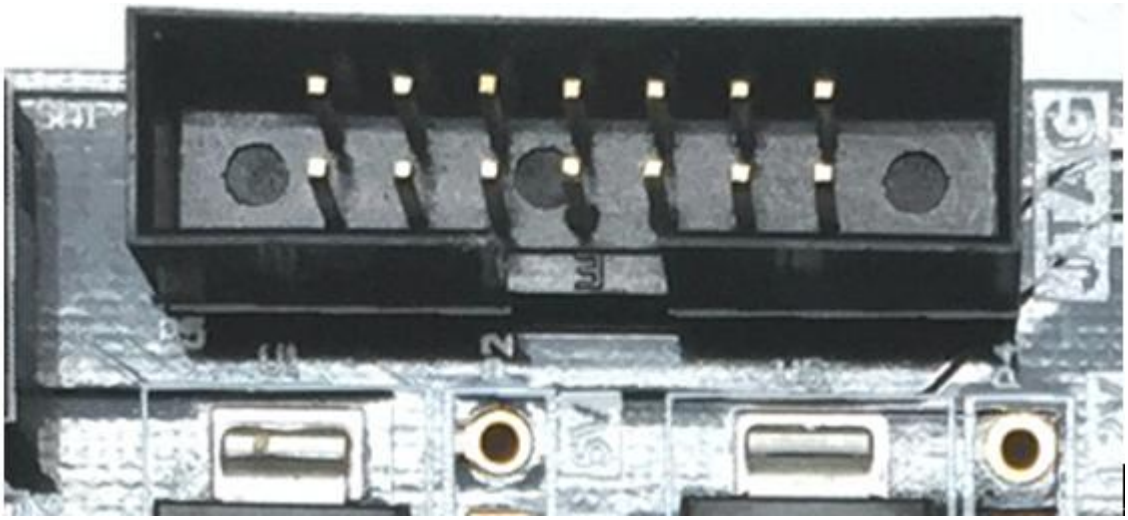


Figure 3-4 Onboard JTAG Connector

2) FPGA Power Supply

There are three power supplies for Spartan-6 FPGA including bank voltage(VCCIO), core voltage(VCCINT) and auxiliary voltage(VCCAUX). The VCCINT power supply voltage is +1.2V, VCCAUX voltage can be +3.3V or +2.5V, in AX309 board it is connected to +3.3V. VCCIO is the power supply for each FPGA BANK, where VCCIO0 is the power supply of FPGA BANK0, VCCIO1~ VCCIO3 respectively power supply of

FPGA BANK~BANK3. In the AX309 board, all of VCCIO pin is connected to +3.3V voltage, so that the IO voltage standard of all bank is +3.3V. Hardware design of FPGA power pin is showed as following Figure 3-5:

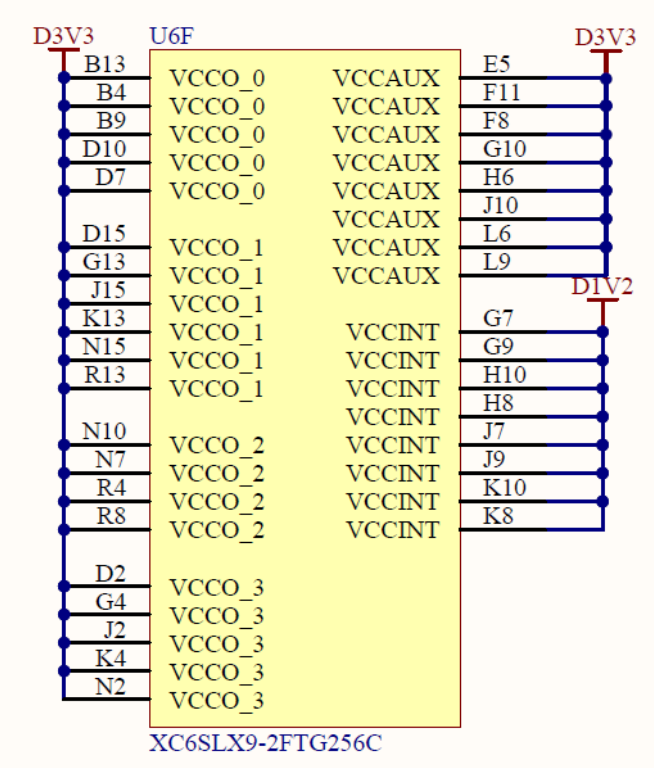


Figure 3-5 FPGA Power Supply

The hardware design of FPGA ground pin is showed as Figure 3-6:

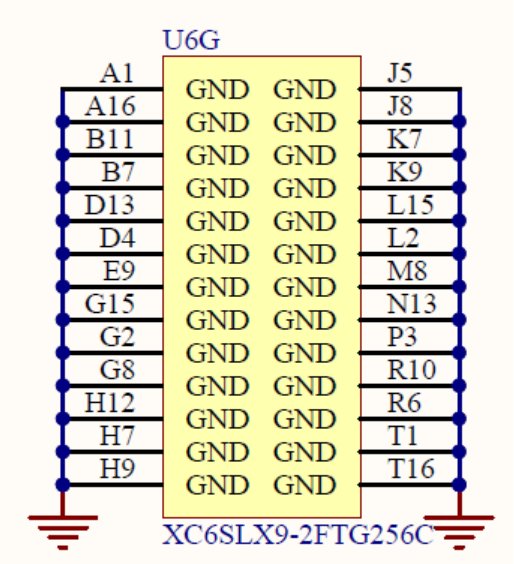


Figure 3-6 FPGA Ground Pin

4. 50Mhz CLOCK

Figure 4-1 is the clock circuit of FPGA system, an 50Mhz crystal oscillator provides the clock source for the whole board. The output of the crystal oscillator is connected to the FPGA T8 Pin (GCLK). This GCLK can be used to drive the user's logic circuit inside the FPGA.

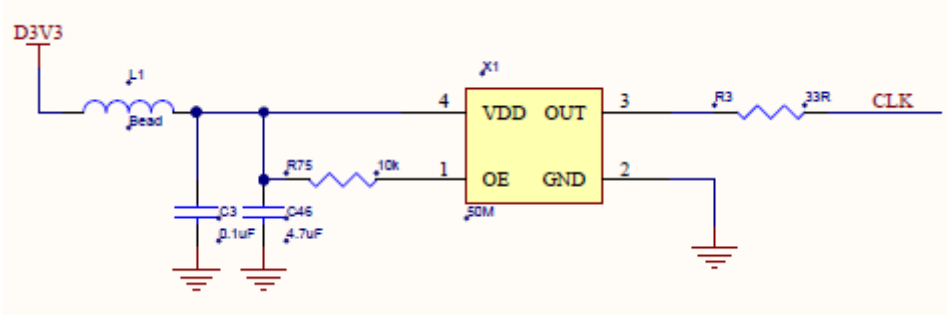


Figure 4-1 50Mhz crystal oscillator

Figure 4-2 shows the onboard 50Mhz crystal oscillator .

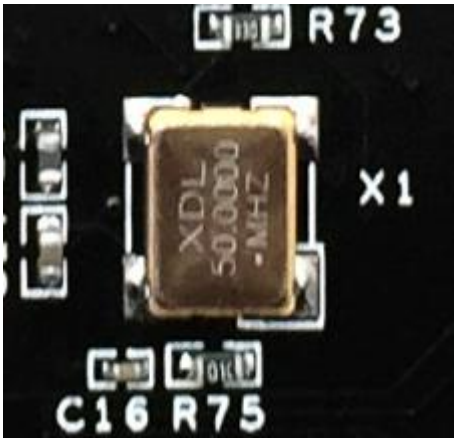


Figure 4-2 50Mhz crystal oscillator onboard

Clock Pin Assignment.

Net Name	FPGA PIN
CLK	T8

5. SPI Flash

The SPI Flash can be used to store the FPGA bitstreams, microblaze application code and other user's data. Table 5-1 shows the equipped SPI Flash device in AX309 board.

Part	Device	Size	Manufacturer
U8	M25P16	16M bit	ST

Table 5-1 SPI Flash

Figure 5-1 is the hardware design of SPI FLASH in AX309 board:

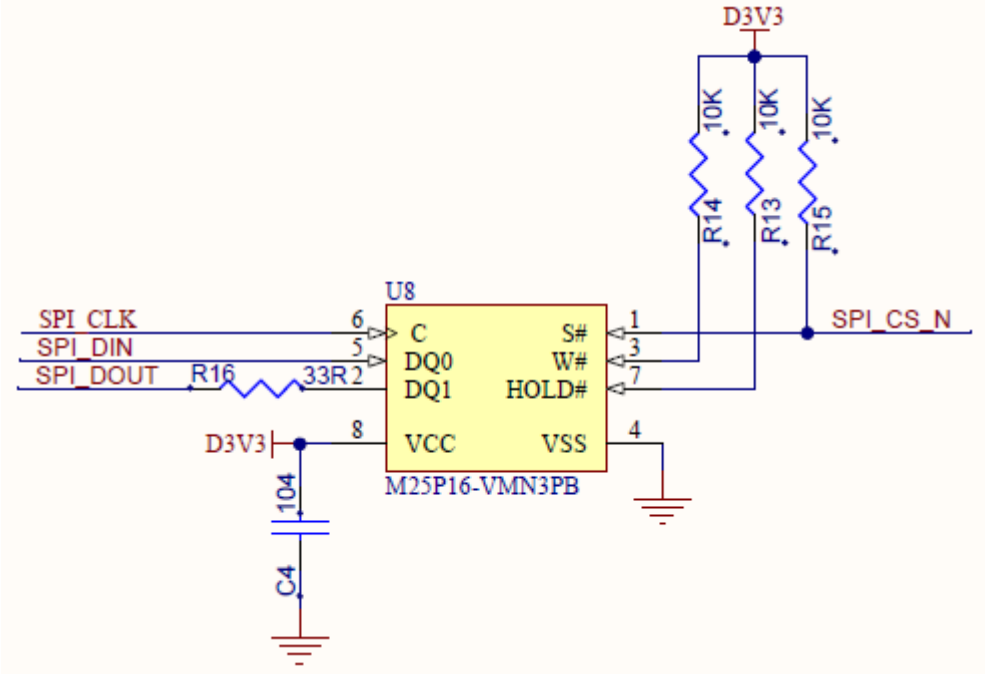


Figure 5-1 Hardware Design of SPI FLASH

Figure 5-2 shows the onboard SPI FLASH.

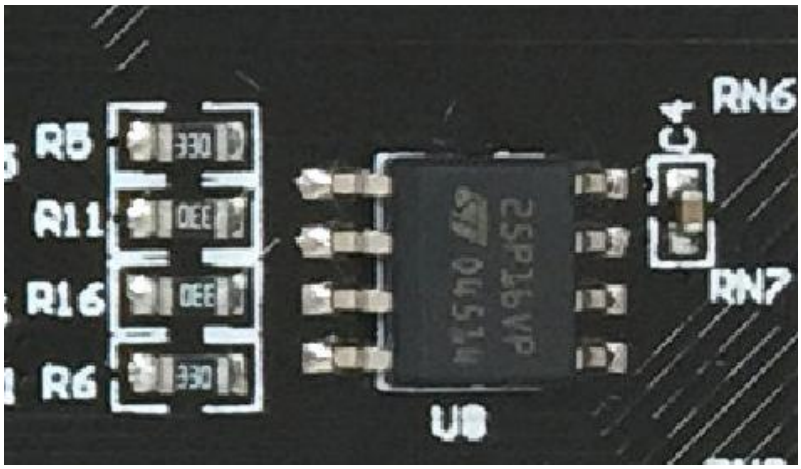


Figure 5-2 SPI Flash Onboard

Pins Assignment of SPI FLASH:

Net Name	FPGA PIN

SPI_CLK	R11
SPI_CS_N	T3
SPI_DIN	T10
SPI_DOUT	P10

6. SDRAM

The equipped SDRAM in AX309 is HY57V2562GTR which is organized in 4 Banks x 4M x 16bits. the data bus between SDRAM and FPGA is 16bit width. The SDRAM is used as data buffer to store large data or information, ideally suited for application of data storage for camera capture, video display and ADDA.

Hardware design of SDRAM is showed as Figure 6-1:

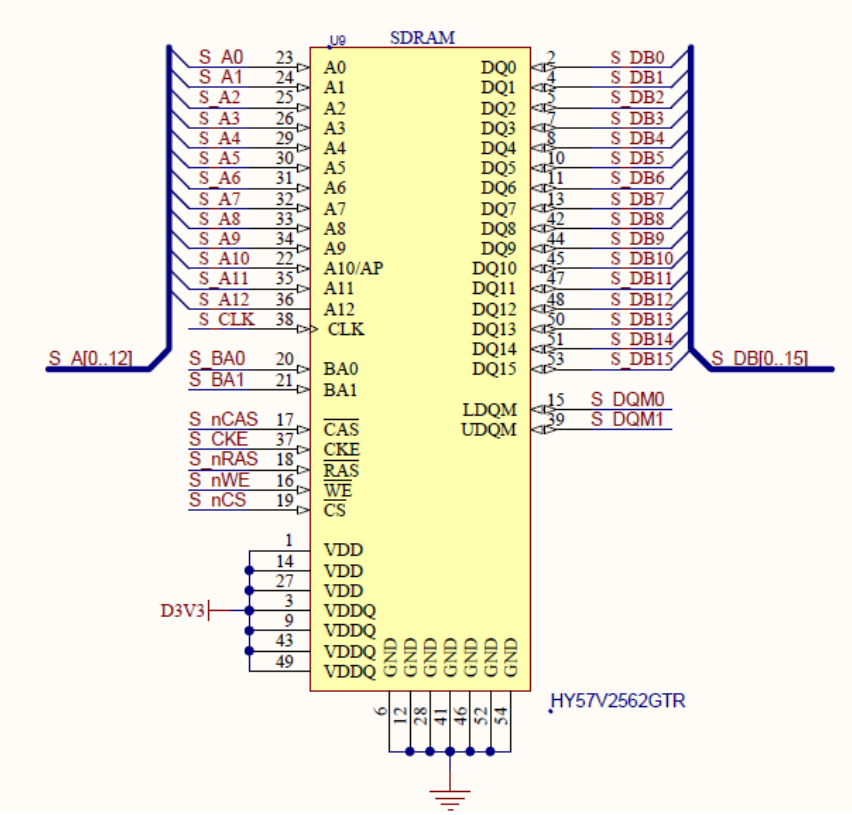


Figure 6-1 SDRAM Hardware Design

Figure 6-2 shows the onboard SDRAM.

Figure 6-2 SDRAM Onboard

PIN Assignment of SDRAM.

Net Name	FPGA PIN
S_CLK	H4
S_CKE	H2
S_NCS	G1
S_NWE	E1
S_NCAS	F2
S_NRAS	F1
S_DQM<0>	E2
S_DQM<1>	H1
S_BA<0>	G6
S_BA<1>	J6
S_A<0>	J3
S_A<1>	J4
S_A<2>	K3
S_A<3>	K5
S_A<4>	P1
S_A<5>	N1
S_A<6>	M2
S_A<7>	M1

S_A<8>	L1
S_A<9>	K2
S_A<10>	K6
S_A<11>	K1
S_A<12>	J1
S_DB<0>	A3
S_DB<1>	B3
S_DB<2>	A2
S_DB<3>	B2
S_DB<4>	B1
S_DB<5>	C2
S_DB<6>	C1
S_DB<7>	D1
S_DB<8>	H5
S_DB<9>	G5
S_DB<10>	H3
S_DB<11>	F6
S_DB<12>	G3
S_DB<13>	F5
S_DB<14>	F3
S_DB<15>	F4

7. EEPROM 24LC04

One 4Kbit EEPROM is used to store the data and serial number as well as the board information and other data. It is connected to FPGA using the I2C interface. The data stored in EEPROM will not lost even board is power off. The hardware design of EEPROM is showed as Figure 7-1:

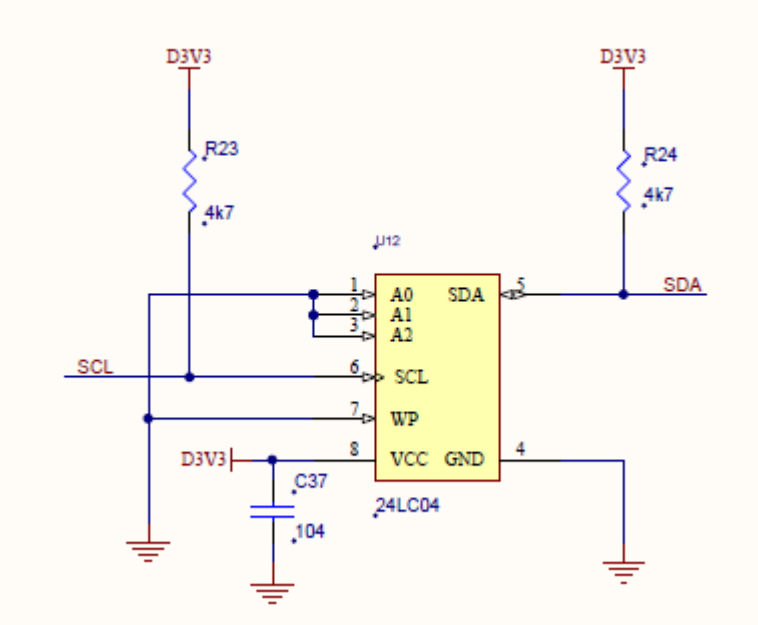


Figure 7-1 EEPROM Design

Figure 7-2 shows the EEPROM on AX309 board.

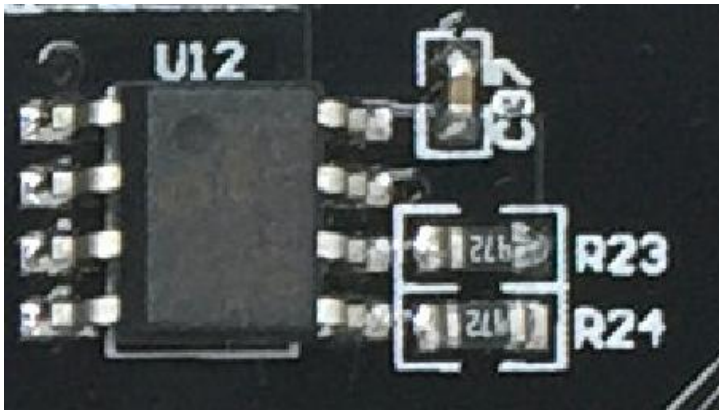


Figure 7-2 Onboard EEPROM

EEPROM PIN Assignment.

Net Name	FPGA PIN
SDA	P12
SCL	N12

8. RTC

A real time clock device(DS1302) is connected to FPGA with serial interface. the DS1302 will provide the time information(Year/Weeks/Hours/Seconds/Minutes) to FPGA system. An external 32.768KHz clock is required to providing accurate clock

source to DS1302 for normal operation. In order that RTC can work alone even if board is power off, a battery need to be equipped on U10 positon, the P/N of battery is CR1220 and it is not mounted by default.

The hardware design of RTC is showed as Figure 8-1:

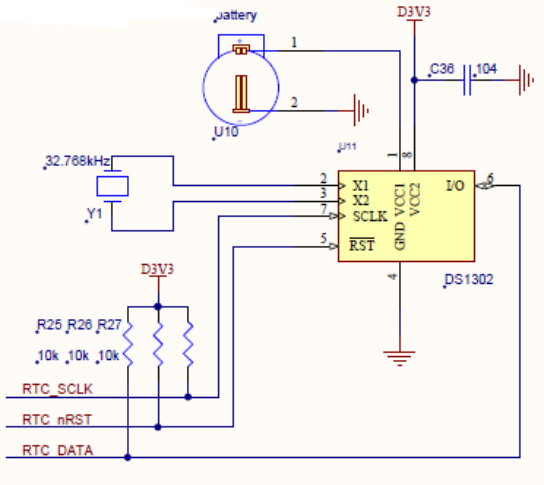


Figure 8-1 RTC Hardware Design

Figure 8-2 shows the DS1302 circuit on AX309 board.

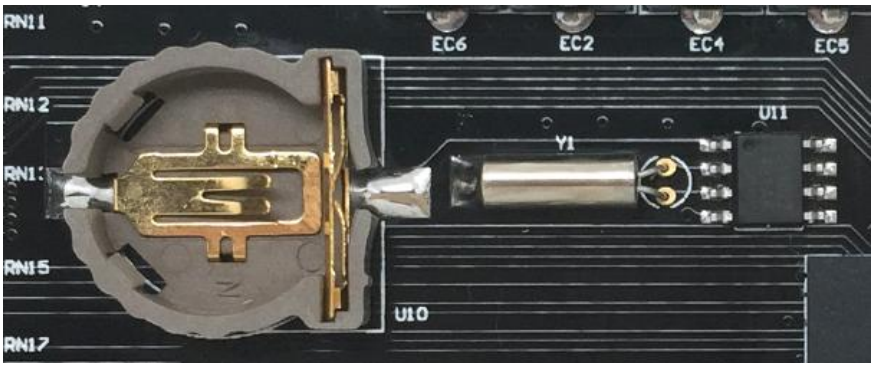


Figure 8-2 DS1302 Circuit Onboard

DS1302 Pin Assignment.

Net Name	FPGA PIN
RTC_SCIK	E13
RTC_nRST	C13
RTC_DATA	D14

9. USB Serial Port

The board provides a MINI USB connector J1 (shared with power input) as a serial port to communicate with PC computer or other device. In AX309 board, we use CP2102 chipset as an USB to UART bridge. When connecting an USB cable, FPGA board can communicate with PC for UART communication. The hardware design of USB UART is showed as Figure 9-1:

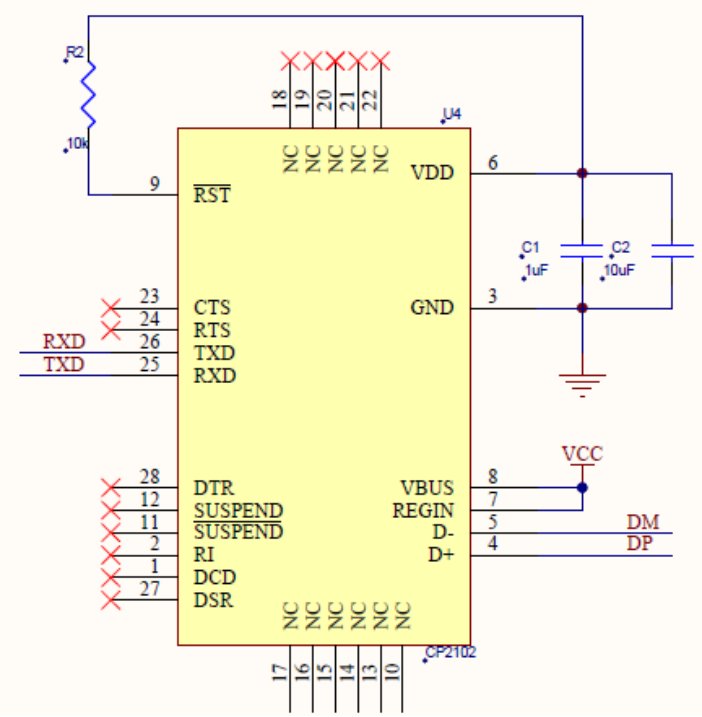


Figure 9-1 USB UART Interface

Figure 9-2 shows the USB UART onboard.

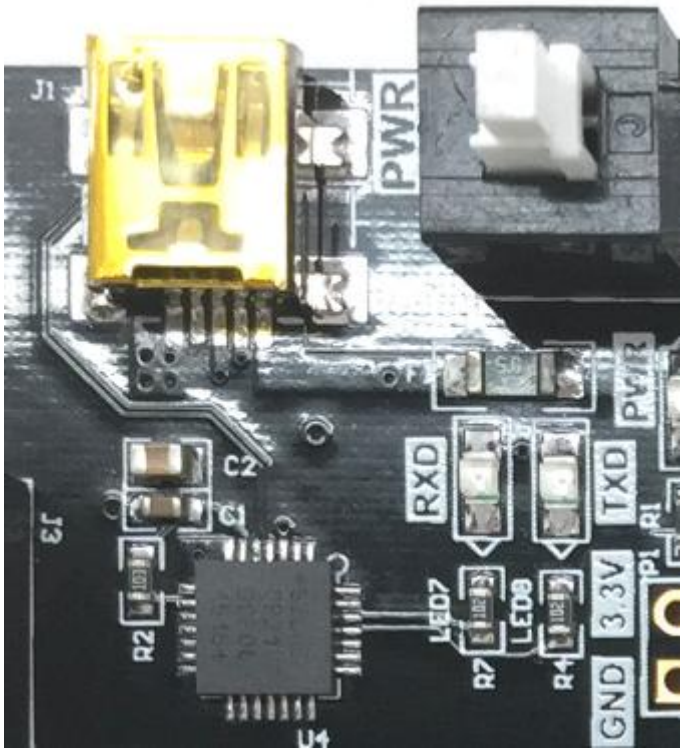


Figure 9-2 USB UART Onboard

There are two LEDs on board to indicate the UART operation status, the RXD LED is used to indicate receiving status, and the TXD LED is used to indicate send status. The indication LEDs is design as Figure 9-3.

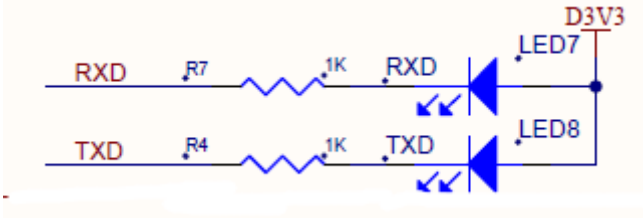


Figure 9-3 USB UART LED Indication

PIN Assignment of USB Uart.

Net Name	FPGA PIN
RXD	C11
TXD	D12

10. VGA Port

There is a VGA display port on AX309 board with 16-bit (RGB565) DAC. Using this VGA

interface, FPGA can display picture or image on VGA monitor. The 16-bit VGA DAC is combined of resistors network, the RGB signals from FPGA is converted to analogy signal through VGA DAC. FPGA also should provide the horizontal sync signal and vertical sync signal to drive VGA monitor. The hardware design of VGA interface is showed as Figure 10-1:

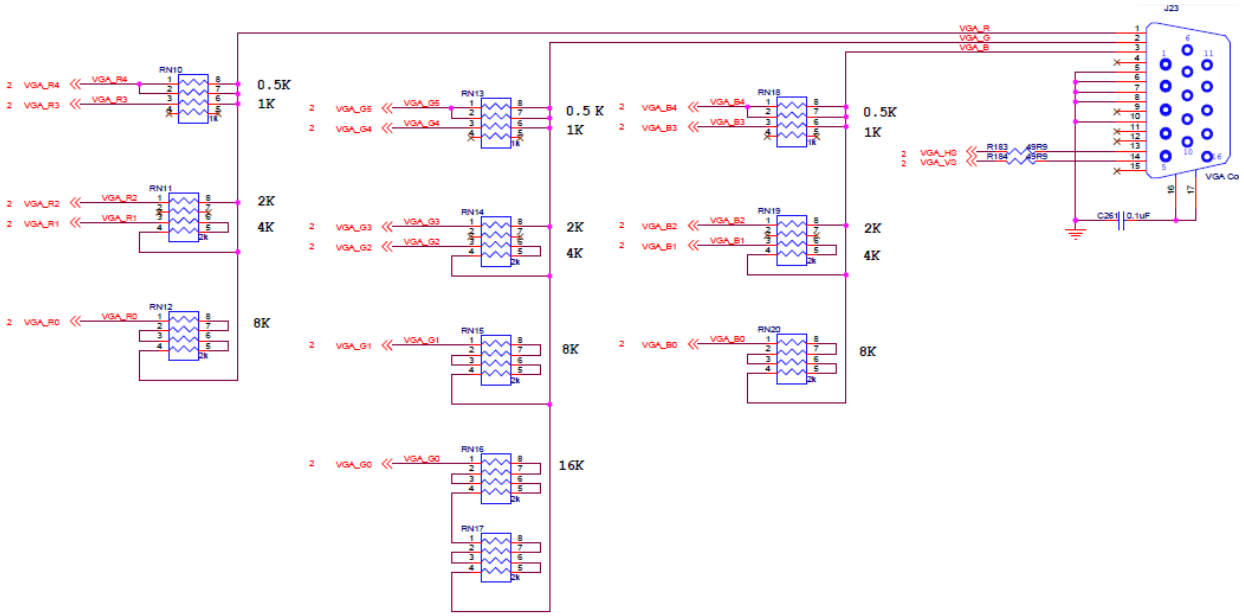


Figure 10-1: VGA Hardware Design

Figure 10-2 shows the VGA interface onboard.

Figure 10-2 VGA Interface Onboard

Pin Assignment of VGA Interface.

Net Name	FPGA PIN	Remark
VGA_D<0>	P7	BLUE<0>
VGA_D<1>	M7	BLUE<1>
VGA_D<2>	P8	BLUE<2>
VGA_D<3>	N8	BLUE<3>
VGA_D<4>	L7	BLUE<4>

VGA_D<5>	M9	GREEN<0>
VGA_D<6>	N9	GREEN<1>
VGA_D<7>	P9	GREEN<2>
VGA_D<8>	L10	GREEN<3>
VGA_D<9>	M10	GREEN<4>
VGA_D<10>	P11	GREEN<5>
VGA_D<11>	M11	RED<0>
VGA_D<12>	M12	RED<1>
VGA_D<13>	L12	RED<2>
VGA_D<14>	N14	RED<3>
VGA_D<15>	M13	RED<4>
VGA_HS	M14	Horizontal sync signal
VGA_VS	L13	Vertical sync signal

11. SD Socket

SD card is a very popular storage device now, in AX309 board a Micro SD socket is designed for SD card access. FPGA uses the SPI interface to read or write the SD card in AX309. The hardware design of SD socket is showed as Figure 11-1.

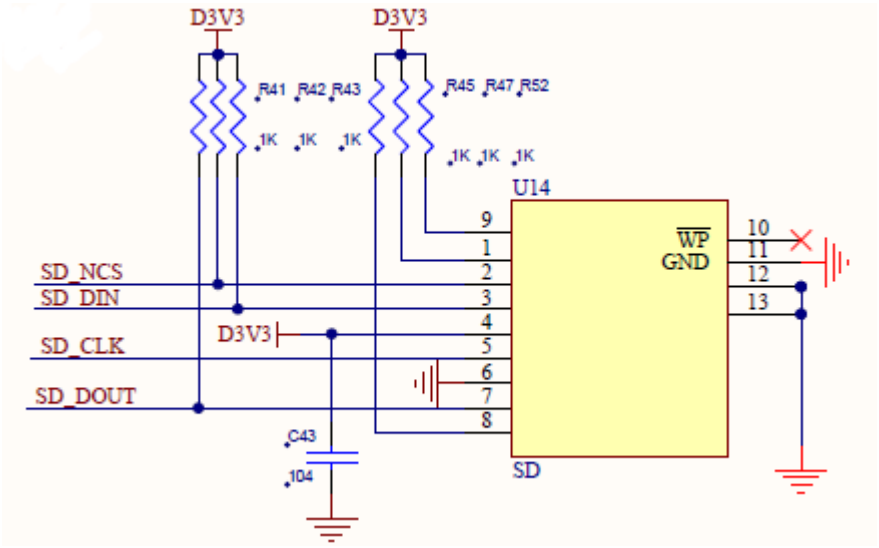


Figure 11-1 SD Socket Design

Figure 11-2 is the SD socket onboard.

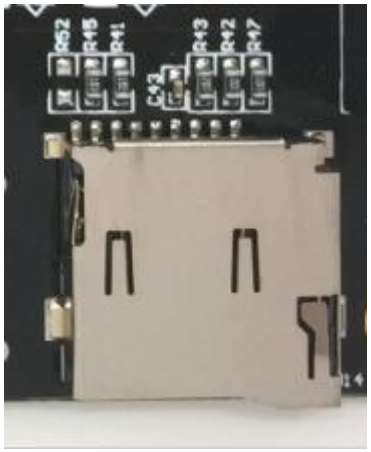


Figure 11-2 SD Socket Onboard

Pin Assignment of SD Socket.

SPI Mode	
Net Name	FPGA PIN
SD_NCS	N3
SD_DIN	L5
SD_CLK	M3
SD_DOUT	L4

12. LED

The board provides 4 onboard RED LEDs. These RED LEDs will light on when high voltage is output from FPGA IO. The design of LEDs is showed as Figure 12-1.

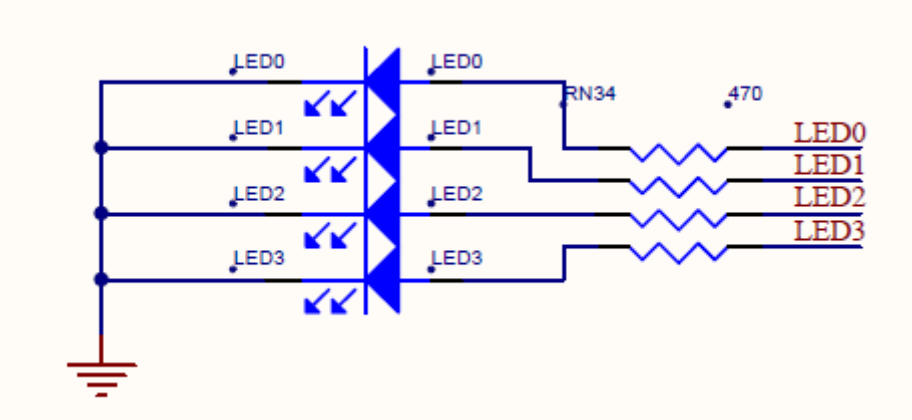


Figure 12-1 LEDs Design

Figure 12-2 is the LEDs onboard.

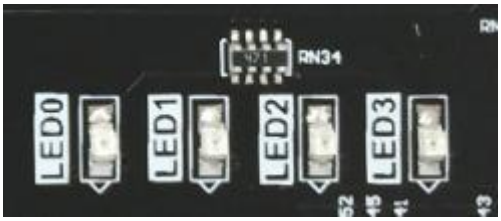


Figure 12-2 4 LEDs Onboard

Pin Assignment of LEDs：

Net Name	FPGA PIN
LED<0>	P4
LED<1>	N5
LED<2>	P5
LED<3>	M6

13. Buttons

The board has six buttons, it includes four user keys (KEY1~KEY4) and two special buttons (PROG and RESET). Signal of KEY1 ~ KEY4 is low voltage when KEY1~KEY4 button is pressed down. The hardware design of the four user keys is shown in Figure 13-1

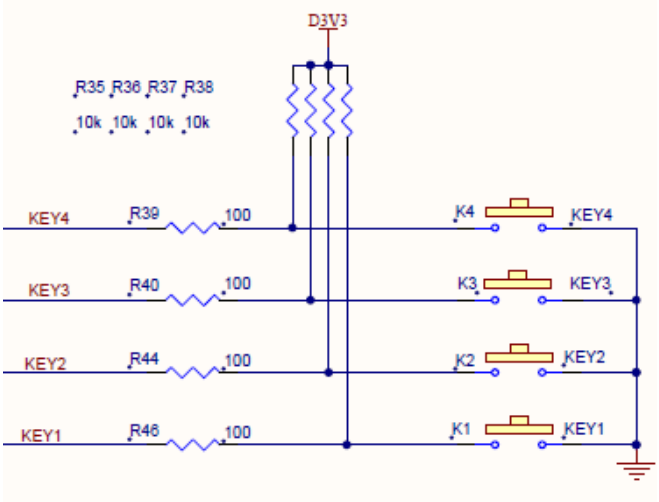


Figure 13-1 Design of User Buttons

There are two buttons for special function, one is for RESET function and another is for CONFIG function. The RESET button is connected to FPGA IO and the CONFIG button is connected to PROGRAM pin of FPGA. The hardware design of these two special buttons is shown in Figure 13-2

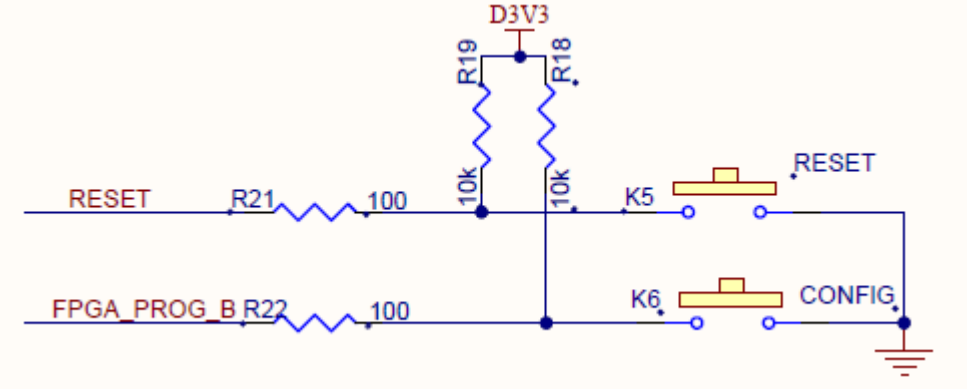


Figure 13-2 Design of Special Buttons

Figure 13-3 is the six buttons onboard.

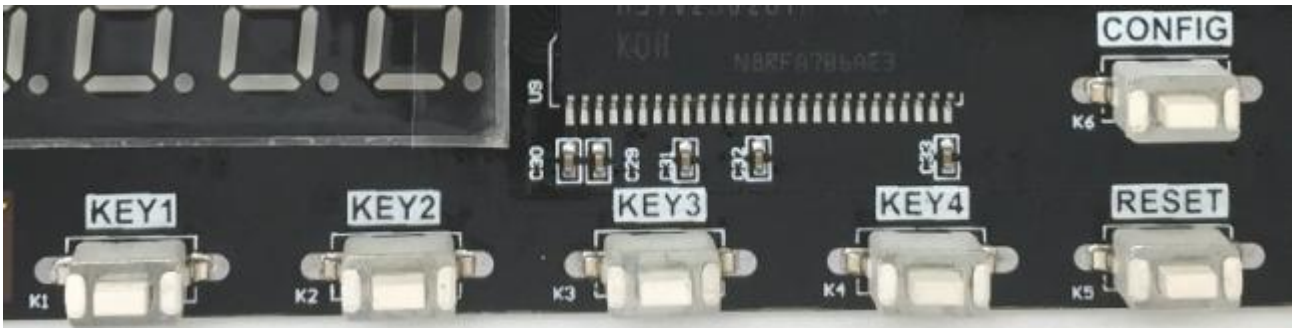


Figure 13-3 Six Button Onboard

Pin Assignment of Buttons.

Net Name	FPGA PIN
KEY1	C3
KEY2	D3
KEY3	E4
KEY4	E3
RESET	L3
PROG	T2

14. Camera Port

The AX309 board contains a 18 pin CMOS camera connector, it can connect to OV5640 camera module to capture video image. Please purchase OV5640 camera module from ALINX Taobao shop if you want to do experiment of video image process. The CMOS camera interface is designed as Figure 14-1:

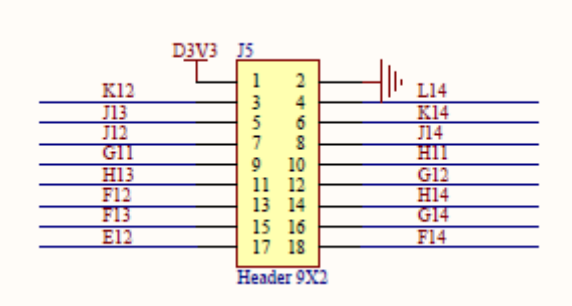


Figure 14-1 CMOS Camera interface

The Camera interface is showed as Figure 14-2.(OV5640 Camera Module is required be purchase separately)

Figure 14-2 Camera Interface With OV5640 module

Pin Assignment of CMOS Camera Interface.

J5	Net Name	FPGA 引脚
3	CMOS_SCLK	K12
4	CMOS_SDAT	L14
5	CMOS_VSYNC	J13
6	CMOS_HREF	K14
7	CMOS_PCLK	J12
8	CMOS_XCLK	J14
9	CMOS_D<7>	G11
10	CMOS_D<6>	H11
11	CMOS_D<5>	H13
12	CMOS_D<4>	G12

13	CMOS_D<3>	F12
14	CMOS_D<2>	H14
15	CMOS_D<1>	F13
16	CMOS_D<0>	G14
17	CMOS_RESET	E12
18	CMOS_PWDN	F14

15. 7-segment displays

The AX309 board has six 7-segment displays which are paired to display numbers in various sizes. Each segment in a display is indexed from A to G, with corresponding positions given in Figure 15-1.

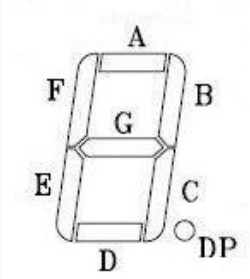


Figure 15-1 Segment Index

Figure 15-2 shows the connection of seven segments (common anode) to pins on FPGA. The segment can be turned on or off by applying a low logic level or high logic level from the FPGA, respectively.

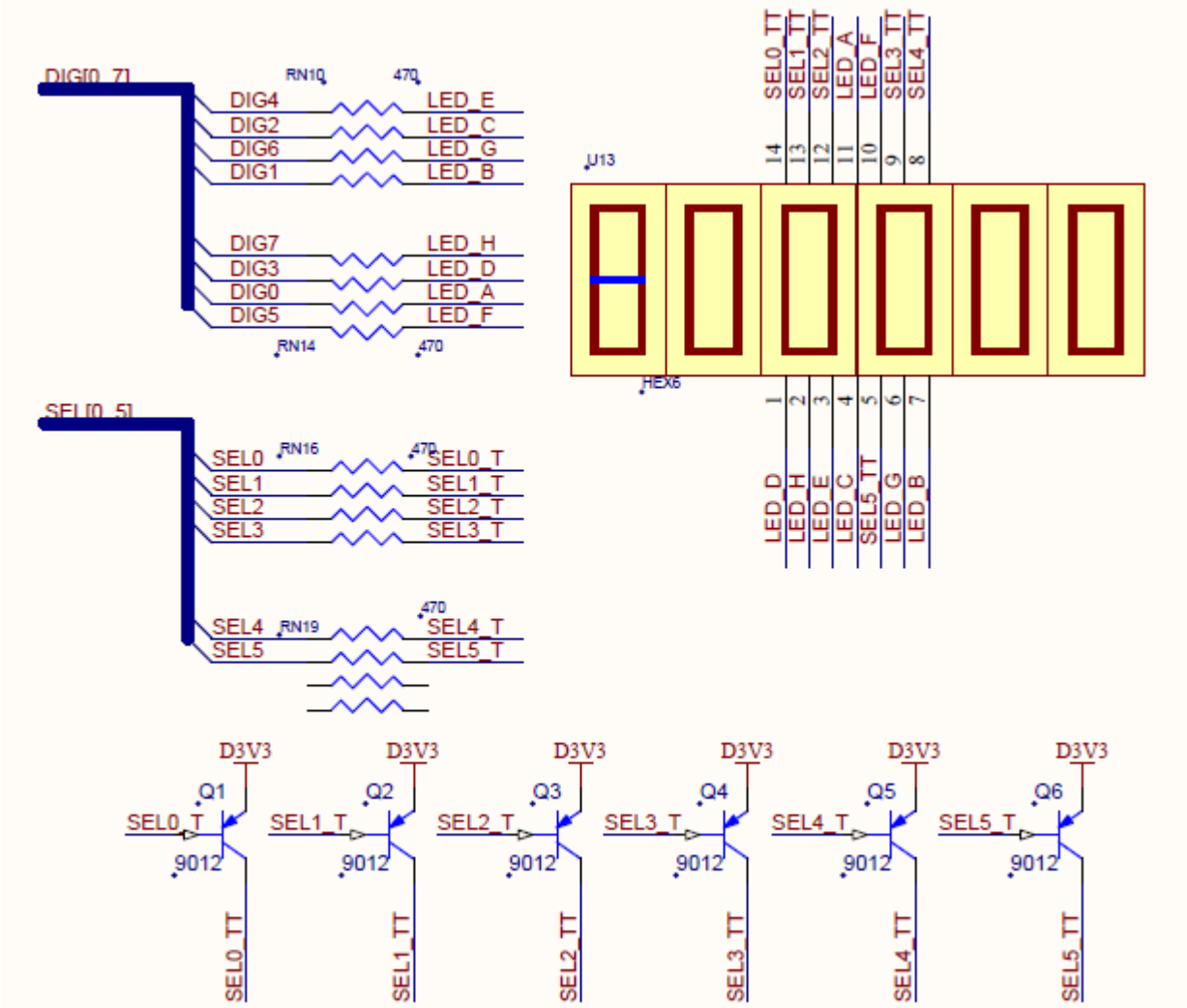


Figure 15-2 Hardware Design of Seven Segments

Figure 15-3 is the Seven Segments on board

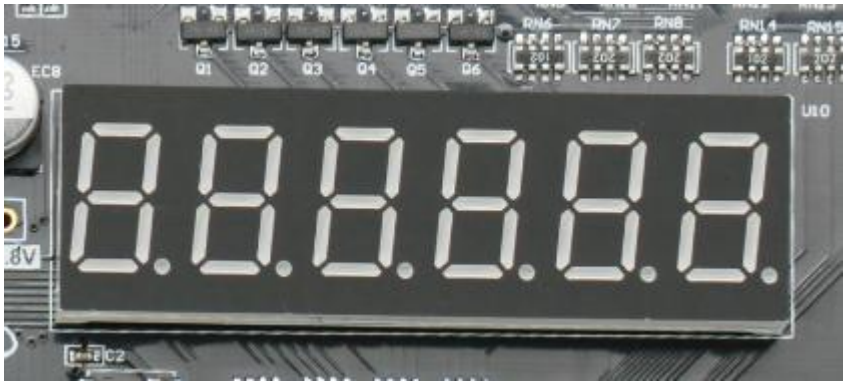


Figure 15-3 Seven Segments on board

Following table shows the pin assignment of FPGA to the 7-segment displays.

Net Name	FPGA PIN	Description
DIG[0]	C7	Seven Segment Digit A

DIG[1]	E6	Seven Segment Digit B
DIG[2]	C5	Seven Segment Digit C
DIG[3]	F7	Seven Segment Digit D
DIG[4]	D6	Seven Segment Digit E
DIG[5]	E7	Seven Segment Digit F
DIG[6]	D5	Seven Segment Digit G
DIG[7]	C6	Seven Segment Digit DP
SEL[0]	D8	#1 Segments Select
SEL[1]	E8	#2 Segments Select
SEL[2]	F9	#3 Segments Select
SEL[3]	F10	#4 Segments Select
SEL[4]	E10	#5 Segments Select
SEL[5]	D9	#6 Segments Select

16. Buzzer

The board has one buzzer which is mainly used for prompt or alarm. the buzzer is controlled by a transistor, when FPGA output a low signal, the buzzer will on and sound, when FPGA output a high signal, the buzzer will off. The hardware design of buzzer is showed as Figure 16-1:

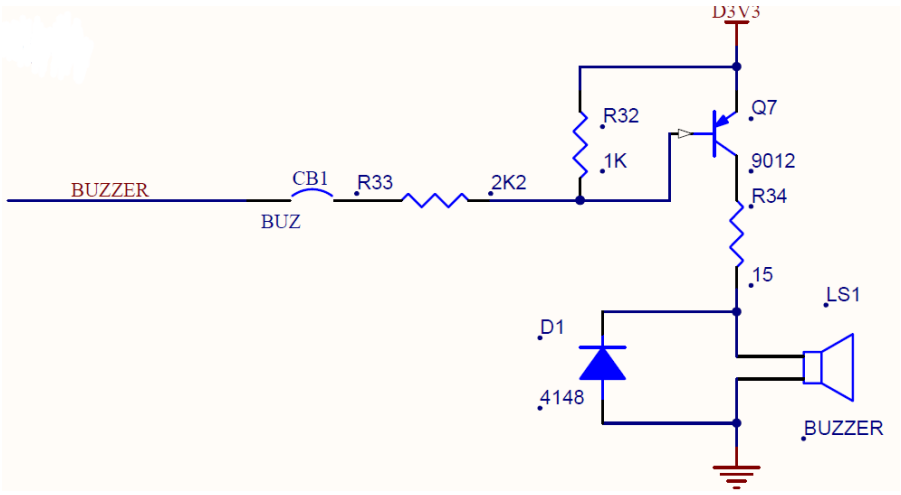


Figure 16-1 Hardware Design of buzzer

Figure 16-2 is showed the buzzer onboard, we can disable the buzzer by removing the

jumper cap of CB1.

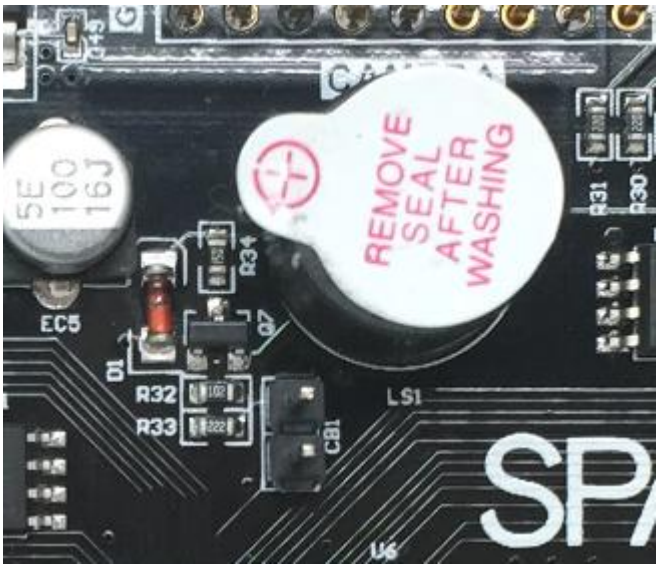


Figure 16-2 Buzzer Onboard

Pin Assignment of Buzzer：

Net Name	FPGA PIN
BUZZER	J11

17. GPIO Expansion Headers

The AX309 Board provides 40-pin expansion header. The header connects directly to 34 pins of the Spartan6 FPGA, and also provides +5.0V (VCC), +3.3V and GND.

The FPGA IO pins on the expansion headers is connected to a 33ohm resistor for protection against high or low voltage level. Figure 17-1 and Figure 17-2 shows the connection circuitry of these two 40-pin expansion headers.

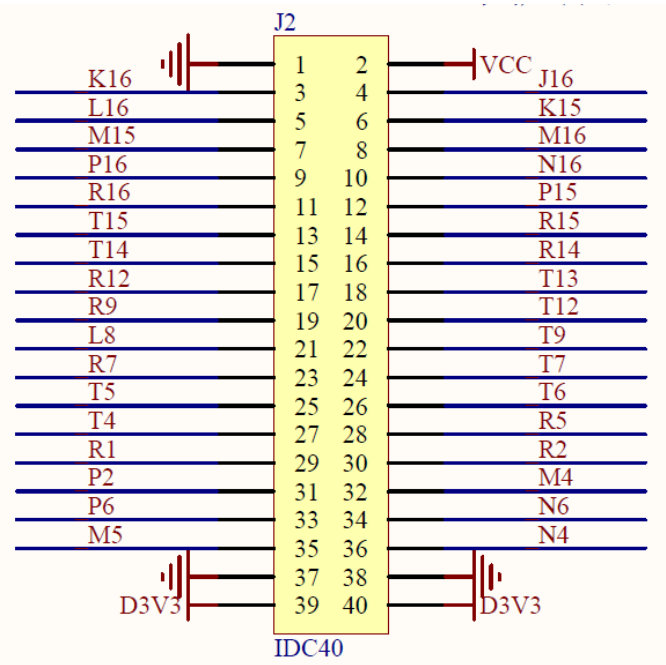


Figure 17-1 J2 Expansion Headers

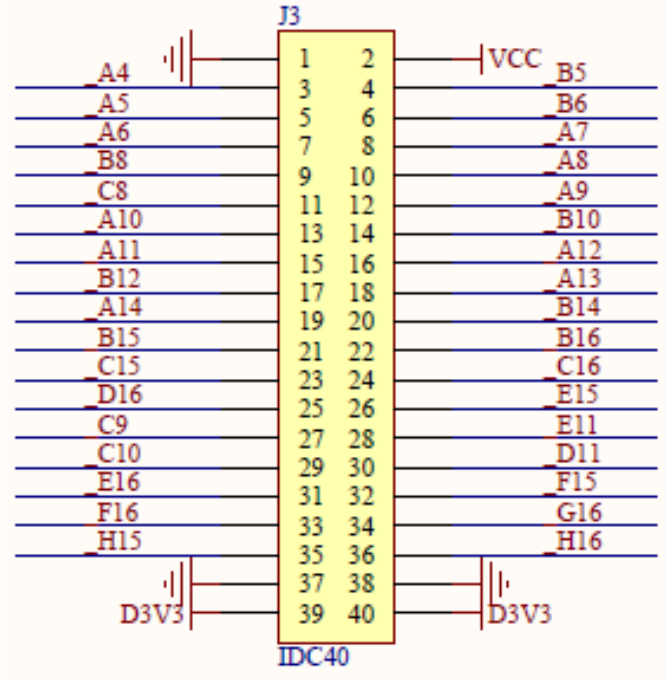


Figure 17-3 J3 Expansion Headers

Figure 17-3 is the header of J2 and J3 on AX309 board, the Pin1, Pin2 and Pin39,Pin40 of connector is marked on PCB board.

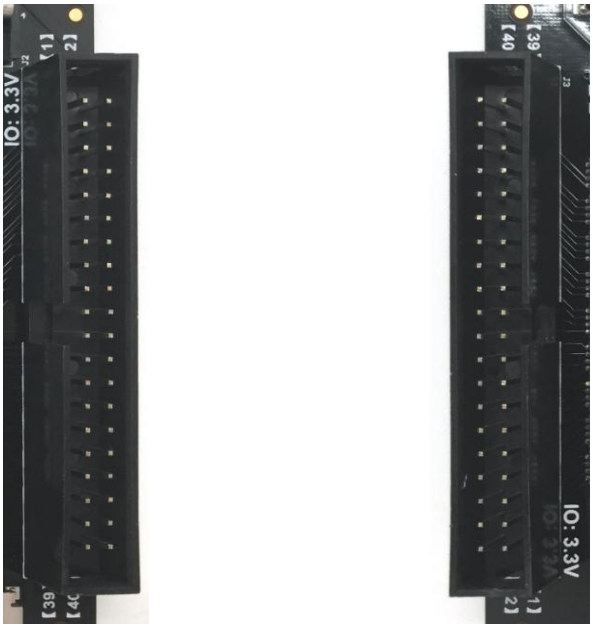


Figure 17-3 J2, J3 Connector Onboard

Expansion Header of AX309 can use to connect ALINX module to expand the additional function, for example connect to LCD module or ADDA module as Figure 17-4.

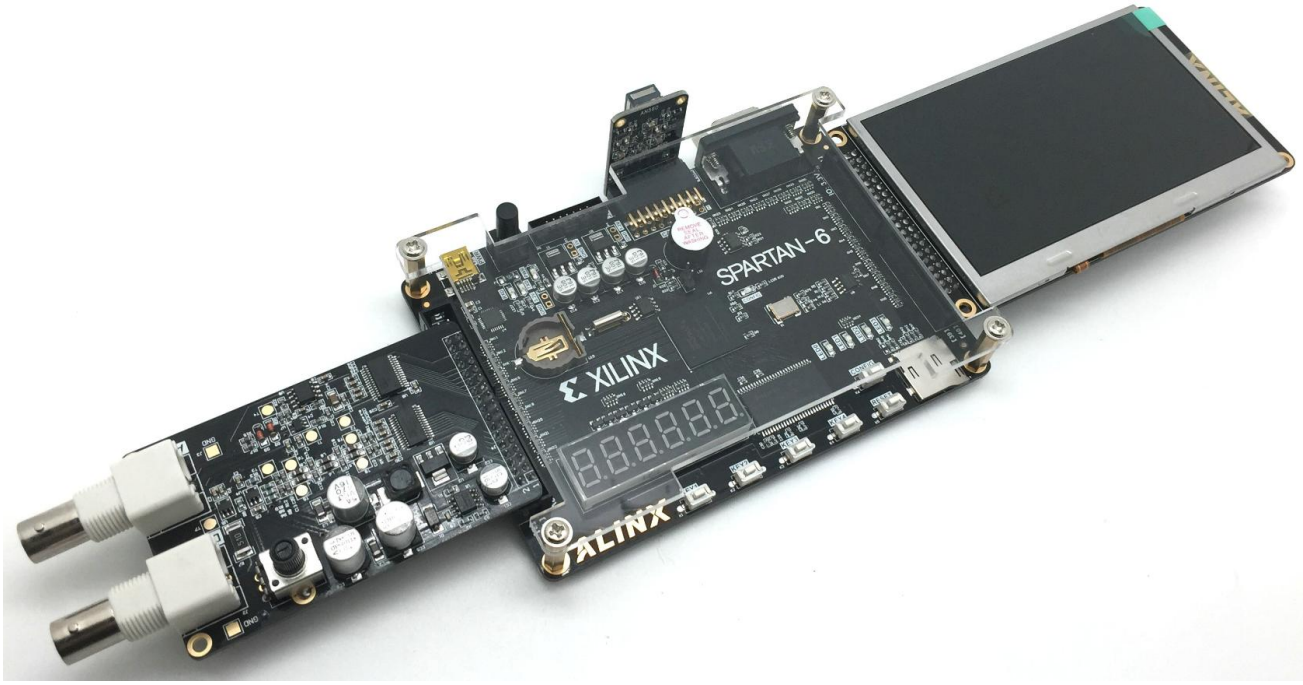


Figure 17-4. Header Connection

Pin Assignment of J2.

J2 PIN	FPGA PIN	J2 PIN	FPGA PIN
1	GND	**2**	VCC5V
3	K16	**4**	J16

5	L16	**6**	K15
7	M15	**8**	M16
9	P16	**10**	N16
11	R16	**12**	P15
13	T15	**14**	R15
15	T14	**16**	R14
17	R12	**18**	T13
19	R9	**20**	T12
21	L8	**22**	T9
23	R7	**24**	T7
25	T5	**26**	T6
27	T4	**28**	R5
29	R1	**30**	R2
31	P2	**32**	M4
33	P6	**34**	N6
35	M5	**36**	N4
37	GND	**38**	GND
39	D3V3	**40**	D3V3

Pin Assignment of J3

J3 PIN	FPGA PIN	J3 PIN	FPGA PIN
1	GND	**2**	VCC5V
3	A4	**4**	B5
5	A5	**6**	B6
7	A6	**8**	A7
9	B8	**10**	A8
11	C8	**12**	A9
13	A10	**14**	B10
15	A11	**16**	A12
17	B12	**18**	A13
19	A14	**20**	B14
21	B15	**22**	B16

23	C15	**24**	C16
25	D16	**26**	E15
27	C9	**28**	E11
29	C10	**30**	D11
31	E16	**32**	F15
33	F16	**34**	G16
35	H15	**36**	H16
37	GND	**38**	GND
39	D3V3	**40**	D3V3