EE-475L: Computer Architecture

Lab Report

Submitted by

Ali Imran 2018-EE-62

Submitted to

Mr. Umer Shahid

Department of Electrical Engineering

University of Engineering and Technology, Lahore, Pakistan

Task 1

For half adder, we have got the following design code.

```
module half_adder #(
    parameter Width=2
) (
    input [Width-1:0] A,B,
    output [Width-1:0] S,output C
);

   xor a1(S[0],A[0],B[0]);
   and a2(X,A[0],B[0]);

   xor a3(S[1],A[1],B[1],X);
   xor a6(Z,A[1],B[1]);
   and a4(Y,A[1],B[1]);

   and a8(I,X,Z);

   or a5(C,I,Y);

   initial begin
       $dumpfile("dump.vcd");
       $dumpvars;
   end

endmodule
```

Listing 1. Half Adder Verilog Code

For testing our code, cocotb has been used along with iverilog and the testbench has been written in python.

```
import cocotb
from cocotb import triggers
from cocotb.triggers import Timer
import random
import logging

@cocotb.test()
async def half_adder_test(dut):
    for i in range(4):
        for j in range(4):
            dut.A.value = i
            dut.B.value = j
```

```
            await triggers.Timer(2,"ns")
```

Listing 2. Half Adder Testbench code

For the above test bench we get the following output.

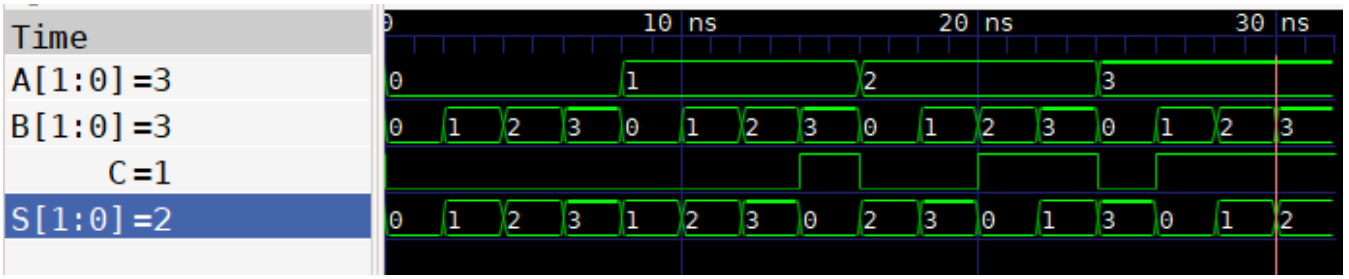

Figure 1. Output Waveform for Half Adder

From the synthesis report we get the following information.

Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
A[0]	C	5.357	SLOW	2.072	FAST
A[0]	S[0]	5.335	SLOW	2.073	FAST
A[0]	S[1]	5.335	SLOW	2.073	FAST
A[1]	C	5.327	SLOW	2.076	FAST
A[1]	S[1]	5.335	SLOW	2.073	FAST
B[0]	C	5.359	SLOW	2.071	FAST
B[0]	S[0]	5.335	SLOW	2.073	FAST
B[0]	S[1]	5.335	SLOW	2.073	FAST
B[1]	C	5.361	SLOW	2.074	FAST
B[1]	S[1]	5.335	SLOW	2.073	FAST

Figure 2. Combinational Delays

Following design utilization summary has been obtained.

Resource	Utilization	Available	Utilization %
LUT	2	63400	0.00
IO	7	210	3.33

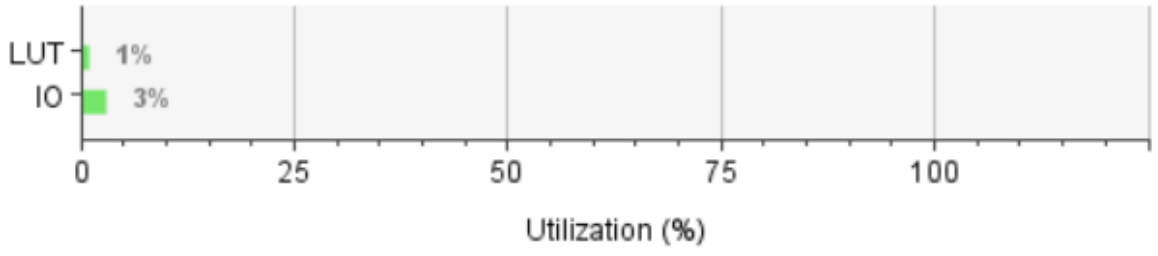

Figure 3. Design Utilization Summary

Following timing summary is obtained.

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	3	Total Number of Endpoints:	3	Total Number of Endpoints:	NA

Figure 4. Timing Summary

Following power summary has been obtained.

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.462 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**31.7°C**
Thermal Margin:	53.3°C (11.6 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

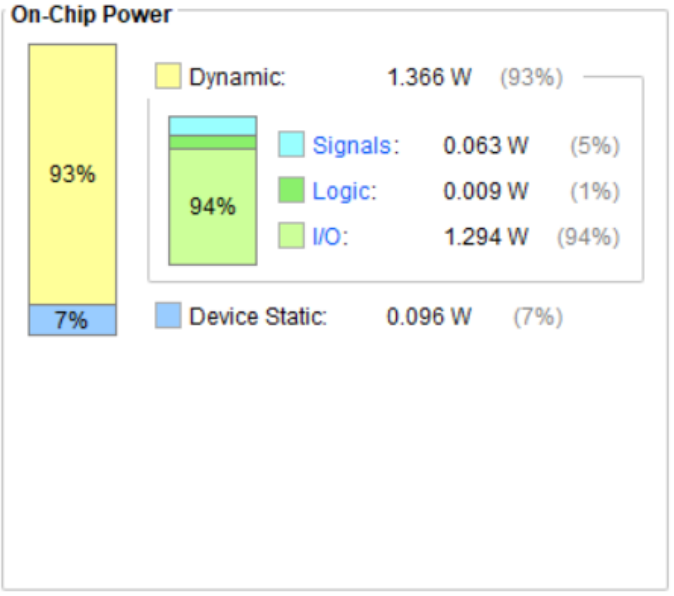

Figure 5. Power Summary

Task 2

For full adder, we have got the following design code which is calling the half adder code from Listing 1.

```
`include "half_adder.sv"
module full_adder #(
    parameter Width=2
) (
    input [Width-1:0] A,B,C_in,
    output [Width-1:0] S,output C_out
);

    wire [1:0] X;
    wire Y,Z;

    half_adder a1 (.A(C_in),.B(X),.S(S),.C(Y));
    half_adder a2(.A(A),.B(B),.S(X),.C(Z));

    or a3(C_out,Y,Z);
```

```
    initial begin
        $dumpfile("dump.vcd");
        $dumpvars;
    end

endmodule
```

Listing 3. Full Adder Verilog Code

For testing our code, cocotb has been used along with iverilog and the testbench has been written in python.

```
import cocotb
from cocotb import triggers
from cocotb.triggers import Timer
import random
import logging

@cocotb.test()
async def half_adder_test(dut):
    for i in range(4):
        for j in range(4):
            for k in range(2):
                dut.A.value = i
                dut.B.value = j
                dut.C_in.value = k
                await triggers.Timer(2,"ns")
                dut._log.info("A = %d, B = %d, C_in = %d, C_out = %d, S =
%d",i,j,k,int(dut.C_out.value),int(dut.S.value))
```

Listing 4. Full Adder Testbench code

For the above test bench we get the following output.

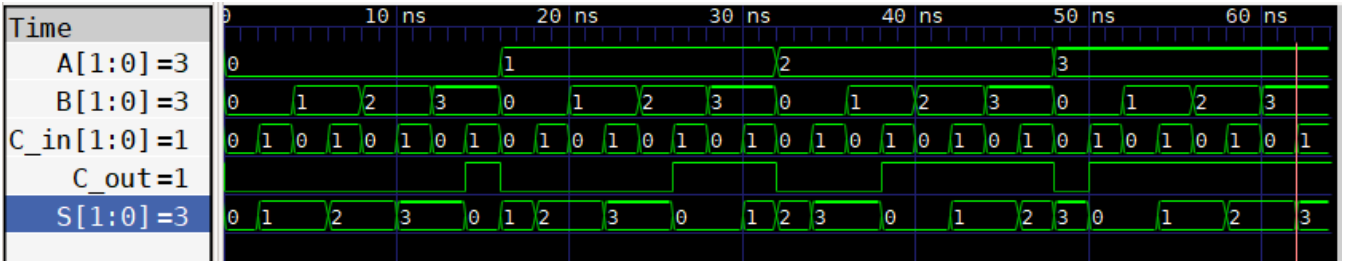

Figure 6. Output Waveform for Full Adder

From the synthesis report we get the following information.

Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
A[0]	C_out	5.335	SLOW	2.073	FAST
A[0]	S[0]	5.335	SLOW	2.073	FAST
A[0]	S[1]	5.335	SLOW	2.073	FAST
A[1]	C_out	5.335	SLOW	2.073	FAST
A[1]	S[1]	5.335	SLOW	2.073	FAST
B[0]	C_out	5.335	SLOW	2.073	FAST
B[0]	S[0]	5.335	SLOW	2.073	FAST
B[0]	S[1]	5.335	SLOW	2.073	FAST
B[1]	C_out	5.335	SLOW	2.073	FAST
B[1]	S[1]	5.335	SLOW	2.073	FAST
C_in[0]	C_out	5.335	SLOW	2.073	FAST
C_in[0]	S[0]	5.335	SLOW	2.073	FAST
C_in[0]	S[1]	5.335	SLOW	2.073	FAST
C_in[1]	C_out	5.335	SLOW	2.073	FAST
C_in[1]	S[1]	5.335	SLOW	2.073	FAST

Figure 7. Combinational Delays

Following design utilization summary has been obtained.

Resource	Utilization	Available	Utilization %
LUT	3	63400	0.00
IO	9	210	4.29

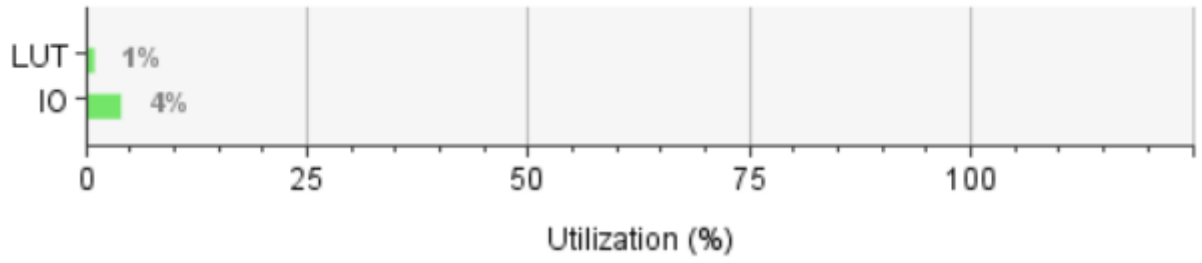

Figure 8. Design Utilization Summary

Following timing summary is obtained.

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	3	Total Number of Endpoints:	3	Total Number of Endpoints:	NA

Figure 9. Timing Summary

Following power summary has been obtained.

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.785 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**33.1°C**
Thermal Margin:	51.9°C (11.2 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

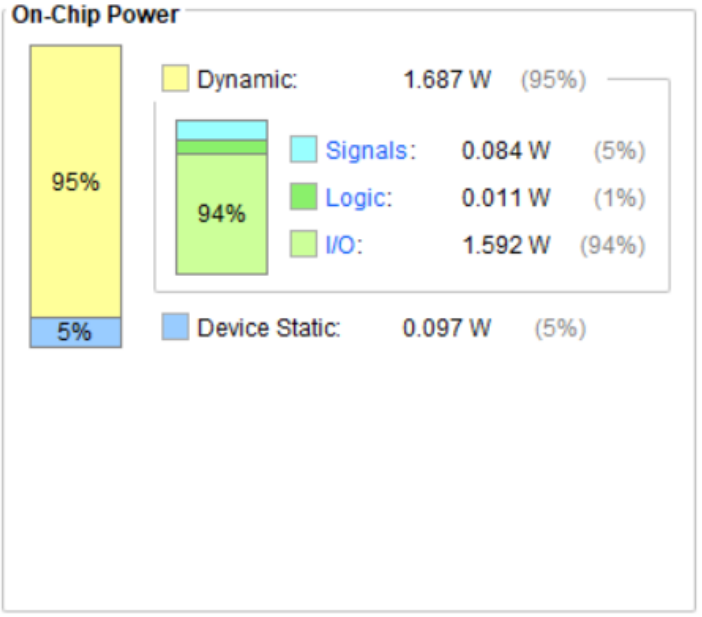

Figure 10. Power Summary

Task 3

For the multiplier, we have got the following design code.

```
module mul4x4 #(
    parameter Width = 4
) (
    input [Width-1:0] A, B,
    output reg [2*Width-1:0] R
);
    reg [Width-1:0] X1,X2,X3,X0;
    reg [2*Width-1:0] Y1,Y2,Y3,Y0;
    always @(*) begin
        X0 = A & {Width{B[0]}};
        X1 = A & {Width{B[1]}};
        X2 = A & {Width{B[2]}};
        X3 = A & {Width{B[3]}};
    end

    always @(*) begin
        Y0 = {4'b0000,X0};
        Y1 = {3'b0000,X1,1'b0};
        Y2 = {2'b0000,X2,2'b0};
        Y3 = {1'b0000,X3,3'b0};

        R = Y0 + Y1 + Y2 + Y3;
    end

    initial begin
```

```
        $dumpfile("dump.vcd");
        $dumpvars;
    end

endmodule
```

Listing 5. Multiplier Verilog Code

For testing our code, cocotb has been used along with iverilog and the testbench has been written in python.

```
import cocotb
from cocotb import triggers
from cocotb.triggers import Timer
import random
import logging

@cocotb.test()
async def mu4x4_test(dut):
    dut.A <= 15
    dut.B <= 15
    await triggers.Timer(2,'ns')

    dut.A <= 2
    dut.B <= 3
    await triggers.Timer(2,'ns')

    dut.A <= 8
    dut.B <= 9
    await triggers.Timer(2,'ns')
```

Listing 6. Multiplier Testbench code

For the above test bench we get the following output.

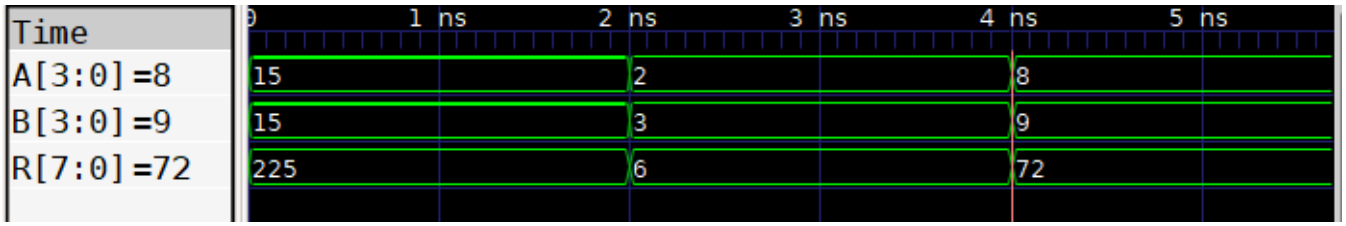

Figure 11. Output Waveform for Multiplier

From the synthesis report we get the following information.

Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
A[0]	R[0]	5.762	SLOW	2.205	FAST
A[0]	R[1]	5.941	SLOW	2.201	FAST
A[0]	R[2]	6.091	SLOW	2.201	FAST
A[0]	R[3]	6.454	SLOW	2.202	FAST
A[0]	R[4]	6.672	SLOW	2.297	FAST
A[0]	R[5]	6.781	SLOW	2.333	FAST
A[0]	R[6]	6.699	SLOW	2.311	FAST
A[0]	R[7]	6.459	SLOW	2.222	FAST
A[1]	R[1]	5.744	SLOW	2.201	FAST
A[1]	R[2]	6.132	SLOW	2.201	FAST
A[1]	R[3]	6.454	SLOW	2.239	FAST
A[1]	R[4]	6.694	SLOW	2.299	FAST
A[1]	R[5]	6.867	SLOW	2.335	FAST
A[1]	R[6]	7.026	SLOW	2.201	FAST
A[1]	R[7]	6.802	SLOW	2.184	FAST
A[2]	R[2]	5.763	SLOW	2.201	FAST
A[2]	R[3]	6.326	SLOW	2.239	FAST
A[2]	R[4]	6.672	SLOW	2.299	FAST
A[2]	R[5]	6.867	SLOW	2.335	FAST
A[2]	R[6]	7.026	SLOW	2.201	FAST
A[2]	R[7]	6.802	SLOW	2.184	FAST
A[3]	R[3]	5.772	SLOW	2.202	FAST
A[3]	R[4]	6.629	SLOW	2.205	FAST
A[3]	R[5]	6.867	SLOW	2.201	FAST
A[3]	R[6]	7.026	SLOW	2.201	FAST
A[3]	R[7]	6.802	SLOW	2.184	FAST
B[0]	R[0]	5.762	SLOW	2.205	FAST
B[0]	R[1]	5.941	SLOW	2.201	FAST
B[0]	R[2]	6.099	SLOW	2.201	FAST
B[0]	R[3]	6.166	SLOW	2.202	FAST
B[0]	R[4]	6.282	SLOW	2.205	FAST
B[0]	R[5]	6.391	SLOW	2.201	FAST
B[0]	R[6]	6.442	SLOW	2.245	FAST
B[0]	R[7]	6.218	SLOW	2.182	FAST
B[1]	R[1]	5.744	SLOW	2.201	FAST
B[1]	R[2]	6.091	SLOW	2.201	FAST
B[1]	R[3]	6.454	SLOW	2.202	FAST
B[1]	R[4]	6.672	SLOW	2.297	FAST
B[1]	R[5]	6.867	SLOW	2.333	FAST
B[1]	R[6]	7.026	SLOW	2.201	FAST
B[1]	R[7]	6.802	SLOW	2.184	FAST
B[2]	R[2]	5.763	SLOW	2.201	FAST
B[2]	R[3]	6.454	SLOW	2.239	FAST
B[2]	R[4]	6.728	SLOW	2.299	FAST
B[2]	R[5]	6.867	SLOW	2.335	FAST
B[2]	R[6]	7.026	SLOW	2.201	FAST
B[2]	R[7]	6.802	SLOW	2.184	FAST
B[3]	R[3]	6.326	SLOW	2.428	FAST
B[3]	R[4]	6.672	SLOW	2.439	FAST
B[3]	R[5]	6.867	SLOW	2.427	FAST
B[3]	R[6]	7.026	SLOW	2.201	FAST
B[3]	R[7]	6.802	SLOW	2.184	FAST

Figure 12. Combinational Delays

Following design utilization summary has been obtained.

Resource	Utilization	Available	Utilization %
LUT	16	63400	0.03
IO	16	210	7.62

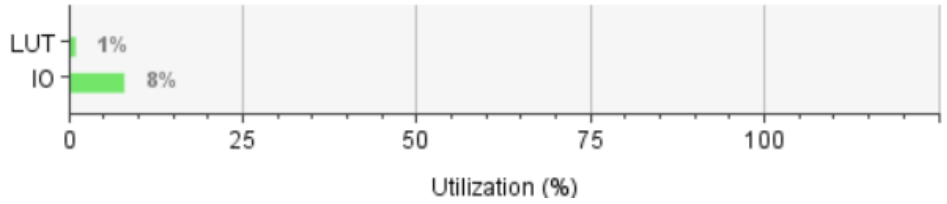

Figure 13. Design Utilization Summary

Following timing summary is obtained.

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	8	Total Number of Endpoints:	8	Total Number of Endpoints:	NA

Figure 14. Timing Summary

Following power summary has been obtained.

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**4.749 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**46.7°C**
Thermal Margin:	38.3°C (8.3 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

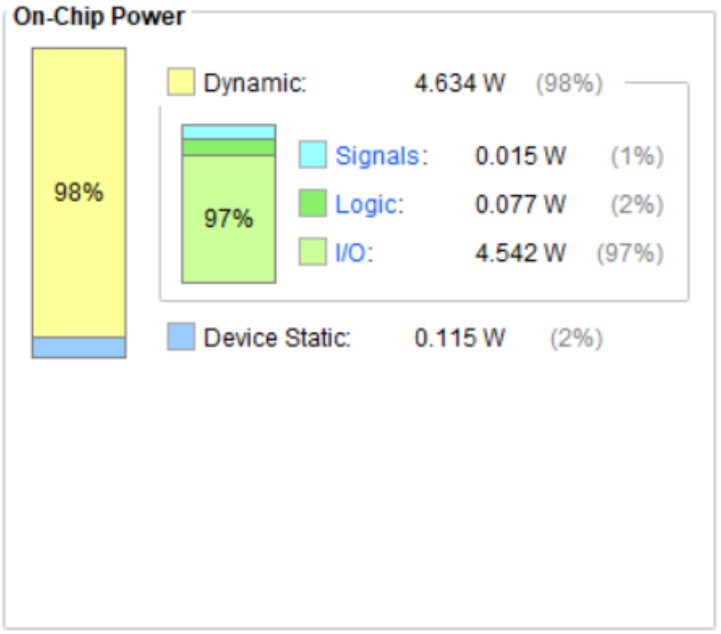

Figure 15. Power Summary