14-nm FinFET Technology for Analog and RF Applications

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***Abstract*— This paper describes the features and performance of an analog and RF device technology development on a 14-nm logic FinFET platform. An optimized single-side gate contact RF device layout shows a F_t/F_{max} of 314/180 GHz and 285/140 GHz for *N* and PFinFET device, respectively. The double-side gate contact structure with contact on either end of active gate enhances the peak F_{max} performance to 227 and 195 GHz for both *N* and PFinFET devices, respectively. A significant boost in the PFinFET RF performance is observed compared to 28-nm planar PFET, which is attributed to the source/drain SiGe epitaxy stressor that results in higher hole carrier mobility. On the other hand, the thin channel body of FinFET structure facilitates a better electrostatic control of gate over the channel region and hence suppresses short channel effects including the drain-induced barrier lowering. Consequently, a significantly higher self-gain (G_m/G_{ds}) 40 and 34 for both NFinFET and PFinFET is achieved. In addition, N/PFinFETs demonstrate superior 1/f noise of 17/35 $fV^2\mu m^2$/Hz at 1 kHz compared to 171/106 $fV^2\mu m^2$/Hz of 28-nm planar N/PFETs. To extend the low-voltage operation and power saving of FinFET RF platform, ultralow V_t N/PFinFETs in the range of 50 mV V_ts are also developed. Furthermore, a deep n-well process is added to the platform to provide device and circuit isolation from substrate and supply noise, while realizing the creation of new devices such as vertical NPN, PCAP, and high breakdown voltage deep n-well junction diodes. Overall, a superior F_t/F_{max}, high self-gain, low 1/f noise, and robust substrate isolation characteristics extend the capability of this new 14-nm FinFET technology to the analog and RF circuit applications.**

***Index Terms*— 5G mobile communication, 14-nm and 28-nm technology, deep n-well isolation, FinFET, logic devices, RF CMOS, wireless communication.**

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I. Introduction

THE FinFET-based logic process technologies have been successfully put into production due to superior scalability, low-power, and high-performance benefits at 14-nm and 16-nm nodes [1]–[3]. With larger component counts in long-term evolution (LTE) phones and emerging sub-6-GHz 5G bands, area scaling is extremely important to accommodate all chipsets within cellphone from factors along with power scaling.

Developing RF and analog capability of the FinFET technology will help in realizing RF + Logic system on chip (SoC) to take advantage of logic power, performance, and area scaling of the advanced FinFET technology [4], [5]. Since design compatibility and low cost are important considerations for migration from the prior planar technology nodes, it is also critical in this paper to consider these factors while developing analog and RF capability in the FinFET technologies. On the other hand, an increasing rate of replacing the analog circuit functions using digitally assisted analog designs favor the 14-nm FinFET technology for its scaled footprint and existing rich digital design portfolio [6], [7]. Therefore, 14-nm FinFET-based optimized RF SoC designs are an attractive choice for designers in the <6-GHz RF application space.

II. 14-nm RF Technology Features

The 14-nm analog and RF technology is an extension of 14-nm based logic FinFET platform technology with V_{dd} (operational voltage) of 0.8 V for core (thin oxide) and 1.2, 1.5, and 1.8 V of input–output (I/O) (thick oxide) RF transistors. Table I shows a comparison of key device parameters of 14-nm core RF FinFET to 28-nm high-K metal gate planar [8] incumbent RF technology. The 14-nm FinFET devices show a clear benefit over 28-nm FETs in terms of drive current (I_d) and transconductance (G_m) for a given design footprint. To understand the intrinsic performance benefits of these devices across technologies a figure-of-merit $F_t.G_m/I_d$ is also shown in Table I.

A deep n-well process is also implemented to provide robust substrate isolation to microvolt level RF and analog signals. In this process, the deep n-well implant species go deeper into silicon compared to other n-well or p-well implants. The deep n-well junctions are formed with p-well (on upper edge of the deep n-well layer) and p-substrate (on the lower edge of the deep n-well layer) in the bulk silicon region below

TABLE I
COMPARISON OF KEY CORE DEVICE DESIGN AND DC/AC PARAMETERS

Technology	14nm FinFET		28nm planar FET (high-k metal gate)	
Device	NFinFET	PFinFET	NFET	PFET
L_{gate}[nm]	14		30	
CPP†[nm]	78		126	
V_{dd}[V]	0.8		1.05	
I_{dsat}[μA/μm]*¥	1523	1433	670	450
G_{msat}[μS/μm]*¥	3017	2748	985	395
F_t/F_{max}(GHz)	314/180	285/140	308/159	185/102
$F_t.G_m/I_d$[GHz/V]	2650	2053	2000	1150

Note: *Normalized to footprint W_{design}, †CPP: Contacted poly (gate) pitch
¥I_{dsat} and G_{msat} are measured at V_{dd}=0.8V

Fin structures. This provides the same performance including ideality and leakage as that of ideal bulk silicon junctions. The deep n-well implant profile is also being used to assist the formation of vertical NPN (VNPN), PCAP (p-type capacitor on a p-well with substrate isolation), and high-voltage p-n-junction diodes.

To extend the 14-nm technology device and circuit's operational capabilities in the 5 V and higher voltage domains, N/PLDFETs (laterally diffused field effect transistor) are successfully developed to simplify RF SoC designs [9]. In addition to these, the 14-nm technology platform offering includes back end of line devices such as alternate polarity metal–oxide–metal capacitors up to 3.3 V operation range, metal–insulator–metal capacitor, and metal precision resistors and inductors with an ultra-thick metal layer.

III. 14-NM RF FINFET DEVICE LAYOUT AND CROSS-SECTIONAL DETAILS

Fig. 1(a) shows a schematic layout of a single-side gate contact (SGC) RF FinFET. *x*- and *y*-direction cross-sectional transmission electron microscopy (TEM) views are shown in Fig. 1(b) and (c). In these cross sections, Fins are wrapped with the replacement metal gate (RMG) materials including high-k gate (HfO_2) oxide, work function, and low-resistance tungsten fills. Critical physical dimensions of the FinFET device technology such as Fin and poly pitch are listed in Table I with 28-nm planar FET parameters as a reference.

In the case of the 14-nm FinFET technology, the active area of devices is patterned in multifins with a 48-nm Fin pitch. In final device structure, the effective width (W_{eff}) of device corresponds to twice the Fin height plus Fin top width, which equals ~89 nm compared to equivalent planar 48-nm space as indicated in Fig. 1(b). It can be observed that the RMG wraps around Fins, as shown in Fig. 1(b), with a narrow space left in between Fins. This geometry causes vertical gate resistance to be high. In *y*-direction TEM view as well, due to tight gate pitch a short gate channel length at the 14-nm technology, a narrow space remains to fill with tungsten contact material post the high-k gate oxide and metal work-function deposition [Fig. 1(c)]. Thus, an overall gate resistance sees a dramatic rise at a scaled channel length and Fin pitch.

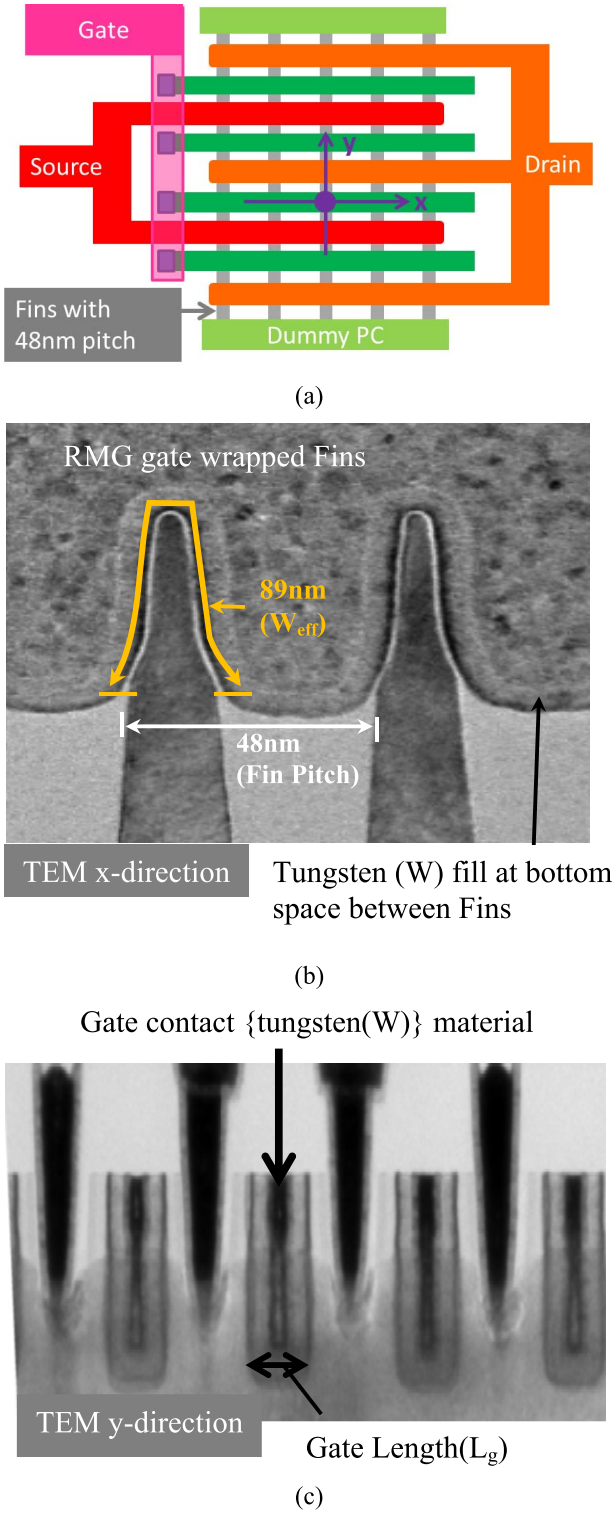


Fig. 1. 14-nm RF FinFET device. (a) Layout schematic. (b) TEM image along the *x*-axis with RMG wrapping Fins. (c) *y*-direction TEM image showing small volume of low resistance contact material fill inside a 14-nm channel length gate.

IV. 14-NM RF FINFET SILICON RESULTS

The cutoff frequency (F_t) and maximum oscillation frequency ($F_{\max}$) of 12-Fin N/PFinFETs have been extracted from S-parameters and are shown in Figs. 2 and 3, respectively.

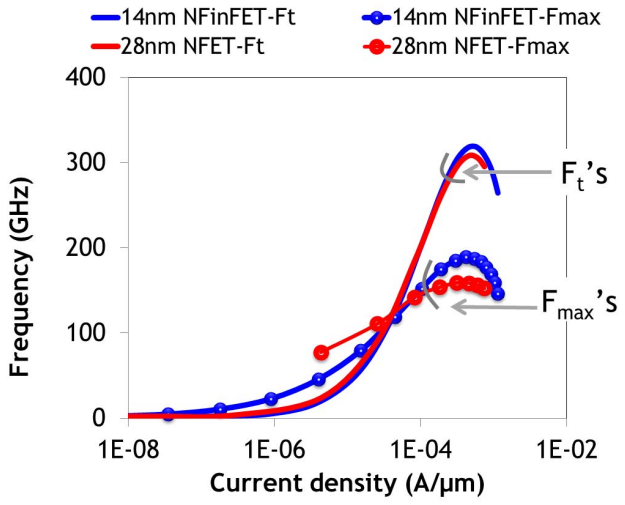


Fig. 2. Metal-1(m1) level cutoff frequency (F_t) and maximum oscillation frequency (F_{max}) versus current density (J_d) from a minimum channel length (L_g) = 14 nm and 12-Fin NFinFET device.

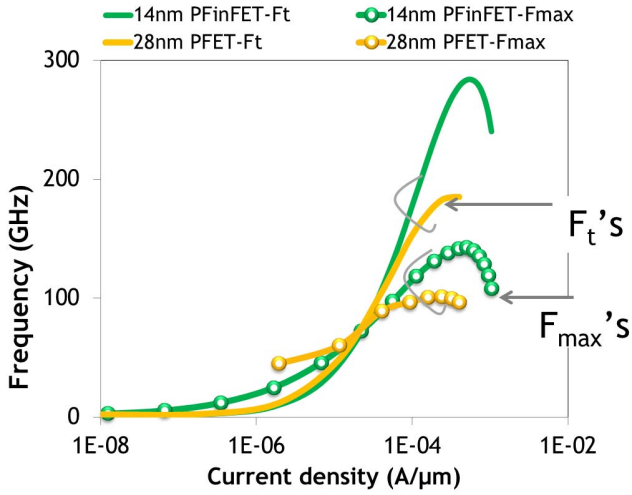


Fig. 3. Metal-1 level F_t and F_{max} versus current density (J_d) from a minimum channel length (L_g) 14-nm and 12Fin PFinFET device.

The pad and the interconnect parasitic have been eliminated by using open, short, and through de-embedding technique at metal-1 level [10] to accurately characterize the intrinsic device RF performance. It can be clearly seen that FinFET achieves higher peak F_t due to superior transconductance(G_m) than 28-nm planar FETs, as listed in Table I.

To have a quantitative comparison between 14-nm and 28-nm technologies, effective widths (W_{eff}) of FET devices equivalent to 1 μm are selected. In case of the 14-nm FinFET technology, 12 Fins give $W_{eff} = 1.068$ μm (12 $\times$ 89 nm Fin perimeter).

In Fig. 3, a significant F_t increase of PFinFET devices is also observed compare to previous node planar PFET devices and now for the first time, it is viewed as comparable to the F_t of NFinFET devices. In the 14-nm FinFETs processing, deep silicon cavities are formed post Fin silicon etch in the source/drain region of FinFET. In the following processing step, a boron-doped SiGe epitaxy stressor is grown in the

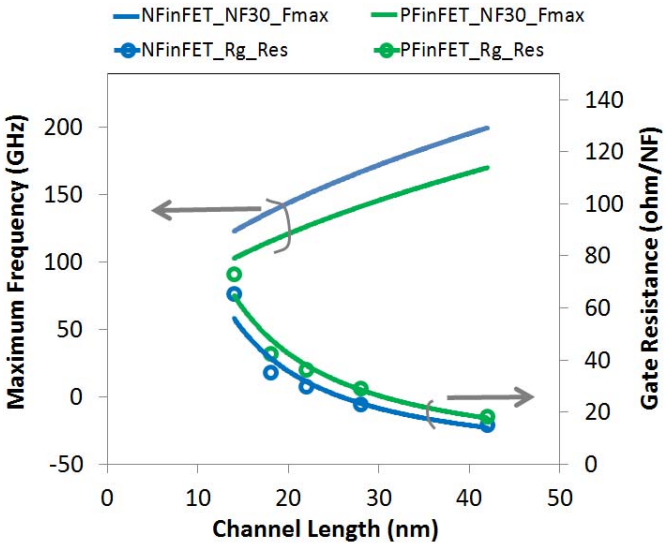


Fig. 4. Maximum oscillation frequency (F_{max}) and gate resistance (R_g) relationship with N/PFinFET channel length (L_g).

cavity space, which exert a compressive stress over the Fin channel region hence boost the overall hole carrier mobility. As a result, a significant increase in the device transconductance (G_m) is observed, which is implicitly reflected in the higher F_t (285 GHz) than that of the 28-nm planar PFETs (185 GHz). The F_{max} of both N and P FinFETs is also significantly higher compared to the 28-nm planar N and PFETs devices as shown in Table I. However, an adverse influence of the gate resistance is seen on the FinFET F_{max} performance (Fig. 4), but FinFET still maintains a higher performance owing to the significantly improved F_t and G_m. In a typical device scaling, the channel length of FET is reduced to get performance benefits; however, the gate resistance increases rapidly especially at channel length (L_g) $<$ 20 nm. This limits F_{max} performance in conjunction with the increased parasitics (gate to source and gate to drain) capacitance due to 3-D FinFET architecture and scaled poly pitch of an advanced technology node.

As discussed earlier in Section III, the gate resistance increases significantly at the 14-nm technology due to shorter channel length and Fin pitch. The overall percentage of low resistance tungsten fill material is decreased as certain thickness of barrier and work-function material deposition is necessitated in RMG gate-stack prior to tungsten fills. On the contrary, previous generation planar technology has longer channel length, which offers more y-direction space to fill with tungsten like low-resistance material. Therefore, a higher volume percentage ratio of the low resistance material is maintained at the shortest offered channel length ($L_g = 30$ nm).

Fig. 4 shows that FinFET with the longer channel length (L_g) improves the F_{max} despite having lower F_t. Therefore, a longer L_g device provides a higher F_{max} device option for RF circuit designs. To understand it more analytically, various parasitic resistance components associated with the FinFET gate wrap around structures are depicted in Fig. 5. The vertical gate resistance (R_{gv}) component is significantly

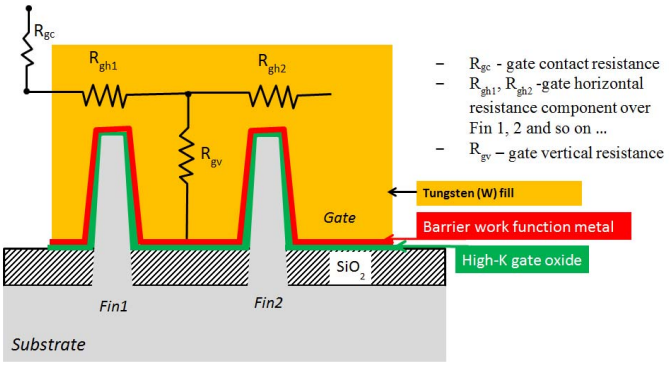


Fig. 5. Gate horizontal and vertical resistance component in the FinFET RMG wrap around gate structures.

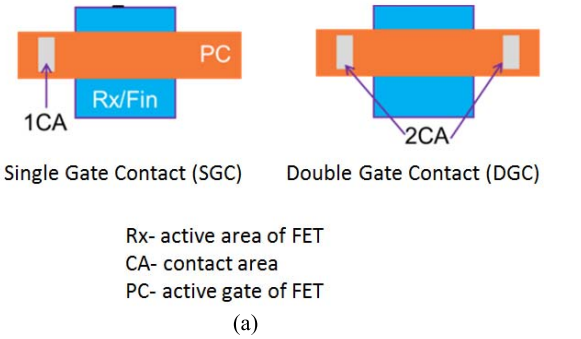


Fig. 6. (a) Layout of the single-side gate contact (SGC) and DGC device structure. (b) Comparison of the SGC and DGC F_{max} performance versus gate voltage (V_{gs}) of the N/PFinFET.

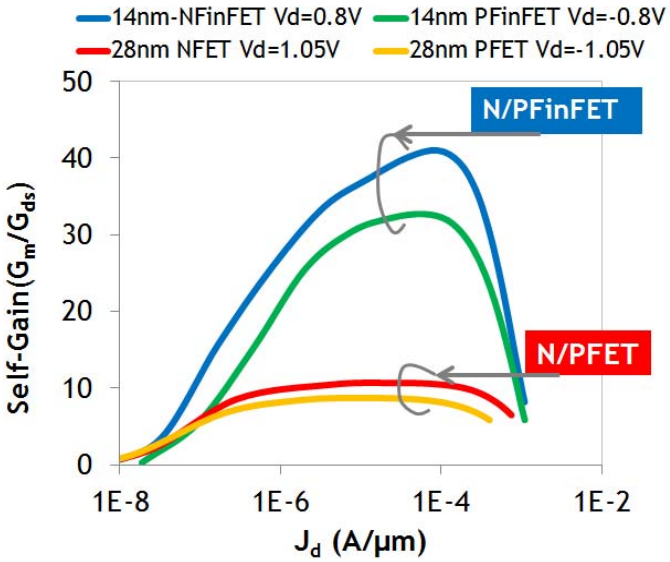


Fig. 7. Self-gain (G_m/G_{ds}) versus current density (J_d) of the N and PFET devices from 14-nm and 28-nm planar technologies, respectively.

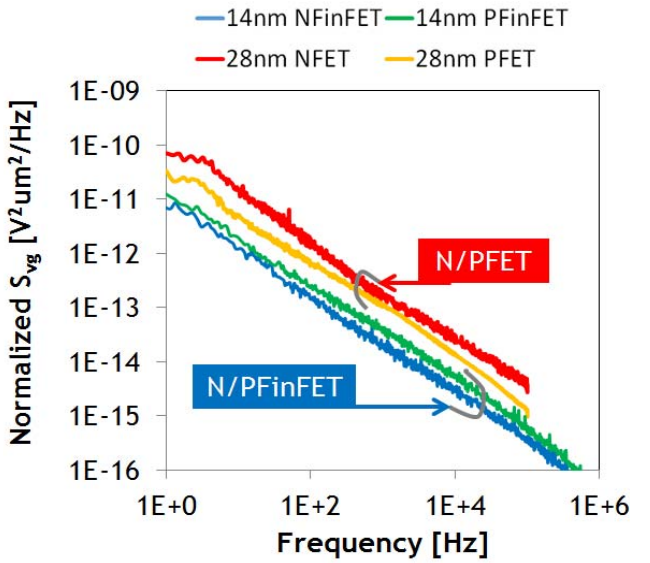


Fig. 8. Normalized input-referred flicker noise (1/f) S_{vg} versus frequency from the 28-nm planar and 14-nm FinFET technologies.

higher and dominant compared to the planar 28-nm technology.

Fig. 6(a) shows the F_{max} improvement achieved by using double-side gate contact (DGC) layout. To make this comparison, the de-embedding and RF structure connections were modified compared to design used for Figs. 2–4 data, mainly to fit the DGC strategies.

From Fig. 6(b), a significant F_{max} improvement 1.26 and 1.40 times that of SGC devices can be achieved for N and PFinFETs DGC structure, respectively. A new figure-of-merit parameter ($F_t.G_m/I_d$) is introduced to standardize the intrinsic RF performance across technologies as shown earlier in Table I. It can be observed that the 14-nm FinFET technology intrinsic performance outperforms 28-nm planar FETs, while maintains a smaller device footprint.

In Fig. 7, self-gain (G_m/G_{ds}) of the 14-nm FinFETs and 28-nm FETs is plotted against the normalized current density (J_d). During the on-state operation, FinFET experiences full channel depletion which leads to a better electrostatic gate control over the channel region. This suppresses the short channel effects; namely, punchthrough and drain-induced barrier lowering, and successfully leads to a better device scaling while having lower output conductance (G_{ds}). This can be clearly perceived from Fig. 7 that the 14-nm FinFET technology achieves more than a 3 times that of the 28-nm technology self-gain. The 3-D architecture of FinFET is benefiting the G_m by having a large W_{eff} in a given device footprint.

Normalized 1/f input referred gate voltage noise spectral densities (S_{vg}) of both 14-nm and 28-nm technologies

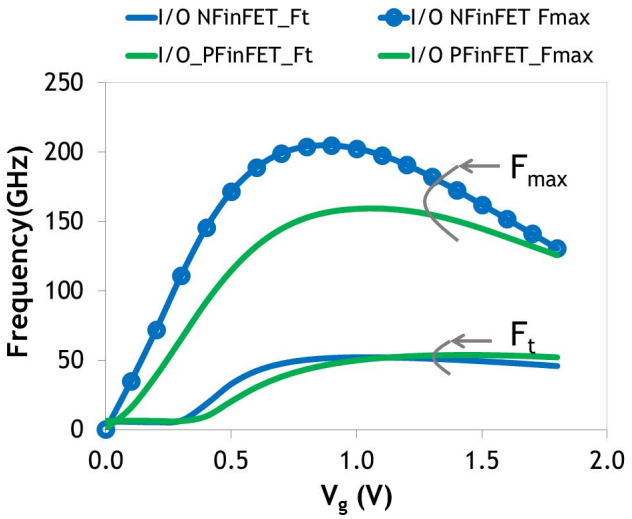


Fig. 9. F_t and F_{max} of 1.8-V I/O of $L_g = 150$ nm N/P FinFET versus V_g (gate bias voltage) characteristics.

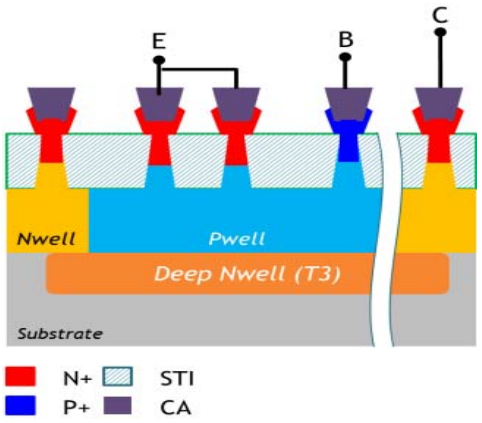


Fig. 10. Schematic *x*-sectional view with label N+/P+ dopant, shallow trench isolation, and CA with emitter (*E*), base (*B*), and collector terminals.

TABLE II
SPECTRA SIMULATION FROM TWO-FIN DEVICE LO CIRCUIT

	SLVT(super low V_t) FinFETs	ULVT(Ultra low V_t) FinFETs
V_{tsat}	180mV	50mV
Power reduction	Reference	up to 30%

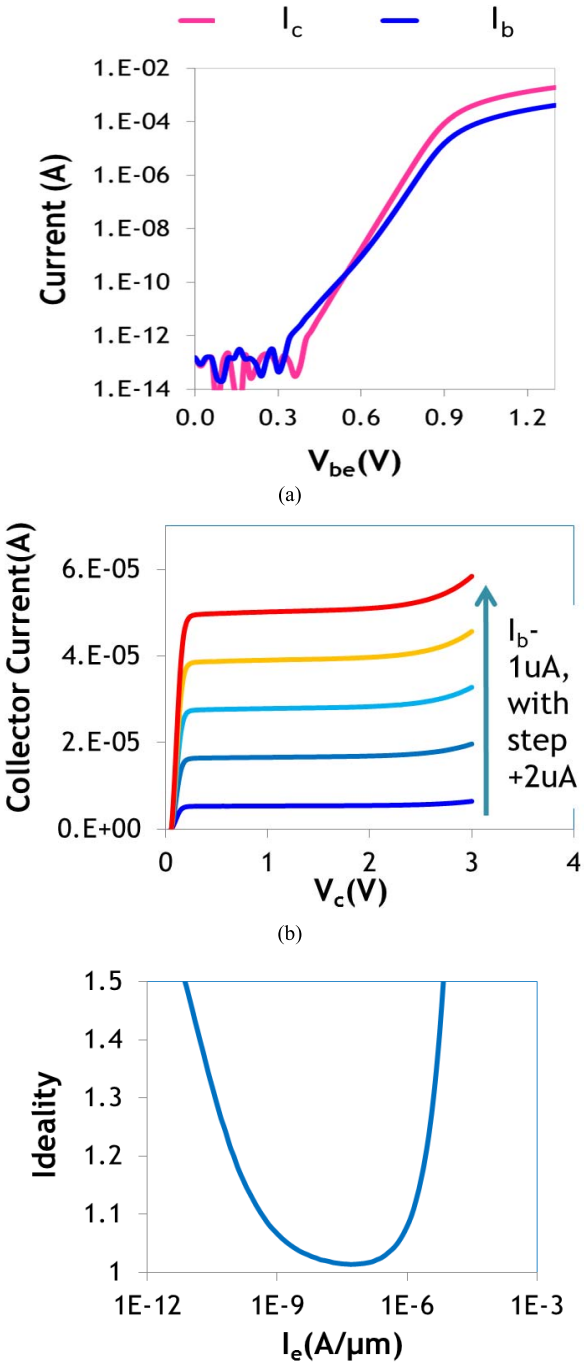
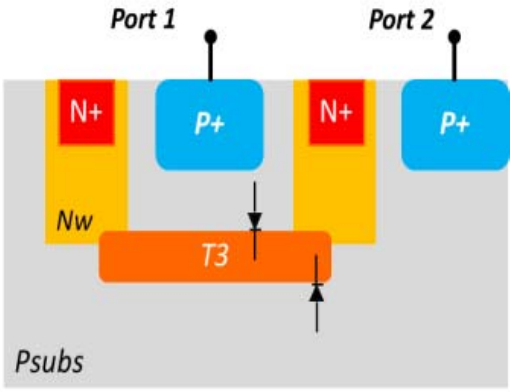


Fig. 11. (a) Gummel characteristics {collector current (I_c), base current (I_b)} versus V_{be} (base–emitter voltage) at 0.8 V of V_{cb} (collector base voltage) of VNPN bipolar transistor. (b) I_c–V_c curve. (c) Ideality characteristics of the VNPN bipolar device.

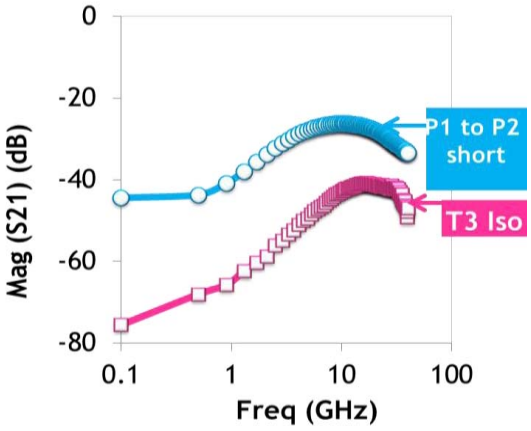
are shown in Fig. 8. The S_{vg} of N and PFinFET devices is 17 and 35 $fV^2\mu m^2/Hz$ at 1 kHz compared to 171 and 106 $fV^2\mu m^2/Hz$ of the 28-nm planar N and PFETs, respectively. The low S_{vg} of FinFETs is attributed to the flow of carriers away from the silicon/gate oxide interface. As a matter of fact during the operation, conduction happens through the thickness of Fins, which is contrary to the surface conduction of bulk silicon planar FETs [11].

The 1.8 V thick gate oxide I/O N/PFinFETs similar to core FinFETs exhibit an excellent peak F_t (50.1/53.5 GHz) and F_{max} (200/160 GHz), as shown in Fig. 9. It can be seen that F_{max} is higher than F_t due to lower gate resistance (R_g) benefit of a longer channel length ($L_g = 150$ nm). Owing to higher voltage operation of these I/O FETs, a high current can be drawn despite having longer channel length, and thereby providing an opportunity to support the cellular and RF power amplifier designs.

For the lower voltage operation, ultralow V_t (ULVT) FinFET devices with reduced V_{dd} are available. These devices



(a)



(b)

Fig. 12. (a) cross-sectional view of the bottom region of deep n-well isolations. (b) Substrate coupling (S21) measured silicon results with deep n-well (T3) isolation or without T3 (P1 to P2 short) structures.

offer significant power reduction in some RF design cases (Table II) near zero V_t operation. To demonstrate the benefit, a two-Fin-based local oscillator (LO) was being simulated for power and performance of both ULVT and super low V_t (SLVT) device flavors. The SLVT is the next lowest V_t (180 mV) device available for designers. In this paper, the ULVT device oscillator circuit shows a power saving up to 30% as indicated in Table II.

V. 14-nm Deep n-Well Analog Device Results

A VNPN bipolar cross-sectional schematic with a deep n-well implant layer is illustrated in Fig. 10. The VNPN device shows a well-behaved Gummel characteristic with a low base current (I_b) at low base–emitter voltage (V_{be}) in Fig. 11(a). This demonstrates a low level of carrier recombination and generation at the emitter and base junction of the bipolar. It provides an alternate device option for temperature sensors circuits. From I_c–V_c characteristics, it can be observed that the VNPN are functional well up to 3 V [Fig. 11(b)]; however, device reliability limits operation to 2.5 V, when impact ionization kick in. In terms of junction quality, the ideality of VNPN bipolar is reaching a 1.03 value at 10 μA/μm [(Fig. 11(c)], which is reasonably close to a planar bulk silicon junction's value of 1.01. As a result, this device has potential to offer another device opportunity for low flicker (1/f) noise circuit designs.

The deep n-well junction either with p-well (upper side) or p-type substrate (lower side) can provide higher junction breakdown voltage due to lower doping of these regions. The deep n-well tub regions can effectively be used to isolate individual device (NFET) or a section of a circuit from the neighboring circuit's voltage, substrate or random supply noise.

Fig. 12(a) shows a schematic of the deep n-well isolation structure used for S21 parameter measurements [10]. The space between port 1 and port 2 is kept at 10 μm for both with and without deep n-well (T3) isolation structures. Fig. 12(b) compares the measured S21 results from these structures. It can be seen that noise reduction is more effective in the 0.1- to 10-GHz frequency range with deep n-well isolation and achieves a maximum of 75-dB substrate noise reduction at 0.1 GHz.

VI. Conclusion

The 14-nm RF FinFET technology demonstrates a record peak F_t(314/285 GHz) for N/PFinFETs. It also achieves significantly higher F_{max} (180/140 GHz) for N/PFinFET compared to the 28-nm planar devices. High RF performance is mainly attributed to higher G_m. To improve F_{max} beyond this, a device optimization is possible including larger L_g and DGCs. A DGC enhanced the F_{max} performance to 227 and 195 GHz of N and P FinFET, respectively. Due to thin body and better short channel control, the FinFET also shows a remarkably high self-gain of 40/34 from N/P-type devices.

With this high self-gain, improved 1/f noise behavior and rich logic intellectual portfolio, the 14-nm RF technology is an attractive choice for advanced RF SoC designs migrating from the 28-nm technology platform. Additional features to the platform like deep n-well process and ULVT devices further extend design capabilities in the ultralow-power circuit area. The 14-nm RF technology provides a total solution for next generation analog and RF designs especially in <6 GHz application space.

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