High Performance 14nm SOI FinFET CMOS Technology with 0.0174μm^2 embedded DRAM and 15 Levels of Cu Metallization

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Abstract

We present a fully integrated 14nm CMOS technology featuring finFET architecture on an SOI substrate for a diverse set of SoC applications including HP server microprocessors and LP ASICs. This SOI finFET architecture is integrated with a 4th generation deep trench embedded DRAM to provide an ultra-dense (0.0174um^2) memory solution for industry leading 'scale-out' processor design. A broad range of Vts is enabled on chip through a unique dual workfunction process applied to both NFETs and PFETs. This enables simultaneous optimization of both lowVt (HP) and HiVt (LP) devices without reliance on problematic approaches like heavy doping or Lgate modulation to create Vt differentiation. The SOI finFET's excellent subthreshold behavior allows gate length scaling to the sub 20nm regime and superior low Vdd operation. This leads to a substantial (>35%) performance gain for Vdd ~0.8V compared to the HP 22nm planar predecessor technology. At the same time, the exceptional FE/BE reliability enables high Vdd (>1.1V) operation essential to the high single thread performance for processors intended for 'scale-up' enterprise systems. A hierarchical BEOL with 15 levels of copper interconnect delivers both high performance wire-ability as well as effective power supply and clock distribution for very large >600mm^2 SoCs.

Technology Description

The critical dimensions for this 14nm technology are shown in Table1. The process flow, along with key device cross sections, is shown in Fig1. The 42nm fin pitch is achieved using sidewall image transfer. The SOI substrate provides multiple advantages for overall finFET integration. Use of an SOI substrate 1) minimizes the process complexity associated with both fin isolation and eDRAM integration, 2) minimizes the parasitic capacitance at the base of the fin, 3) simplifies patterning of the active fins, and 4) minimizes each component of fin structural variability (i.e. height, thickness, and profile).

It is important to underscore a key point concerning fin height selection in a HP finFET technology. To enable high frequency operation (near Vmax), it is imperative to minimize the back-end RC delay so that it represents a small fraction of the critical path's overall gate delay. In this paradigm, excessively tall fins lead to unfavorable power/performance trade-offs (Fig2). In this work, careful design/technology co-optimization has resulted in the selection of an ideal fin height that supports enterprise server class performance at the lowest power envelope.

The resulting SOI finFET device response is shown in Fig3. High G_m is achieved through a combination of gatestack, epi S/D, and contact interface optimization. The SOI finFET architecture enables a SCE that is well controlled down to the sub-20nm Lgate regime (Fig4). This device behavior, coupled to the optimized fin height selection and parasitic capacitance optimization, has resulted in a performance improvement of >35% over the predecessor 22nm technology node [2] (Fig5). Furthermore, this performance gain stretches over a broad Vt range (from 100nA/um HP FETs to sub 1nA/um LP and SRAM array FETs which are featured in many ASICs). It is generally difficult to support such a wide Vt range in a finFET technology. Typically, Vt separation is achieved by doping, which carries with it many negative consequences to finFET response [3]. As a result, most industry standard finFET offerings restrict the allowable Vt range available to a designer. In this work, we apply an innovative dual WF process to generate widely spaced Vts (for both N/P) without reliance on doping to create the Vt separation [4]. The dopant removal enables 1) significant performance enhancement for HiVt (LP) devices due to the mobility gain (Fig6) and 2) significant Vt mismatch (Vmin) reduction for low leakage SRAM cells due to the RDF reduction (Fig7).

As mentioned earlier, one of the key advantages of the SOI substrate is the ability to co-integrate deep trench eDRAM with logic. In this work, the 14nm eDRAM unit cell has been scaled down to 0.0174um^2, which provides a unique memory solution for cache starved processors (Fig8). This cell scaling and performance (access time) have largely been enabled by the finFET device architecture. The SCE improvement achieved in the pass gate has allowed for significant reduction of both Lgate and Vt, without compromising retention specifications. The unique challenge of DT integration with fins comes in the control of the strap resistance between the SOI crystalline fin and the highly doped poly-crystalline fin (Fig9). The epi S/D module has been engineered to minimize the resistance at this interface through growth optimization on the two different underlying materials. A top down of the interface after epi S/D is shown in Fig10. This overall finFET based cell design, together with optimization of the strap resistance, has resulted in a cell access time that is 0.7X of the previous best-in-class value achieved by our 22nm technology.

The TDDB and BTI results for this technology are shown in Fig11 and Fig12. Both pass the specifications required to support 10 year lifetime at Vmax >1.1V. This technology provides up to 15 levels of Cu metallization. The hierarchical BEOL architecture (Fig13) begins with 64nm pitch at M1/Mx and expands up to ultra thick levels required for efficient clock and power distribution across a >600mm^2 chip. Throughout the BE, metallization processes have been developed so that wire resistance and EM lifetime can be optimized simultaneously (Fig 14).

Conclusions

A HP 14nm SOI finFET technology has been developed featuring >35% performance improvement, an ultra-dense 0.0174um^2 embedded DRAM memory cell, and dual WF gatestack enablement that achieves optimized HP and LP devices simultaneously on chip.

References
[1] S-T. Chen et al., IITC/MAM 2011
[2] S. Narasimha et al., IEDM 2012
[3] C-H. Lin et al., VLSI 2012
[4] K. Seo et al., VLSI 2014

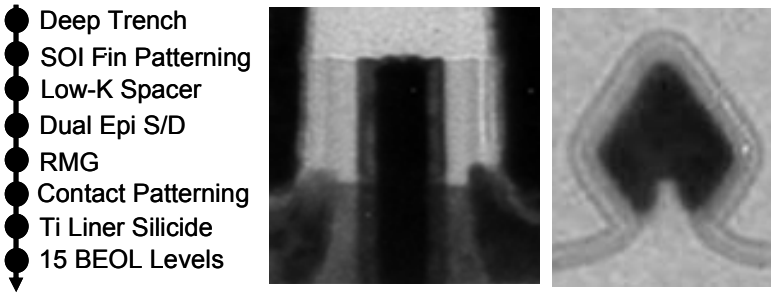

Fig. 1 Process flow and cross sections for 14nm SOI finFET technology.

Table 1 Key technology scaling rules and attributes. Patterning details for the 64nm M1/Mx provided in Ref [1].

Level	Pitch
Fin	42nm
Gate (single pattern w/ cut)	80nm
Contact	80nm
M1 (Bi-directional)	64nm
Mx	64nm
BE Hierarchy: 1X,1.25X,2X,4X,8X,40X	
eDRAM cell area 0.0174 μm^2	

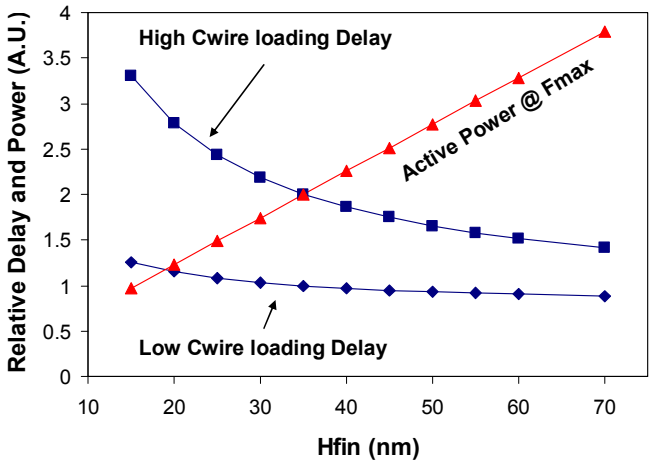

Fig. 2 Power performance optimization as a function of Hfin. High performance designs require low Cwire critical paths. These paths do not benefit from Hfin increase.

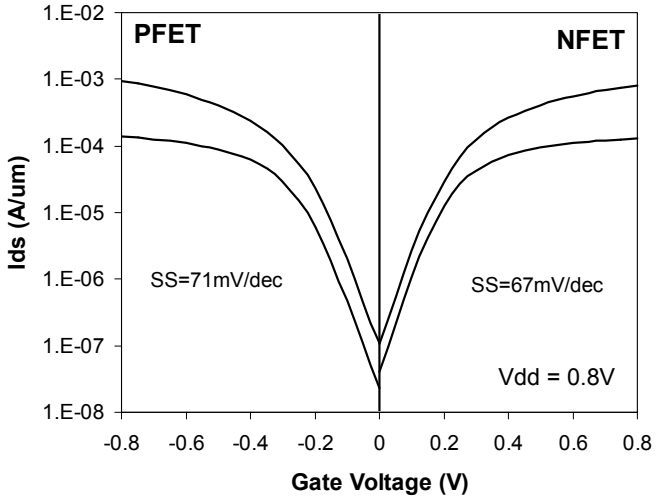

Fig. 3 Nominal DC Id-Vg response for HP devices at 0.8V. The curves reflect Idsat values of 808/935 μA/um (N/P) for HP devices. These Id values are normalized by the true Si FIN perimeter (and not fin pitch). AC values (without self-heating) are 5% higher than the DC values shown here.

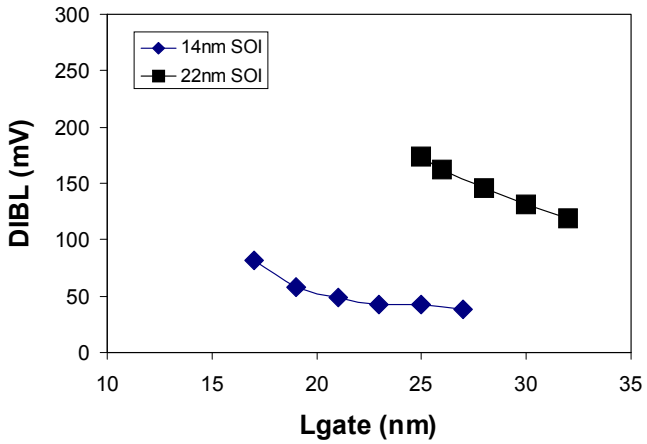

Fig. 4 DIBL response of 14nm SOI finFETs compared to 22nm SOI planar devices. SCE control is demonstrated down to the sub-20nm gate length regime.

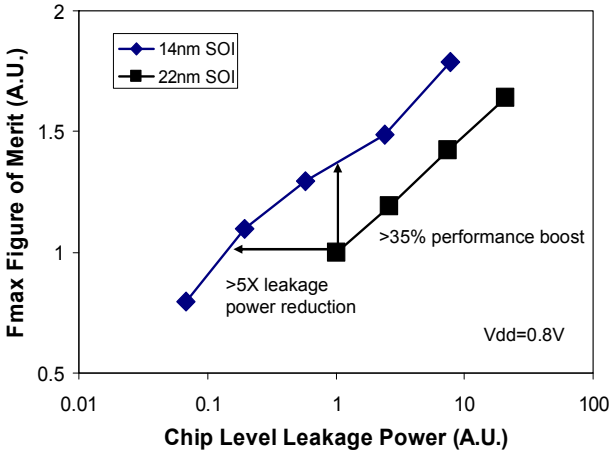

Fig. 5 14nm SOI finFET performance benchmarking at fixed leakage compared to our 22nm SOI HP technology. This 14nm gains exceed 35% (Vdd 0.8V).

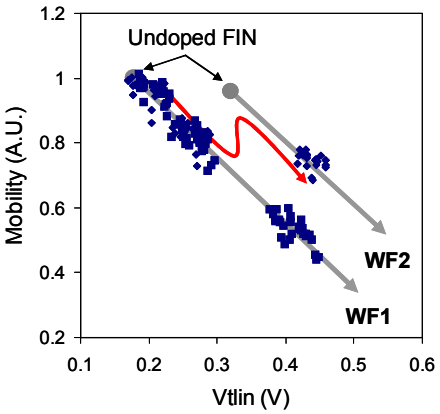

Fig. 6 Benefit of dual WF design for the mobility response of the hiVt (LP) device offerings. The grey arrows point in the direction of increasing doping.

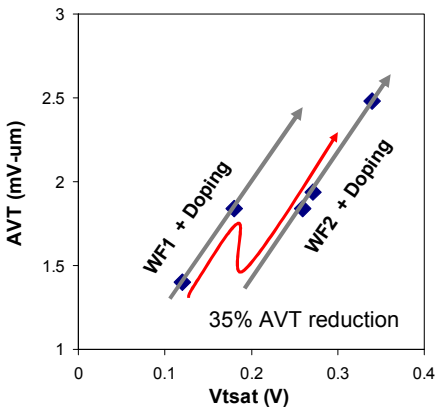

Fig. 7 Benefit of dual WF design for optimization of SRAM AVt through Vt mismatch and RDF control.

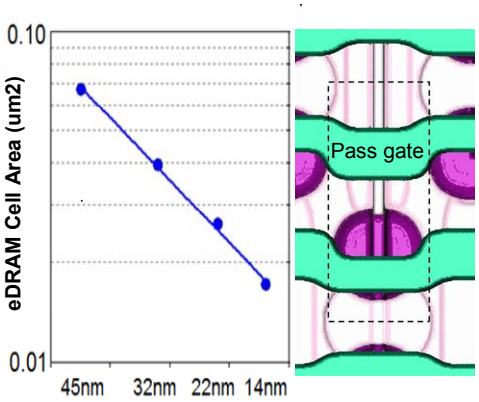

Fig. 8 IBM eDRAM area scaling over the last 4 generations culminating in the 0.0174um^2 cell in 14nm SOI finFET technology.

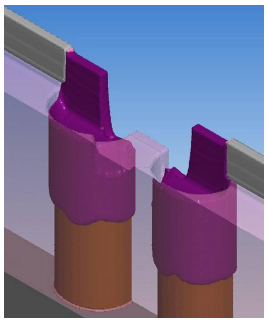

Fig. 9 Representative image after fin patterning. The interface between the crystalline (SOI) and polycrystalline (trench) segments defines the 'strap' region.

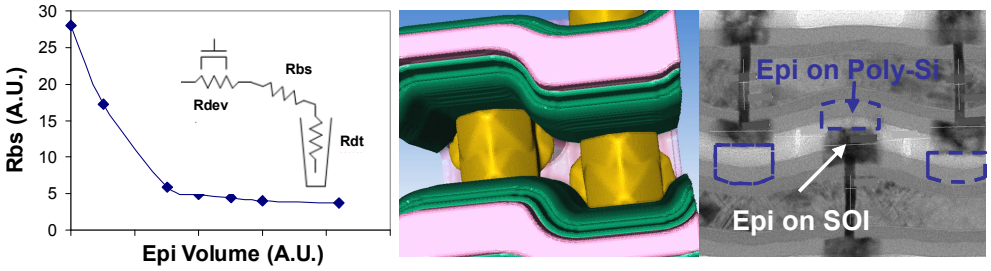

Fig. 10 Importance of the epi S/D process on the buried strap resistance. The TEM illustrates how the epi growth proceeds from both the SOI and poly seed regions

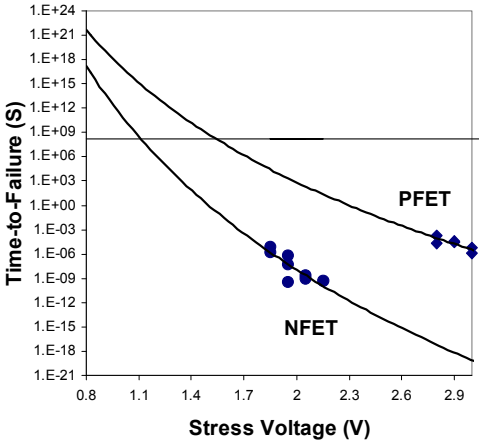

Fig. 11 TDDB response for 14nm SOI N/P finFETs. The yield projections support 10 year EOL specifications for Vmax of >1.1V.

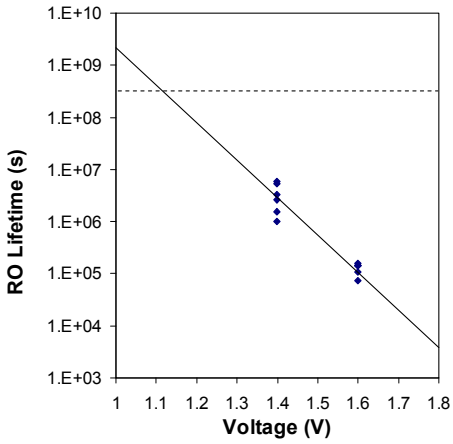

Fig. 12 Combined BTI response for 14nm SOI N/P finFETs. The projections support 10year EOL specifications for Vmax of >1.1V.

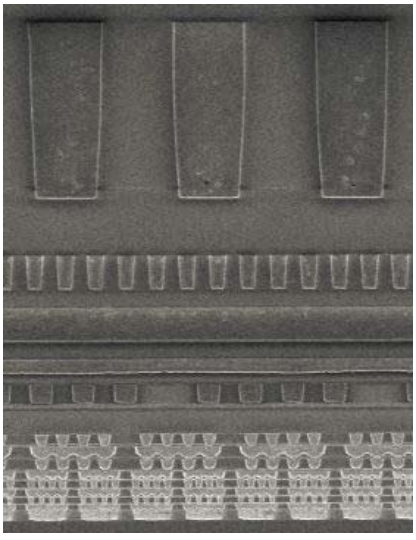

Fig. 13 Hierarchical back end reflecting 1X, 1.25X, 2X, 4X, 8X, 40X layering.

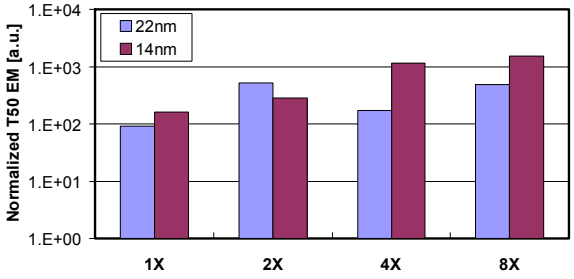

Fig. 14 EM optimization for the 1x, 4X, 8X BE levels in 14nm (compared to 22nm)