ERI Design: IDEA and POSH

ALIGN: Analog **L**ayout**, I**ntelligently **G**enerated from **N**etlists

University of Minnesota (Prime)

Texas A&M

Intel

IDEA and POSH Phase I Integration Meeting

Detroit, Michigan

17 July 2019– 19 July 2019

Team Members at the Integration Meeting

Kishor Kunal

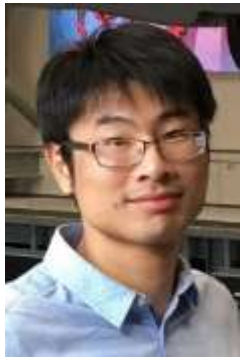
Meghna Madhusudan

Arvind Sharma

Jitesh Poojary

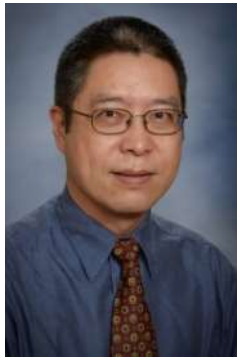
Tonmoy Dhar

Ramesh Harjani



Wenbin Xu

Yaguang Li



Jiang Hu

Parijat Mukherjee

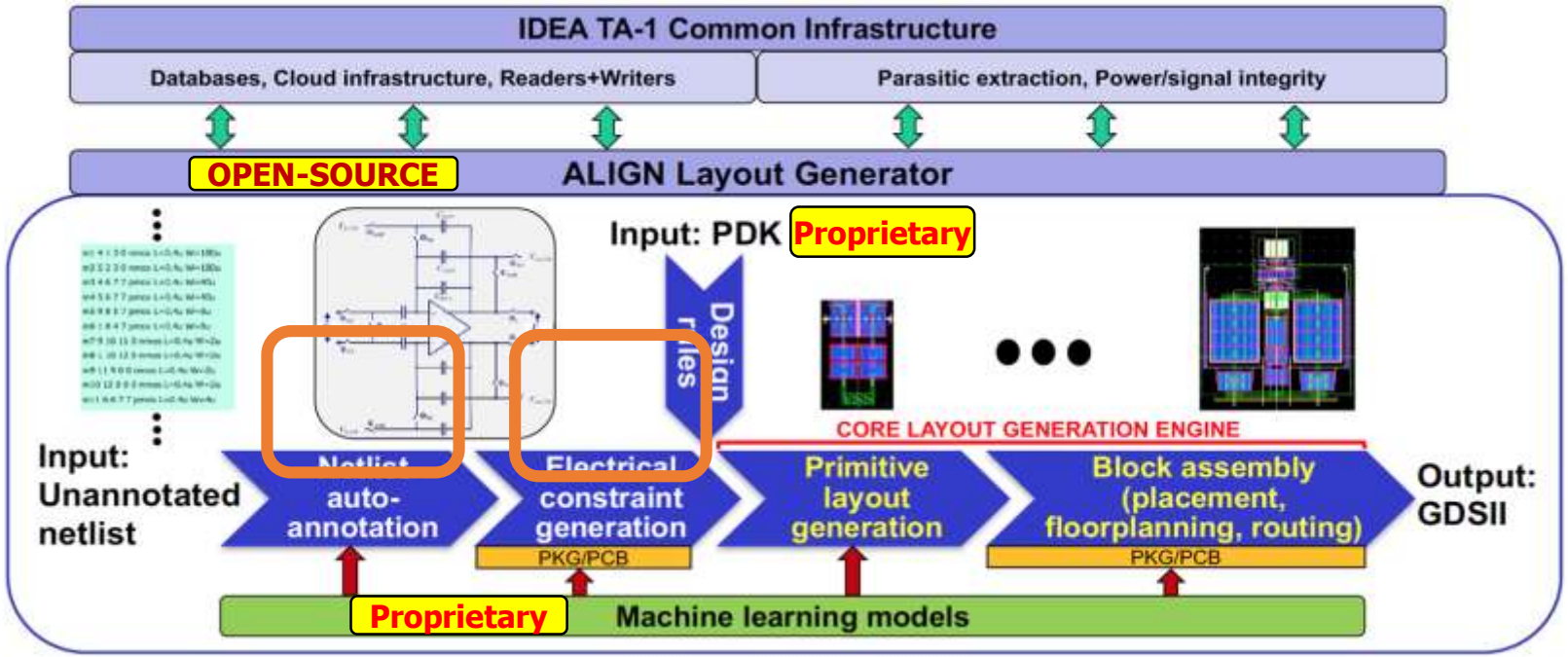
Steve Burns

Sachin Sapatnekar

Overview

Goal: No-human-in-the-loop layout generation from netlist to GDSII.

Technical Approach



Overview

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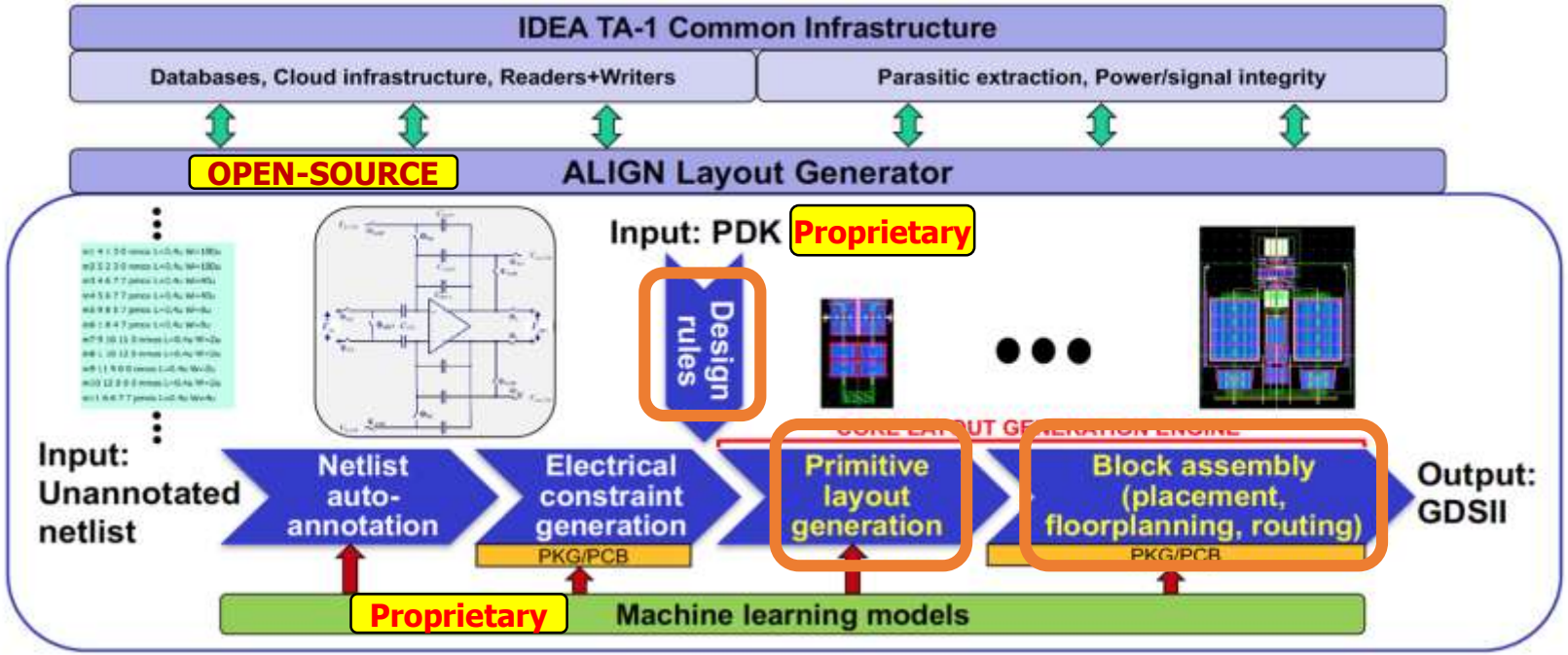

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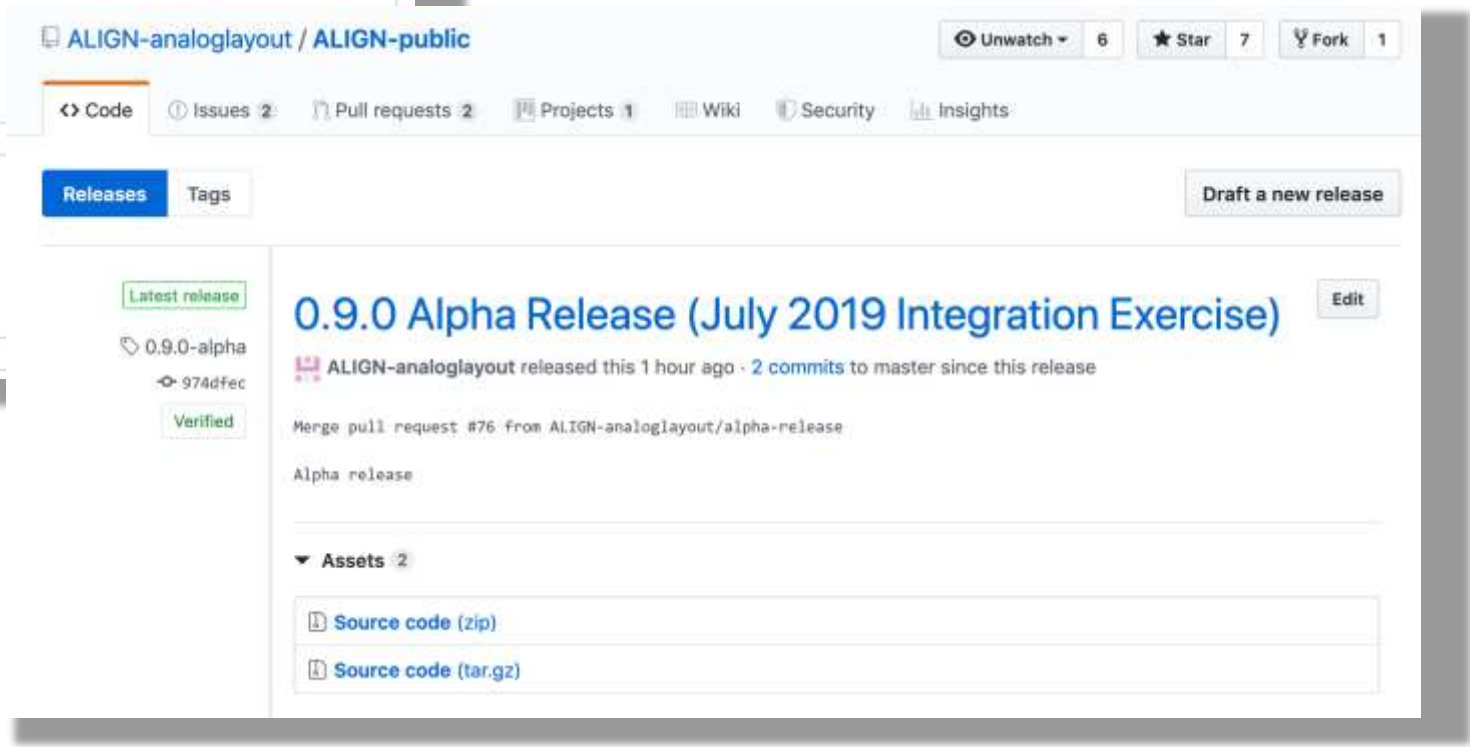
The ALIGN Github Repo: Alpha Release



https://github.com/ALIGN-analoglayout/ALIGN-public

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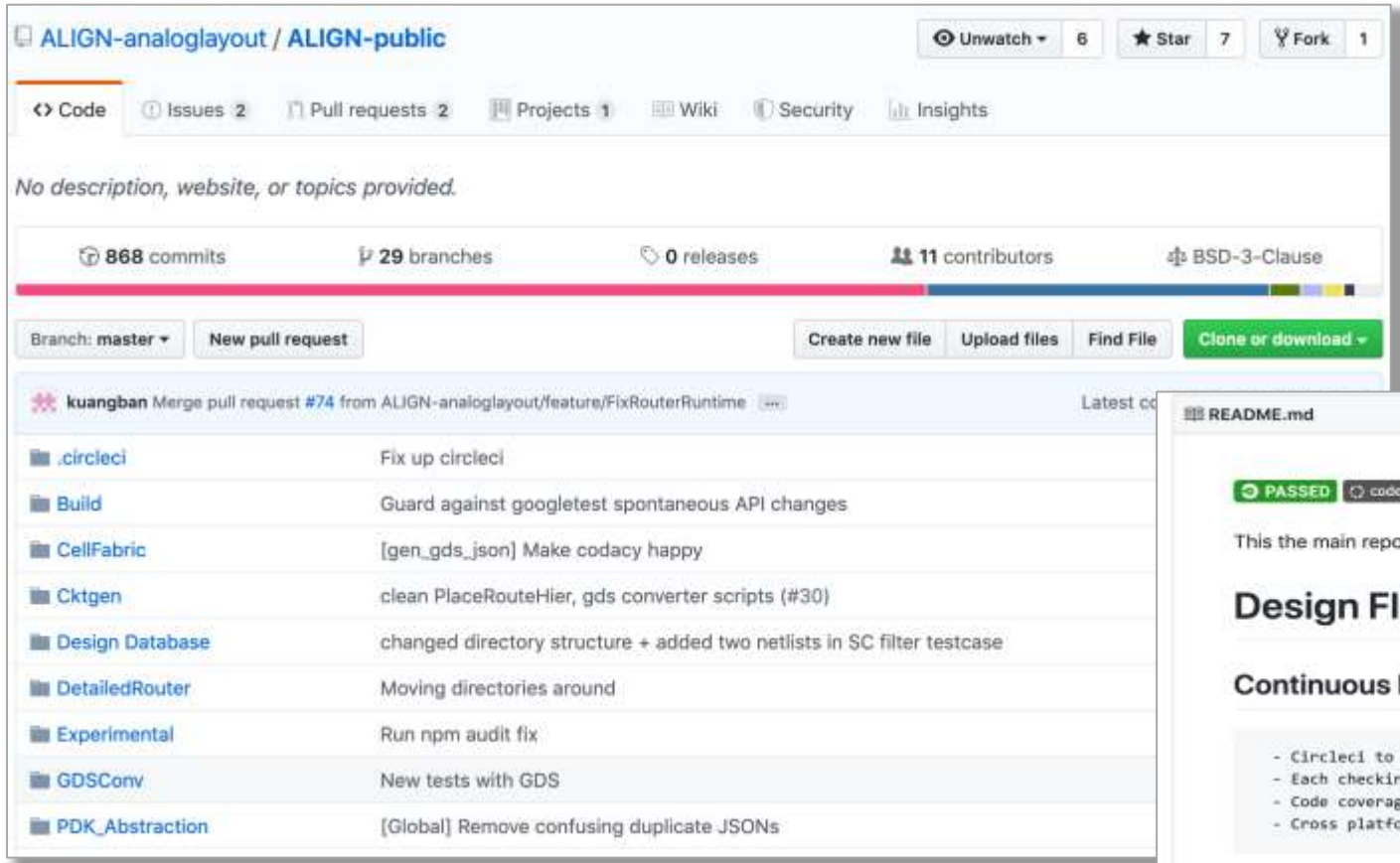

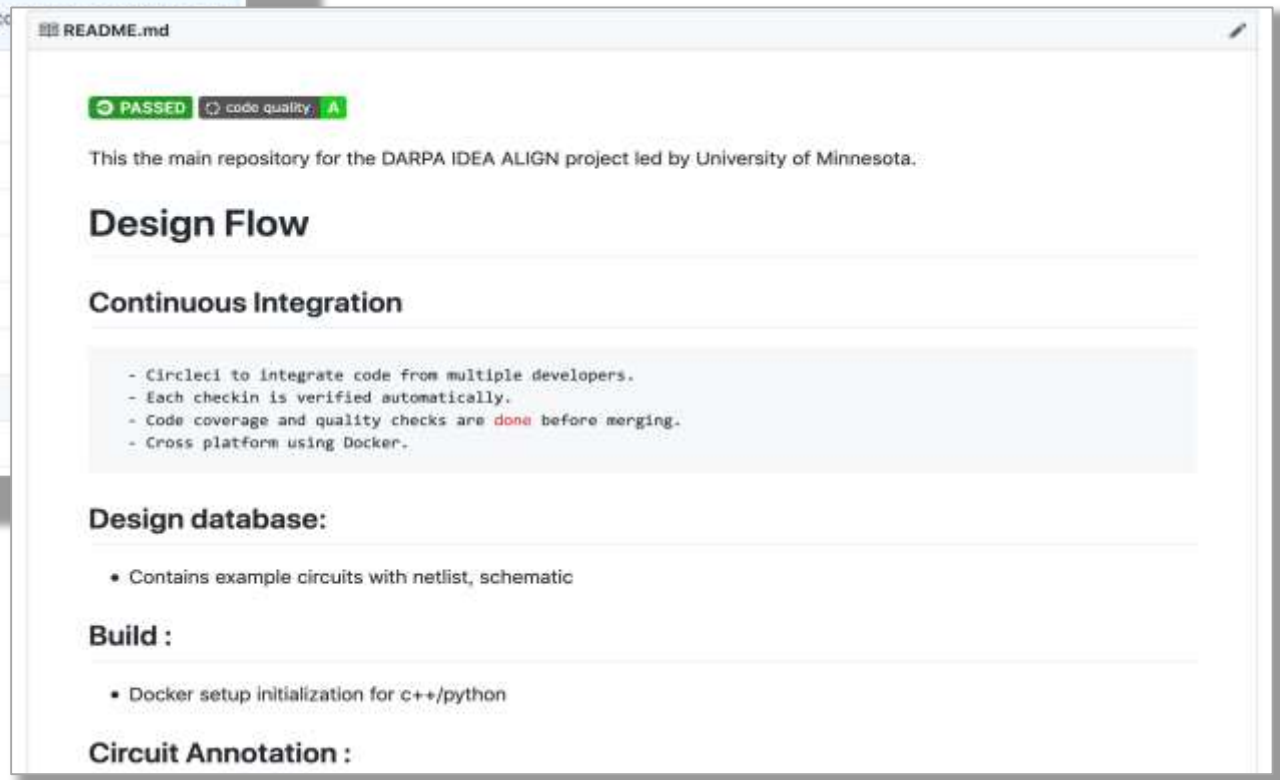

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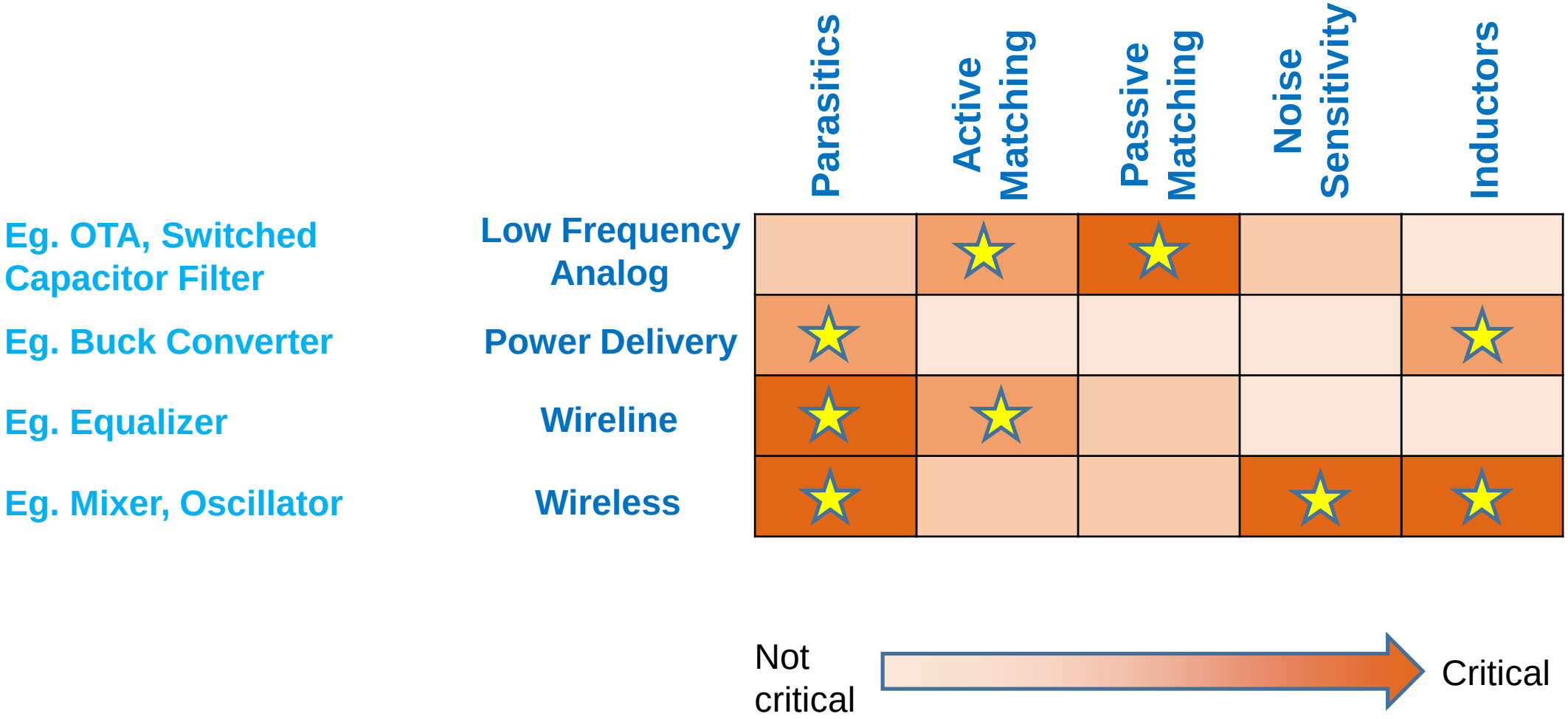
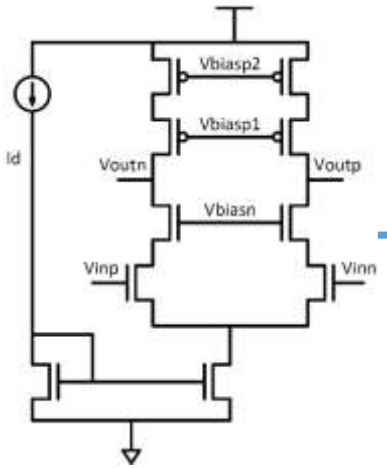
Classification of Analog Circuits: Layout Compiler

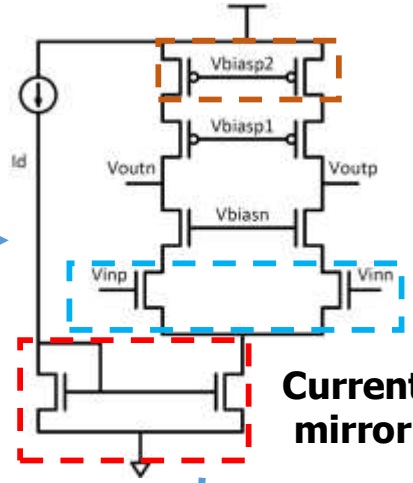
ALIGN target circuits: Low-frequency analog, wireline, wireless, power delivery



DEMO: OTA

Telescopic OTA





Netlist Annotation

Differential pair

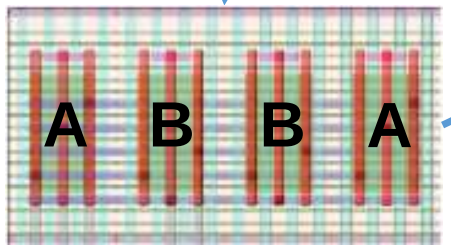
Current mirror

Primitive layout generation

DRC correct by construction

Symmetry

Common centroid

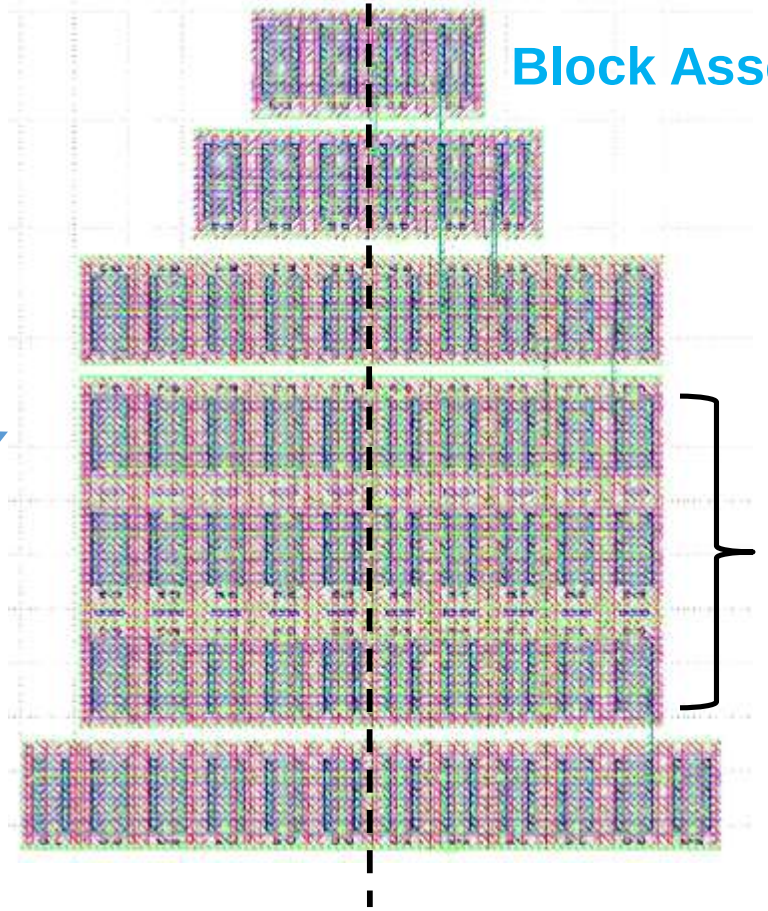


Axis of symmetry

Matching

Symmetric routing

Block Assembly

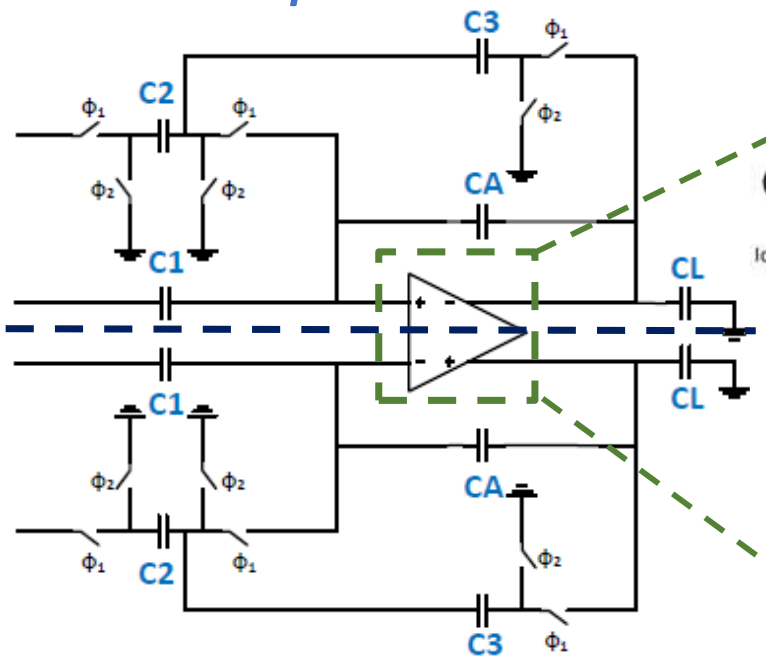


Differential pair

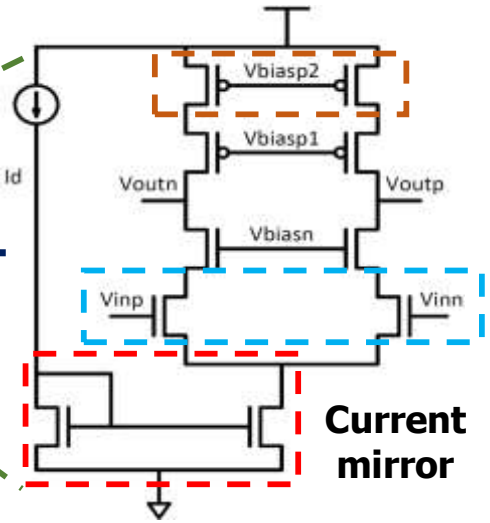
Current mirror

DEMO: Switched Capacitor Filter

Switched Capacitor Filter

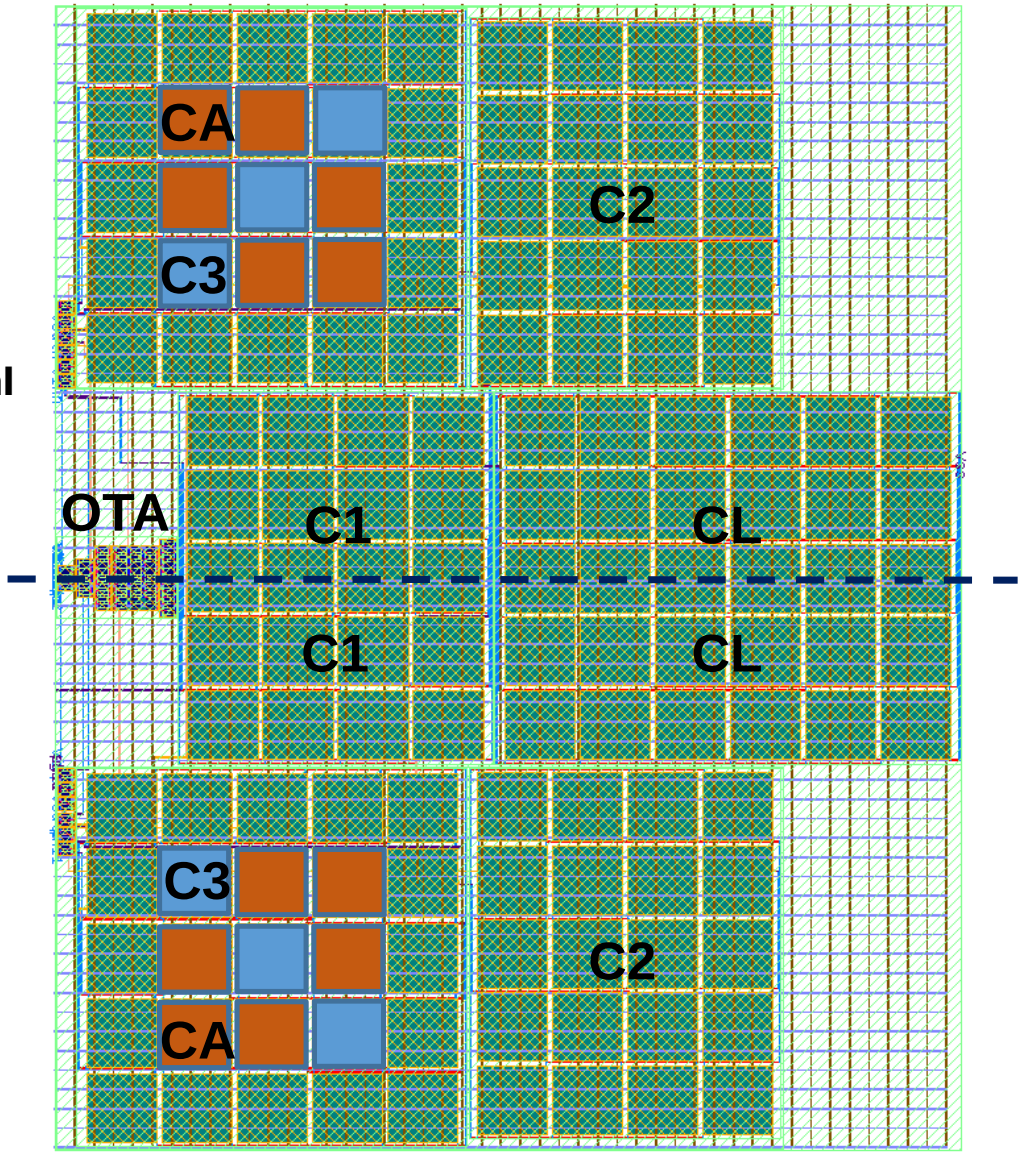


Telescopic OTA

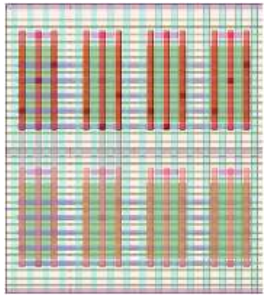


Differential pair

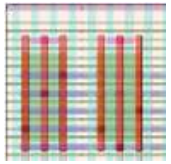
Current mirror



Differential Pair (OTA Primitives)

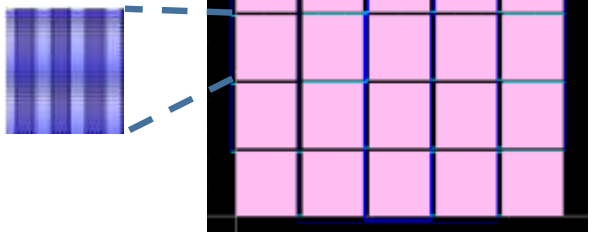


Switch



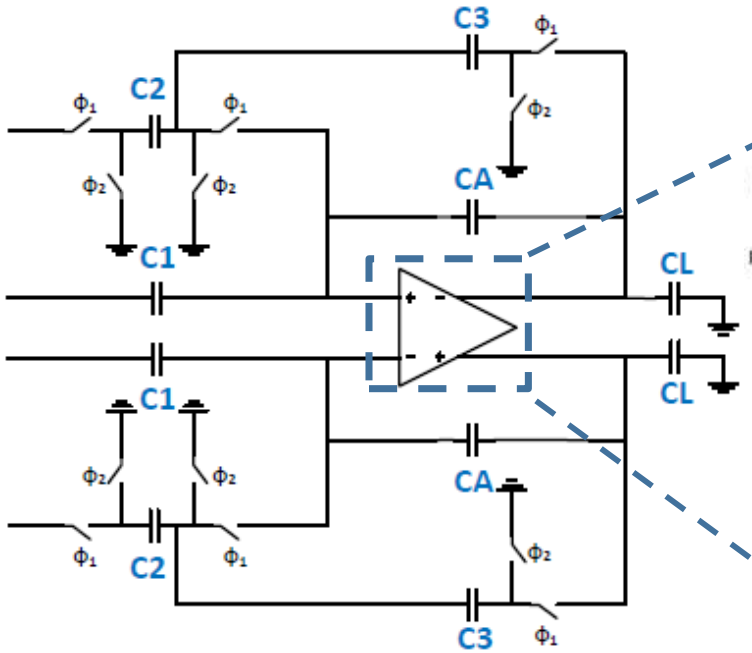
Capacitor Array (common centroid)

Unit C

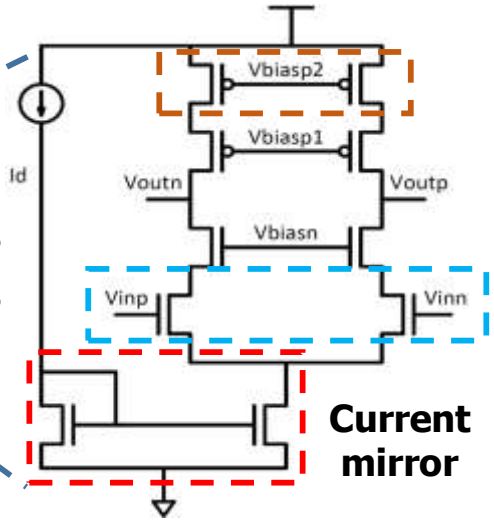


Performance Analysis: Switched Capacitor Filter

Switched Capacitor Filter

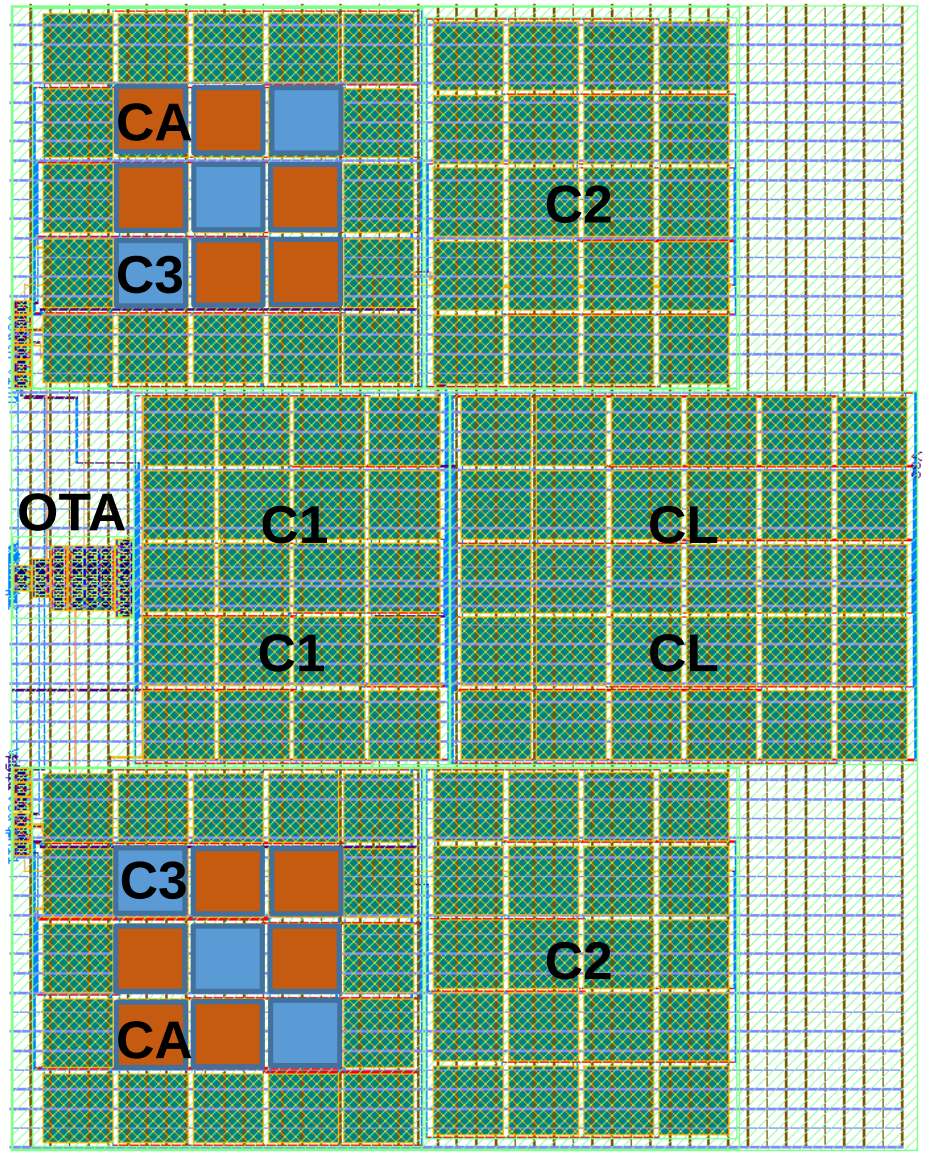


Telescopic OTA



Differential pair

Current mirror

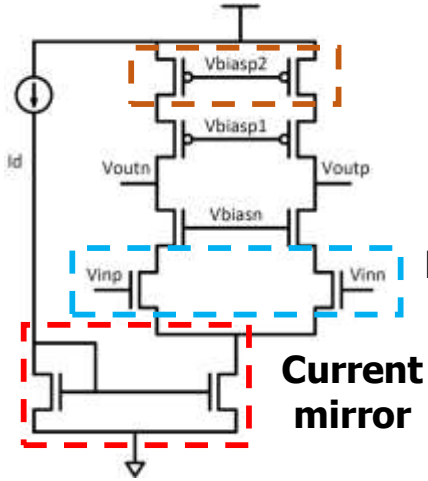


[ASAP7nm]

Specification	Unit	Schematic	Post – Layout	Shift
Inband gain	dB	5.53	5.48	-1 %

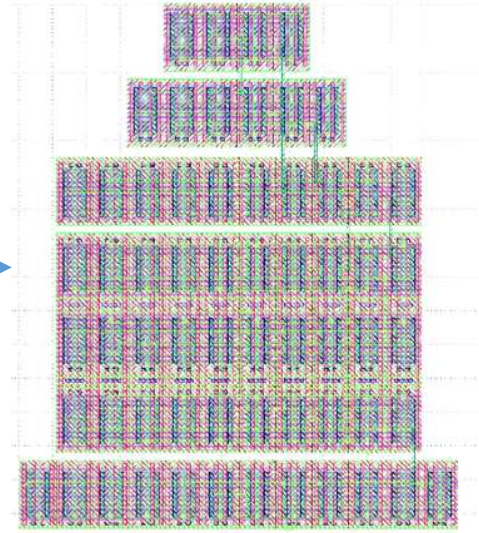
Performance Analysis: OTA

Telescopic OTA



Differential pair

Current mirror

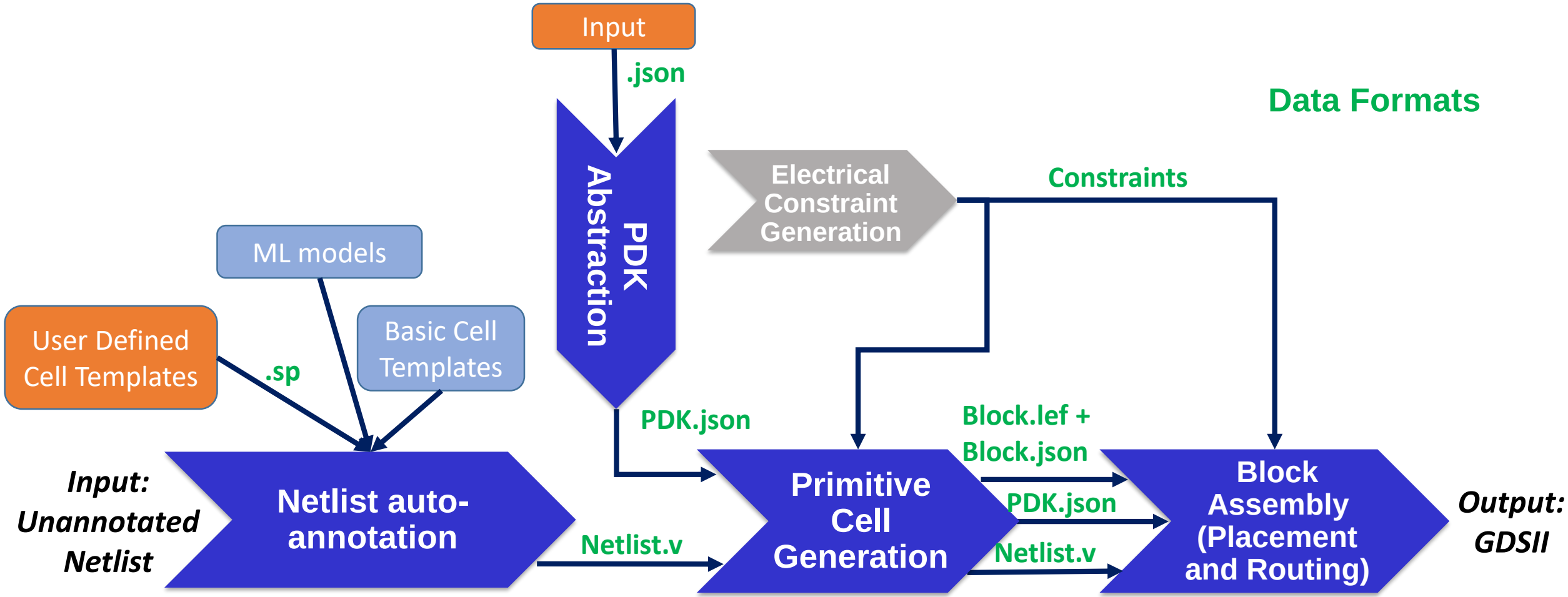


[ASAP7nm]

Specification	Unit	Schematic	Post – Layout (RC extract)	Shift	Post - Layout (C only extract)	Shift
AC Gain	dB	39.295	37.25	-5 %	39.29	0 %
3 dB frequency	MHz	10.648	10.473	-2 %	10.473	-2 %
Unity Gain Frequency	MHz	493.62	382.95	-22 %	489.85	-1 %
Input Offset	mV	0	0.145	-	0	-

Points to a 28% reduction in gm

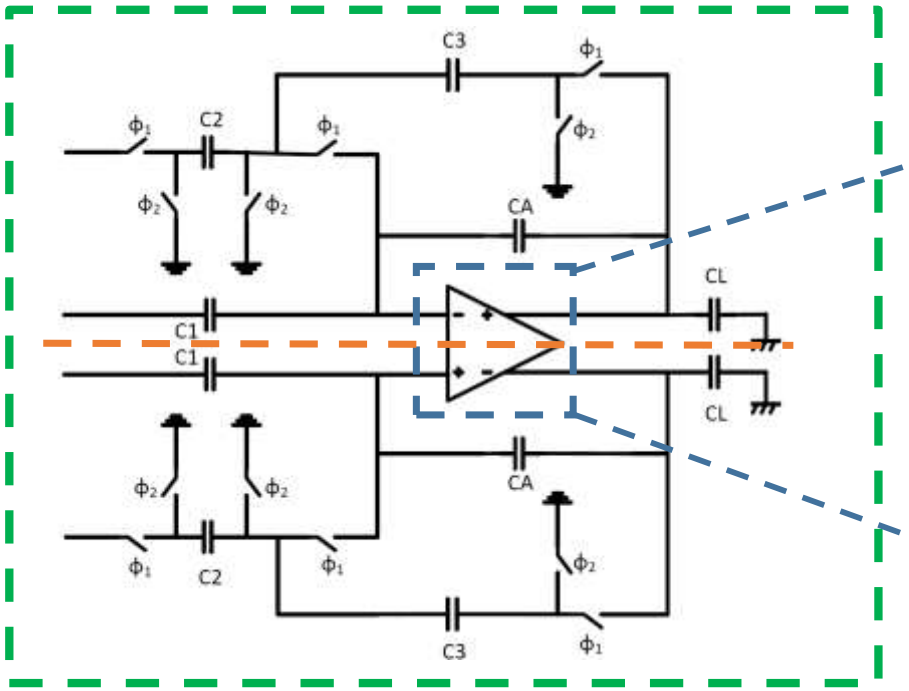
Overall Design Flow



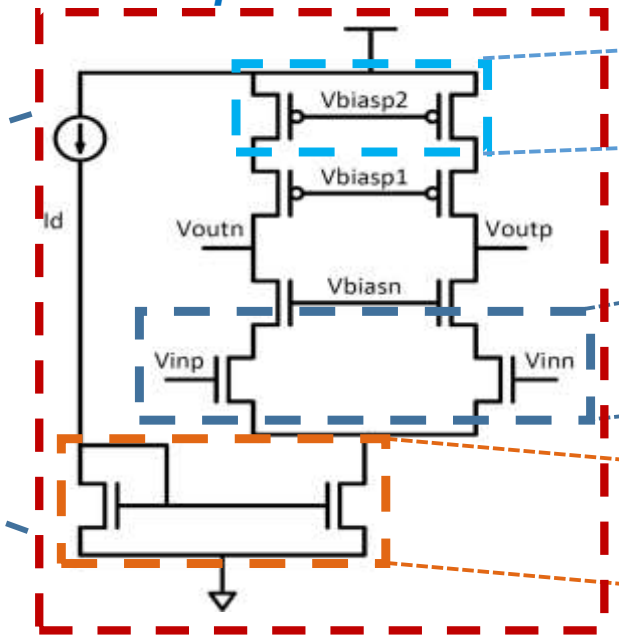
Stages of the flow

Auto-annotation and the Concept of Hierarchy

Switched Capacitor Filter

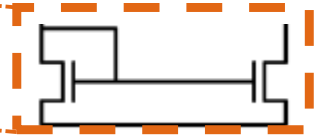


Telescopic OTA



Differential pair

Current mirror



Block

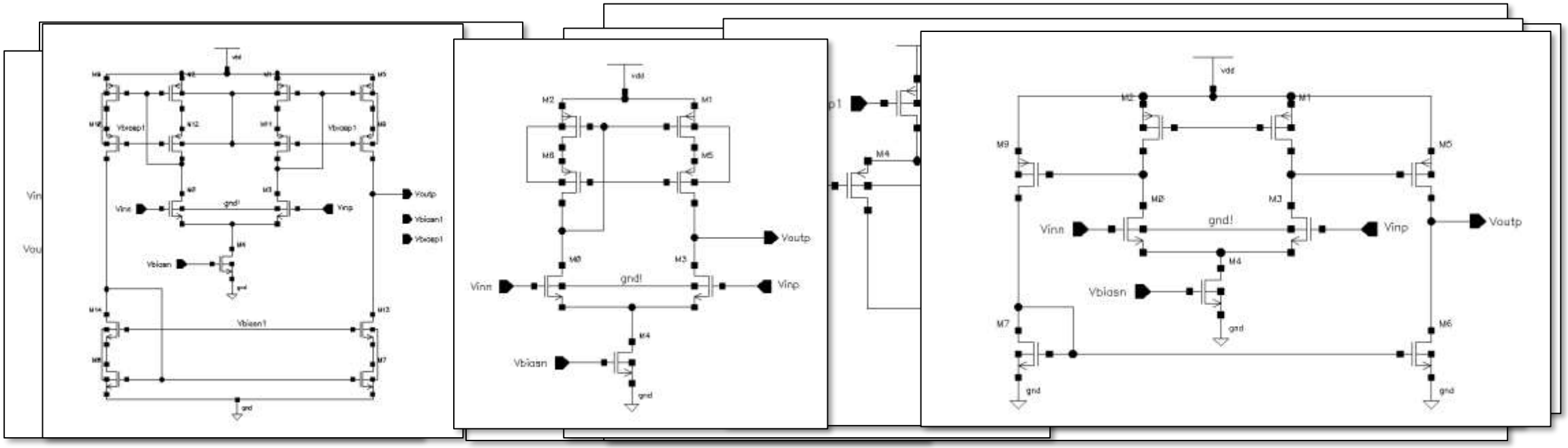
Sub block

Primitives

Auto-annotation of Input Netlists

Higher-level blocks have many variants – hard to enumerate

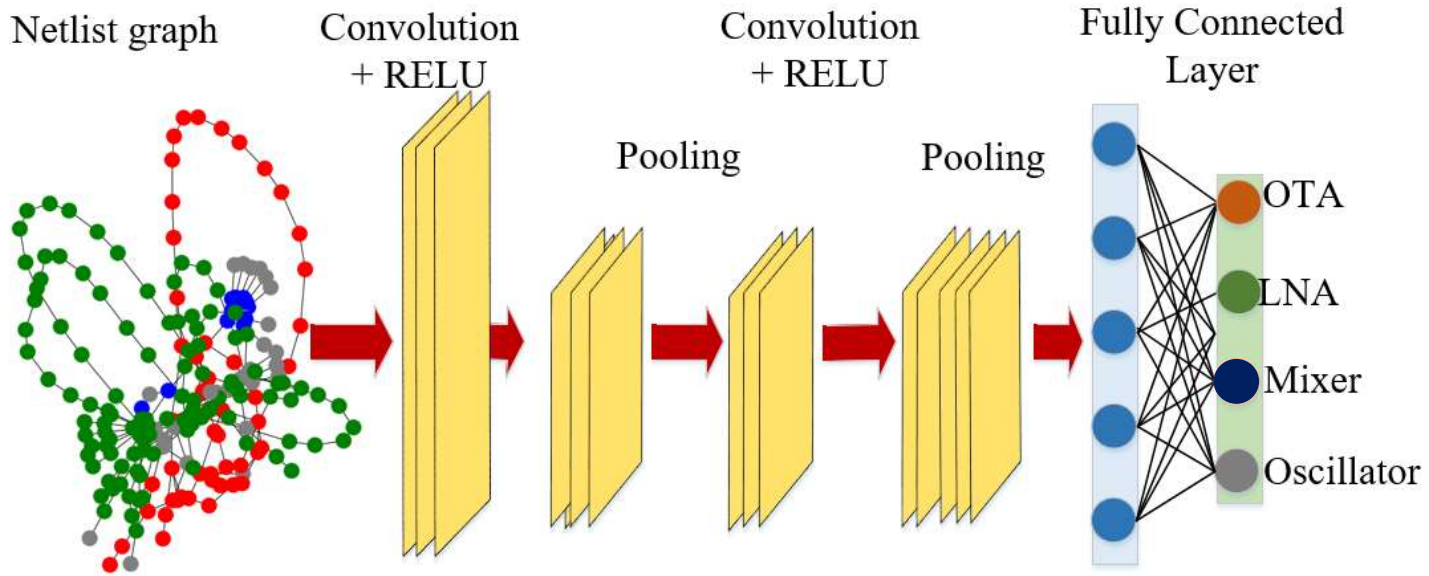
These are just a few types of OTAs:



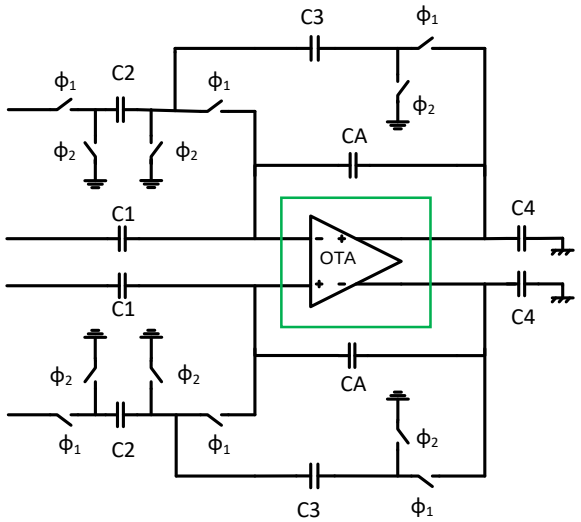
Graph-based neural network: Key differentiator from prior approaches!

Useful in identifying and annotating such structures with constraints (symmetry, common centroid,…)

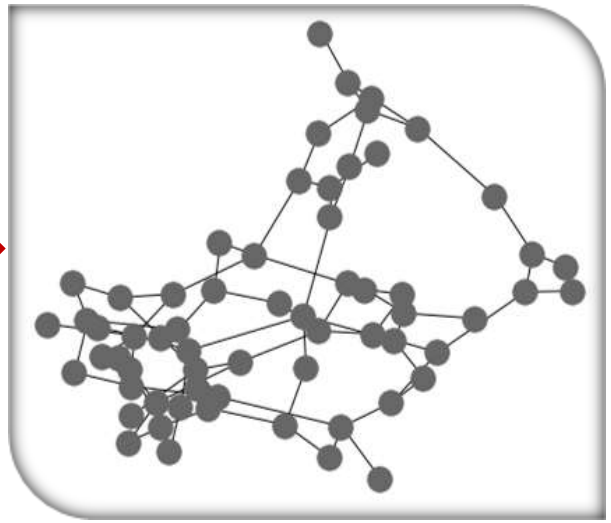
Recognizing Sub-blocks within a Switched-capacitor Filter



Netlist

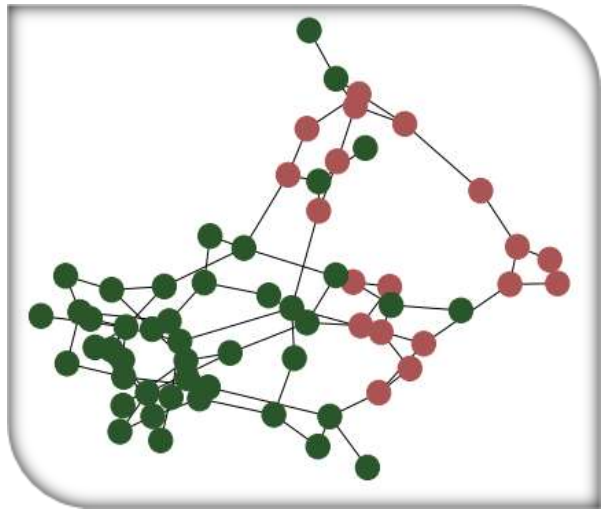


Graph



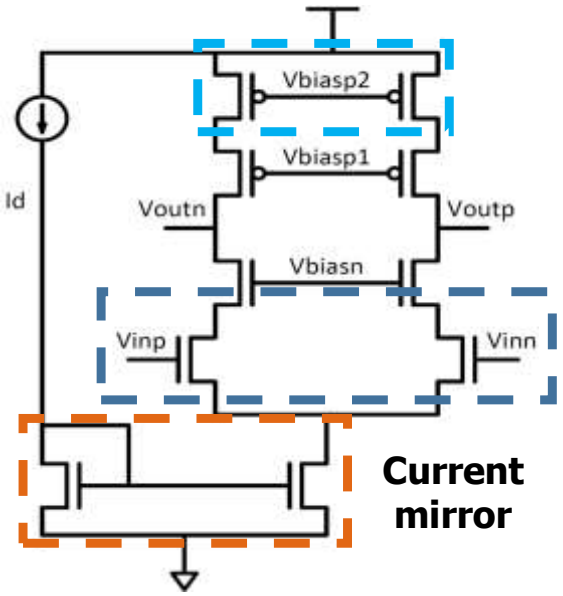
GCN

● = OTA node

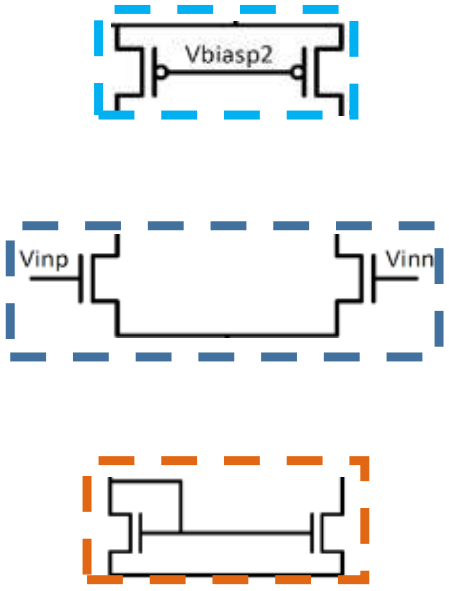


Finding Primitives Within Sub-blocks

Primitives have fixed structures and can be detected using graph matching

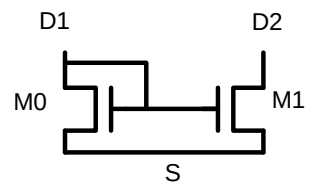


Extracted primitives

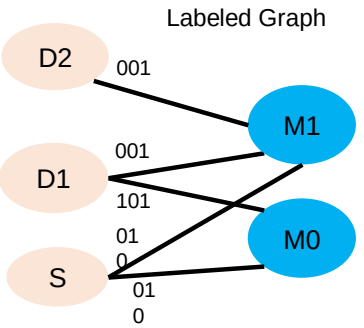


Constraints

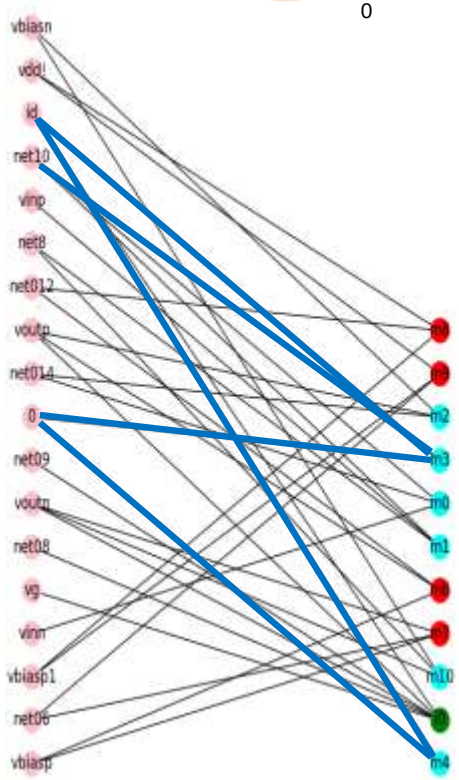
Primitive layout generation



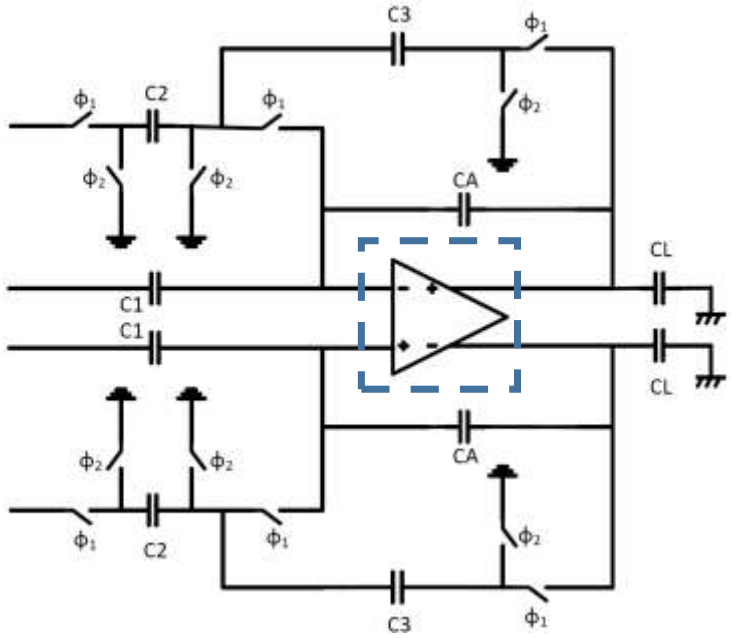
Current mirror



OTA graph



GCN-based Recognition: Switched Capacitor Filter



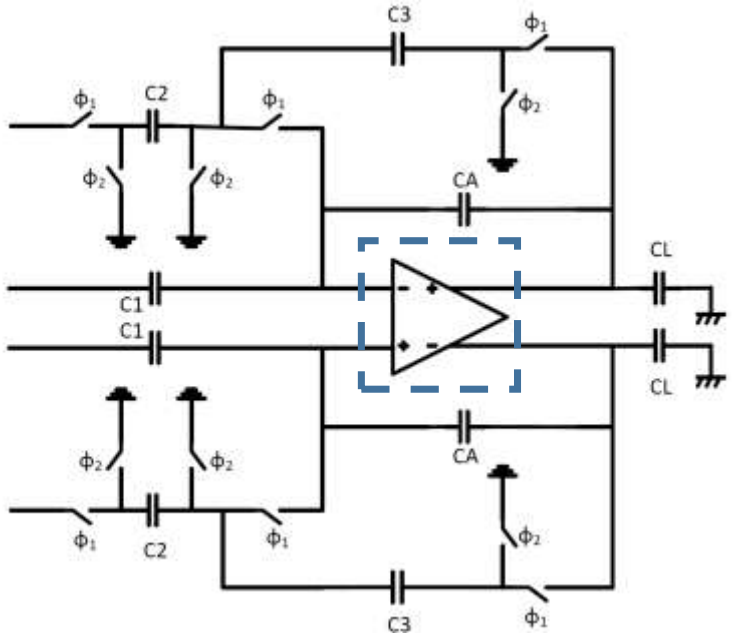
Switched capacitor filter circuit

Actual Class

Predicted class	OTA	BIAS
OTA	21	0
BIAS	1	35

Classification result

GCN-based Recognition: Switched Capacitor Filter



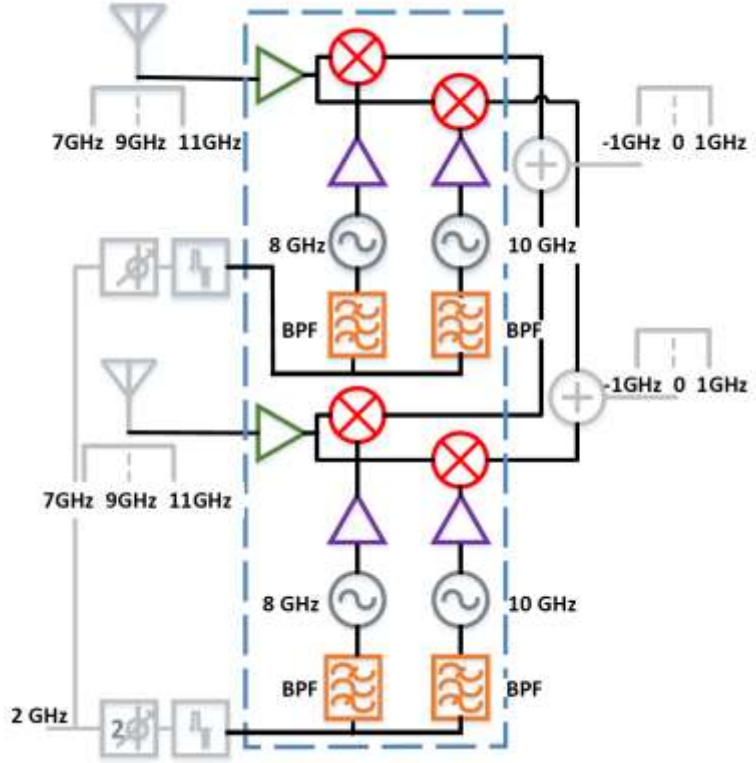
Switched capacitor filter circuit

Actual Class

Predicted class	OTA	BIAS
OTA	22	0
BIAS	0	35

Classification result after postprocessing

GCN-based Recognition: Phased Array Receiver



Phased array receiver

Actual Class

Predicted class

	LNA	MIXER	OSC	BPF	BUF	INV
LNA	78	0	0	0	0	0
MIXER	0	120	0	0	0	0
OSC	0	0	132	0	0	0
BPF	0	0	0	136	0	0
BUF	0	0	0	0	32	0
INV	0	0	0	0	0	24

Classification results after postprocessing

PDK Abstraction: Concepts

Philosophy: Simplify design by restricting layout onto grids

Distance-based design rules become enforced either:

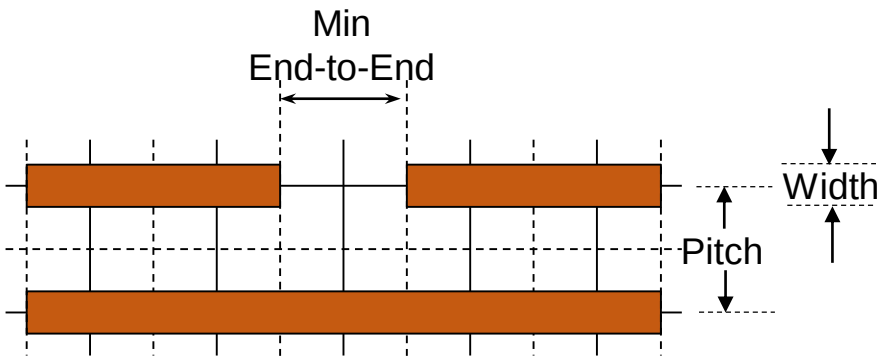
- By adherence of objects to the grid, or
- By Boolean rules relating the presence/absence of objects on the grid

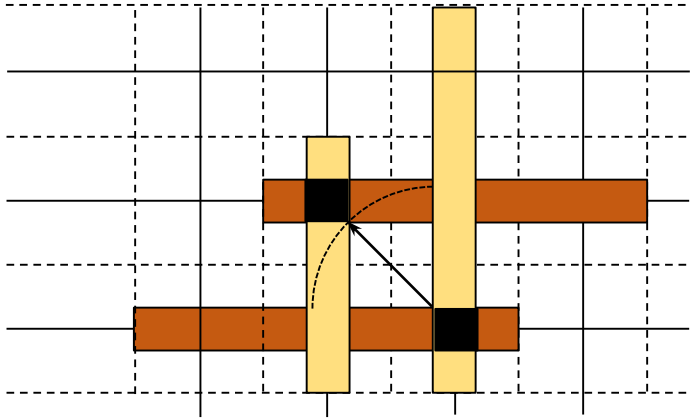
Examples: Pitch, width and space, minimum end-to-end, via rules

~8x reduction in the abstracted rules compared to PDK DRCs

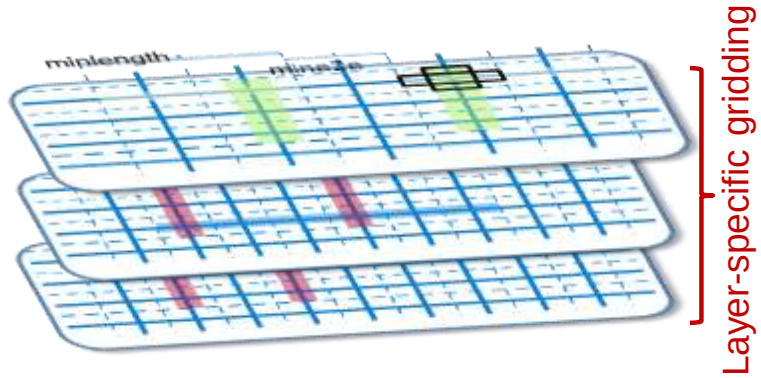
Applied to

- Commercial PDKs (FinFET: GF12/14, Bulk: TSMC65), ASAP7, a FinFET Mock PDK*
- Internally within Intel to 22, 14, 10, 7, 5, 3nm process technologies





Via-to-via rule: diagonal vias disallowed



[* Design rules for FinFET MockPDK available on ALIGN github]

PDK Abstraction: Creating Grids

Simpler regular grid generated from common code and process constants stored in JSON format

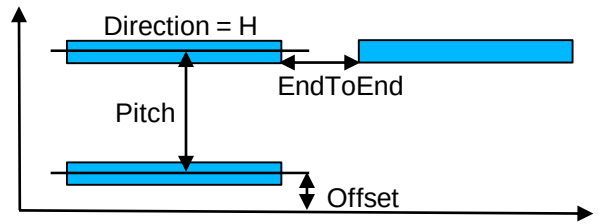
Adequate for GF12, ASAP7, TSMC65

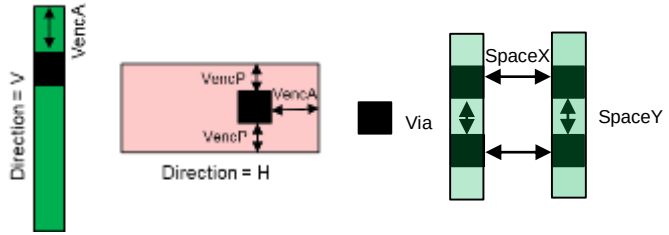
Python syntax used to denote custom gridding patterns

Needed for latest Intel processes: 14nm, 10nm, 7nm, and beyond

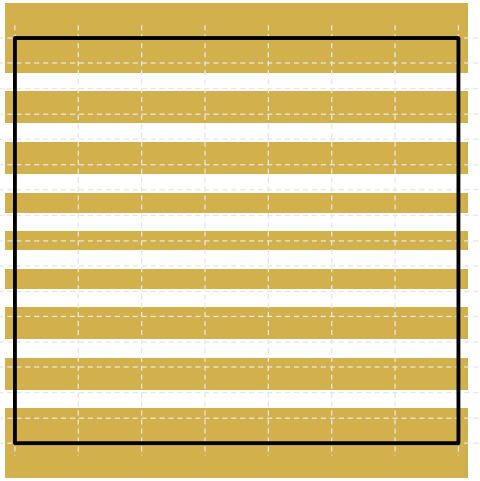

```
"Layer": "M2",
"LayerNo": 8,
"Direction": "H",
"Color": ["c2", "c1"],
"Pitch": 84,
"Width": 32,
"MinL": 200,
"MaxL": null,
"EndToEnd": 48,
"Offset": 0
```

```
"Layer": "V2",
"LayerNo": 15,
"Stack": ["M2", "M3"],
"SpaceX": 76,
"SpaceY": 76,
"WidthX": 32,
"WidthY": 32,
"VencA_L": 20,
"VencA_H": 20,
"VencP_L": 0,
"VencP_H": 4,
"MinNo": 1
```

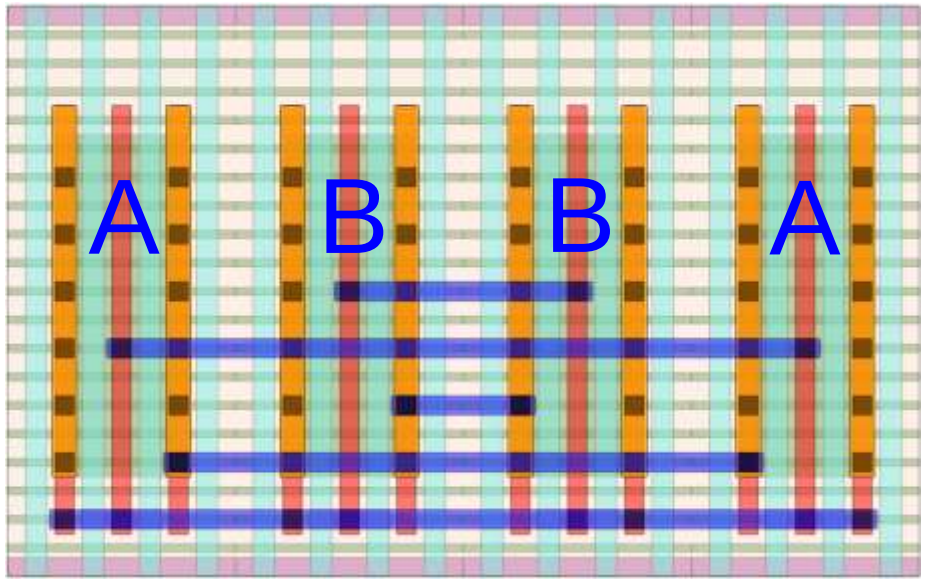



```
c = 0
a = [w,m,m,n,n,n,m,m,w]
for (u,v) in zip(a[:-1],a[1:]):
   m0.addCenterLine( c, u)
   c += u//2 + s + v//2
m0.addCenterLine( c, a[-1])
```

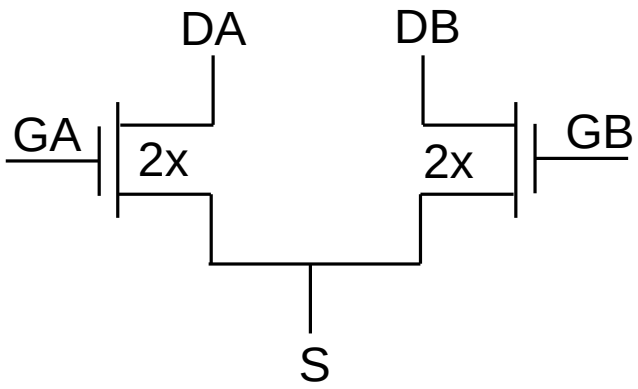


Primitive Cell Generation: Multiple Layout Patterns

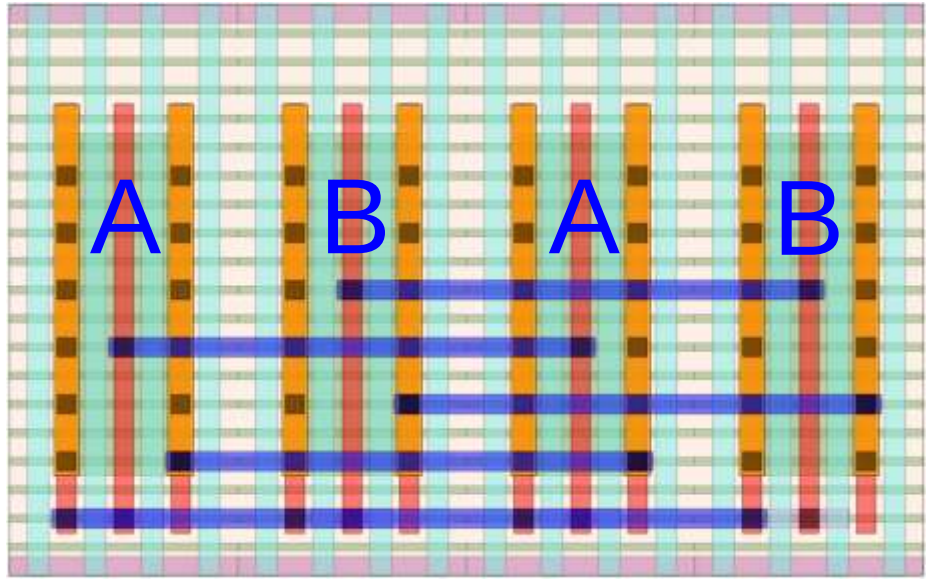
Cell generation module can generate two different patterns: Common centroid and Interdigitated



Common centroid

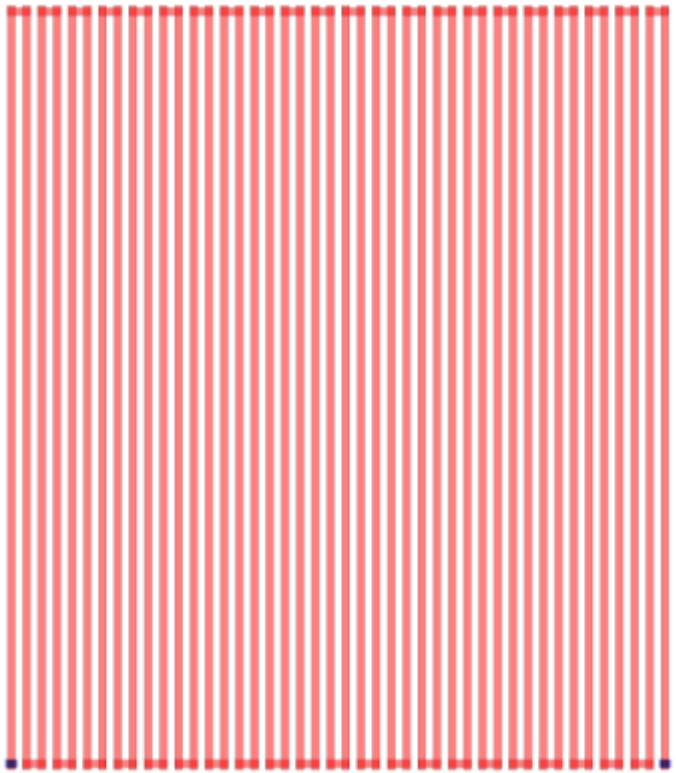


Differential pair

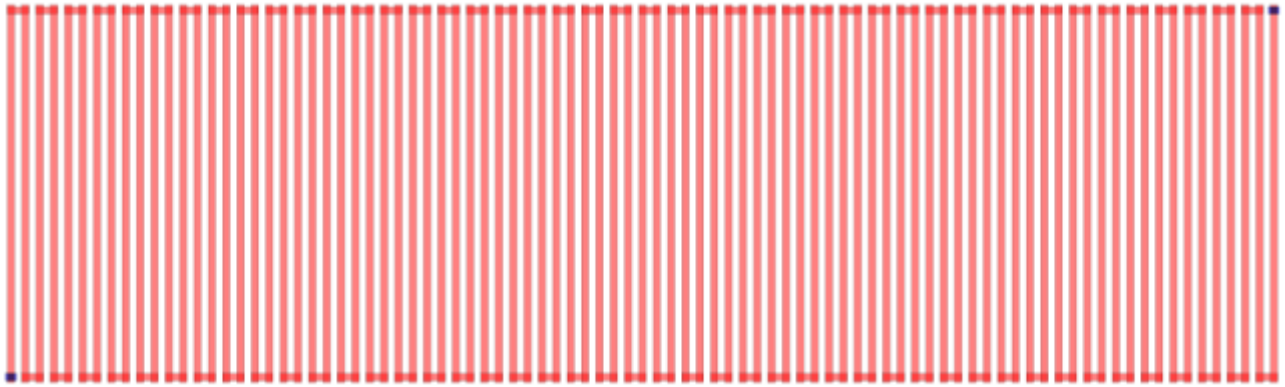


Interdigitated

Primitive Cell Generation: Multiple Aspect Ratios

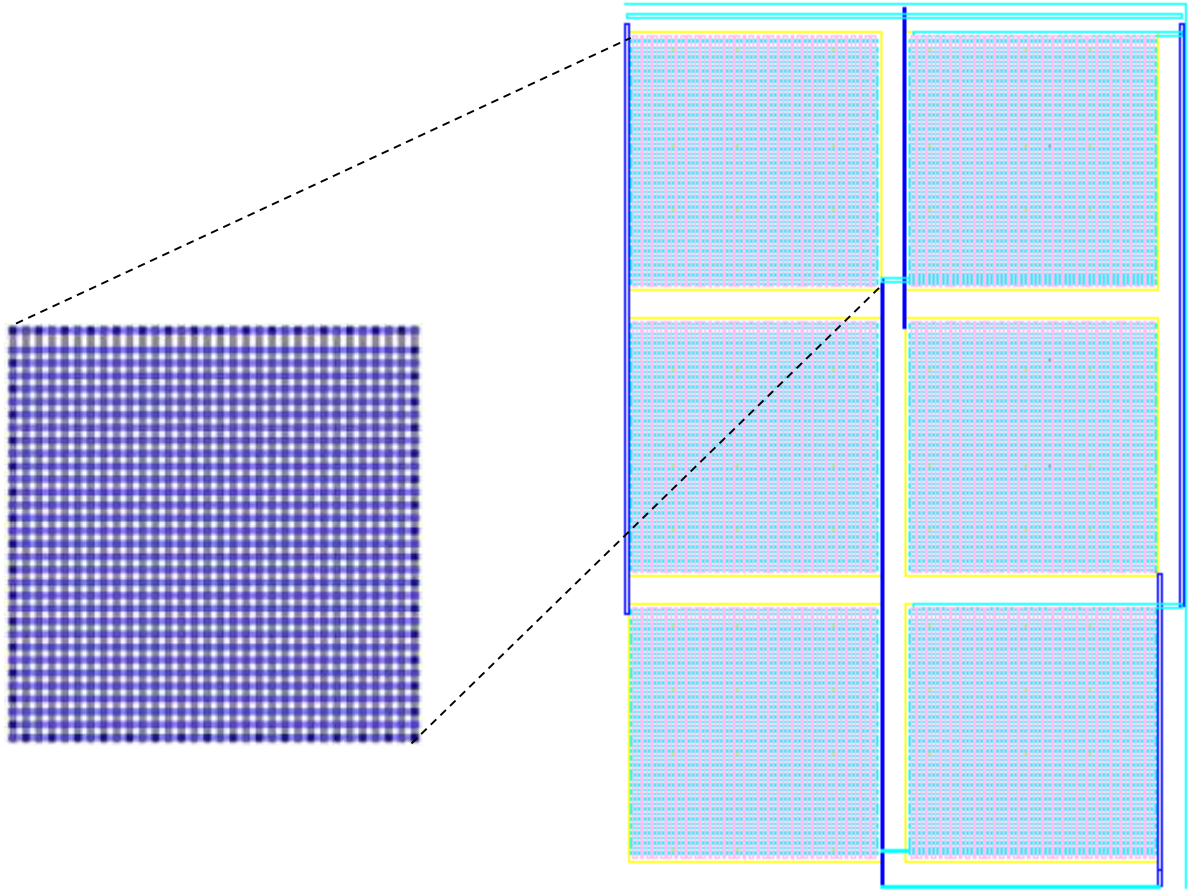


10K resistor
Aspect Ratio:1x2



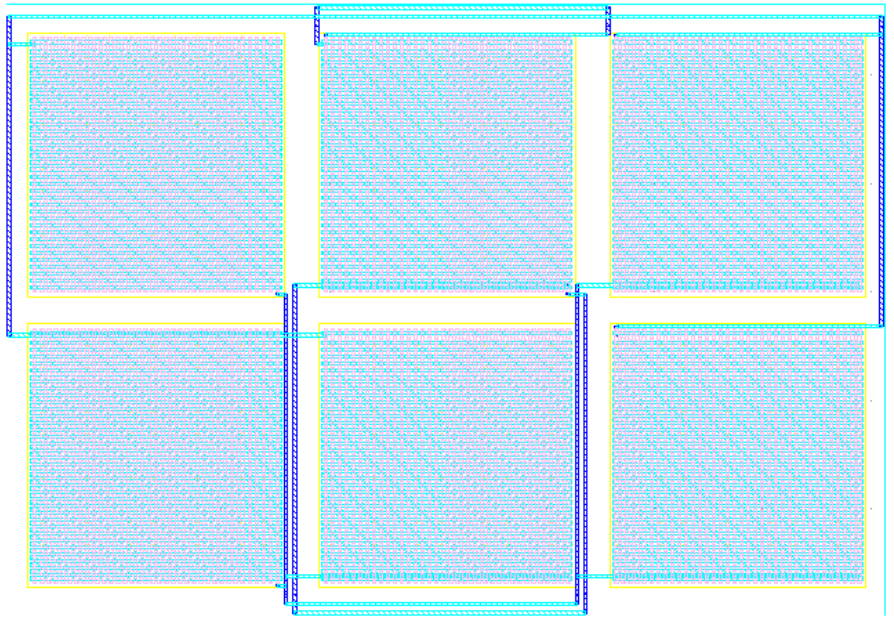
10K resistor
Aspect Ratio: 2x1

Primitive Cell Generation: Capacitors and Arrays



Unit Capacitor: 10fF

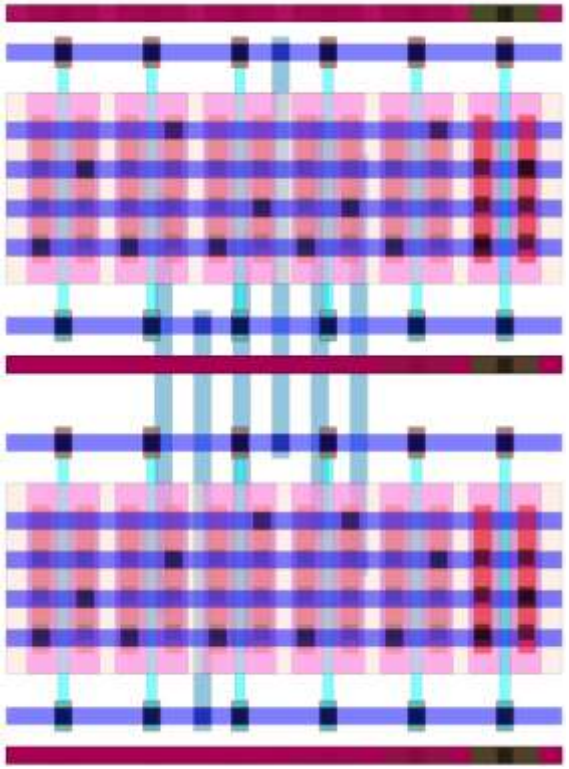
50fF Capacitor Array
Aspect Ratio: 2x3



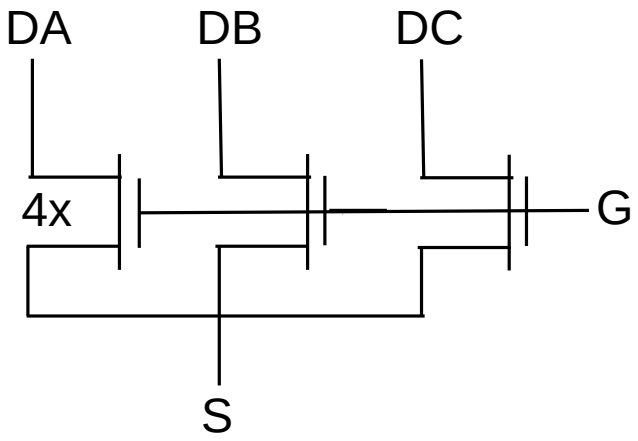
50fF Capacitor Array
Aspect Ratio: 3x2

Primitive Cell Generation: Bulk Technology

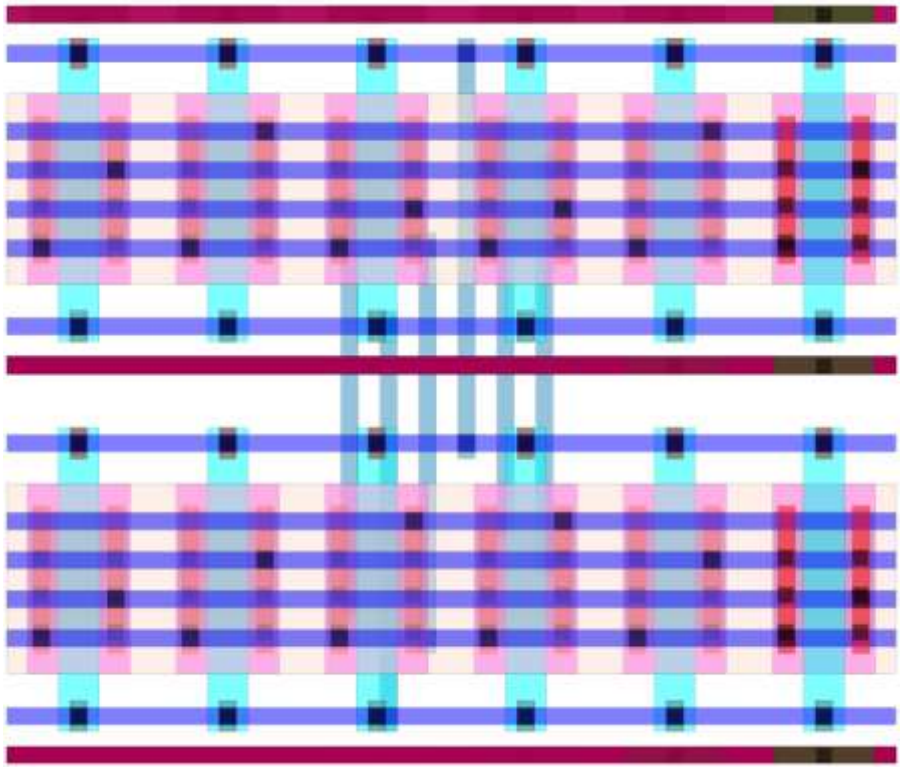
In a bulk technology cells are parameterized by # Fingers, active width, gate length ..



Lg: Lmin



Current mirror bank



Lg: 4xLmin

Primitive Cell Generation: User-specified Primitives

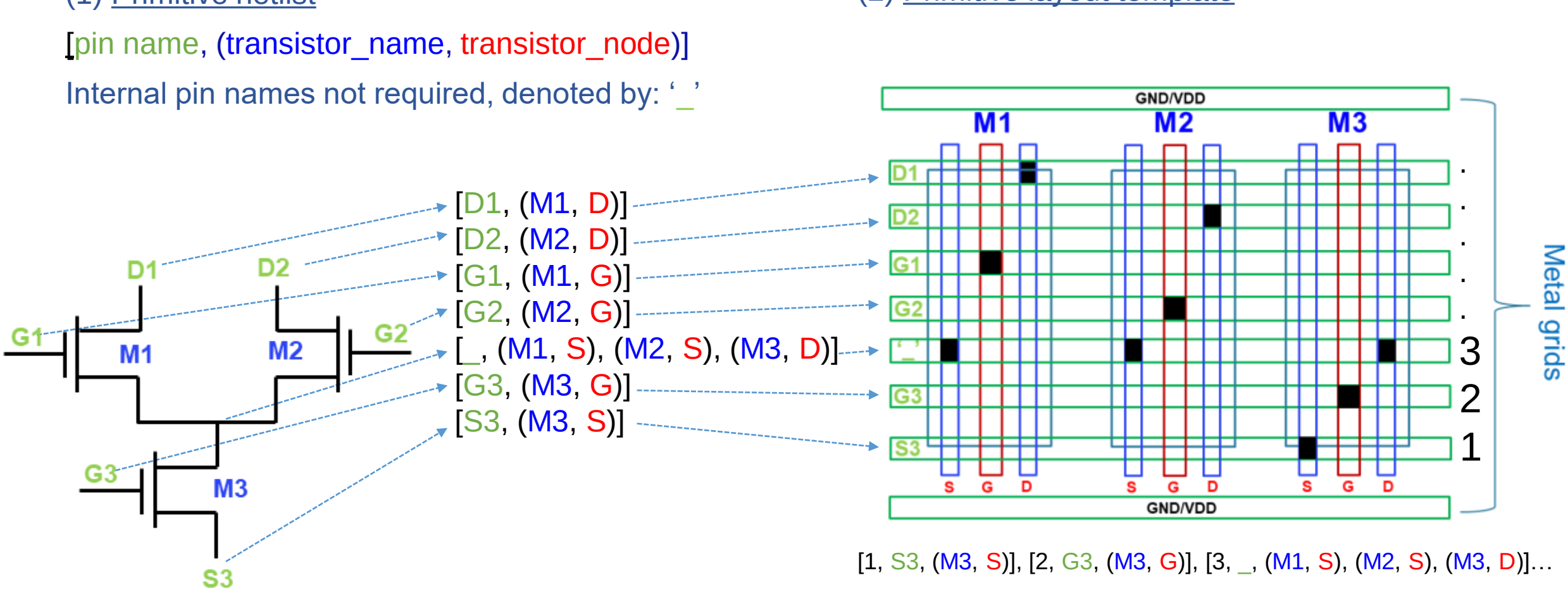
The user can specify new primitives by providing:

(1) Primitive netlist

[pin name, (transistor_name, transistor_node)]

Internal pin names not required, denoted by: '_'

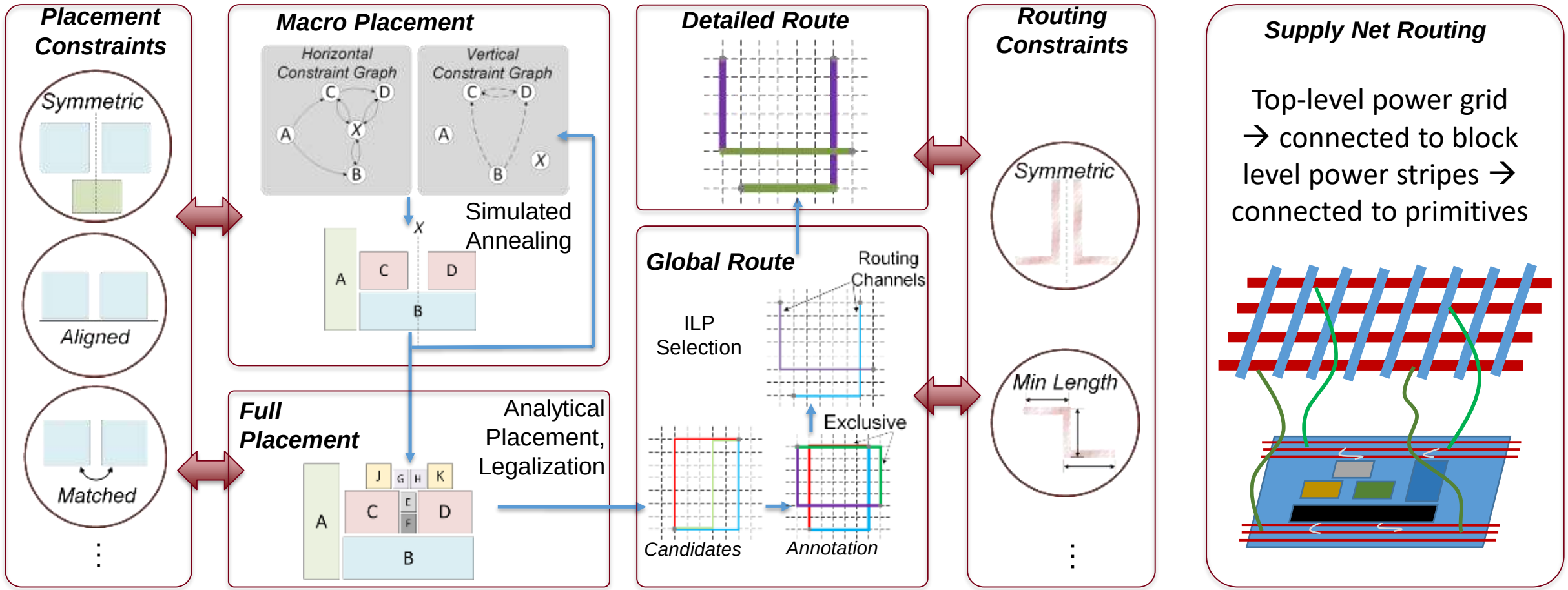
(2) Primitive layout template



Block Assembly, Placement and Routing

Primitives >> sub-blocks >> larger sub-blocks >> system assembly

Incorporates analog constraints at every stage (including constraints "pushed up" from primitives)



Block Assembly, Placement and Routing: Multiple Aspect Ratios

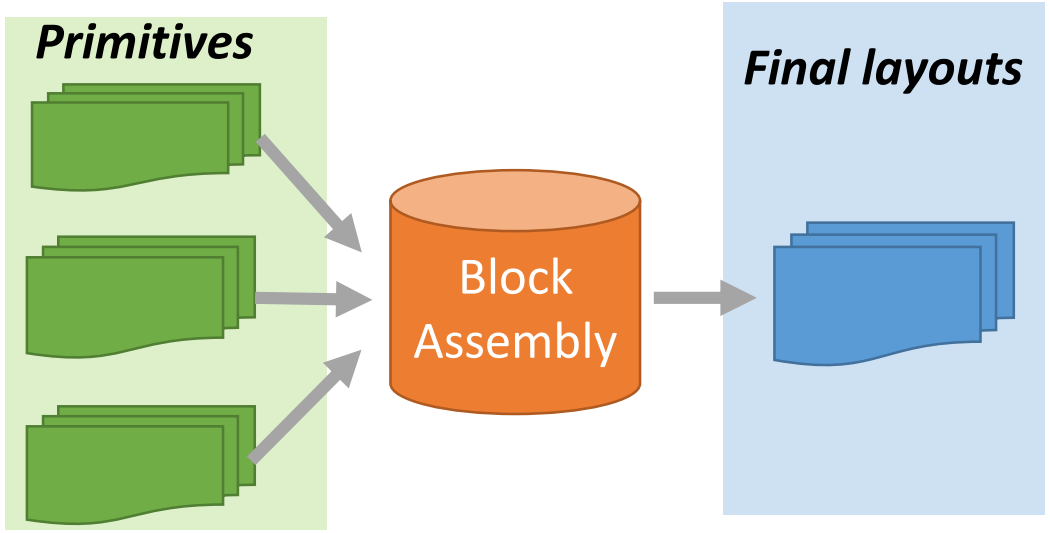
Flexible block assembly for layouts in multi aspect ratios

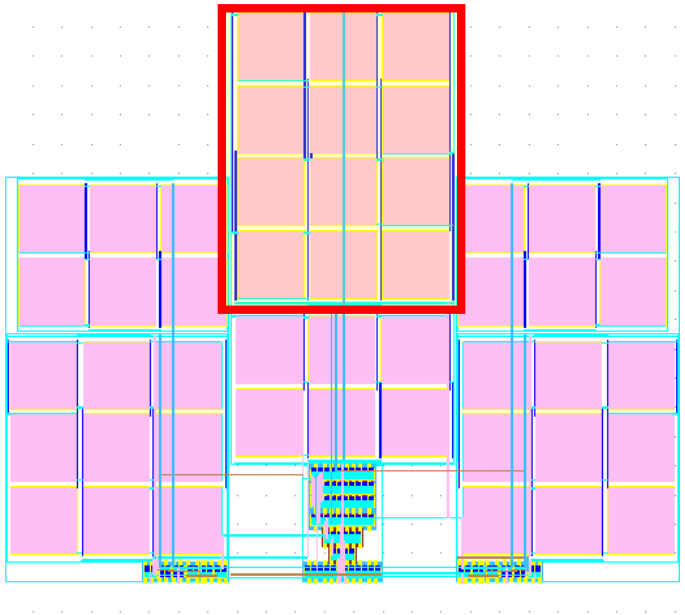
Input primitives

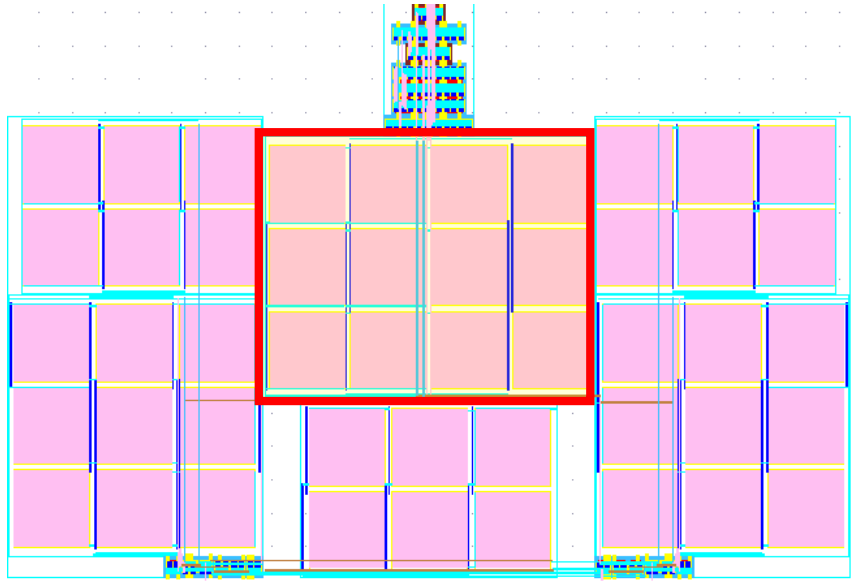
- Single block schematic
- Multiple sets of layouts in different aspect ratios

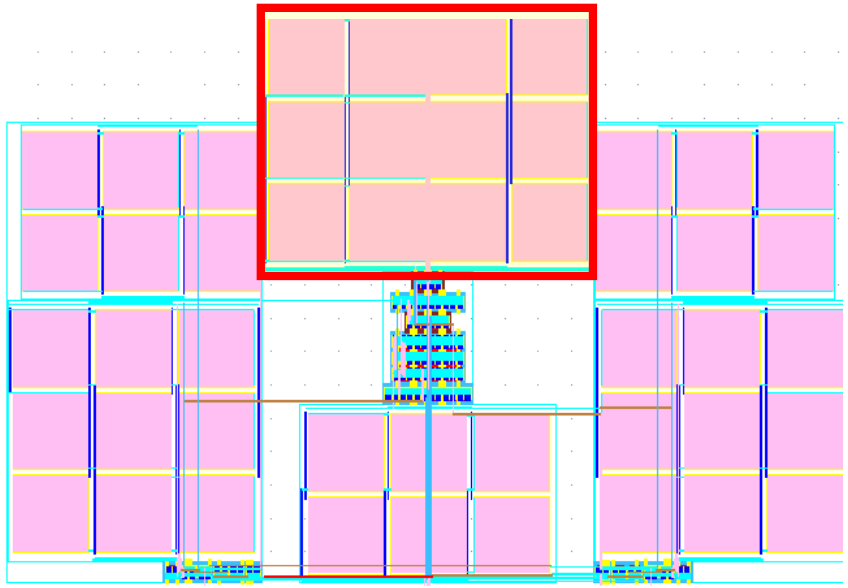
Output layouts

- Different combinations of primitive block layouts
- Multiple layouts in different aspect ratios









Intel Analog Detailed Router

We have open-sourced (BSD 3-clause license) Intel's existing internally developed detailed router for analog circuits: https://github.com/ALIGN-analoglayout/AnalogDetailedRouter

Inputs:

- Grid Abstraction of Process and Design Rules
- Terminals (Connected Entities)
- Existing Physical Wires
- Global Routes

Output:

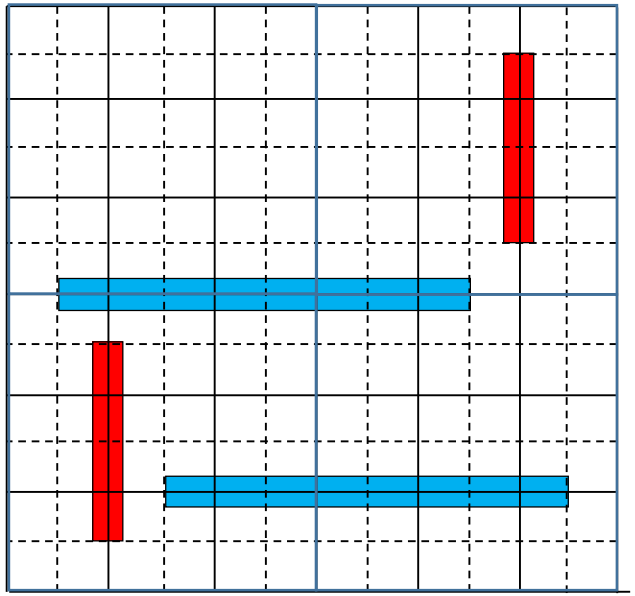
- Detailed routes connecting at least one terminal from each CE

Approach:

- Generate multiple candidate routing segments and use SAT to select a set of segments that connects the terminals (for all nets simultaneously) without creating shorts and design rule violations.

Features:

- Applied to multiple processes within Intel (10, 14, 22FFL, 7, …)
- Allows different grid templates in different regions of the block
- Follows global routes (specifies most analog constraints)
- Expands global route into multiple detailed tracks (max current)



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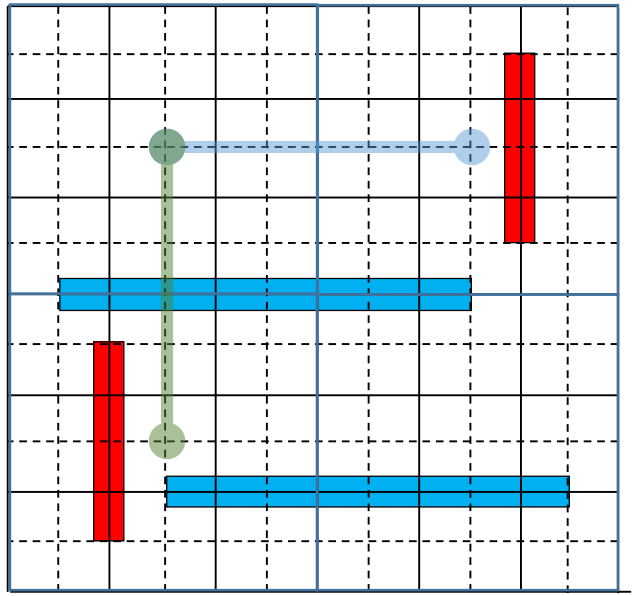

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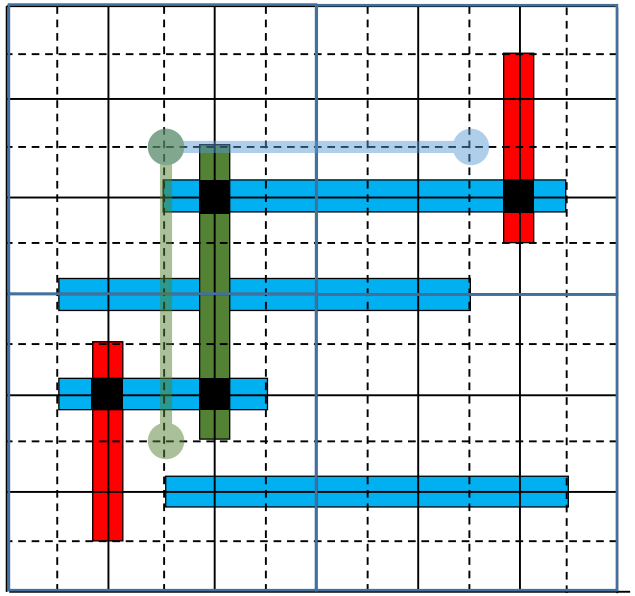

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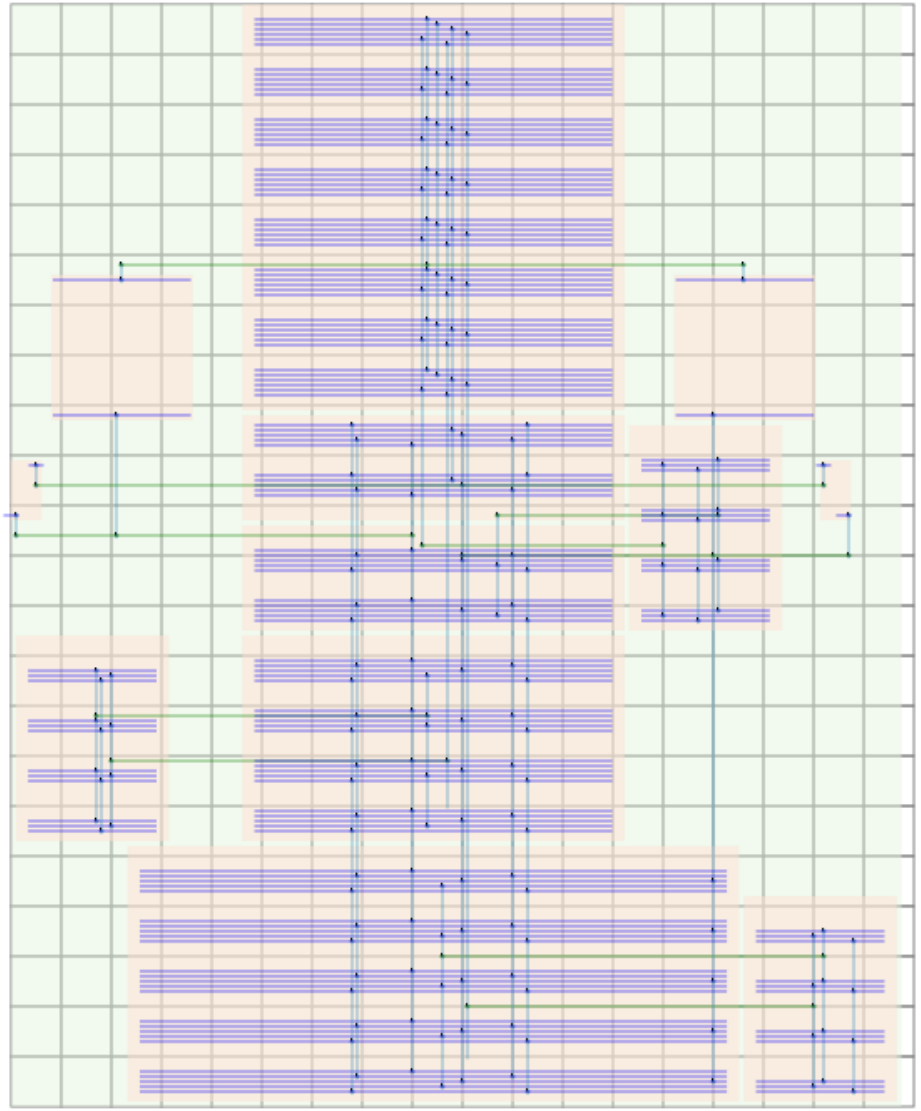
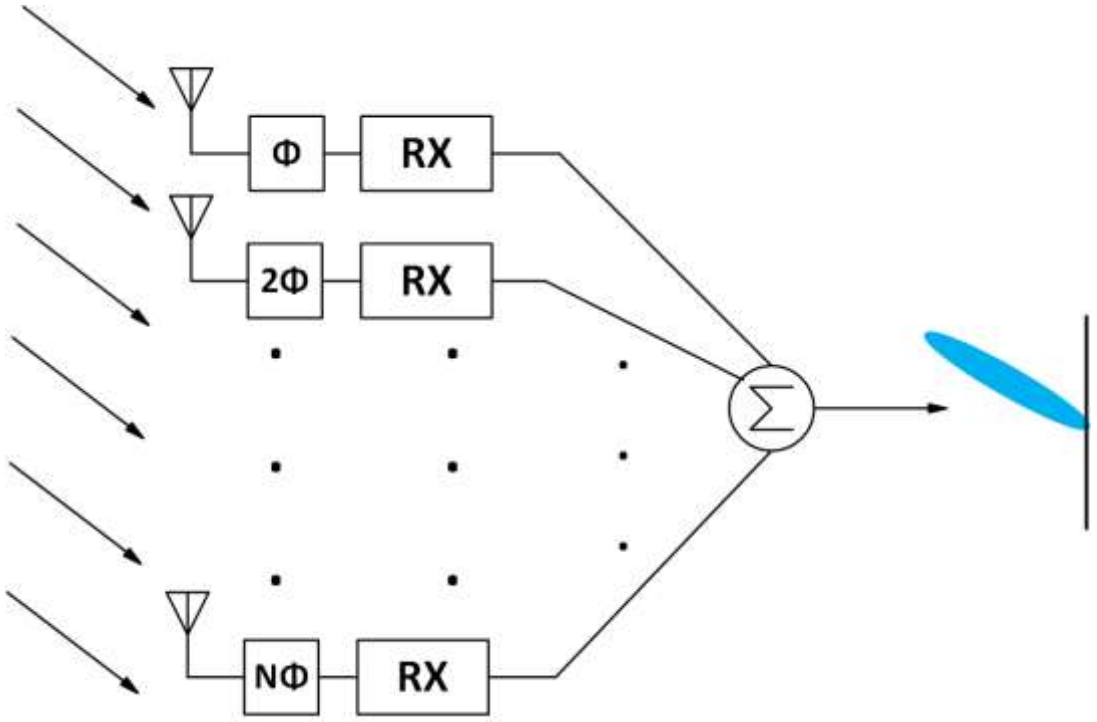


9GHz Phased Array

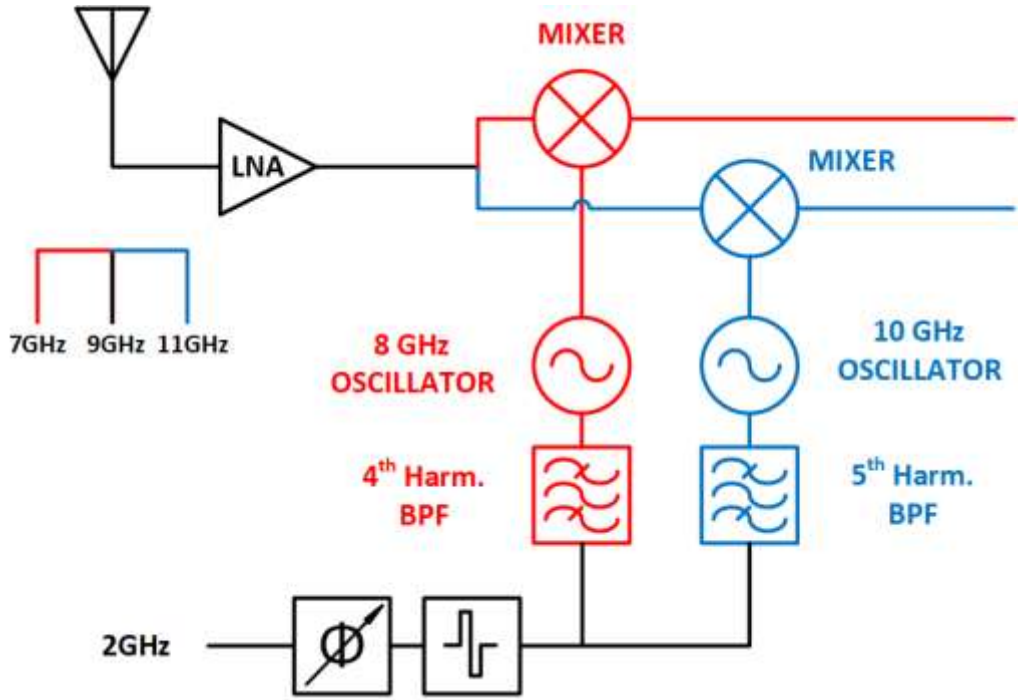
Phased Array Receiver: Components

Applications:
- mm-Wave communication (5G)
- RADAR

Design Blocks:
- Low noise amplifier (LNA)
- Mixer
- Oscillator
- Band pass filter (BPF)



Phased array receiver block diagram

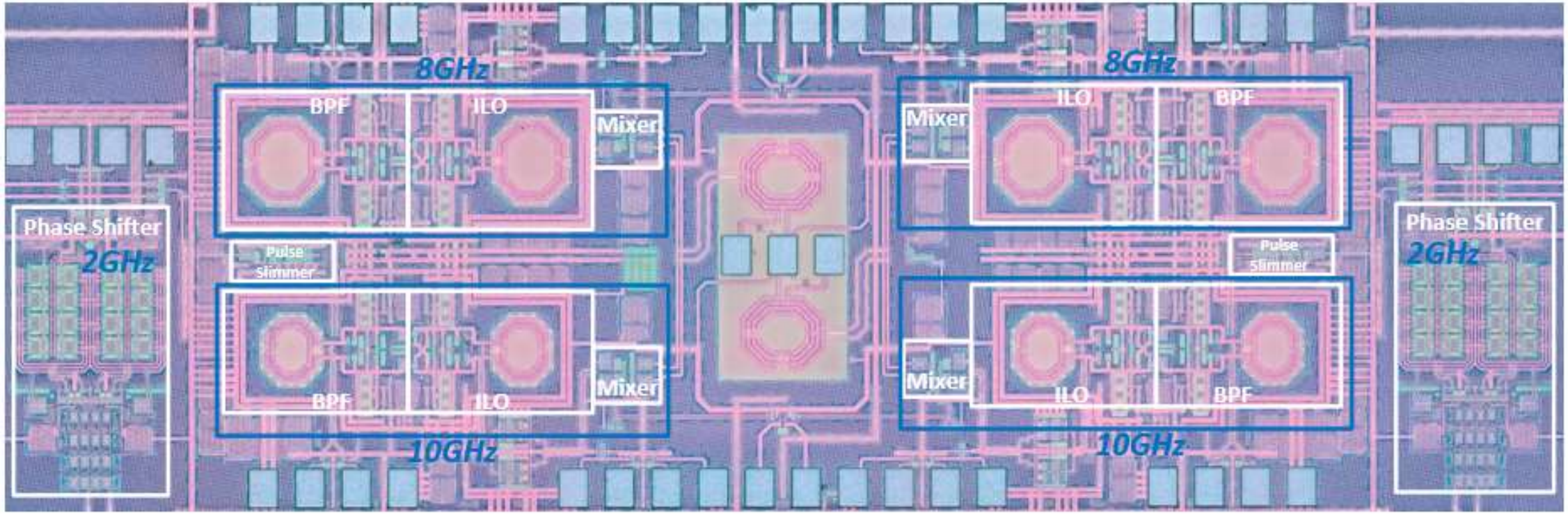


Wideband receiver block diagram

Phased Array Receiver: Chip Micrograph

TSMC's 65nm GP CMOS process

Active area (excluding test circuits) is 2.7mm^2



[ESSCIRC 2018]

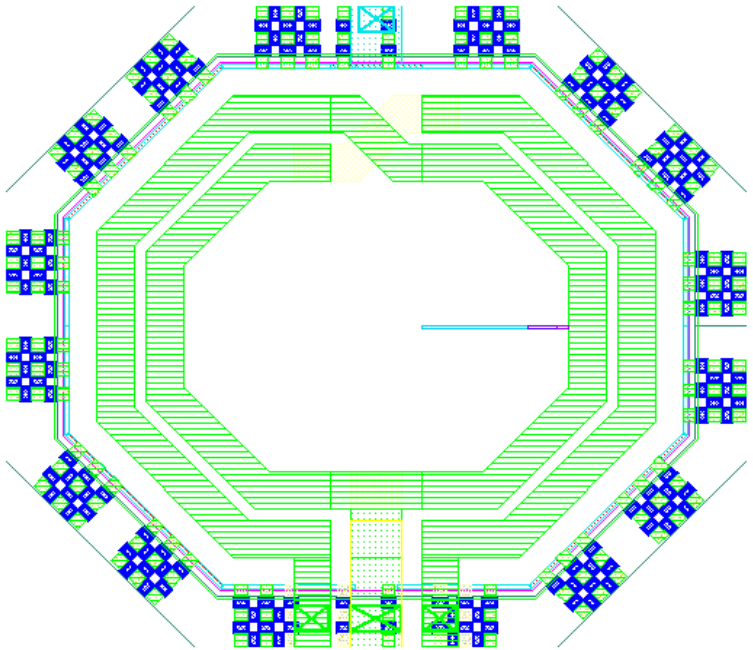
Hand Crafted

Phased Array Receiver: Cell Generation

Special PDK Cells (RF transistors, inductors, capacitors, etc.) are characterized and non-gridded.

The cells are treated as black box

- We make sure that the cell pins are on grids so that our PnR tool can make connections in between the blocks.



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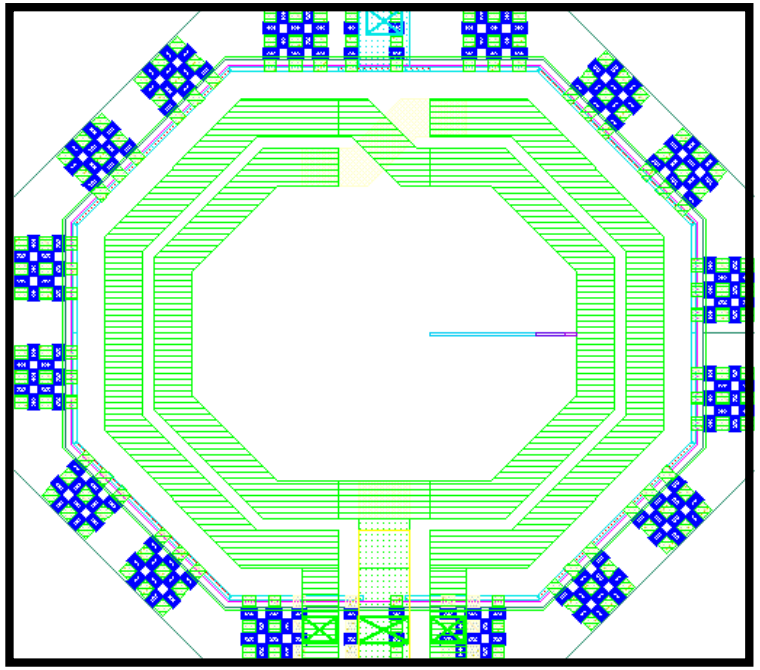

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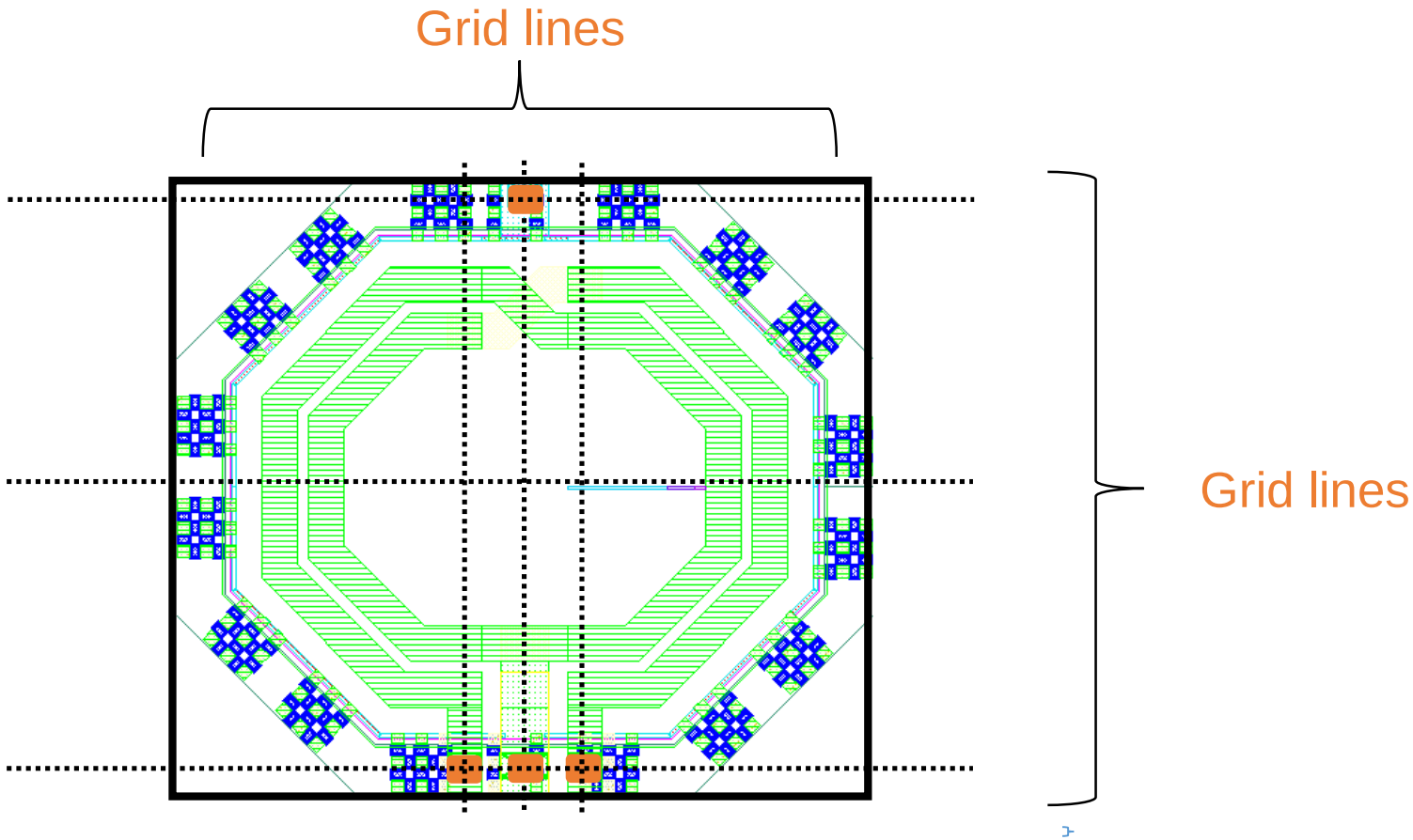

Inductor cell from PDK treated as a black box

Phased Array Receiver: Cell Generation

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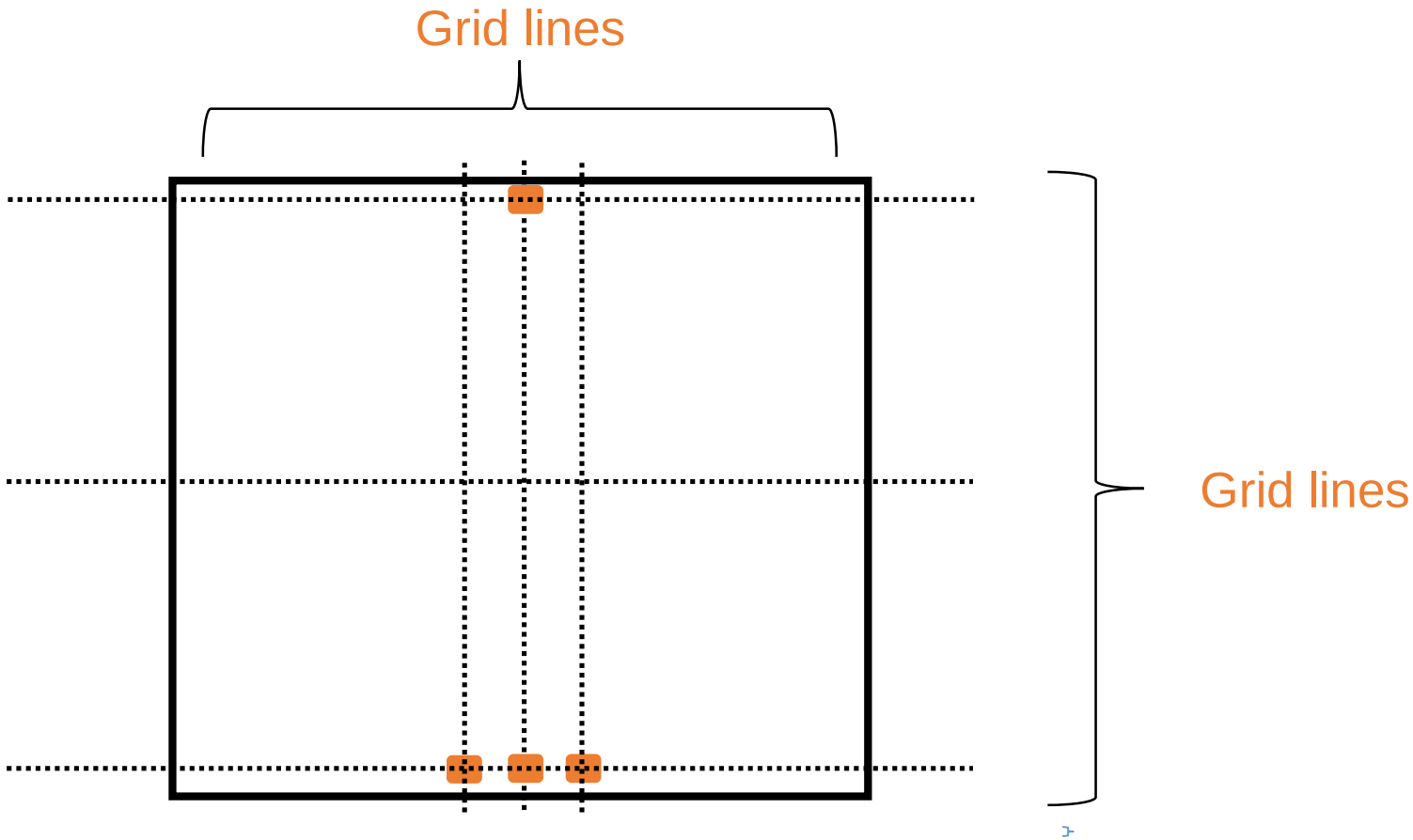
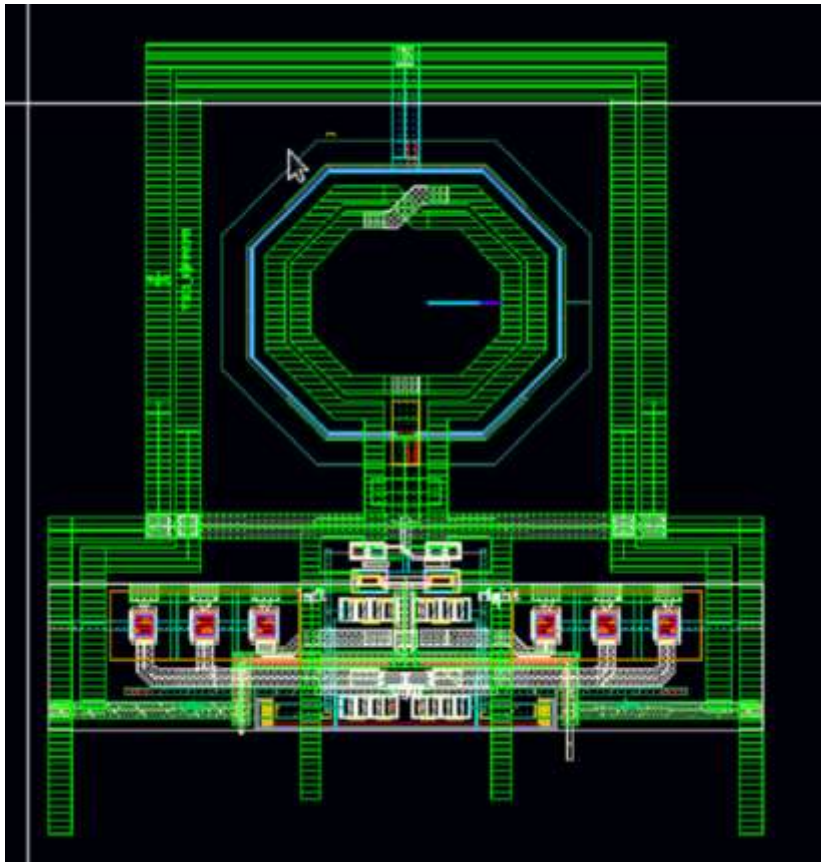


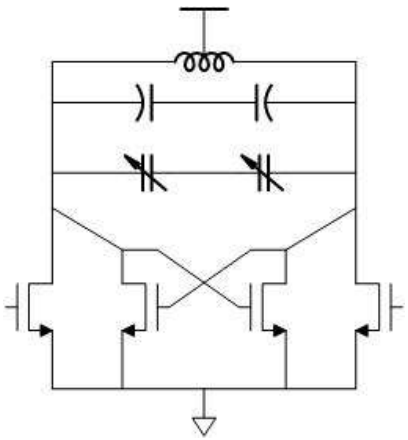
Inductor cell from PDK treated as a black box

Phased Array Receiver: Block Layouts

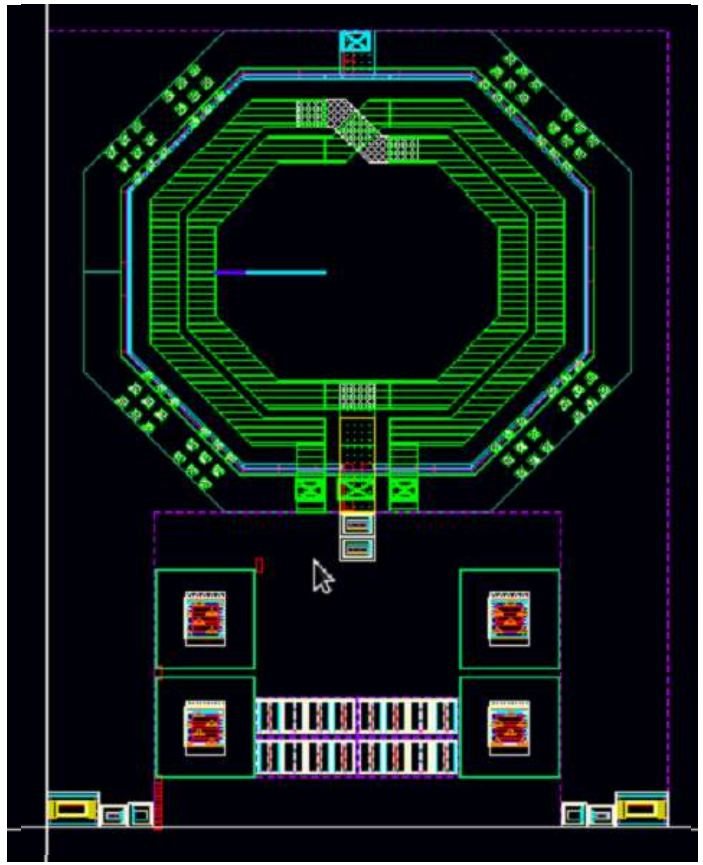
Band pass filter (BPF)



Hand-Crafted layout



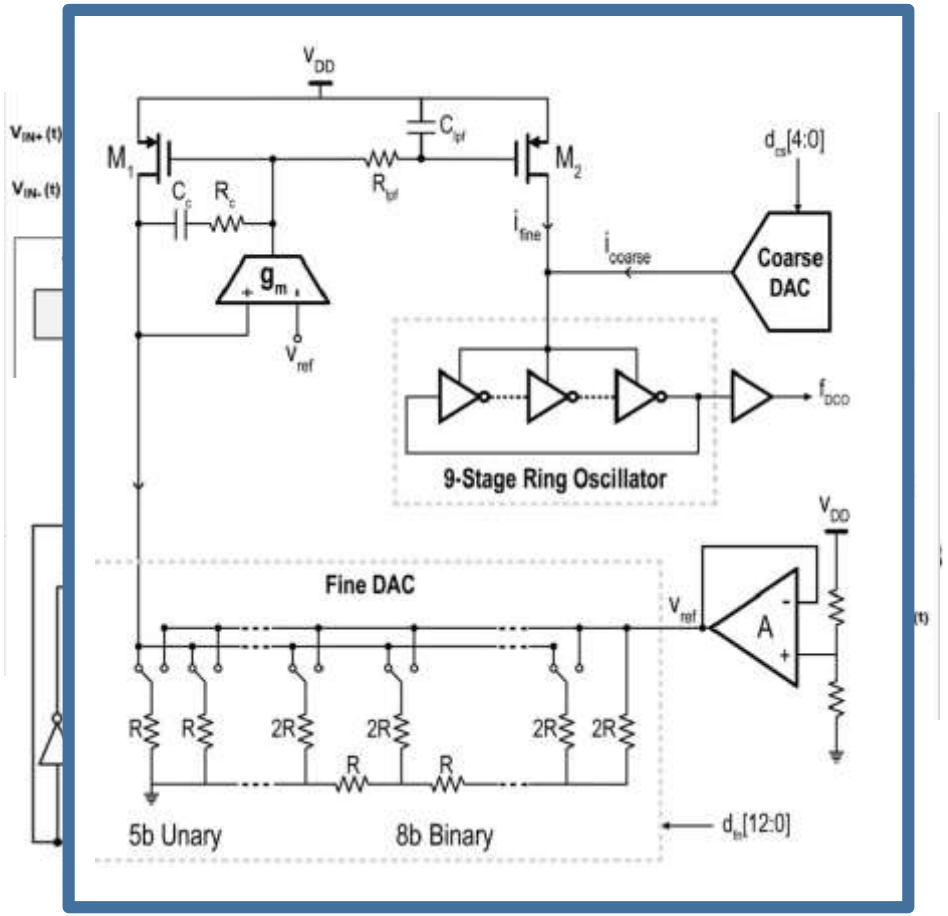
BPF schematic

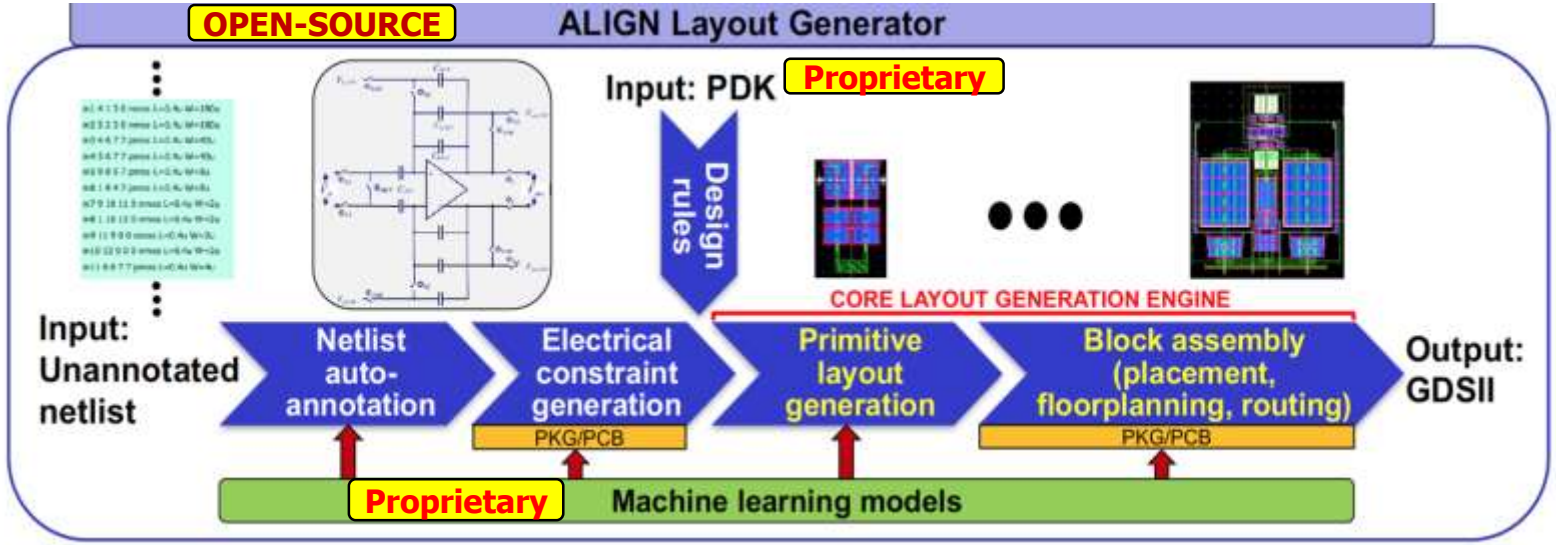


ALIGN generated layout

ALIGN: General & Extendable

Digitally Controlled Oscillator (DCO): ISSCC 2018 …





ALIGN: General & Extendable

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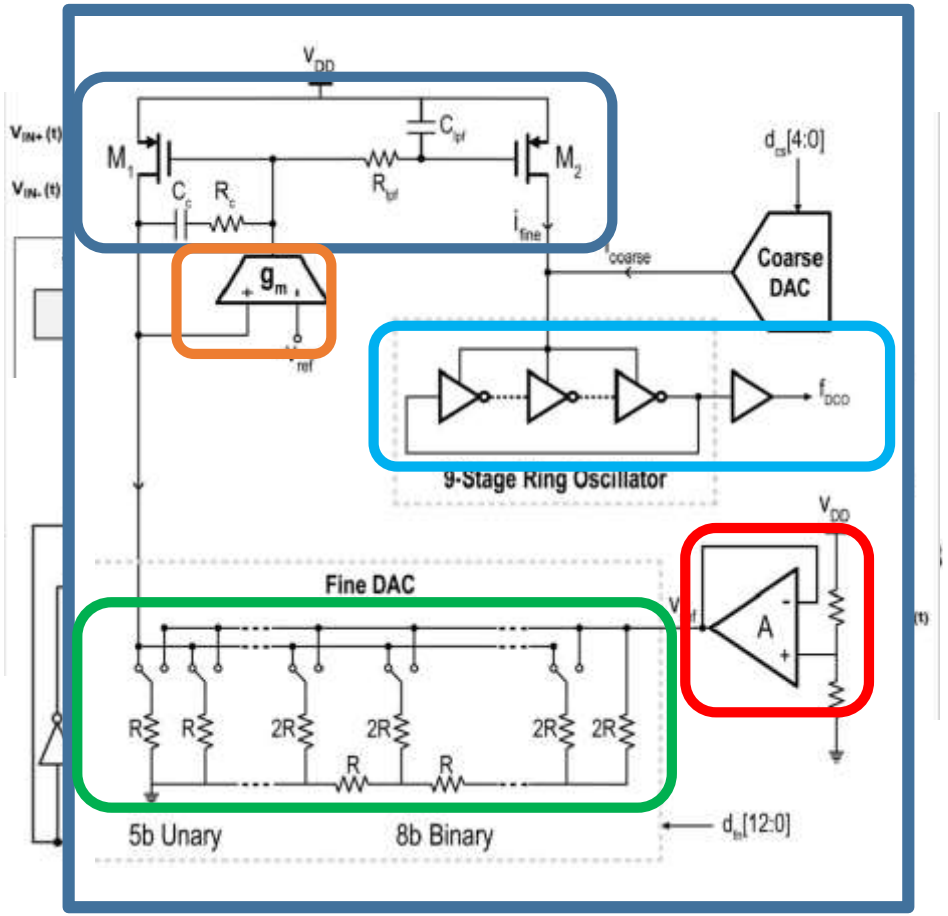
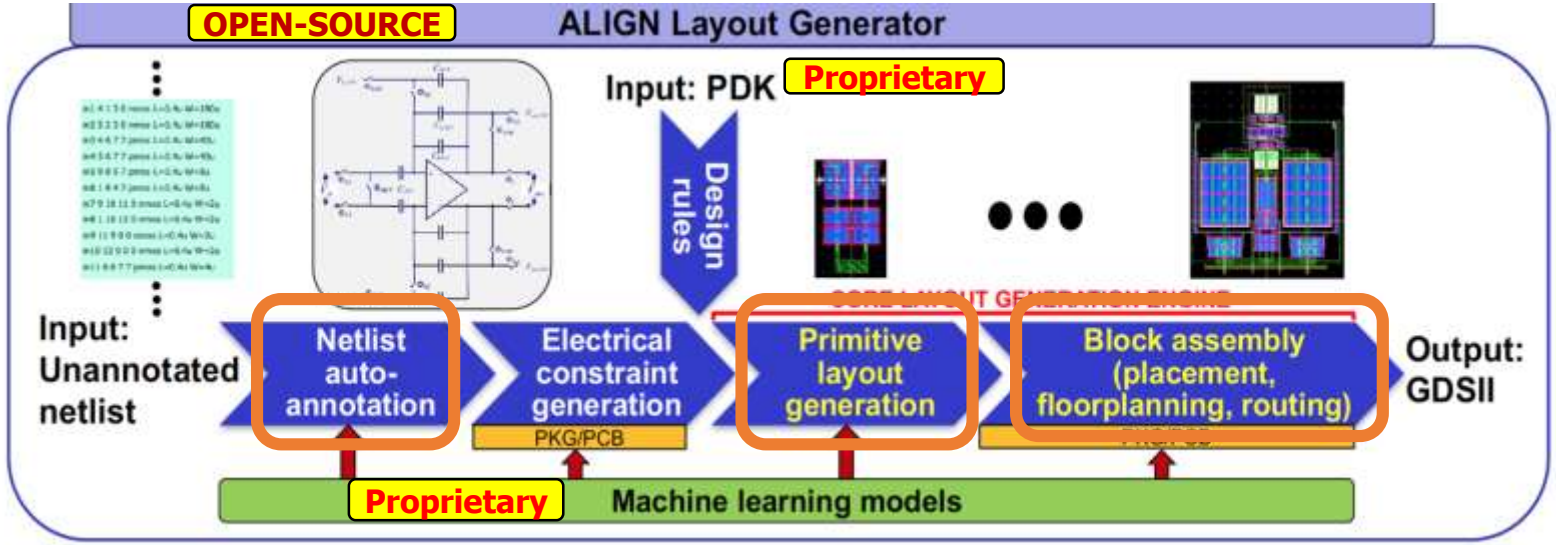
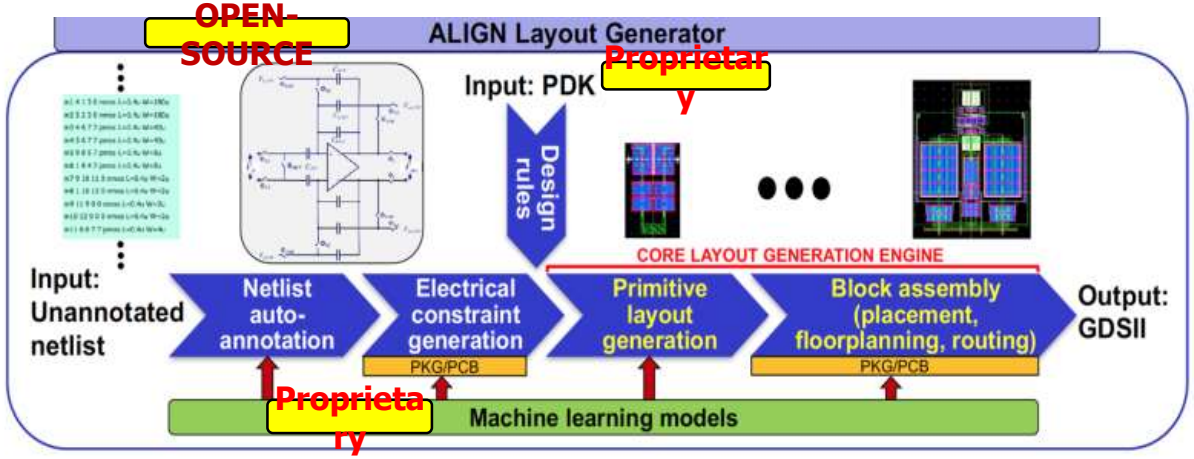




ALIGN: Push Button Layout Compiler

Alpha release: https://github.com/ALIGN-analoglayout/ALIGN-public



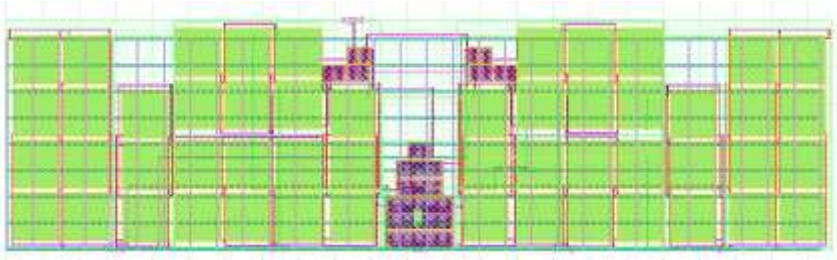
Progress since the Jan integration meeting

- Global routing/ Detailed routing
- Performance analysis
- More classes in ML based recognition
- Cell generation for RF cells and bulk technologies

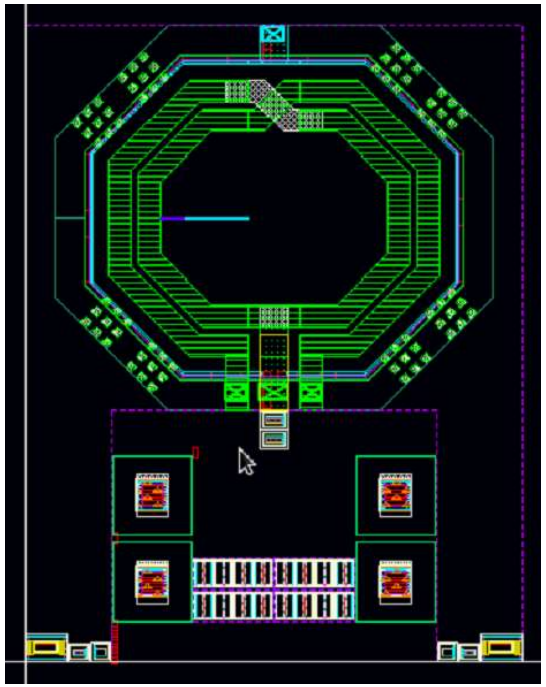
DEMO

- OTA
- Switched-capacitor filter
- Wireline equalizer (offline)

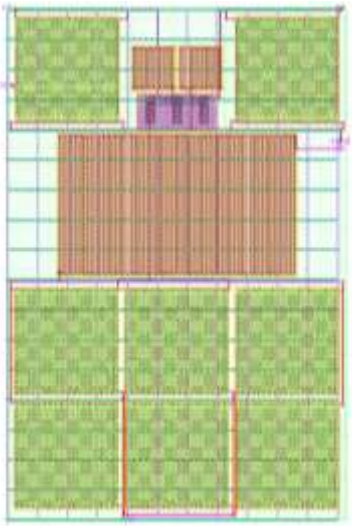
Any Questions?



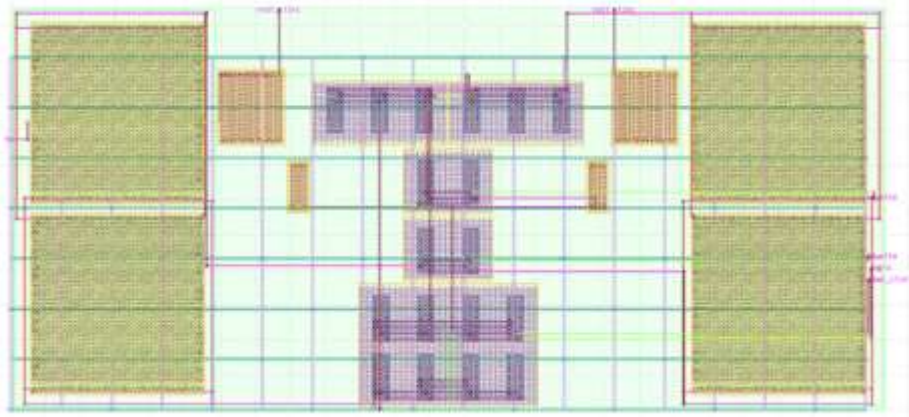
Switched capacitor filter [Mock FinFET]



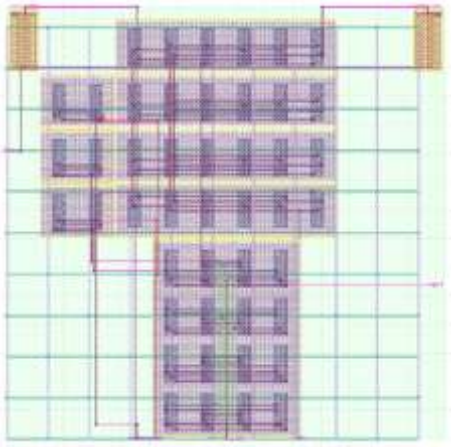
Bandpass Filter [Bulk 65nm]



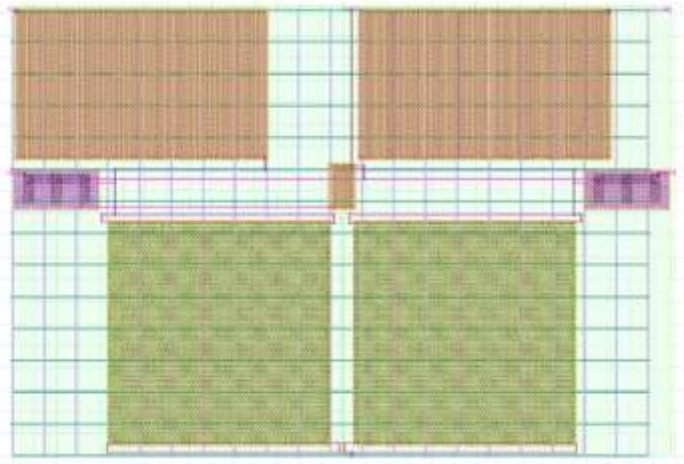
Single to differential converter [Mock FinFET]



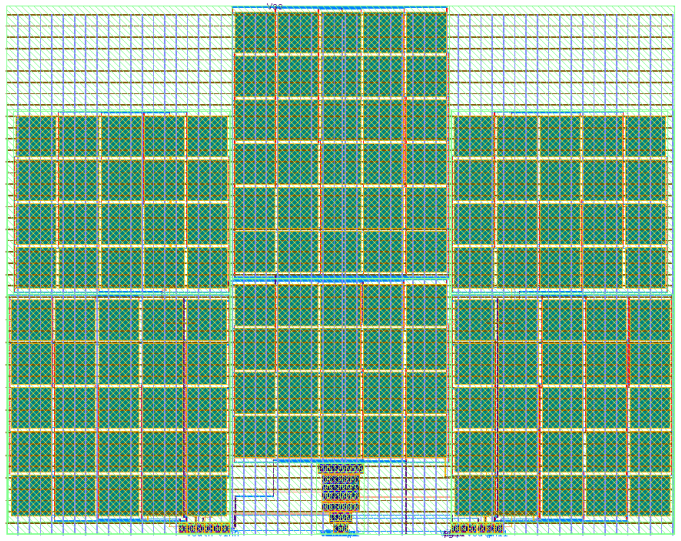
Linear equalizer [Mock FinFET]



Variable gain amplifier [Mock FinFET]



Adder [Mock FinFET]



Switched capacitor filter [ASAP7nm]

The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.