4-bit Processor

Registers Information:

Memory : 16x8 bit
AR, PC, DR, AC,INPR,OUTR : 4 Bit
IR : 8 Bit

Commands Set:

Fetch	T_0:	AR ←PC
	T_1:	IR ← M[AR], PC ← PC + 1
Decode	T_2:	DO...D15 ← Decode IR(4 - 7), AR ← IR(0 – 3)
Memory Reference		
AND	D_0T_3	DR ← M[AR]
	D_0T_4	AC ←AC ∧ DR, SC ← 0
ADD	D_1T_3	DR ← M[AR]
	D_1T_4	AC ←AC + DR, E ← C_{out}, SC ← 0
LDA	D_2T_3	DR ← M[AR]
	D_2T_4	AC ← DR, SC ← 0
STA	D_3T_3	M[AR] ←AC, SC ←0
BUN	D_4T_3	PC ←AR, SC ←0
BSA	D_5T_3	M[AR] ← PC, AR ← AR + 1
	D_5T_4	PC ←AR, SC ←0
RET	D_6T_3	PC ← M[AR], SC ← 0
Register-Reference		
CLA	D_7T_3:	AC ←0
CLE	D_8T_3:	E←0
CMA	D_9T_3:	AC ←AC'
INC	$D_{10}T_3$:	AC ←AC + 1
CIR	$D_{11}T_3$:	AC ← shr AC, AC(3) ← E, E ← AC(0)
CIL	$D_{12}T_3$:	AC ← shl AC, AC(0) ← E, E ←AC(3)
INP	$D_{13}T_3$:	AC ← INPR
OUT	$D_{14}T_3$:	OUTR ← AC
HLT	$D_{15}T_3$:	S←0