RT-HIL Hardware Prototyping of Synchrophasor and Active Load-Based Power System Oscillation Damping Controller

G.M. Jonsdottir*, M.S. Almas*, M. Baudette*, M.P. Palsson¶, L. Vanfretti*†
*SmarTS Lab, KTH-Royal Institute of Technology, Stockholm, Sweden
Email: {gmjon, msalmas, baudette, luigiv}@kth.se
†R&D Department, Statnett SF, Oslo, Norway, Email: luigi.vanfretti@statnett.no
¶System Planning Department, Landsnet, Reykjavik, Iceland, Email: magnip@landsnet.is

***Abstract*—The Icelandic power system is characterized by two areas that oscillate against each other during stressed system operation, and may lead to an islanding of system. Conventional stabilizing methods are being used to their full capacity, thus new options are being explored to prevent system break-ups. There is potential in exploiting large industrial loads to enhance system stability. In this paper a hardware prototype of a synchrophasor-based active load controller for oscillation damping is presented. The performance of the controller is analysed using Real-Time Hardware-in-the-Loop (RT-HIL) approach.**

***Index Terms*—Active Load Control, Oscillation Damping, Real-Time Hardware-in-the-Loop, Hardware Prototype, Wide-Area Control System, Phasor Measurement Unit**

I. Introduction

The Icelandic power system consists of two meshed 220 kV networks, located in the south-western and the eastern part of the island. The generation (hydro and geothermal plants) and the load (the capital region, two aluminium smelters and other industrial loads) are mainly concentrated in the south-western region. The eastern network consists of a 6×115 MW hydro plant feeding an aluminium smelter. These networks are interconnected through two 132 kV transmission lines, forming a ring around the island. There is an active power transmission limit of 100 MW, from the south-western part to the eastern part of the island, as illustrated in Fig. 1. This limit is due to small signal stability constraints. The Icelandic system has two inter-area oscillatory modes (0.6 and 0.8 Hz).

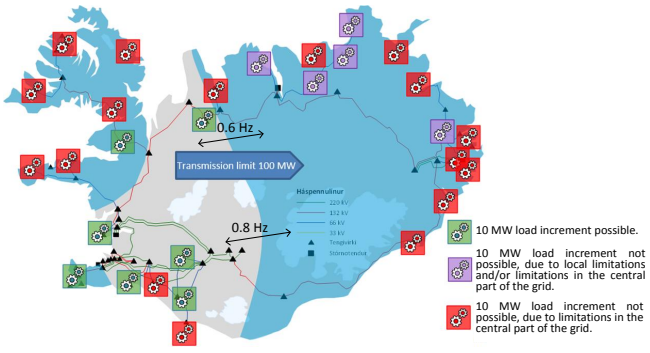

Fig. 1. The Icelandic power system indicating the 100 MW transmission limit between the south-western and the eastern part of the island.

Conventional means for stabilizing the system, such as the use of Power System Stabilizers (PSSs) [1] in generators, and supplementary damping controls in Flexible AC Transmission systems (FACTS) [2], have been used to their full potential in the Icelandic system. Therefore the Icelandic Transmission System Operator (TSO) is exploring new methods to prevent system islanding due to inter-area oscillations. One of the methods being explored it the use of industrial loads, to damp inter-area oscillations.

Active load control was discussed as early as in 1968 [3]. Today, loads are still largely uncontrollable, and their use in power system operation and control is limited to emergency conditions, f.ex. load shedding schemes to prevent under-frequency operation or to avoid blackouts. About 80% of the total load consumption in Iceland comes from industrial loads [4]. Three aluminium plants comprise the largest part of the industrial load, nearly 1300 MW from a total of approximately 2100 MW. Two are located in the south-west and one is located in the east. This originated the idea to control the load of aluminium smelters to prevent the separation of the Icelandic system.

This paper presents the design, development and hardware prototyping of a synchrophasor- and active load-based oscillation damping controller, using Real-Time Hardware-in-the-Loop (RT-HIL) simulation. The load control algorithm is deployed on a National Instrument's Compact Reconfigurable I/O controller (NI-cRIO) [5] and is tested by executing the 2-area 4-machine Klein-Rogers-Kundur power system model [6] in real-time using Opal-RT's eMEGAsim Real-Time Simulator (RTS). Commercial Phasor Measurement Units (PMUs) are coupled to the RTS and different (local and remote) synchrophasor signals are fed to the hardware controller to analyze the performance of the load control algorithm.

The remainder of this paper is organized as follows. The test power system model is described in Section II. The load control algorithm designed, and the hardware architecture for the controller prototype, are presented in Section III. In Section IV the RT-HIL experimental setup is explained. Testing results are presented in Section V, and are analysed in Section VI. Finally, in Section VII, conclusions are drawn and future work is outlined.

II. Test Power System Modelling

The two-area four-machine Klein-Rogers-Kundur power system model [6], designed specifically to study inter-area oscillations, was selected to test the load control algorithm.

This model resembles the Icelandic system with its two remote areas that are interconnected through weak and heavily loaded tie-lines. The PMU locations in the power system model are shown in Fig. 2. Three PMUs are located in each area and one in the middle of the tie lines connecting the two areas. The system was modelled in the MATLAB/SIMULINK environment using the SimPowerSystems (SPS) [7] and executed in real-time on 4-cores of OPAL-RT's eMEGAsim RTS with a discrete step size of $50\,\mu$s. The system is inherently unstable in the absence of any oscillation damping controller due to an inter-area oscillatory mode of 0.64 Hz.

The load is divided between the two areas in such a way that that active power is transferred from Area 1 to Area 2. Therefore, the load control algorithm is used to modulate the active power consumption of the load in Area 2. To analyze the performance of the load control algorithm the following disturbance was introduced in the power system model.

Scenario: A $5\,\%$ magnitude step increase in the reference voltage of Generator 1 applied for 4 cycles at $t = 60$ s.

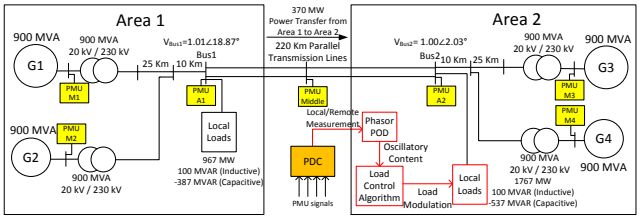

Fig. 2. The two-area four-machines Klein-Rogers-Kundur power system model. PMUs stream out phases and positive sequence synchrophasors for both voltages and currents at 50 frames/s.

III. Load Control Algorithm Design and Hardware Deployment

A. Load Control Algorithm Design

The load control algorithm designed for deployment in the hardware prototype controller is shown in Fig. 3. The load control algorithm uses the Phasor POD approach [8] that exploits the fact that the frequency of oscillation is usually well known, and it separates the input signal into its average value and its oscillatory content, for the set frequency. This approach was selected because its settings are independent of the network topology, and it offers phase compensation, allowing the algorithm to utilize different local and remote synchrophasor measurement as input signals.

The input signal for the load control algorithm is the oscillatory content generated by the Phasor POD algorithm. First the algorithm calculates the derivative of the oscillatory content of the input signal. When the active power transfer increases, the active load consumption in Area 2 is also increased. On the other hand when the active power transfer decreases, the active power consumption in Area 2 is also decreased. The amplitude of the active load consumption is determined by the maximum value of the oscillatory signal, which is determined for each cycle, when the load increases. In a similar way, the amount of load shed is determined by the minimum value of the oscillatory component of the input signal for each cycle [9].

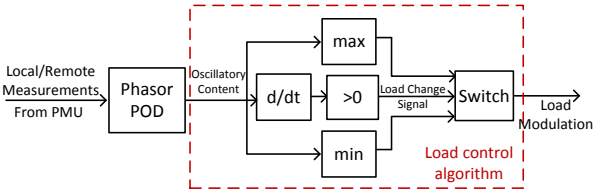

Fig. 3. The active load control algorithm.

B. Hardware Deployment of the Load Control Algorithm

The NI-Compact Reconfigurable-I/O (NI-cRIO) is a modular, reconfigurable control and acquisition system that can be programmed using the graphical programming LabVIEW platform [5]. The embedded hardware platform that the load control algorithm is deployed on is a NI-cRIO-9076. It has a 4-slot Xilinx Spartan-6LX45 Field-Programmable Gate Array (FPGA) and a 400 MHz real-time processor.

The main aim of using the NI-cRIO platform is to develop a hardware prototype controller and test it in the SmarTS Lab environment [10]. Once thoroughly tested in a real-time laboratory environment it should be possible to integrate the controller into the Icelandic system, without major modifications. It is therefore desirable that the controller can receive a PDC stream, directly in the NI-cRIO. This is not an option because there is no PMU data-mediation software readily available today that can be executed on the NI-cRIO. To address this issue, a typical computer is used to receive the PMU measurements which are transmitted using the IEEE C37.118.2 protocol [11].

A three level design was thus necessary to implement the algorithm using LabVIEW, as shown in Fig. 4. The first level is executed on a typical computer, where Statnett's Synchrophasor Software Development Kit (S^3DK) [12] is used to unwrap the IEEE C37.11.8.2 protocol into raw measurements and provide them as LabVIEW data types. The measurements are then forwarded to the real-time processor on the NI-cRIO.

The second level runs on the real-time processor of the NI-cRIO. It handles all the communication between the typical computer, and the FPGA of the NI-cRIO. It recives the raw PMU measurements, allows to select and/or process the synchrophasor data to derive the controller input signal and forwards the selected input signal to the FPGA.

In the third and final level, running on the FPGA of the NI-cRIO, is the load control algorithm implemented. The computation speed of the FPGA was set to $100\,\mu$s to avoid overruns because the algorithm was exhausting the overall resources of the FPGA. It computes the load modulation signal for the selected input signal and sends it to the analog output of the NI-cRIO.

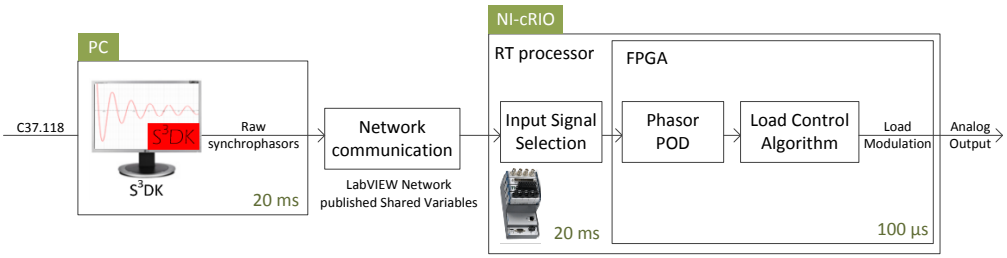

Fig. 4. The hardware deployment of the load controller.

IV. RT-HIL Experimental Setup

The RT-HIL experimental setup, for testing the active load control algorithm, is shown in Fig. 5. The power system model is executed on the RTS. Three-phase voltages and currents from the desired buses are sent to the PMUs. The PMUs compute the synchrophasors and stream them out in the C37.118.2 format. The Phasor Data Concentrator (PDC) time aligns the synchrophasor measurements from the PMUs, and creates a concentrated output stream. S^{3}DK parses the C37.118.2 protocol and provides access to the raw synchrophasor measurements. The hardware controller (NI-cRIO) processes the raw measurements to generate an input signal for the load control algorithm. Finally the output module of the NI-cRIO sends the load modulation signal to the RTS through its analog input. The load modulation signal is used to change the active load demand of the load in Area 2, in the power system model.

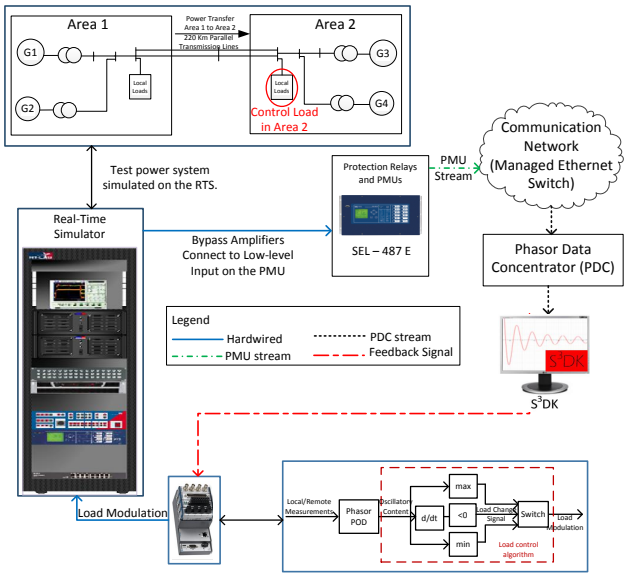

Fig. 5. RT-HIL experimantal setup.

V. Simulation Results

To verify and validate the load control algorithm design and implementation, it is first tested using the Real-Time Software-in-the-Loop (RT-SIL) approach. Both the power system model and the controller are simulated in real-time, on the same RTS but on separate cores that only communicate through digital inputs and outputs on the simulator. By analysing the performance of the controller when it is tested using the RT-SIL approach, the requirements for the hardware and computational resources of the hardware prototype can be estimated [9].

In this section the results from testing the algorithm using both the RT-SIL and the RT-HIL approach are presented. This is realized to emphasize the impact of different factors that the hardware prototype controller is exposed to in the RT-HIL setup, which are very similar to those one can expect in an actual field deployment. To test the load control algorithm, and to find the most effective input signal, eight different syncrhophasor input signals are tested and analyzed. The PMU locations for the input signals are shown in Fig. 2. The input signals tested are listed here below.

1. Active Power transfer from Area 1 to Area 2 (P_{12}) measured by PMU Middle.
2. Positive sequence voltage magnitude PMU A1 (V^+_{Area1})
3. Positive sequence voltage magnitude PMU A2 (V^+_{Area2})
4. Positive sequence current magnitude PMU A1 (I^+_{Area1})
5. Positive sequence current magnitude PMU A2 (I^+_{Area2})
6. The positive sequence voltage phase angle difference between PMU A1 and A2 ($V_{\varphi Area1} - V_{\varphi Area2}$)
7. The average value of the positive sequence voltage magnitude difference between PMU A1 and A2 $\left(\frac{V_{M1}+V_{M2}}{2} - \frac{V_{M3}+V_{M4}}{2}\right)$
8. The average value of the positive sequence voltage phase angle difference between Area 1 and Area 2 $\left(\frac{V_{\varphi M1}+V_{\varphi M2}}{2} - \frac{V_{\varphi M3}+V_{\varphi M4}}{2}\right)$

A. RT-SIL

In Fig. 6, RT-SIL simulation results are shown. The figure shows a comparison of using different synchrophasor controller input signals, when subjecting the system to a small disturbance. The input signal that provides the worst damping

compared to the other input signals is input signal 7, the voltage magnitude difference $\left(\frac{V_{M1}+V_{M2}}{2} - \frac{V_{M3}+V_{M4}}{2}\right)$. All the remaining input signals achieve adequate damping, within 10 s after the disturbance.

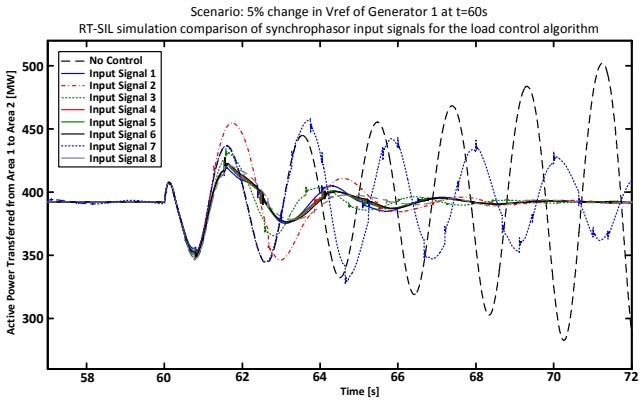

Fig. 6. Active power response using eight different input signals to test the controller using RT-SIL simulation.

B. RT-HIL

Figures 7-8 compare the results using different controller input signals, when subjecting the system to a small disturbance and performing RT-HIL simulation. The damping provided by the algorithm for all the input signals is reduced. This is principally because of time delays, scaling and noise in the RT-HIL experimental setup. These aspects will be further discussed in Section VI. In RT-HIL testing, damping is achieved for all the input synchrophasors but after a longer time as compared to RT-SIL.

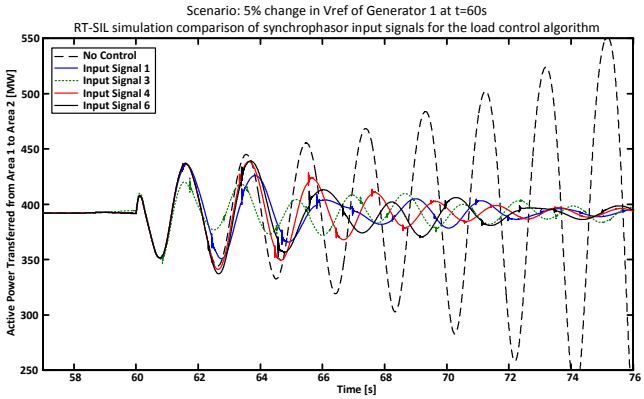

Fig. 7. Active power response using input signals 1, 3, 4 and 6, to test the controller using RT-HIL simulation.

VI. Discussion

To further analyze the controller's response to different input signals, four control performance metrics are analysed. The metrics considered are *decay ratio*, *overshoot*, *undershoot* and *settling time*. *Decay ratio* (DR) shows how fast the oscillation decreases. It is the ratio between the peak of the first oscillation

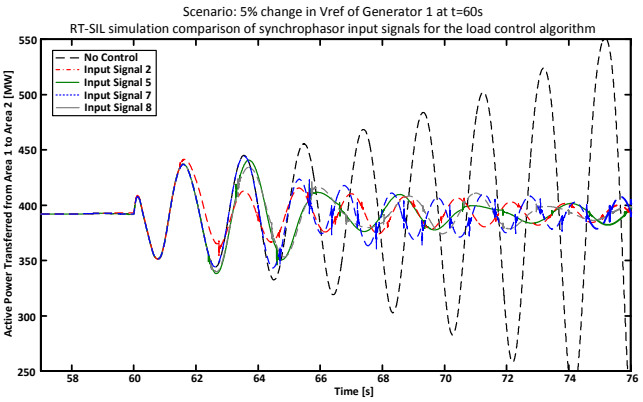

Fig. 8. Active power response using input signals 2, 5, 7 and 8, to test the controller using RT-HIL simulation.

(a) and the next peak of oscillation (b), $\mathrm{DR} = \mathrm{b/a}$. The *overshoot* and the *undershoot* are the highest and the lowest deviations in the active power transfer after the disturbance. These are important to consider because of the transmission limits between the two areas. The *settling time* is the time at which the oscillations have decreased to a value that is within $\pm 1\%$ change from the original active power transfer between the areas.

In Table I, the performance metrics, for RT-SIL simulation are shown. Input signal 8, the voltage angle difference at machine buses $\left(\frac{V_{\varphi M1}+V_{\varphi M2}}{2} - \frac{V_{\varphi M3}+V_{\varphi M4}}{2}\right)$, shows the best overall performance [1]. Input signals 2 (V^{+}_{Area1}) and 3 (V^{+}_{Area2}) have a slightly longer settling time and a higher overshoot compared to the other input signals. All the input signals except input signal 7 $\left(\frac{V_{M1}+V_{M2}}{2} - \frac{V_{M3}+V_{M4}}{2}\right)$, are suitable for damping the inter-area oscillations.

TABLE I
RT-SIL CONTROL PERFORMANCE METRICS.

Input signal	Decay Ratio	Overshoot [MW]	Undershoot [MW]	Settling Time [s]
1.	0.906	32.3	-42.8	6.13
2.	0.906	63.0	-45.8	6.63
3.	0.907	42.8	-44.3	6.50
4.	0.904	34.6	-44.4	6.10
5.	0.904	34.5	-43.6	6.06
6.	0.905	35.0	-45.0	6.15
7.	1.009	66.5	-64.0	32.81
8.	**0.904**	**32.6**	**-47.2**	**5.31**

The same performance metrics are used to evaluate the performance of each of the signals, for RT-HIL simulation, the results are shown in Table II. When compared to the results for RT-SIL simulation (Table I) the deteriorating performance of the controller while in RT-HIL mode of operation is obvious. All four performance metrics have significantly worse results, eg. the settling time is more than doubled.

[1]The most important metric is the *Settling Time*. Notice that input signal 8 offers a 14.3% improvement on the damping performance compared to input signal 1 ($(6.13 - 5.31)/\frac{6.13+5.31}{2} = 14.3\%$)

TABLE II
RT-HIL CONTROL PERFORMANCE METRICS.

Input signal	Decay Ratio	Overshoot [MW]	Undershoot [MW]	Settling Time [s]
1.	0.935	44.6	-41.2	12.63
2.	0.951	49.2	-40.8	21.74
3.	0.925	31.5	-45.6	25.88
4.	0.981	46.4	-51.0	14.74
5.	0.959	48.7	-53.9	25.89
6.	0.945	47.1	-54.9	18.15
7.	0.969	52.4	-48.8	49.80
8.	**0.964**	**45.0**	**-52.2**	**17.32**

The major factor contributing to the difference between the RT-SIL and RT-HIL results are the latency, the scaling and the noise in the RT-HIL setup as well as the difference in implementation of the load control algorithm in RT-SIL and RT-HIL.

The main reason causing the RT-HIL performance of the controller to be worse is the latency in the RT-HIL setup. Time delays have a large impact on power system feedback control loops since the response of the control is delayed, resulting in negative contribution towards damping [13]. To compensate for the delay, phase compensation of the load controller must be determined and changed. Certain parts of the process have fixed time delays (Real-time Simulator, PMU, NI-cRIO) while others have non-deterministic delays (PDC, S^3DK (since running on a typical computer), the communication protocols).

The analog inputs and outputs of the equipment in the RT-HIL experimental setup have low-level voltage limits. The OPAL-RT RTS has an analog output limit of $\pm 16\,\mathrm{V}$, the NI-cRIO analog output module has a limit of $\pm 10\,\mathrm{V}$, etc. Therefore the signals have to be scaled up and down in different points throughout the RT-HIL setup. When the signal is scaled down, signal resolution deteriorates and this in turn results in a decrease in signal to noise ratio.

A particular challenge when developing this control prototype is the fact that the same programming language and development platform can not be used for developing the SIL and the HIL controller. Therefore there is a noticeable difference in the algorithm implementation between SIL and HIL that affects the results.

VII. CONCLUSION

In this paper a hardware prototype load controller was developed and tested for damping of inter-area oscillations, using the RT-HIL approach. Eight different input signals, both local and remote synchrophasors, for the active load control algorithm were compared. The input signals all provided damping to the inter-area oscillation. The input signals that gave the worst overall results were voltage magnitude and voltage magnitude difference. The other five input signals, including positive sequence current, active power and voltage angle difference are all suitable options for providing damping to the $0.64\,\mathrm{Hz}$ inter-area oscillation. To study the impact of the RT-HIL setup the damping performance of the load controller for RT-SIL and RT-HIL approach was compared. Several factors in the RT-HIL setup, for example latencies, noise and scaling have a negative impact on the damping performance of the controller.

In future work an equivalent model of the Icelandic system will be made. The load controller will be integrated into the system and its damping performance in the system, will be studied. Because the Icelandic power system has several oscillatory modes, the controller has to be adapted to damp multiple oscillatory modes, both local and inter-area. Improvements to the algorithm, including making it adaptive towards communication latencies and input signal selection, will be presented in future publications.

ACKNOWLEDGMENT

This work was financially supported by Nordic Energy Research through the Strong^{2}rid project and by Statnett SF, the Norwegian Power System Operator. The authors would like to acknowledge the technical support from Landsnet, the Icelandic Power System Operator.

REFERENCES

[1] IEEE, "Tutorial Course on Power System Stabilization via Excitation Control", IEEE PES General Meeting, Tampa, Florida, June 2007.

[2] K. Uhlen, L. Vanfretti, M.M. de Oliveira, A. B. Leirbukt, V. H. Aarstrand, and J.O. Gjerde, "Wide-Area Power Oscillation Damper Implementation and Testing in the Norwegian Transmission Network," IEEE PES General Meeting 2012, San Diego, CA, USA.

[3] R. H. Park, "Improved reliability of bulk power supply by fast load control", in *Proceedings of the 1968 American Power conference*, 1968, pp. 445-457.

[4] Raforkutölfræði, "Raforkunotkun, stóriðja, almenningur og skerðanleg notkun (21.11.2013) (load consumption, industrial load, residential load, reducible load)," 2013. [Online]. Available: http://goo.gl/FeqSJ5

[5] LabVIEW Online Documentation 'What is Compact RIO'. [Online]. Available: http://www.ni.com/compactrio/whatis/

[6] M. Klein , G. Rogers and P. Kundur "A fundamental study of inter-area oscillations in power systems", IEEE Trans. Power Syst., vol. 6, no. 3, pp.914 -921 1991 .

[7] The MathWorks, "SimPowerSystems User Guide", Available Online.

[8] L. Angquist and C. Gama, "Damping algorithm based on phasor estimation", *PES Winter Meeting, 2001 IEEE*, Vol. 3, pp. 1160-1165.

[9] G. M. Jonsdottir, M. S. Almas, M. Baudette, M. Palsson, and L. Vanfretti, "RT-SIL Performance Analysis of Synchrophasor-and-Active Load-Based Power System Damping Controllers," in *PES General Meeting, 2015 IEEE*, 2015.

[10] M. Almas, M. Baudette, L. Vanfretti, S. Lovlund, and J. Gjerde, "Synchrophasor network, laboratory and software applications developed in the strong2rid project," in *PES General Meeting, 2014 IEEE*, 2014, pp. 1–5.

[11] "IEEE Standard for Synchrophasor Data Transfer for Power Systems," *IEEE Std C37.118.2-2011 (Revision of IEEE Std C37.118-2005)*, Dec 2011.

[12] L. Vanfretti, V. Aarstrand, M. Almas, V. Peric, and J. Gjerde, "A software development toolkit for real-time synchrophasor applications," in *PowerTech, 2013 IEEE Grenoble*, June 2013, pp. 1–6.

[13] C. Danielson, L. Vanfretti, M. S. Almas, Y. Choompoobutrgool, and J. Gjerde, "Analysis of communication network challenges for synchrophasor-based wide-area applications," in *IREP Symposium*. IEEE, 2013, pp. 1–13.