Hardware	Inputs	Outputs	NOT	ANDk [1]	ANDk+1 [2]	ANDr [3]	ANDl1 [4]	ANDm [5]	AND2	AND3	AND4	AND5	AND6	AND7	AND8	AND9	AND10	AND11	AND12	AND13	AND14	AND15	AND16	AND17	AND18	AND19
	2	4	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	3	8	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	4	16	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	5	32	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	6	64	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	7	128	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	8	256	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	9	512	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
SLD (ANDn) [6]	10	1024	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	11	2048	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	12	4096	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	13	8192	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	14	16384	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	15	32768	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	16	65536	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
	17	131072	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	18	262144	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	2	4	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	3	8	1	1	0	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	4	16	1	1	0	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	5	32	1	1	0	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	6	64	1	1	0	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	7	128	1	1	0	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8	256	1	1	0	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	9	512	1	1	0	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SLD (AND2) [7]	10	1024	1	1	0	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	11	2048	1	1	0	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	12	4096	1	1	0	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	13	8192	1	1	0	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	14	16384	1	1	0	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	32768	1	1	0	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	16	65536	1	1	0	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	17	131072	1	1	0	0	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	18	262144	1	1	0	0	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	2	4	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	3	8	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	4	16	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	5	32	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	6	64	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	7	128	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	8	256	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	9	512	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
SLD EN (ANDn) [8]	10	1024	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	11	2048	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	12	4096	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	13	8192	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	14	16384	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	15	32768	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
	16	65536	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	17	131072	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	18	262144	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	2	4	1	1	1	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	3	8	1	1	1	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	4	16	1	1	1	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	5	32	1	1	1	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Hardware	Inputs	Outputs	NOT	ANDk [1]	ANDk+1 [2]	ANDr [3]	AND11 [4]	ANDm [5]	AND2	AND3	AND4	AND5	AND6	AND7	AND8	AND9	AND10	AND11	AND12	AND13	AND14	AND15	AND16	AND17	AND18	AND19
SLD EN (AND2) [9]	6	64	1	0	1	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	7	128	1	0	1	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8	256	1	0	1	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	9	512	1	0	1	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	10	1024	1	0	1	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	11	2048	1	0	1	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	12	4096	1	0	1	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	13	8192	1	0	1	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	14	16384	1	0	1	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	32768	1	0	1	0	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	16	65536	1	0	1	0	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	17	131072	1	0	1	0	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	18	262144	1	0	1	0	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2LD (ANDn)	2	4	2	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	3	8	1	0	0	1	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	4	16	1	0	0	1	0	0	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	5	32	1	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	6	64	1	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	7	128	1	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8	256	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	9	512	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	10	1024	1	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	11	2048	1	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	12	4096	1	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	13	8192	1	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	14	16384	1	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	15	32768	1	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	16	65536	1	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	17	131072	1	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	18	262144	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2LD (AND2)	2	4	2	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	3	8	1	0	0	1	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	4	16	1	0	0	1	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	5	32	1	0	0	1	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	6	64	1	0	0	1	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	7	128	1	0	0	1	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8	256	1	0	0	1	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	9	512	1	0	0	1	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	10	1024	1	0	0	1	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	11	2048	1	0	0	1	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	12	4096	1	0	0	1	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	13	8192	1	0	0	1	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	14	16384	1	0	0	1	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	32768	1	0	0	1	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	16	65536	1	0	0	1	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	17	131072	1	0	0	1	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	18	262144	1	0	0	1	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3DD (MD) (ANDn)	4	16	1	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	5	32	1	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	6	64	1	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	7	128	1	0	0	0	1	1	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8	256	1	0	0	0	1	1	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	9	512	1	0	0	0	1	1	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	10	1024	1	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	11	2048	1	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Hardware analysis table (three hardware variants compared across input/output sizes and AND-gate decomposition counts).

Hardware	Inputs	Outputs	NOT	ANDk [1]	ANDk+1 [2]	ANDr [3]	AND1 [4]	ANDm [5]	AND2	AND3	AND4	AND5	AND6	AND7	AND8	AND9	AND10	AND11	AND12	AND13	AND14	AND15	AND16	AND17	AND18	AND19	l1
(AND2)	12	4096	1	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4
	13	8192	1	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5
	14	16384	1	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5
	15	32768	1	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6
	16	65536	1	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	6
	17	131072	1	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	6
	18	262144	1	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	6
3DD (MD) (AND2)	4	16	1	0	0	0	1	1	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2
	5	32	1	0	0	0	1	1	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2
	6	64	1	0	0	0	1	1	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2
	7	128	1	0	0	0	1	1	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3
	8	256	1	0	0	0	1	1	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3
	9	512	1	0	0	0	1	1	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3
	10	1024	1	0	0	0	1	1	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4
	11	2048	1	0	0	0	1	1	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4
	12	4096	1	0	0	0	1	1	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4
	13	8192	1	0	0	0	1	1	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5
	14	16384	1	0	0	0	1	1	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5
	15	32768	1	0	0	0	1	1	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5
	16	65536	1	0	0	0	1	1	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6
	17	131072	1	0	0	0	1	1	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6
	18	262144	1	0	0	0	1	1	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6

Hardware	Inputs	Outputs	NOT	ANDk [1]	ANDk+1 [2]	ANDr [3]	AND1 [4]	ANDm [5]	AND2	AND3	AND4	AND5	AND6	AND7	AND8	AND9	AND10	AND11	AND12	AND13	AND14	AND15	AND16	AND17	AND18	AND19	r
	2	4	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	1
	3	8	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	2
	4	16	2	0	Z [10]	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2
	5	32	1	0	Z	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3
	6	64	1	0	Z	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3
	7	128	1	0	Z	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4
Composed 3LD (ANDn)	8	256	1	0	Z	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4
	9	512	1	0	Z	0	0	0	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5
	10	1024	1	0	Z	0	0	0	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5
	11	2048	1	0	Z	0	0	0	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6
	12	4096	1	0	Z	0	0	0	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6
	13	8192	1	0	Z	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	7
	14	16384	1	0	Z	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	7
	15	32768	1	0	Z	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8
	16	65536	1	0	Z	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8
	17	131072	1	0	Z	0	0	0	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	9
	18	262144	1	0	Z	0	0	0	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	9

Hardware	Inputs	Outputs	NOT	ANDk [1]	ANDk+1 [2]	ANDr [3]	AND1 [4]	ANDm [5]	AND2	AND3	AND4	AND5	AND6	AND7	AND8	AND9	AND10	AND11	AND12	AND13	AND14	AND15	AND16	AND17	AND18	AND19	r
	2	4	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	1
	3	8	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	2
	4	16	2	0	Z [11]	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2
	5	32	1	0	Z	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3
	6	64	1	0	Z	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3
	7	128	1	0	Z	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4
Composed 3LD (AND2)	8	256	1	0	Z	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4
	9	512	1	0	Z	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5
	10	1024	1	0	Z	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5
	11	2048	1	0	Z	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6
	12	4096	1	0	Z	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6
	13	8192	1	0	Z	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	7
	14	16384	1	0	Z	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	7
	15	32768	1	0	Z	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8
	16	65536	1	0	Z	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8
	17	131072	1	0	Z	0	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	9

Hardware	Inputs	Outputs	NOT	ANDk [1]	ANDk+1 [2]	ANDr [3]	AND1 [4]	ANDm [5]	AND2	AND3	AND4	AND5	AND6	AND7	AND8	AND9	AND10	AND11	AND12	AND13	AND14	AND15	AND16	AND17	AND18	AND19	l1	l2	l3
	18	262144	1	0	0	Z	Z	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	9		
	4	16	1	0	0	Z	Z	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	1	1
	5	32	1	0	0	Z	Z	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	2	1
	6	64	1	0	0	Z	Z	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	2	2
	7	128	1	0	0	Z	Z	0	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	2	2
	8	256	1	0	0	Z	Z	0	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	3	2
	9	512	1	0	0	Z	Z	0	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	3	3
Cascaded 3LD (ANDn)	10	1024	1	0	0	Z	Z	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	3	3
	11	2048	1	0	0	Z	Z	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	3
	12	4096	1	0	0	Z	Z	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	4
	13	8192	1	0	0	Z	Z	0	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	4	4
	14	16384	1	0	0	Z	Z	0	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	5	4
	15	32768	1	0	0	Z	Z	0	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	5	5
	16	65536	1	0	0	Z	Z	0	2	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	6	5	5
	17	131072	1	0	0	Z	Z	0	2	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	6	6	5
	18	262144	1	0	0	Z	Z	0	2	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	6	6	6
	4	16	1	0	0	Z	Z	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	1	1
	5	32	1	0	0	Z	Z	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	2	1
	6	64	1	0	0	Z	Z	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	2	2
	7	128	1	0	0	Z	Z	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	2	2
	8	256	1	0	0	Z	Z	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	3	2
	9	512	1	0	0	Z	Z	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	3	3
Cascaded 3LD (AND2)	10	1024	1	0	0	Z	Z	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	3	3
	11	2048	1	0	0	Z	Z	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	3
	12	4096	1	0	0	Z	Z	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	4
	13	8192	1	0	0	Z	Z	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	4	4
	14	16384	1	0	0	Z	Z	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	5	4
	15	32768	1	0	0	Z	Z	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	5	5
	16	65536	1	0	0	Z	Z	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	6	5
	17	131072	1	0	0	Z	Z	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	6	5
	18	262144	1	0	0	Z	Z	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	6	6
	7	128	2	0	0	Z	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4		
	8	256	2	0	0	Z	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4		
	9	512	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5		
	10	1024	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5		
	11	2048	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6		
Composed 4LD (ANDn)	12	4096	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6		
	13	8192	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	7		
	14	16384	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	7		
	15	32768	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8		
	16	65536	1	0	0	Z	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8		
	17	131072	1	0	0	Z	0	0	3	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	9		
	18	262144	1	0	0	Z	0	0	3	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	9		
	7	128	2	0	0	Z	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	8	256	2	0	0	Z	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	9	512	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	10	1024	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	11	2048	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Composed 4LD (AND2)	12	4096	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	13	8192	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	14	16384	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	15	32768	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	16	65536	1	0	0	Z	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	17	131072	1	0	0	Z	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	18	262144	1	0	0	Z	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

Hardware	Inputs	Outputs	NOT	ANDk [1]	NDk+1 [2]	ANDr [3]	AND1 [4]	NDm [5]	AND2	AND3	AND4	AND5	AND6	AND7	AND8	AND9	AND10	AND11	AND12	AND13	AND14	AND15	AND16	AND17	AND18	AND19	l1	l2	l3	l4
	5	32	1	0	0	2	2	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	1	1	1
	6	64	1	0	0	2	2	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	2	1	1
	7	128	1	0	0	2	2	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	2	2	1
	8	256	1	0	0	2	2	0	4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	2	2	2
Cascaded 4LD (ANDn)	9	512	1	0	0	2	2	0	3	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	3	2	2
	10	1024	1	0	0	2	2	0	3	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	3	2	2
	11	2048	1	0	0	2	2	0	3	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	3	3	2
	12	4096	1	0	0	2	2	0	3	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	3	3	3
	13	8192	1	0	0	2	2	0	3	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	3	3
	14	16384	1	0	0	2	2	0	3	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	3	3
	15	32768	1	0	0	2	2	0	3	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	4	3
	16	65536	1	0	0	2	2	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	4	4
	17	131072	1	0	0	2	2	0	3	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	4	4	4
	18	262144	1	0	0	2	2	0	3	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	5	4	4
	5	32	1	0	0	2	2	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	1	1	1
	6	64	1	0	0	2	2	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	2	1	1
	7	128	1	0	0	2	2	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	2	2	1
	8	256	1	0	0	2	2	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	2	2	2
Cascaded 4LD (AND2)	9	512	1	0	0	2	2	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	3	2	2
	10	1024	1	0	0	2	2	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	3	2	2
	11	2048	1	0	0	2	2	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	3	3	2
	12	4096	1	0	0	2	2	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	3	3	3
	13	8192	1	0	0	2	2	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	3	3
	14	16384	1	0	0	2	2	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	3	3
	15	32768	1	0	0	2	2	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	4	3
	16	65536	1	0	0	2	2	0	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	4	4
	17	131072	1	0	0	2	2	0	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	4	4	4
	18	262144	1	0	0	2	2	0	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	5	4	4
Composed 5LD (ANDn)	16	65536	1	0	0	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8			
	17	131072	1	0	0	0	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	9			
	18	262144	1	0	0	0	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	9			

Hardware	Inputs	Outputs	NOT	ANDk [1]	NDk+1 [2]	ANDr [3]	AND1 [4]	NDm [5]	AND2	AND3	AND4	AND5	AND6 … AND19	l1	l2	l3	l4	l5
	6	64	1	0	0	2	2	0	5	0	0	0	0	2	1	1	1	1
	7	128	1	0	0	2	2	0	5	0	0	0	0	2	2	1	1	1
	8	256	1	0	0	2	2	0	5	0	0	0	0	2	2	2	1	1
	9	512	1	0	0	2	2	0	5	0	0	0	0	3	2	2	2	1
Cascaded 5LD (ANDn)	10	1024	1	0	0	2	2	0	4	0	0	0	0	3	3	2	2	2
	11	2048	1	0	0	2	2	0	4	1	0	0	0	3	3	2	2	2
	12	4096	1	0	0	2	2	0	4	1	0	0	0	3	3	3	2	2
	13	8192	1	0	0	2	2	0	4	1	0	0	0	3	3	3	3	2
	14	16384	1	0	0	2	2	0	4	1	0	0	0	3	3	3	3	3
	15	32768	1	0	0	2	2	0	4	1	0	0	0	4	4	3	3	3
	16	65536	1	0	0	2	2	0	4	0	1	0	0	4	4	4	3	3
	17	131072	1	0	0	2	2	0	4	0	1	0	0	4	4	4	3	3
	18	262144	1	0	0	2	2	0	4	0	1	0	0	4	4	4	3	3
	6	64	1	0	0	2	2	0	5	0	0	0	0	2	1	1	1	1
	7	128	1	0	0	2	2	0	5	0	0	0	0	2	2	1	1	1
	8	256	1	0	0	2	2	0	5	0	0	0	0	2	2	2	1	1
	9	512	1	0	0	2	2	0	5	0	0	0	0	3	2	2	2	1
Cascaded 5LD (AND2)	10	1024	1	0	0	2	2	0	6	0	0	0	0	3	3	2	2	2
	11	2048	1	0	0	2	2	0	6	0	0	0	0	3	3	2	2	2
	12	4096	1	0	0	2	2	0	6	0	0	0	0	3	3	3	2	2
	13	8192	1	0	0	2	2	0	6	0	0	0	0	3	3	3	3	2
	14	16384	1	0	0	2	2	0	6	0	0	0	0	3	3	3	3	3
	15	32768	1	0	0	2	2	0	6	0	0	0	0	4	4	3	3	3
	16	65536	1	0	0	2	2	0	6	0	0	0	0	4	4	3	3	3

(Columns AND6 through AND19 contain 0 for all rows.)

Hardware	Inputs	Outputs	NOT	NNDk [1	NNDk+1 [2	ANDr [3	ANDl1 [4	NDm [5	AND2	AND3	AND4	AND5	AND6	AND7	AND8	AND9	AND10	AND11	AND12	AND13	AND14	AND15	AND16	AND17	AND18	AND19					
	17	131072	1	0	0	2	2	0	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	3	3	3
	18	262144	1	0	0	2	2	0	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4	4	3	3

[1] not included in the standard calculations, just for reference

[2] not included in the standard calculations, just for reference

[3] not included in the standard calculations, just for reference

[4] not included in the standard calculations, just for reference

[5] not included in the standard calculations, just for reference

[6] multi-input AND gates allowed

[7] multi-input AND gates not allowed

[8] multi-input AND gates allowed

[9] multi-input AND gates allowed

[10] Indeterminate, none at this level

[11] Indeterminate, none at this level