Real-Time Imaging and Control

Practice

MSCV/ESIREM

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Basics 2 - Sequential Logic

Problems marked with $\star$ are longer and/or harder than the other exercises.

Problem 1

You shall not flip-flop

1. Write the equation/truth tables of the D, T and JK flip-flops
2. Using the chronogram shown in figure 1, draw the output Q (assume that Q starts at 0) for a rising-edge triggered D flip-flop, a falling-edge triggered T flip-flop and a rising-edge triggered JK flip-flop.

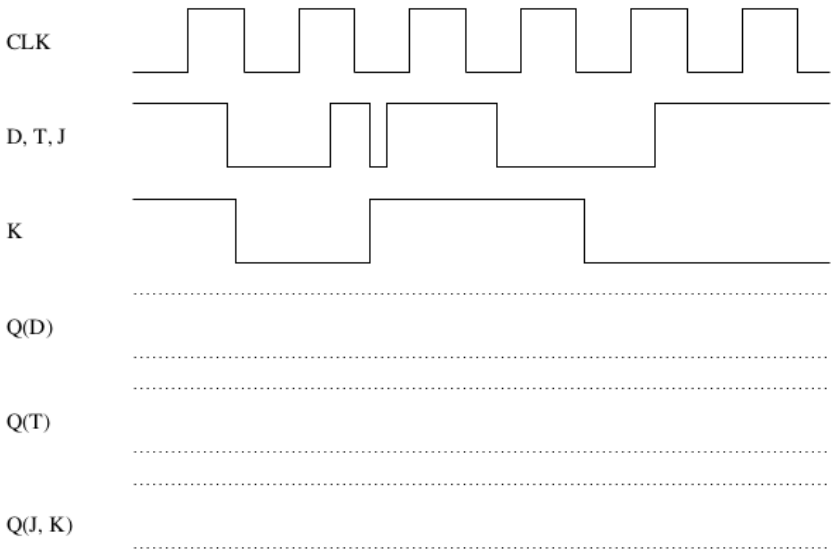

Figure 1: Chronogram

Problem 2

Welcome to the (State) Machine
A finite state machine shown in figure 2 has one input, X, and one output, Z, and two state variables, A and B, and a clock input, CLK.

1. Give the state transition table for this FSM
2. Draw the state diagram for this FSM
3. Fill in the timing diagram in figure 3. You may neglect propagation delay in the logic, assuming it to be zero. We also assume that the initial state has $A = 0, B = 1$

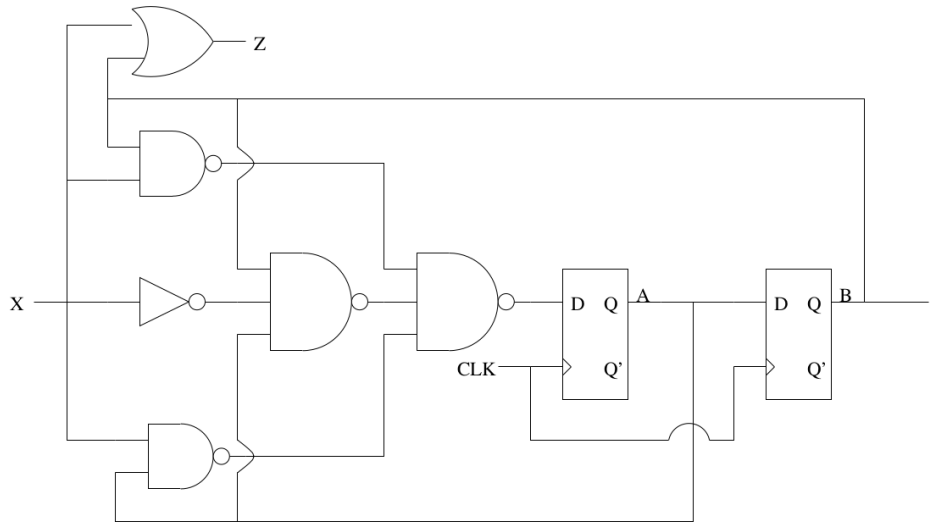

Figure 2: A circuit

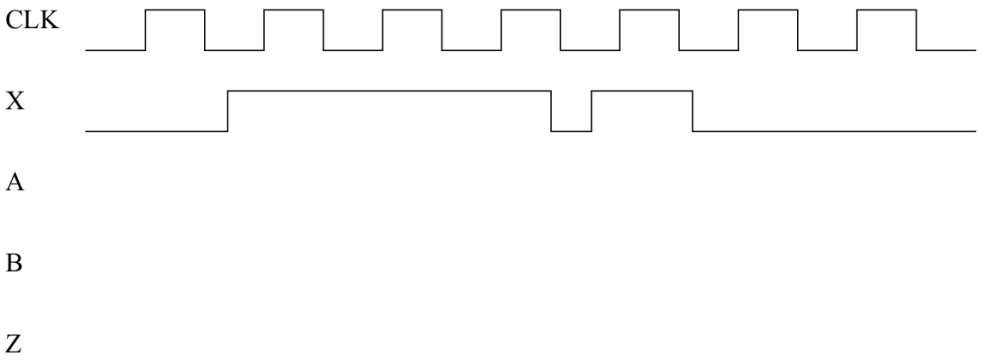

Figure 3: Chronogram for the FSM

Problem 3

Doomsday Machine
Note: S is the sum output of the adder, and C is the carry output.

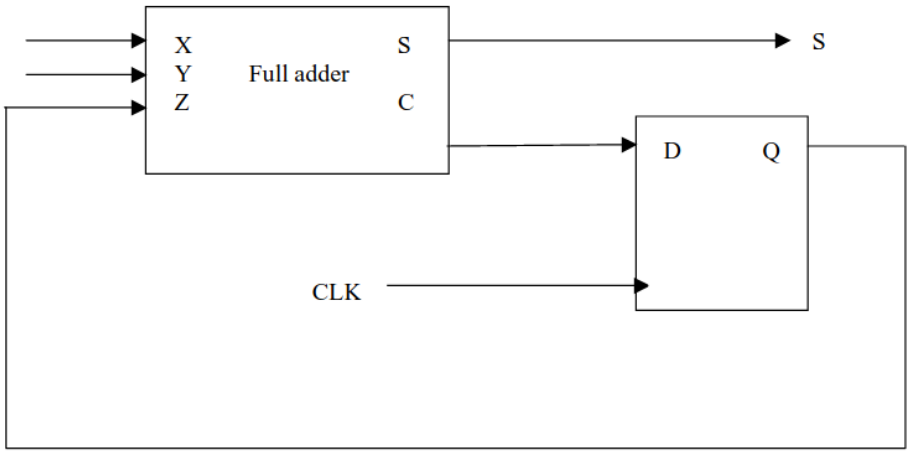

Figure 4: Another FSM

1. Derive the truth table for the circuit shown 4
2. Draw the state diagram for this circuit (be sure to show the output S in the diagram)
3. Is the finite state machine of the Moore type or the Mealy type? Explain.
4. Assume that the timing characteristics for the flip-flop are $t_{qcc} = t_{setup} = t_{hold} = 2\mu s$, and for the full adder $t_{pd} = 4\mu s$. Assuming that all inputs (X and Y) are synchronous with the system clock, what is the greatest clock speed at which the system could run?

Remark 1. *The following exercises on counters are fundamental in digital logic. It is highly recommended to do at least one problem.*

Problem 4

1. Recall the truth table for the JK flip-flop
2. By remarking that pulling J and K high makes a T flip-flop from a JK flip-flop, we will make a 2-bit counter.
   - To simplify the schematic work, you can use a T flip-flop instead of a JK flip-flop.
   - Write the state transition table for the 2-bit counter.
   - Deduce a potential logic circuit implementing a 2-bit counter.

Problem 5

Almost Final Countdown⋆

Design a 3-bit counter that can count up or down on the rising edge of the clock. There are two input signals:

- a clock signal,
- a signal to indicate whether the counter should count up or down.

If the up/down (noted U/D) signal is high, then the counter will count up. If the input signal is low, the counter will count down.
On reset, the count will return to zero.

1. Give the state transition table for this FSM.
2. Use K-maps to find the simplified expressions for inputs to the D flip-flops.
3. Draw the logic diagram for this counter

Problem 6

Summer of '74⋆

The 74-393 is called a ripple counter because the effect of a clock edge has to "ripple" through the counter to cause a change in the value. Only the clock triggers the least significant bit; the rest must be triggered by the bit preceding it.
A 74-163 is a synchronous counter because ALL bits of the counter are triggered directly by the clock; Propose an architecture for both the 393 and 163. Both are 4-bit counters.

Problem 7

Remark 2. *This problem is longer than the others. Also, the state transition tables will be bigger than the other problems among the 3.*

A Ticket to Park⋆

At Centre Condorcet, David and Aurore are thinking of using an automated parking ticket machine to control the number of guest cars that a student can bring.
The card reader tells the controller whether the car is a student or a guest car. Only one guest car is allowed per student at a discount rate only when s/he follows the member at the exit (within the allotted time). The second guest must pay the regular parking fees.
We know the overall system has the following signals:

- Signals from the card reader: MEMBER and GUEST
- Signals from the toll booth: TOKEN (meaning one toke received),
- EXP (time for discounted guest payment has expired).

- Signal to the gate: OPEN
- Reset signal: RESET

The fees are listed here: students are free, Guest with a student is 1 Token, and Guest is 2 Tokens.

1. Draw a truth table that corresponds to the FSM.
2. Draw the equivalent Karnaugh map.
3. Draw a state diagram, carefully labeled. Be sure to indicate which state the FSM is in after a RESET.
4. Is this a Moore or Mealy machine?