Addendum on the VHDL introduction

Antoine Lavault[1,2]

[1]Apeira Technologies

[2]UMR CNRS 9912 STMS, IRCAM, Sorbonne Université

January 19, 2024

Contents

Contents

Generic keyword

generic is a special kind of constant that can be applied to an entity during its initialization

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY vote IS GENERIC (W : POSITIVE := 4); -- here
PORT (
    votes : IN STD_LOGIC_VECTOR(W - 1 DOWNTO 0);
    approval : OUT STD_LOGIC);
END vote;
ARCHITECTURE behavioural OF vote IS
    CONSTANT nMin : NATURAL := W / 2; -- used to estimate nMin
BEGIN
    PROCESS (votes)
        VARIABLE compte : NATURAL RANGE 0 TO votes'length;
    BEGIN
        ...
    END PROCESS;
END behavioural;
```

Subtypes

```
TYPE in_lowert_20 IS RANGE 0 TO 19;
TYPE real_matrix_1_by_10 IS ARRAY (1 TO 10) OF real;
TYPE arraySLV3 IS ARRAY (NATURAL RANGE <>) OF STD_LOGIC_VECTOR(2 DOWNTO 0);
CONSTANT vectors : tableauSLV3 :=
("000", "001", "010", "011", "100", "101", "110", "111");
TYPE month_name IS (january, february, march, avril, may, june,
    july, august, september, october, november, december);
TYPE date IS RECORD
    day : INTEGER RANGE 1 TO 31;
    month : month_name;
    year : POSITIVE RANGE 1 TO 3000;
END RECORD;
CONSTANT independence : date := (27, october, 2017);
```

Attributes cont.

- A'left, A'right: leftmost, rightmost index of A
- A'high, A'low: highest, lowest index of A
- A'range: the range of indices in A
- A'length: number of elements in A
- T'left/right/high/low: leftmost, ..., values for type T
- T'image(x): string representation of X of type T.
- T'value(x): value of type T converted from the string X.

```
PROCESS (votes)
    VARIABLE count : NATURAL RANGE 0 TO votes'length;
BEGIN
    count := 0;
    FOR k IN votes'RANGE LOOP
        ...
```

Functions and Procedures

- Functions and procedures can be defined in the declarative part of an architecture or as part of a package.
- Functions and procedures can be overloaded, i.e., same identifier, different parameters.

```
FUNCTION andGate(V : STD_LOGIC_VECTOR) RETURN STD_LOGIC IS
    VARIABLE result : STD_LOGIC := '1';
BEGIN
    FOR k IN V'RANGE LOOP
        result := result AND V(k);
    END LOOP;
    RETURN result;
END;
```

Procedures - Example

Procedures look a lot like functions... But they aren't functions.
In VHDL, a procedure is a subprogram employed to execute specific actions without returning values, primarily used for their side effects and the ability to modify signals passed as input parameters, enabling code organization and reuse within processes or blocks. This also makes them able to handle multi-output problems through side effects.
In C/C++, it would be a `void` function that works only through side effects. Note the use of in/out to describe how the parameters are used inside the procedure.

```
PROCEDURE IncrementValue(ValueToIncrement : IN OUT INTEGER) IS
BEGIN
    ValueToIncrement <= ValueToIncrement + 1;
END IncrementValue;
```

Functions vs Procedures

- A function
  - Is a sub-program returning a unique result
  - The function always returns something
  - If parameters are given, they cannot be modified
  - A function is called in an expression
- A procedure
  - doesn't return a value like a function but can return values by declaring out or inout signals in the parameter list.
  - parameters in the parameter list can be of in, out, inout type
  - Is part of the concurrent domain (through side effects)

Note that for both structures, it is possible to use restrictions on parameters' classes, like constant, signal, variable, or file. Also, note that functions do not accept variables as valid class restrictions.

Basics for sequential VHDL - D latch

```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY D_latch IS
    PORT (
        G : IN STD_LOGIC; -- control
        D : IN STD_LOGIC; -- data
        Q : OUT STD_LOGIC
    );
END D_latch;
ARCHITECTURE D_latch OF D_latch IS
BEGIN
    PROCESS (G, D) IS
    BEGIN
        IF (G = '1') THEN
            Q <= D;
            -- else -- implicit :: do not change Q
        END IF;
    END PROCESS;
END D_latch;
```

Sequential VHDL - DFF

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY D_FF IS
    PORT (
        CLK : IN STD_LOGIC; -- clock
        D : IN STD_LOGIC; -- in
        Q : OUT STD_LOGIC -- out
    );
END D_FF;
ARCHITECTURE D_FF OF D_FF IS
BEGIN
    PROCESS (CLK) IS
    BEGIN
        IF (CLK = '1' AND CLK'event) THEN
            Q <= D;
        END IF;
    END PROCESS;
END D_FF;
```

Contents

Example circuit

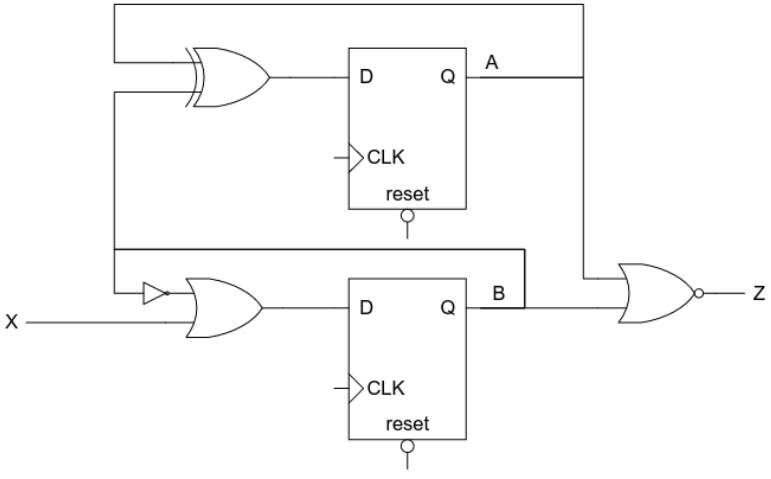

Figure: Caption

How to?

- Define the entity and its ports
- Define the architecture and the output of the FFs
- Model the flip-flops:
  - General form (process...)
  - Reset signal
  - Equations of the FF inputs
- Model the output

Which gives us...

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
ENTITY seq_crct IS
    PORT (
        reset, CLK, X : IN STD_LOGIC;
        Z : OUT STD_LOGIC);
END seq_crct;
ARCHITECTURE arch1 OF seq_crct IS
    SIGNAL A, B : STD_LOGIC;
BEGIN
    PROCESS (CLK, reset) IS
    BEGIN
        IF (reset = '0') THEN A <= '0';
            B <= '0';
        ELSIF (rising_edge(CLK)) THEN      <= A XOR B;
            B <= x OR NOT(B);
        END IF;
    END PROCESS;
    z <= NOT(A OR B);
END arch1;
```

Contents

Example

We want to make an inkjet printer. The usual colors used here are cyan, magenta, yellow, and black (key): the CYMK system. The black cartridge will be used as much as possible in order not to use too many color cartridges.
To convert RGB to CYMK, we have the following set of equations :

$$C_t = 255 - R \tag{1}$$
$$Y_t = 255 - G \tag{2}$$
$$M_t = 255 - B \tag{3}$$
$$K = min(Ct, Mt, Yt) \tag{4}$$
$$C = C_t - K \tag{5}$$
$$Y = Y_t - K \tag{6}$$
$$M = M_t - K \tag{7}$$
$$\tag{8}$$

CYMK conversion

We know that :

- the values are integers and are between 0 and 255.
- valid types are `Integer`, `Natural`, `Signed` and `Unsigned`
- we need a subtraction
- we need a minimum

In VHDL

```
ENTITY convRGB2CMYK IS PORT (
    red, green, blue : IN unsigned(7 DOWNTO 0);
    cyan, magenta, yellow, black : OUT unsigned(7 DOWNTO 0));
END convRGB2CMYK;
ARCHITECTURE arch2 OF convRGB2CMYK IS
BEGIN
    PROCESS (red, green, blue)
        VARIABLE cyant, magentat, yellowt, blackt1, blackt2 : unsigned(7 DOWNTO 0);
    BEGIN
        cyant := 255 - red; magentat := 255 - green; yellowt := 255 - blue;
        IF cyant < magentat THEN blackt1 := cyant; ELSE blackt1 := magentat;
        END IF;
        IF blackt1 < yellowt THEN blackt2 := blackt1; ELSE blackt2 := yellowt;
        END IF;
        cyan <= cyant - blackt2; magenta <= magentat - blackt2;
        yellow <= yellowt - blackt2;
        black <= blackt2;
    END PROCESS;
END arch2;
```

Assignment cont.

Be wary of type conversions and sizes!

```
LIBRARY ieee;
USE ieee.numeric_std.ALL;
ENTITY democode2 IS
    PORT (A8, B8 : IN signed(7 DOWNTO 0);
        R8 : OUT signed(7 DOWNTO 0);
        R9, S9, T9 : OUT signed(8 DOWNTO 0);
        R7 : OUT signed(6 DOWNTO 0));
END;
ARCHITECTURE arch OF democode2 IS
BEGIN
    R8 <= A8 + B8; -- ok, might overflow
    S8 <= A8 + 100; -- ok, might overflow
    R9 <= (A8(A8'left) & A8) + (B8(B8'left) & B8); -- ok
    S9 <= resize(A8, S9'length) + resize(B8, S9'length); -- ok
    T9 <= A8 + B8; -- no, incompatible ranges
    R7 <= A8(6 DOWNTO 0) + B8(6 DOWNTO 0); -- ok, might overflow
END arch;
```

Aggregates

```
-- positional association
VARIABLE Data_1 : BIT_VECTOR (0 TO 3) := ('0', '1', '0', '1');
-- named association
VARIABLE Data_2 : BIT_VECTOR (0 TO 3) := (1 => '1', 0 => '0', 3 => '1', 2 => '0');
-- positional association with range
SIGNAL Data_Bus : STD_LOGIC_VECTOR (15 DOWNTO 0);
Data_Bus <= (15 DOWNTO 8 => '0', 7 DOWNTO 0 => '1');
-- Named association in record
VARIABLE Status_Var : Status_Record := (Code => 57, Name => "MOVE");
-- keyword others may be used to refer to all elements not already mentioned:
SIGNAL Data_Bus : STD_LOGIC_VECTOR (15 DOWNTO 0);
Data_Bus <= (14 DOWNTO 8 => '0', OTHERS => '1');
-- Use of keyword others
SIGNAL Data_Bus : STD_LOGIC_VECTOR (15 DOWNTO 0);
Data_Bus <= (OTHERS => 'Z');
```

Contents

Why use file IO ?

Reading a file is useful during tests with test-benches.

- The described system might have previously been implemented with a high-level system like Python, Matlab, or even C. This is useful to generate a lot of test cases (input + output)
- Using this ground truth would benefit a more exhaustive test policy. More coverage = better.

The other way round, writing to files is interesting when:

- the simulation is extremely long
- we want partial results
- we want to process the results further (e.g, an image)

Example

Let's suppose we want to test the following code :

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;
ENTITY detectFirst IS
    PORT (
        I : IN unsigned(5 DOWNTO 0);
        F : OUT STD_LOGIC
    );
END detectFirst;
ARCHITECTURE dataflow OF detectFirst IS
BEGIN
    WITH to_integer(I) SELECT
    F <=
        '1' WHEN 2 | 3 | 5 | 7 | 11 | 13 | 17 |
        19 | 23 | 29 | 31 | 37 | 41 | 43 |
        47 | 53 | 59 | 61 | 63,
        '0' WHEN OTHERS;
END dataflow;
```

The test file

Our test file is similar to:

```
-- column 1 : integers from 0 to 63
-- column 2: F for first, N for not first
0 N
1 N
2 F
3 F
4 N
5 F
...
```

Test-bench with IO

Import the textio package!

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;
USE std.textio.ALL;
ENTITY detectFirstTB IS
END detectFirstTB;
ARCHITECTURE arch2 OF detectFirstTB IS
    SIGNAL I : unsigned(5 DOWNTO 0); -- signal for test vectors
    SIGNAL F : STD_LOGIC; -- signal for the test output
    CONSTANT filename : STRING := "first.txt";
    FILE vectors : text OPEN read_mode IS filename;
BEGIN
    UUT : ENTITY detectFirst(dataflow) PORT MAP (I, F);
```

Test-bench with IO

```
PROCESS
    VARIABLE linebuffer : line; -- pointer to a string object
    VARIABLE n : INTEGER;
    VARIABLE c : CHARACTER;
BEGIN
    WHILE NOT endfile(vectors) LOOP
        readline(vectors, linebuffer);
        IF linebuffer(1 TO 2) /= "--" then -- passer les lignes de commentaires
            read(linebuffer, n); -- reading the integer
            read(linebuffer, c); -- reading the space
            read(linebuffer, c); -- reading the output: first or not
            I <= to_unsigned(n, 6);
            WAIT FOR 10 ns;
            ASSERT ((c = 'P') = (F = '1') AND (c = 'N') = (F = '0'))
            REPORT "input error " & INTEGER'image(n) SEVERITY error;
        END IF;
    END LOOP;
    deallocate(linebuffer); -- release the memory
    REPORT "all done" SEVERITY failure;
END PROCESS;
```

Writing with IO

```
FILE results : text OPEN write_mode IS "results.txt";
PROCESS
    VARIABLE buffer_ : line; -- pointer to string object
BEGIN
    -- writeline frees the pointer when it's done. We need a copy if we want to reuse it
    write(buffer_, STRING'(" ** simulation output, detectFirstTB.vhd ** "));
    writeline(results, buffer_); -- write in file
    FOR k IN 0 TO 63 LOOP -- exhaustive test
        I <= to_unsigned(k, 6);
        WAIT FOR 10 ns;
        write(buffer_, STRING'("time: "));
        write(buffer_, now, unit => ns);
        write(buffer_, STRING'(", int: ") & INTEGER'image(k));
        write(buffer_, STRING'(", out: ") & STD_LOGIC'image(F));
        writeline(results, buffer_); --  write in file
    END LOOP;
    REPORT "all done" SEVERITY failure;
END PROCESS;
```

Contents

Blinking LEDs.
This might be useful at some point.
Maybe.

Exercise 1

Give the VHDL for the following register:

- 8 bits in/out
- Loading on a falling clock edge and when *load* is high
- Synchronous reset to $0xf4$ when *reset* is low

Solution 1

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY REGISTER IS
    GENERIC (W : INTEGER := 8);
    PORT (
        reset, CLK, load : IN STD_LOGIC;
        D : IN STD_LOGIC_VECTOR(W - 1 DOWNTO 0);
        Q : OUT STD_LOGIC_VECTOR(W - 1 DOWNTO 0));
END REGISTER;
ARCHITECTURE arch OF REGISTER IS
BEGIN
    PROCESS (CLK, reset)
    BEGIN
        IF falling_edge(CLK) THEN
            IF reset = '0' THEN   Q <= X"F4";
            ELSIF load = '1' THEN Q <= D;
            END IF;
        END IF;
    END PROCESS;
END arch;
```

Exercise 2

What does this do?

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY mystery IS
    PORT (
        a, b, c : IN STD_LOGIC;
        s : IN STD_LOGIC_VECTOR (1 DOWNTO 0);
        o : OUT STD_LOGIC);
END mystery;
ARCHITECTURE arch OF mystery IS
BEGIN
    PROCESS (a, b, c, s)
    BEGIN
        IF (s = "00")    THEN o <= a;
        ELSIF (s = "01") THEN o <= b;
        ELSIF (s = "10") THEN o <= c;
        ELSE                  o <= c;
        END IF;
    END PROCESS;
END arch;
```

Solution 2

This is a 4-input multiplexer with a control signal s. Note that inputs 2 and 3 are linked to output c.

How to design complex systems?

Break them into manageable chunks. Always have a pen and paper to have an idea of the overall data flow and design structure.