Hardware Architecture

```
                              ┌──────────────┐        ┌──────────────────┐
                              │   AXI DMA    │◄──────►│   my_ip (HDL)    │
                              └──────────────┘        └──────────────────┘
                                    ▲
┌──────────────────────────┐        │
│ Zynq7 Processing System  │◄──────►│
└──────────────────────────┘        │
                                    ▼
                              ┌──────────────┐        ┌──────────────────┐
                              │   AXI DMA    │◄──────►│  AXIS_TRY (HLS)  │
                              └──────────────┘        └──────────────────┘
```
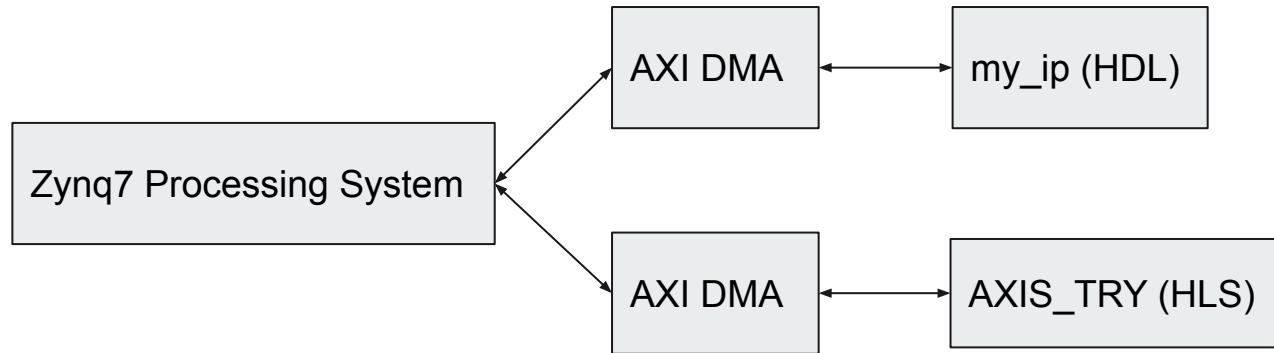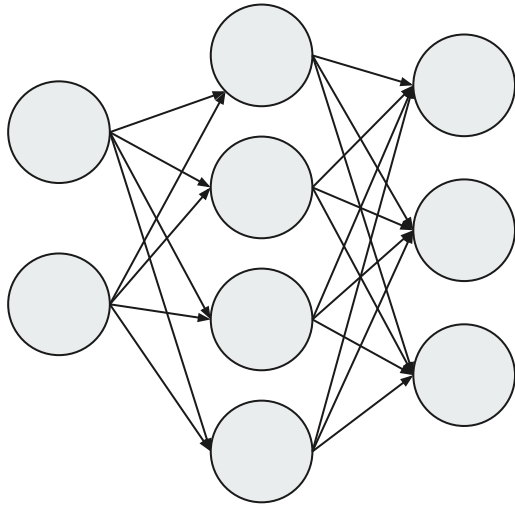
Software

Neural Network

1. Number of Hidden Nodes: 5
2. Number of Hidden Layer: 1
3. Number of Output Nodes: 3
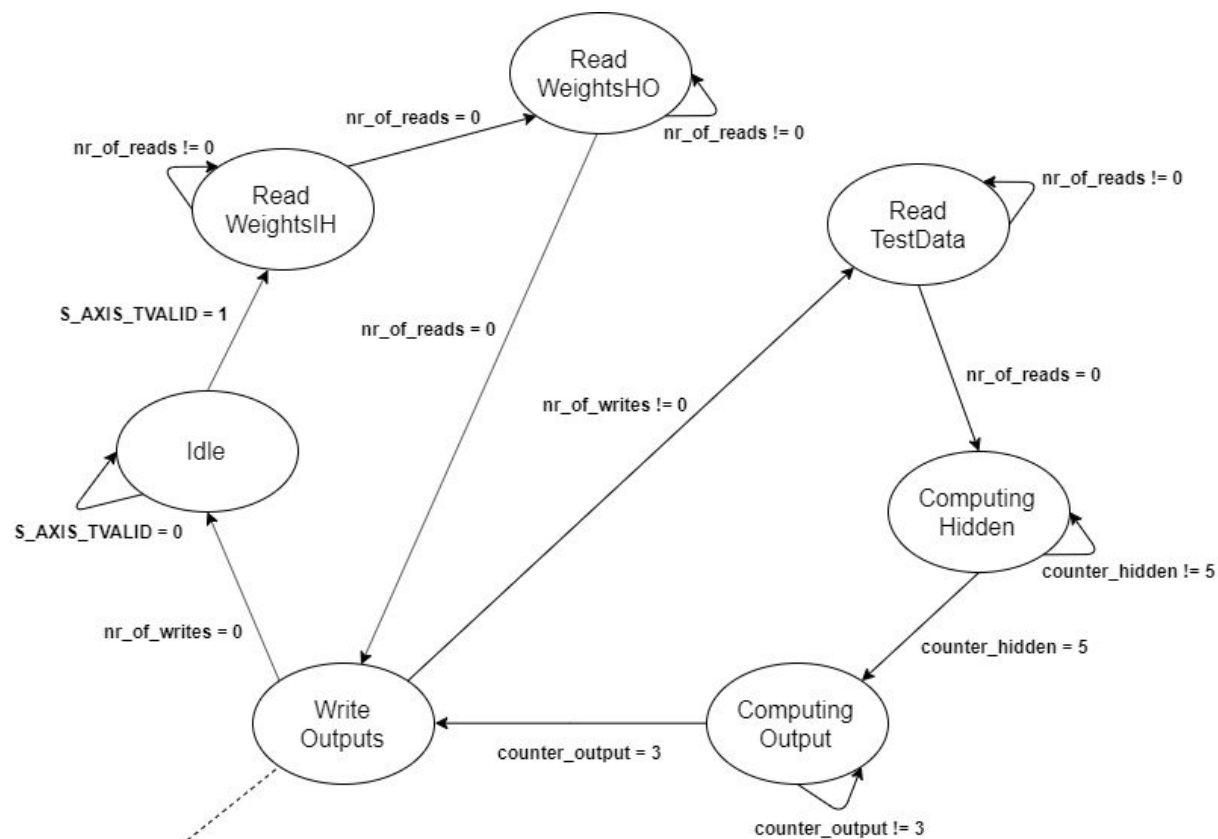4. Activation function used: Sigmoid

Stored Weights to be used for prediction using HLS, HDL and C implementation

Prediction of test data using coprocessor

1. After training, stored weights and test data will be converted to fixed point format of Q8.8.
2. To pass these data over to our coprocessor, we first pass the weights over using AXIS and if successful, we will receive an integer of '12345'.
3. A timer will begin at this point.
4. Following which, we will pass over the test data one at a time (13 features in one transfer), and receive the prediction for each transfer.
5. Step 4 will repeat itself for the total number of test data that we have which is 36.
6. The timer will end at this point
7. After the prediction is complete, we will calculate the accuracy of the prediction with the actual test labels that we have.
8. The accuracy score and time taken will be printed out.

HDL - FSM

Read WeightsHO

nr_of_reads = 0

nr_of_reads != 0

Read WeightsIH

nr_of_reads != 0

nr_of_reads = 0

S_AXIS_TVALID = 1

Idle

S_AXIS_TVALID = 0

nr_of_writes != 0

nr_of_writes = 0

Read TestData

nr_of_reads != 0

nr_of_reads = 0

Computing Hidden

counter_hidden != 5

counter_hidden = 5

Write Outputs

counter_output = 3

Computing Output

counter_output != 3

Output
M_AXIS_TDATA = (nr_of_writes == NUMBER_OF_OUTPUT_WORDS - 1) ? **12345** : prediction

Hardware Utilization

	HDL	HLS
LUTs - logic	379	317
Luts - memory	80	59
Flip-flops	135	251
Block Ram	0	2 x 18k
DSPs	3	2

Time (ms) for prediction

	C	HLS	HDL
Run 1	0.3831	0.3134	0.1819
Run 2	0.3829	0.3135	0.1818
Run 3	0.3828	0.3133	0.1818
Run 4	0.3824	0.3137	0.1816
Run 5	0.3825	0.3137	0.1815
Avg	0.3827	0.3135	0.1817

Enhancements

Loop unrolling - HLS

	Before	After
LUTs - logic	317	587
LUTs - memory	59	59
Flip-flops	251	579
Block Ram	2 x 18k	2 x 18k
DSPs	2	2
Time taken (ms)	0.3135	0.2635

Sequential Multiplier - HDL

	Before	After
LUTs - logic	379	435
LUTs - memory	80	80
Flip-flops	135	230
Block Ram	0	0
DSPs	3	0
Time taken (ms)	0.1817	0.7297