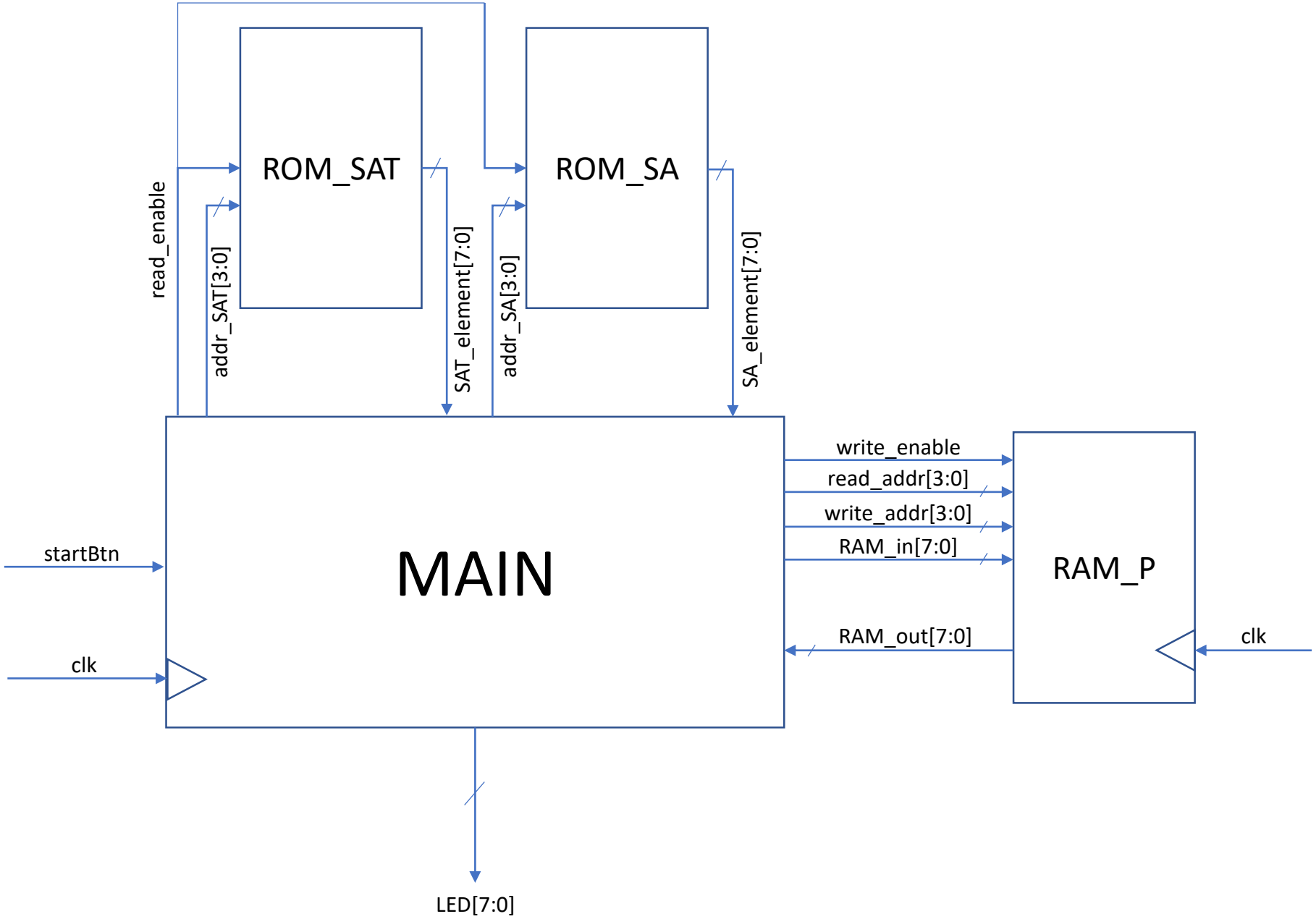
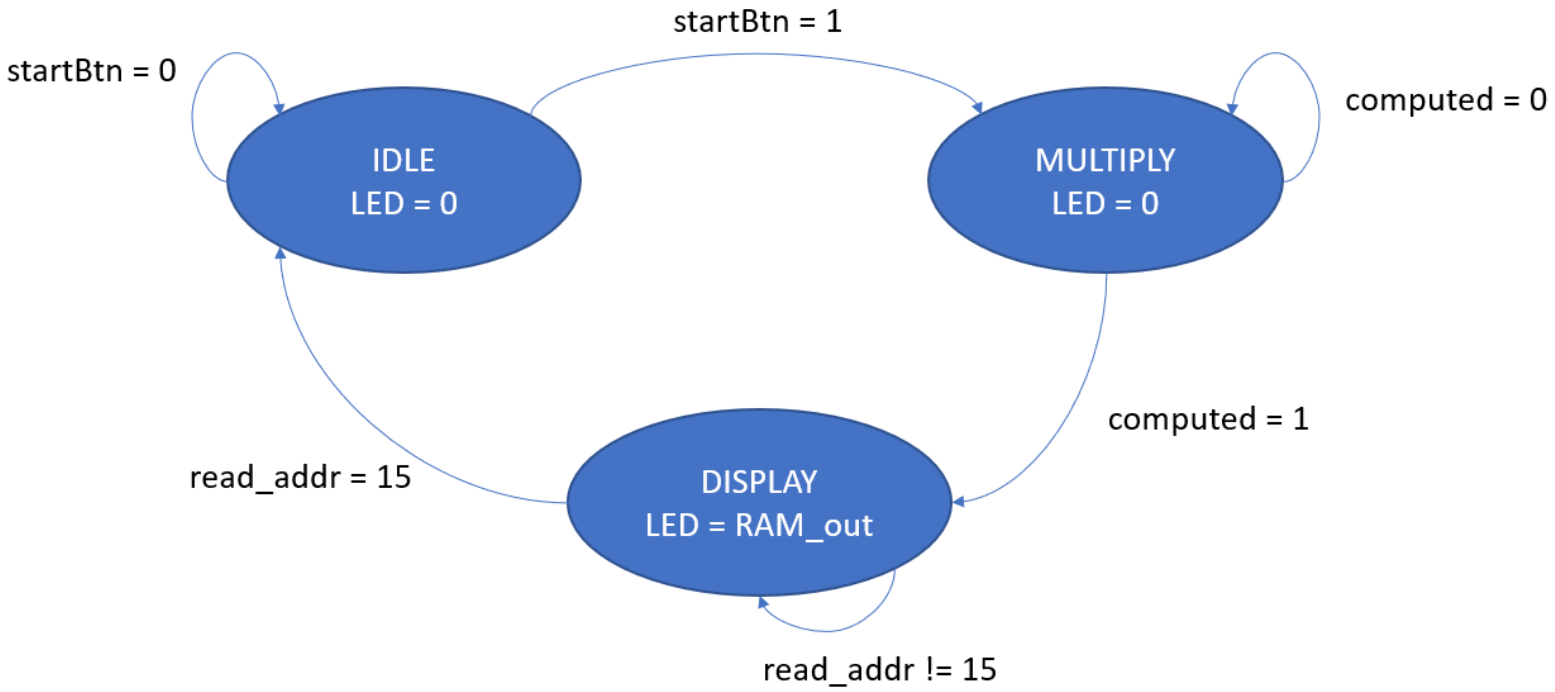
System Architecture

1. After startBtn is pressed, read_enable will be set to 1 to allow reading of ROM values.
2. Following which, these ROM values will be used to calculate the matrix multiplication and values for the product matrix which will be stored in RAM_P.
3. write_enable will be set to 1 after each computation of new elements to allow the new values to be written in RAM_P, with the address being write_addr.
4. After computation of all values are done, the LED will be assigned values from RAM_out, which are the values in RAM_P based on read_addr.



FSM



1. After startBtn is pressed, the state will change from IDLE to MULTIPLY. During MULTIPLY state, values will be read from ROMs to be used to do matrix multiplication.
2. Every cycle in MULTIPLY state represents reading of different values from ROM for matrix multiplication. At every 4 cycles the values of each element are stored in RAM_P. After the matrix multiplication is finished, computed will be set to 1 and the state will change to DISPLAY.
3. In state DISPLAY, the LED will be set to RAM_out values. Each cycle in DISPLAY state represents different RAM_out values being set to LED. Only after read_addr is 15, which means that all 16 values have been displayed, will the state change back to IDLE state.

Resources

Slice Logic Distribution

Site Type	Used	Fixed	Available	Util%
Slice	35	0	13300	0.26
SLICEL	21	0		
SLICEM	14	0		
LUT as Logic	87	0	53200	0.16
using O5 output only	0			
using O6 output only	71			
using O5 and O6	16			
LUT as Memory	8	0	17400	0.05
LUT as Distributed RAM	8	0		
using O5 output only	0			
using O6 output only	0			
using O5 and O6	8			
LUT as Shift Register	0	0		
LUT Flip Flop Pairs	23	0	53200	0.04
fully used LUT-FF pairs	3			
LUT-FF pairs with one unused LUT output	18			
LUT-FF pairs with one unused Flip Flop	20			
Unique Control Sets	5			

Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	140	0.00
RAMB36/FIFO*	0	0	140	0.00
RAMB18	0	0	280	0.00

DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	220	0.00

As we used distributed memory for both RAMs and ROMs, Block RAM usage is 0. We used distributed memory as it is more efficient since the number of values to be stored are minimal and FPGAs has a high number of LUTs. SLICEM are used for memory related LUTs whereas SLICEL are used for logic related LUTs. The 8 LUTs used as distributed RAM is for RAM whereas ROMs are implemented using LUT as Logic.