Module 3

Embedded System Concepts

3.1 What is an Embedded System?

- An embedded system is an electronic/electro-mechanical system designed to perform a specific function and is a combination of both hardware and firmware (software).
- Every embedded system is unique, and the hardware as well as the firmware is highly specialized to the application domain. Embedded systems are becoming an inevitable part of any product or equipment in all fields including household appliances, telecommunications, medical equipment, industrial control, consumer products, etc.

3.2 EMBEDDED SYSTEMS vs. GENERAL COMPUTING SYSTEMS

The Embedded System and the General purpose computer are at two extremes. The embedded system is designed to perform a specific task whereas as per definition the general purpose computer is meant for general use. It can be used for playing games, watching movies, creating software, work on documents or spreadsheets etc. Following are certain specific points that differentiate between embedded systems and general purpose computers:

Embedded Systems Vs General Computing Systems

General Purpose System	Embedded System
A system which is a combination of generic hardware and General Purpose Operating System for executing a variety of applications	A system which is a combination of special purpose hardware and embedded OS for executing a specific set of applications
Contain a General Purpose Operating System (GPOS)	May or may not contain an operating system for functioning
Applications are alterable (programmable) by user (It is possible for the end user to re-install the Operating System, and add or remove user applications)	The firmware of the embedded system is pre-programmed and it is non-alterable by end-user (There may be exceptions for systems supporting OS kernel image flashing through special hardware settings)
Performance is the key deciding factor on the selection of the system. Always 'Faster is Better'	Application specific requirements (like performance, power requirements, memory usage etc) are the key deciding factors
Less/not at all tailored towards reduced operating power requirements, options for different levels of power management.	Highly tailored to take advantage of the power saving modes supported by hardware and Operating System
Response requirements are not time critical	For certain category of embedded systems like mission critical systems, the response time requirement is highly critical
Need not be deterministic in execution behavior	Execution behavior is deterministic for certain type of embedded systems like 'Hard Real Time' systems

3.3 HISTORY OF EMBEDDED SYSTEMS:

- Embedded systems were in existence even before the IT revolution. In the olden days embedded systems were built around the old vacuum tube and transistor technologies and the embedded algorithm was developed in low level languages.
- Advances in semiconductor and Nano-technology and IT revolution gave way to the development of miniature embedded systems.
- The first recognized modem embedded system is the Apollo Guidance Computer (AGC) developed by the MIT Instrumentation Laboratory for the lunar expedition. They ran the inertial guidance systems of both the Command Module (CM) and. the Lunar Excursion Module (LEM). The Command Module was designed to encircle the moon while the Lunar Module and its crew were designed to go down to the moon surface and land there safely.
- MIT's original design was based on 4K words of fixed memory (Read Only Memory) and 256 words of erasable memory (Random Access Memory).
- The first mass-produced embedded system was the guidance computer for the Minuteman-I missile in 1961. It was the 'Autonetics D-l7 guidance computer, built using discrete transistor logic and a hard-disk for main memory. The first integrated circuit was produced in September 1958 but computers using them didn't begin to appear until 1963.

3.4 CLASSIFICATION OF EMBEDDED SYSTEMS:

The classifications of embedded systems are:

1. Based on generation
2. Complexity and performance requirements
3. Based on deterministic behavior
4. Based on triggering.

1. **Classification Based on generation:**

This classification is based on the order in which the embedded processing systems evolved from the first version to where they are today. As per this criterion, embedded systems can be classified into:

- **First Generation:**
  - The early embedded systems were built around 8bit microprocessors like 8085 and Z80, and 4bit microcontrollers.
  - Simple in hardware circuits with firmware developed in Assembly code.
  - Digital telephone keypads, stepper motor control units etc. are examples of this.
- **Second Generation:**
  - These are embedded systems built around 16bit microprocessors and 8 or 16 bit microcontrollers, following the first generation embedded systems.
  - The instruction set for the second generation processors/controllers were much more complex and powerful than the first generation processors/controllers.
  - Some of the second generation embedded systems contained embedded operating systems for their operation.
  - Data Acquisition Systems, SCADA systems, etc. are examples of second generation embedded systems.
- **Third Generation:**
  - With advances in processor technology, embedded system developers started making use of powerful 32bit processors and 16bit microcontrollers for their design.
  - A new concept of application and domain specific processors/controllers like Digital Signal Processors (DSP) and Application Specific Integrated Circuits (ASICs) came into the picture.
  - The instruction set of processors became more complex and powerful and the concept of instruction pipelining also evolved.
  - Dedicated embedded real time and general purpose operating systems entered into the embedded market. Embedded systems spread its ground to areas like robotics, media, industrial process control, networking, etc.

- **Fourth Generation:**
  - The advent of System on Chips (SoC), reconfigurable processors and multicore processors are bringing high performance, tight integration and miniaturisation into the embedded device market.
  - The SoC technique implements a total system on a chip by integrating different functionalities with a processor core on an integrated circuit.
  - The fourth generation embedded systems are making use of high performance real time embedded operating systems for their functioning. Smart phone devices, mobile internet devices (MIDs), etc. are examples of fourth generation embedded systems.

2. Classification Based on Complexity and Performance:

This classification is based on the complexity and system performance requirements. According to this classification, embedded systems can be grouped into:

- **Small-Scale Embedded Systems**:
  - Embedded systems which are simple in application needs and where the performance requirements are not time critical fall under this category.
  - An electronic toy is a typical example of a small-scale embedded system. Small-scale embedded systems are usually built around low performance and low cost 8 or 16 bit microprocessors/microcontroliers.
  - A small-scale embedded system may or may not contain an operating system for its functioning.
- **Medium-Scale Embedded Systems:**
  - Embedded systems which are slightly complex in hardware and firmware (software) requirements fall under this category.
  - Medium-scale embedded systems are usually built around medium performance, low cost 16 or 32 bit microprocessors/microcontrollers or digital signal processors.
  - They usually contain an embedded operating system (either general purpose or real time operating system) for functioning.

- **Large-Scale Embedded Systems/Complex Systems**:
  - Embedded systems which involve highly complex hardware and firmware requirements fall under this category. They are employed in mission critical applications demanding high performance. Such systems are commonly built around high performance 32 or 64 bit RISC processors/controllers or Reconfigurable System on Chip (RSoC) or multi-core processors and programmable logic devices.
  - They may contain multiple processors/controllers and co-units/hardware accelerators for offloading the processing requirements from the main processor of the system.
  - Complex embedded systems usually contain a-high performance Real Time Operating System (RTOS) for task scheduling, prioritization and management.

3. **Based on Deterministic Behaviour:**
   - This classification is applicable for "Real Time" systems.
   - The task execution behavior for an embedded system may be deterministic or nondeterministic.
   - Based on execution behavior Real Time embedded systems are divided into Hard and Soft.
4. **Based on triggering:**

   Embedded systems which are "Reactive" in nature can be based on triggering. Reactive systems can be:
   - Event triggered
   - Time triggered

3.5 APPLICATIONS OF EMBEDDED SYSTEM:

The application areas and the products in the embedded domain are countless.

1. Consumer Electronics: Camcorders, Cameras.
2. Household appliances: Washing machine, Refrigerator.
3. Automotive industry: Anti-lock braking system(ABS), engine control.

4. Home automation & security systems: Air conditioners, sprinklers, fire alarms.
5. Telecom: Cellular phones, telephone switches.
6. Computer peripherals: Printers, scanners.
7. Computer networking systems: Network routers and switches.
8. Healthcare: EEG, ECG machines.
9. Banking & Retail: Automatic teller machines, point of sales.
10. Card Readers: Barcode, smart card readers.

3.6 PURPOSE OF EMBEDDED SYSTEMS:

Each embedded system is designed to serve-the purpose of any one or a combination of the following tasks:

1. Data collection/Storage/Representation
2. Data communication
3. Data (signal) processing
4. Monitoring
5. Control
6. Application specific user interface

1) Data Collection/Storage/Representation

- Embedded system designed for the purpose of data collection performs acquisition of data from the external world.
- Data collection is usually done for storage, analysis, manipulation and transmission.
- Data can be analog or digital.
- Embedded systems with analog data capturing techniques collect data directly in the form of analog signal whereas an embedded system with digital data collection mechanism converts the analog signal to the digital signal using analog to digital converters.

- If the data is digital it can be directly captured by digital embedded system.
- A digital camera is a typical example of an embedded System with data collection/storage/representation of data.
- Images are captured and the captured image may be stored within the memory of the camera. The captured image can also be presented to the user through a graphic LCD unit.

2) Data Communication:

- Embedded data communication systems are deployed inapplications from complex satellite communication to simple home networking systems.
- The transmission of data is achieved either by a wire-lin medium or by a wire-less medium. Data can either be transmitted by analog means or by digital means.
- Wireless modules-Bluetooth, Wi-Fi.
- Wire-line modules-USB, TCP/IP.
- Network hubs, routers, switches are examples of dedicated data transmission embedded systems.

3) Data (Signal) Processing:

- Embedded systems with signal processing functionalities are employed in applications demanding signal processing like speech coding, audio video codec, transmission applications etc.
- A digital hearing aid is a typical example of an embedded system employing data processing. Digital hearing aid improves the hearing capacity of hearing impaired person.

4) Monitoring:

- All embedded products coming under the medical domain are with monitoring functions.
- Almost all embedded products coming under the medical domain are with monitoring functions only. They are used for determining the state of some variables using input sensors.

- Electro cardiogram machine is intended to do the monitoring of the heartbeat of a patient but it cannot impose control over the heartbeat.
- Other examples with monitoring function are digital CRO, digital multi-meters, and logic analysers.

5) Control:

- Embedded systems with control functionalities impose control over some variables according to the changes in input variables.
- A system with control functionality contains both sensors and actuators Sensors are connected to the input port for capturing the changes in environmental variable and the actuators connected to the output port are controlled according to the changes in the input variable.
- Air conditioner system used to control the room temperature to a specified limit is a typical example for CONTROL purpose.

6) Application Specific User Interface:

- Buttons, switches, keypad, lights, bells, display units etc, are application specific user interfaces.
- Mobile phone is an example of application specific user interface.
- In mobile phone the user interface is provided through the keypad, system speaker, vibration alert etc.

The Typical Embedded System

INTRODUCTION

• A typical embedded system (Figure) contains a single chip controller, which acts as the master brain of the system. The controller can be a Microprocessor' (e.g. Intel 8085) or a microcontroller (e.g. Atmel AT89C51) or a Field Programmable Gate Array (FPGA) device (e.g. Xilinx Spartan) or a Digital Signal Processor (DSP) (e.g. Blackfin® Processors from Analog

Devices) or an Application Specific Integrated Circuit (ASIC)/Application Specific Standard Product (ASSP) (e.g. ADE7760 Single Phase Energy Metering IC from) Analog Devices for energy metering applications).

- Embedded hardware/software systems are basically designed to regulate a physical variable or to manipulate the state of some devices by sending some control signals to the Actuators or devices connected to the O/p ports of the system, in response to the input signals provided by the end users or Sensors which are connected to the input ports.

- Hence an embedded system can be viewed as a reactive system. The control is achieved by processing the information coming from the sensors and user interfaces, and controlling some actuators that regulate the physical variable.

- Key boards, push button switches, etc. are examples for common user interface input devices whereas LEDs, liquid crystal displays, piezoelectric buzzers, etc. are examples for common user interface output devices for a typical embedded system.

- It should be noted that it is not necessary that all embedded systems should incorporate these I/O user interfaces. It solely depends on the type of the application for which the embedded system is designed.

- For example, if the embedded system is designed for any handheld application, such as a mobile handset application, then the system should contain user interfaces like a keyboard for performing input operations and display unit for providing users the status of various activities in progress.

- Some embedded systems do not require any manual intervention for their operation. They automatically sense the variations in the input parameters in accordance with the changes in the real world, to which they are interacting through the sensors which are connected to the input port of the system.

- The sensor information is passed to the processor after signal conditioning and digitization.

• Upon receiving the sensor data the processor or brain of the embedded system performs some pre-defined operations with the help of the firmware embedded in the system.

• Then it sends some actuating signals to the actuator connected to the output port of the embedded system, which in turn acts on the controlling variable to bring the controlled variable to the desired level to make the embedded system work in the desired manner.

• The Memory of the system is responsible for holding the control algorithm and other important configuration details.

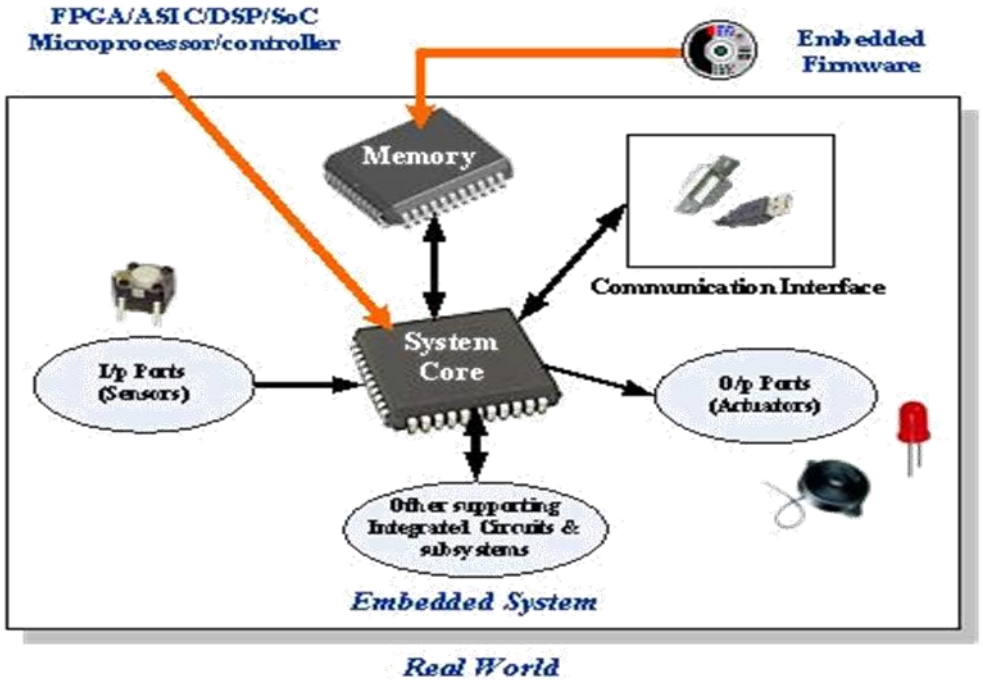


Fig: Elements of an embedded system

• For most of embedded systems, the memory for storing the algorithm or configuration data is of fixed type, which is a kind of Read Only Memory (ROM) and it is not available for the end user for modifications, which means the memory is protected from unwanted user interaction by implementing some kind of memory protection mechanism.

• The most common types of memories used in embedded systems for control algorithm storage are OTP, PROM, UVEPROM, EEPROM and FLASH.

- Depending on the control application, the memory size may vary from a few bytes to megabytes.

- Sometimes the system requires temporary memory for performing arithmetic operations or control algorithm execution and this type of memory is known as “working memory”.

Random Access Memory (RAM) is used in most of the systems as the working memory.

- Various types of RAM like SRAM, DRAM and NVRAM are used for this purpose. The size of the RAM also varies from a few bytes to kilobytes or megabytes depending on the application.

- An embedded system without a control algorithm implemented memory is just like a new born baby. It is having all the peripherals but is not capable of making any decision depending on the situational as well as real world changes.

- The only difference is that the memory of a new born baby is self-adaptive, meaning that the baby will try to learn from the surroundings and from the mistakes committed. For embedded systems it is the responsibility of the designer to impart intelligence to the system.

- In a controller-based embedded system, the controller may contain internal memory for storing the control algorithm and it may be an EEPROM or FLASH memory varying from a few kilobytes to mega¬ bytes.Such controllers are called controllers with on-chip ROM, e.g. Atmel AT89C51.

- Some controllers may not contain on-chip memory and they require an external (off-chip) memory for holding the control algorithm, e.g. Intel 8031 AH.

3.7 CORE OFTHE EMBEDDED SYSTEM

Embedded systems are domain and application specific and are built around a central core.

The core of the embedded system falls into any one of the following categories:

1. **General Purpose and Domain Specific Processors**

   - Microprocessors
   - Microcontrollers
   - Digital Signal Processors

2. **Application Specific Integrated Circuits (ASICs)**

3. **Programmable Logic Devices (PLDs)**

4. **Commercial off-the-shelf Components (COTS)**

If you examine any embedded system you will find that it is built around any of the core units mentioned above.

A. General Purpose and Domain Specific Processors

- Almost 80% of the embedded systems are processor/controller based.

- The processor may be a microprocessor or a microcontroller or a digital signal processor, depending on the domain and application.

- Most of the embedded systems in the industrial control and monitoring applications make use of the commonly available microprocessors or microcontrollers.

- Domains which require signal processing such as speech coding, speech recognition, etc. make use of special kind of digital signal processors supplied by manufacturers like, Analog Devices, Texas Instruments, etc.

a. Microprocessors

• A Microprocessor is a silicon chip representing a central processing unit (CPU), which is capable of performing arithmetic as well as logical operations according to a predefined set of instructions, which is specific to the manufacturer.

• In general the CPU contains the Arithmetic and Logic Unit (ALU), control unit and working registers. A microprocessor is a dependent unit and it requires the combination of other hardware like memory, timer unit, and interrupt controller, etc. for proper functioning.

• Intel claims the credit for developing the first microprocessor unit Intel 4004, a 4bit processor which was released in November 1971. It featured IK data memory, a 12bit program counter and 4K program memory, sixteen 4bit general purpose registers and 46 instructions.

• In 1972,14 more instructions were added to the 4004 instruction set and the program space is upgraded to 8K. Also interrupt capabilities were added to it and it is renamed as Intel 4040.

• It was quickly replaced in April 1972 by Intel 8008 which was similar to Intel 4040, the only difference was that its program counter was 14 bits wide and the 8008 served as a terminal controller.

• In April 1974 Intel launched the first 8 bit processor, the Intel 8080, with 16bit address bus and program counter and seven 8bit registers (A-E,H,L: BC, DE, and HL pairs formed the 16bit register for this processor).

• Intel 8080 was the most commonly used processors for industrial control and other embedded applications in the 1975s. Since the processor required other hardware components as mentioned earlier for its proper functioning, the systems made out of it were bulky and were lacking compactness.

• Immediately after the release of Intel 8080, Motorola also entered the market with their processor, Motorola 6800 with a different architecture and instruction set compared to 8080.

- In 1976 Intel came up with the upgraded version of 8080-Intel 8085, with two newly added instructions, three interrupt pins and serial I/O. Clock generator and bus controller circuits were built-in and the power supply part was modified to a single +5 V supply.

- In July 1976 Zilog entered the microprocessor market with its Z80 processor as competitor to Intel. It was an improved version of Intel's 8080 processor, maintaining the original 8080 architecture and instruction set with an 8bit data bus and a 16bit address bus and was capable of executing all instructions of 8080.

- It included 80 more new instructions and it brought out the concept of register banking by doubling the register set. Z80 also included two sets of index registers for flexible design.

- Technical advances in the field of semiconductor industry brought a new dimension to the microprocessor market and twentieth century witnessed a fast growth in, processor technology.

- 16, 32 and 64 bit processors came into the place of conventional 8bit processors. The initial 2 MHz clock is now an old story. Today processors with clock speeds up to 2.4 GHz are available in the market.

- More and more competitors entered into the processor market offering high speed, high performance and low cost processors for customer design needs.

- Intel, AMD, Free scale, IBM, TI, Cyrix, Hitachi, NEC, LSI Logic, etc. are the key players in the processor market.

- Intel still leads the market with cutting edge technologies in the processor industry.

- Different instruction set and system architecture are available for the design of a microprocessor.

- Harvard and Von-Neumann are the two common system architectures for processor design.

- Processors based on Harvard architecture contains separate buses for program memory and data memory, whereas processors based on Von-Neumann architecture shares a single system bus for program and data memory.

- Reduced Instruction Set Computing (RISC) and Complex Instruction Set Computing (CISC) are the two common Instruction Set Architectures (ISA) available for processor design.

General Purpose Processor (GPP) vs. Application-Specific Instruction Set Processor (ASIP)

- A General Purpose Processor (GPP) is a processor designed for general computational tasks. The processor running inside the laptop or desktop (Pentium 4/AMD Athlon, etc.) is a typical example for general purpose processor.

- They are produced in large volumes and targeting the general market. Due to the high volume production, the per unit cost for a chip is low compared to ASIC or other specific ICs.

- A typical general purpose processor contains an Arithmetic and Logic Unit (ALU) and Control Unit (CU).

- Application Specific Instruction Set Processors (ASIPs) are processors with architecture and instruction set optimized to specific-domain/application requirements like network processing, automotive, telecom, media applications, digital signal processing, control applications, etc.

- ASIPs fill the architectural spectrum between general purpose processors and Application Specific Integrated Circuits (ASICs).

- The need for an ASIP arises when the traditional general purpose processor are unable to meet the increasing application needs.

- Most of the embedded systems are built around application specific instruction set processors. Some microcontrollers (like automotive AVR, USB AVR from Atmel), system on

chips, digital signal processors, etc. are examples for application specific instruction set processors (ASIPs).

- ASIPs incorporate a processor and on-chip peripherals, demanded by the application requirement, program and data memory.

b. Microcontrollers

- A Microcontroller is a highly integrated chip that contains a CPU, scratch pad RAM, special and general purpose register arrays, on chip ROM/FLASH memory for program storage, timer and interrupt control units and dedicated I/O ports.

- Microcontrollers can be considered as a super set of microprocessors. Since a microcontroller contains all the necessary functional blocks for independent working, they found greater place in the embedded domain in place of microprocessors. Apart from this, they are cheap, cost effective and are readily available in the market.

- Texas Instrument's TMS1000 is considered as the world's first microcontroller. We cannot TI followed Intel's 4004/4040, 4 bit processor design and added some amount of RAM, program storage memory (ROM) and I/O support on a single chip, there by eliminated the requirement of multiple hardware chips for self-functioning.

- Provision to add custom instructions to the CPU was another innovative feature of TMS 1000. TMS 1000 was released in 1974.

- In 1977 Intel entered the microcontroller market with a family of controllers coming under one umbrella named MCS-48™ family. The processors came under this family were

8038HL, 8039HL, 8040AHL, 8048H, 8049H and 8050AH.

- Intel 8048 is recognized as Intel's first microcontroller and it was the most prominent member in the MCS-48™family.

- The design of 8048 adopted a true Harvard architecture where program and data memory shared the same address bus and is differentiated by the related control signals.

- Eventually Intel came out with its most fruitful design in the 8bit microcontroller domain-the 8051 family and its derivatives. It is the most popular and powerful 8bit microcontroller ever built.

- It was developed in the 1980s and was put under the family MCS-51. Almost 75% of the microcontrollers used in the embedded domain were 8051 family based controllers during the 1980—90s.

- 8051 processor cores are used in more than 100 devices by more than 20 independent manufacturers like Maxim, Philips, Atmel, etc. under the license from Intel.

- Due to the low cost, wide availability, memory efficient instruction set, mature development tools and Boolean processing (bit manipulation operation) capability, 8051 family derivative microcontrollers are much used in high-volume consumer electronic devices, entertainment industry7 and other gadgets where cost-cutting is essential.

- Another important family of microcontrollers used in industrial control and embedded applications is the PIC family micro controllers from Microchip Technologies. It is a high performance RISC microcontroller complementing the CISC features of 8051.

- Some embedded system applications require only 8bit controllers whereas some embedded applications requiring superior performance and computational needs demand 16/32bit microcontrollers. I

- Infineon, Freescale, Philips, Atmel, Maxim, Microchip etc. are the key suppliers of 16bit microcontrollers. Philips tried to extend the 8051 family microcontrollers to use for 16bit applications by developing the Philips XA (extended Architecture) microcontroller series.

- 8bit microcontrollers are commonly used in embedded systems where the processing power is not a big constraint. As mentioned earlier, more than 20 companies are producing different flavours of the 8051 family microcontroller. They try to add more and more

functionalities like built in SPI, I2C serial buses, USB controller, ADC, Networking capability, etc. So the competitive market is driving towards a one-stop solution chip in microcontroller domain. High processing speed microcontroller families like ARM11 series are also available in the market, which provides solution to applications requiring hardware acceleration and high processing capability.

- Freescale, NEC, Zilog, Hitachi, Mitsubishi, Infineon, ST Micro Electronics, National, Texas Instruments, Toshiba, Philips, Microchip, Analog Devices, Daewoo, Intel, Maxim, Sharp, Silicon Laboratories, TDK, Triscend, Winbond, Atmel, etc. are the key players in the microcontroller market.

- Atmel has got special significance. They are the manufacturers of a variety of Flash memory based microcontrollers. They also provide In-System Programmability for the controller.

- The Flash memory technique helps in fast reprogramming of the chip and thereby reduces the product development time. Atmel also provides another special family of microcontroller called AVR, an 8bit RISC Flash microcontroller, fast enough to execute powerful instructions in a single clock cycle.

- The instruction set architecture of a microcontroller can be either RISC or CISC.

- Microcontrollers are designed for either general purpose application requirement (general purpose controller) or domain- specific application requirement (application specific instruction set processor).

- The Intel 8051 microcontroller is a typical example for a general purpose microcontroller, whereas the automotive AVR microcontroller family from Atmel Corporation is a typical example for ASIP specifically designed for the automotive domain.

Microprocessor vs Microcontroller:

Microprocessor	Microcontroller
A silicon chip representing a Central Processing Unit (CPU), which is capable of performing arithmetic as well as logical operations according to a pre-defined set of Instructions	A microcontroller is a highly integrated chip that contains a CPU, scratch pad RAM, Special and General purpose Register Arrays, On Chip ROM/FLASH memory for program storage, Timer and Interrupt control units and dedicated I/O ports
It is a dependent unit. It requires the combination of other chips like Timers, Program and data memory chips, Interrupt controllers etc for functioning	It is a self contained unit and it doesn't require external Interrupt Controller, Timer, UART etc for its functioning
Most of the time general purpose in design and operation	Mostly application oriented or domain specific
Doesn't contain a built in I/O port. The I/O Port functionality needs to be implemented with the help of external Programmable Peripheral Interface Chips like 8255	Most of the processors contain multiple built-in I/O ports which can be operated as a single 8 or 16 or 32 bit Port or as individual port pins
Targeted for high end market where performance is important	Targeted for embedded market where performance is not so critical (At present this demarcation is invalid)
Limited power saving options compared to microcontrollers	Includes lot of power saving features

c. Digital Signal Processors

• Digital Signal Processors (DSPs) are powerful special purpose 8/16/32 bit microprocessors designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications.

• Digital signal processors are 2 to 3 times faster than the general purpose microprocessors in signal processing applications.

• DSPs implement algorithms in hardware which speeds up the execution whereas general purpose processors implement the algorithm in firmware and the speed of execution depends primarily on the clock for the processors.

• In general, DSP can be viewed as a microchip designed for performing high speed computational operations for 'addition', 'subtraction', 'multiplication' and 'division'.

• A typical digital signal processor incorporates the following key units:

Program Memory: Memory for storing the program required by DSP to process the data

Data Memory: Working memory for storing temporary variables and data/signal to be processed.

Computational Engine: Performs the signal processing in accordance with the stored program memory. It incorporates many specialized arithmetic units and each of them operates simultaneously to increase the execution speed.

It also incorporates multiple hardware shifters for shifting operands and thereby saves execution time.

I/O Unit: Acts as an interface between the outside world and DSP. It is responsible for capturing signals to be processed and delivering the processed signals.

Audio video signal processing, telecommunication and multimedia applications are typical examples where DSP is employed.

Digital signal processing employs a large amount of real-time calculations. Sum of products (SOP) calculation, convolution, fast fourier transform (FFT), discrete fouriertransfonn (DFT), etc, are some of the operations performed by digital signal processors.

Blackfin processor from Analog Devices is an example of DSP which delivers breakthrough signal-processing performance and power efficiency while also offering a full 32-bit RISC MCU programming model.

Blackfin processors present high-performance, homogeneous software targets, which allows flexible resource allocation between hard real-time signal processing tasks and non real-time control tasks.

System control tasks can often run in the shadow of demanding signal processing and multimedia tasks.

RISC vs. CISC Processors/Controllers

• For determining the RISC/CISC criteria. Some of the important criteria are listed below:

RISC	CISC
Lesser no. of instructions	Greater no. of Instructions
Instruction Pipelining and increased execution speed	Generally no instruction pipelining feature
Orthogonal Instruction Set (Allows each instruction to operate on any register and use any addressing mode)	Non Orthogonal Instruction Set (All instructions are not allowed to operate on any register and use any addressing mode. It is instruction specific)
Operations are performed on registers only, the only memory operations are load and store	Operations are performed on registers or memory depending on the instruction
Large number of registers are available	Limited no. of general purpose registers
Programmer needs to write more code to execute a task since the instructions are simpler ones	Instructions are like macros in C language. A programmer can achieve the desired functionality with a single instruction which in turn provides the effect of using more simpler single instructions in RISC
Single, Fixed length Instructions	Variable length Instructions
Less Silicon usage and pin count	More silicon usage since more additional decoder logic is required to implement the complex instruction decoding.
With Harvard Architecture	Can be Harvard or Von-Neumann Architecture

• The term RISC stands for Reduced Instruction Set Computing. As the name implies, all RISC processors/controllers possess lesser number of instructions, in the range of 30 to 40.

• CISC stands for Complex Instruction Set Computing. From the definition itself it is clear that the instruction set is complex and instructions are high in number.

• From a programmers point of view RISC processors are comfortable since s/he needs to learn only a few instructions, whereas for a CISC processor s/he needs to learn more number of instructions and should understand the context of usage of each instruction.

• Atmel AVR microcontroller is an example for a RISC processor and its instruction set contains only 32 instructions.

• The original version of 8051 microcontroller (e.g. AT89C51) is a CISC controller and its instruction set contains 255 instructions.

• Remember it is not the number of instructions that determines whether a processor/controller is CISC or RISC. There are some other factors like pipelining features, instruction set type, etc.

Harvard vs. Von-Neumann Processor/Controller Architecture

- The terms Harvard and Von-Neumann refers to the processor architecture design.
- Microprocessors/controllers based on the Von-Neumann architecture shares a single common bus for fetching both instructions and data. Program instructions and data are stored in a common main memory.
- Von-Neumann architecture based processors/controllers first fetch an instruction and then fetch the data to support the instruction from code memory. The two separate fetches slows down the controller's operation.
- Von-Neumann architecture is also referred as Princeton architecture, since it was developed by the Princeton University.
- Microprocessors/controllers based on the Harvard architecture will have separate data bus and instruction bus. This allows the data transfer and program fetching to occur simultaneously on both buses.
- With Harvard architecture, the data memory, can be read and written while the program memory is being accessed.
- These separated data memory and code memory buses allow one instruction to execute while the next instruction is fetched ("pre-fetching"). The pre-fetch theoretically allows much faster execution than Von-Neumann architecture.
- Since some additional hardware logic is required for the generation of control signals for this type of operation it adds silicon complexity to the system.
- Figure explains the Harvard and Von-Neumann architecture concept.

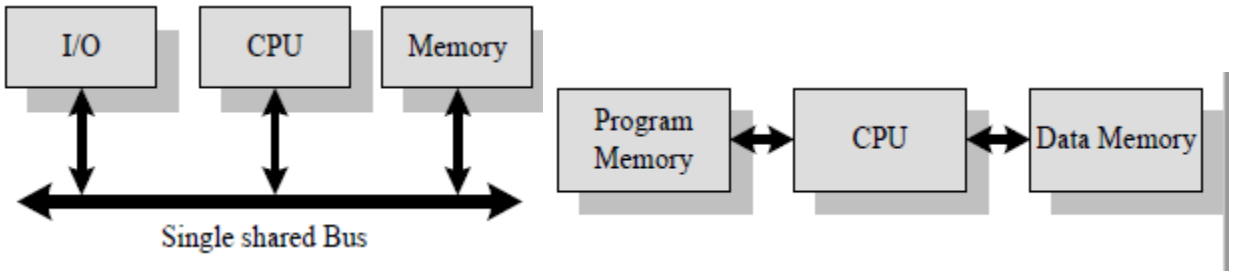


Fig: Harvard vs Von-Neumann architecture

Harvard Architecture	Von-Neumann Architecture
Separate buses for Instruction and Data fetching	Single shared bus for Instruction and Data fetching
Easier to Pipeline, so high performance can be achieved	Low performance Compared to Harvard Architecture
Comparatively high cost	Cheaper
No memory alignment problems	Allows self modifying codes
Since data memory and program memory are stored physically in different locations, no chances for accidental corruption of program memory	Since data memory and program memory are stored physically in same chip, chances for accidental corruption of program memory

Big-Endian vs. Little-Endian Processors/Controllers

• Endianness specifies the order in which the data is stored in the memory by processor operations in a multi byte system (Processors whose word size is greater than one byte).

• Suppose the word length is two byte then data can be stored in memory in two different ways:

[1] Higher order of data byte at the higher memory and lower order of data byte at location just below the higher memory.
[2] Lower order of data byte at the higher memory and higher order of data byte at location just below the higher memory.

Little-endian means the lower-order byte of the data is stored in memory at the lowest address, and the higher-order byte at the highest address. (The little end comes first.)

For example, a 4 byte long integer Byte3 Byte2 Bytel ByteO will be stored in the memory as shown below:

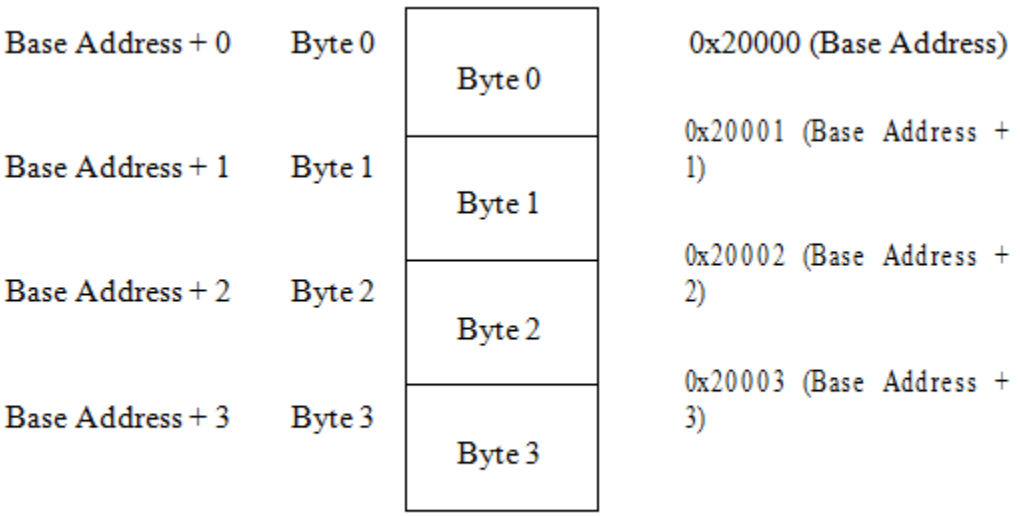


Fig: Little-Endian operation

Big-endian means the higher-order byte of the data is stored in memory at the lowest address, and the lower-order byte at the highest address. (The big end comes first.)

For example, a 4 byte long integer Byte3 Byte2 Bytel ByteO will be stored in the memory as follows:

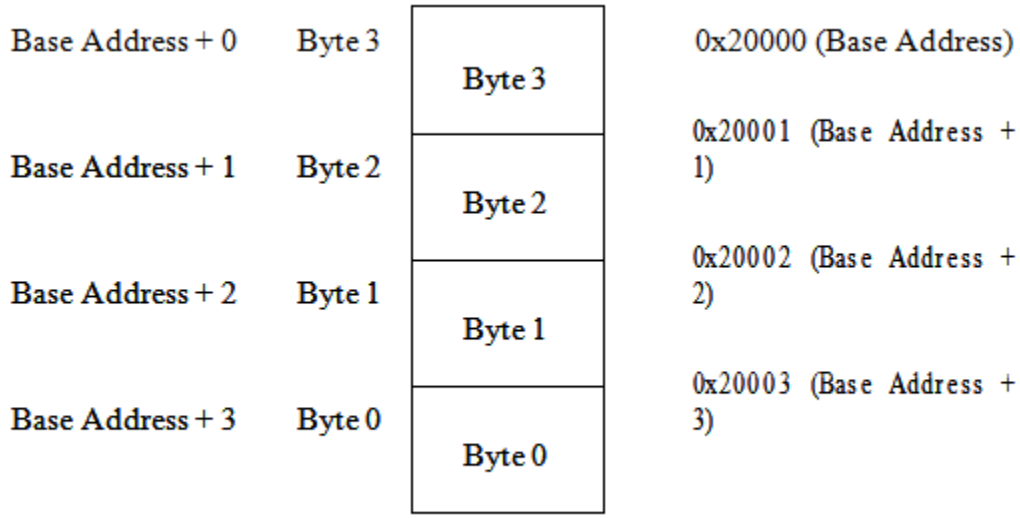


Fig: Big-Endian operation

Load Store Operation and Instruction Pipelining

- As mentioned earlier, the RISC processor instruction set is orthogonal, meaning it operates on registers. The memory access related operations are perforated by the special instructions load and store.

- If the operand is specified as memory location, the content of it is loaded to a register using the load instruction.

- The instruction store, stores data from a specified register to a specified memory location.

- The concept of Load Store Architecture is illustrated with the following example:

- Suppose x, y and z are memory locations and we want to add the contents of x and y and store the result in location z. Under the load store architecture the same is achieved with 4 instructions as shown in Figure.

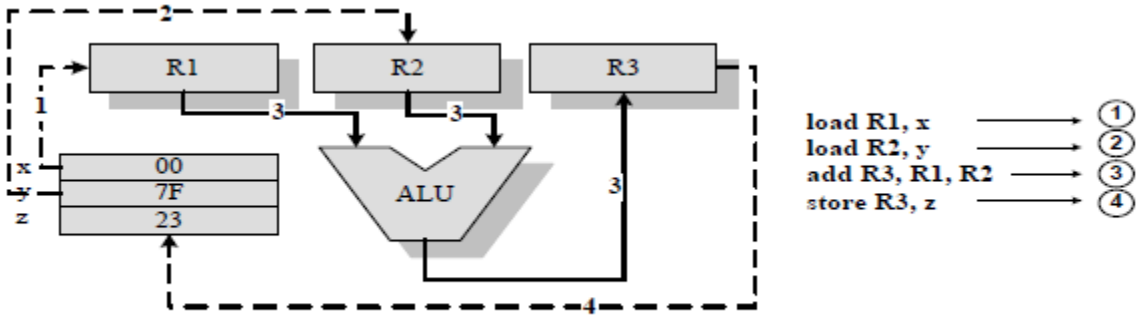


Fig: The concept of load store architecture.

•The first instruction load Rl, xloads the register R1 with the content of memory location x.

- The second instruction load R2,y loads the register R2 with the content of memory location y.

- The instruction add R3, Rl, R2 adds the content of registers Rl and R2 and stores the result in register R3.

- The next instruction store R3,z stores the content of register R3 in memory location z.

- The conventional instruction execution by the processor follows the fetch-decode-execute sequence. Where the 'fetch' part fetches the instruction from program memory or code memory and the decode part decodes the instruction to generate the necessary control signals.

- The execute stage reads the operands, perform ALU operations and stores the result.

- In conventional program execution, the fetch and decode operations are performed in sequence. For simplicity let's consider decode and execution together.

- During the decode operation the memory address bus is available and if it is possible to effectively utilize it for an instruction fetch, the processing speed can be increased.

- In its simplest form instruction pipelining refers to the overlapped execution of instructions.

- Under normal program execution flow it is meaningful to fetch the next instruction to execute, while the decoding and execution of the current instruction is in progress.

- If the current instruction in progress is a program control flow transfer instruction like jump or call instruction, there is no meaning in fetching the instruction following the current instruction. In such cases the instruction fetched is flushed and a new instruction fetch is performed to fetch the instruction.

- Whenever the current instruction is executing the program counter will be loaded with the address of the nextinstruction. In case of jump or branch instruction, the new location is known only after completion of the jump or branch instruction.

- Depending on the stages involved in an instruction (fetch, read register and decode, execute instruction, access an operand in data memory, write back the result to register, etc.), there can be multiple levels of instruction pipelining. Figure 2.6 illustrates the concept of instruction pipelining for single stage pipelining.

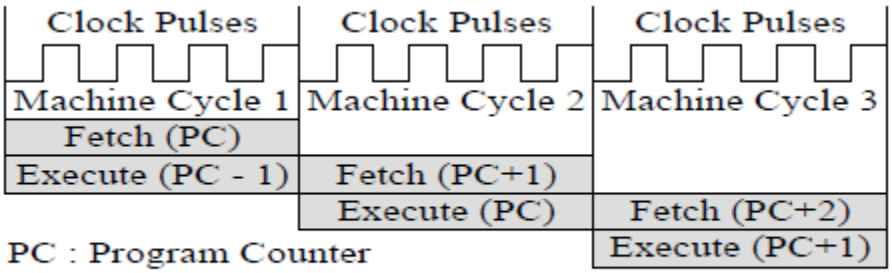


Fig: The single-stage pipelining concept

B. Application Specific Integrated Circuits (ASICs)

- Application Specific Integrated Circuit (ASIC) is a microchip designed to perform a specific or unique application. It is used as replacement to conventional general purpose logic chips.

- It integrates several functions into a single chip and there by reduces the system development cost.

- Most of the ASICs are proprietary products. As a single chip, ASIC consumes a very small area in the total system and thereby helps in the design of smaller systems with high capabilities/functionalities.

- ASICs can be pre-fabricated for a special application or it can be custom fabricated by using the components from a re-usable 'building block' library of components for a particular customer application.

- ASIC based systems are profitable only for large volume commercial productions. Fabrication of ASICs requires a non-refundable initial investment for the process technology and configuration expenses. This investment is known as Non-Recurring Engineering Chargen(NRE) and it is a onetime investment.

- If the Non-Recurring Engineering Charges (NRE) is borne by a third party and the Application Specific Integrated Circuit (ASIC) is made openly available in the market, the ASIC is referred as Application Specific Standard Product (ASSP).

- The ASSP is marketed to multiple customers just as a general-purpose product is, but to a smaller number of customers since it is for a specific application. “The ADE7760 Energy-Meter ASIC developed by Analog Devices for Energy metering applications is a typical example for ASSP”.

- Since Application Specific Integrated Circuits (ASICs) are proprietary products, the developers of such chips may not be interested in revealing the internal details of it and hence it is very difficult to point out an example of it.

- Moreover it will create legal disputes if an illustration of such an ASIC product is given without getting prior permission from the manufacturer of the ASIC.

C. Programmable Logic Devices

- Logic devices provide specific functions, including device-to-device interfacing, data communication, signal processing, data display, timing and control operations, and almost every other function a system must perform.

- Logic devices can be classified into two broad categories-fixed and programmable.

- The circuits in a fixed logic device are permanent, they perform one function or set of functions-once manufactured, they cannot be changed.

- Programmable Logic Devices (PLDs) offer customers a wide range of logic capacity, features, speed, and voltage characteristics-and these devices can be re-configured to perform any number of functions at any time.

- With programmable logic devices, designers use inexpensive software tools to quickly develop, simulate, and test their designs. Then, a design can be quickly programmed into a device, and immediately tested in a live circuit.

- The PLD that is used for this prototyping is the exact same PLD that will be used in the final production of a piece of end equipment, such as a network router, a DSL modem, a DVD player, or an automotive navigation system.

- There are no NRE costs and the final design is completed much faster than that of a custom, fixed logic device.

- Another key benefit of using PLDs is that during the design phase-customers can change the circuitry as often as they want until the design operates to their satisfaction. That's because PLDs are based on re-writable memory technology-to change the design, the device is simply reprogrammed.

- Once the design is final, customers can go into immediate production by simply programming as many PLDs as they need with the final software design file.

CPLDs and FPGAs :

- The two major types of programmable logic devices are Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs).

- Of the two, FPGAsoffer the highest amount of logic density, the most features, and the highest performance.

- The largest FPGA now shipping, part of the Xilinx Virtex™^ line of devices, provides eight million "system gates" (the relative density of logic).

- These advanced devices also offer features such as built-in hardwired processors (such as the IBM power PC), substantial amounts of memory, clock management systems, and support for many of the latest, very fast device-to-device signaling technologies.

- FPGAs are used in a wide variety of applications ranging from data processing and storage, to instrumentation, telecommunications, and digital signal processing.

- CPLDs, by contrast, offer much smaller amounts of logic-up to about 10,000 gates. But CPLDs offer very predictable timing characteristics and are therefore ideal for critical control applications.

- CPLDs such as the Xilinx CoolRunner™^ series also require extremely low amounts of power and are very inexpensive, making them ideal for cost-sensitive, battery-operated, portable applications such as mobile phones and digital handheld assistants.

Advantages of PLD:

PLDs offer a number of important advantages over fixed logic devices, they are as follows

- PLDs offer customers much more flexibility during the design cycle because design iterations are simply a matter of changing the programming file, and the results of design changes can be seen immediately in working parts.

- PLDs do not require long lead times for prototypes or production parts-the PLDs are already on a distributor's shelf and ready for shipment.

- PLDs do not require customers to pay for large NRE costs and purchase expensive mask sets-PLD suppliers incur those costs when they design their programmable devices and are able to amortize those costs over the multi-year lifespan of a given line of PLDs.

- PLDs allow customers to order just the number of parts they need, when they need them, allowing them to control inventory. Customers who use fixed logic devices often end up with-excess inventory which must be scrapped, or if demand for their product surges, they may be caught short of parts and face production delays.

- PLDs can be reprogrammed even after a piece of equipment is shipped to a customer. In fact, thanks to programmable logic devices, a number of equipment manufacturers now tout the ability to add new features or upgrade products that already are in the field. To do this, they simply upload a new programming file to the PLD, via the Internet, creating-new hardware logic in the system.

- Advanced process technologies help PLDs in a number of key areas: faster performance, integration of more features, reduced power consumption, and lower cost.

- FPGAs are especially popular for prototyping ASIC designs where the designer can test his design by downloading the design file into an FPGA device. Once the design is set, hardwired chips are produced for faster performance.

D. Commercial Off-the-Shelf Components (COTS)

- A Commercial Off-the-Shelf (COTS) product is one which is used 'as-is'.
- COTS products are designed in such a way to provide easy integration and interoperability with existing system components.
- The COTS component itself may be developed around a general purpose or domain specific processor or an Application Specific Integrated circuit or a programmable logic device.
- Typical examples of COTS hardware unit are remote controlled toy car control units including the RT circuitry part, high performance, high frequency microwave electronics (2-200 GHz), high bandwidth analog-to-digital converters, devices and components for operation at very high temperatures, electro-optic IR imaging arrays, UV/IR detectors, etc.
- The major advantage of using COTS is that they are readily available in the market, are cheap and a developer can cut down his/her development time to a great extent. This in turn reduces the time to market your embedded systems.
- The TCP/IP plug-in module available from various manufactures like 'WIZnet', 'Freescale', 'Dynalog', etc. are very good examples of COTS product .
- This network plug-in module gives the TCP/IP connectivity to the system you are developing. There is no need to design this module yourself and write the firmware for the TCP/ IP protocol and data transfer.
- Everything will be readily supplied by the COTS manufacturer. What you need to do is identify the COTS for your system and give the plug-in option on your board according to the hardware.

- Plug-in connections given in the specifications of the COTS.

- Though multiple vendors supply COTS for thesame application, the major problem faced by the enduser is that there are no operational and manufacturing standards.

- A Commercial off-the-shelf (COTS) component manufactured by a vendor need not have hardware plug-in and firmware interface compatibility with one manufactured by a second - vendor for the same application.

- This restricts the end-user to stick to a particular vendor for particular COTS. This greatly affects the product design.

- The major drawback of using COTS components in embedded design is that the manufacturer of the COTS component may withdraw the product or discontinue the production of the COTS at any time if a rapid change in technology occurs, and this will adversely affect a commercial manufacturer of the embedded system which makes use of the specific COTS product.

3.8 MEMORY

- Memory is an important part of a processor/controller based embedded systems.

- Some of the processors/controllers contain built in memory and this memory is referred as on-chip memory.

- Others do not contain any memory inside the chip and requires external memory to be connected with the controller/processor to store the control algorithm. It is called off-chip memory.

- Also some working memory is required for holding data temporarily during certain operations.

- There are different types of memory used in embedded system applications:

[1] Program Storage Memory (ROM)

1. Masked ROM (MROM)
2. Programmable Read Only Memory (PROM)/ (OTP)
3. Erasable Programmable Read Only Memory (EPROM)
4. Electrically Erasable Programmable Read Only Memory (EEPROM)
5. FLASH

[2] Read-Write Memory/Random Access Memory (RAM)

1. Static RAM (SRAM)
2. Dynamic RAM (DRAM)
3. NVRAM

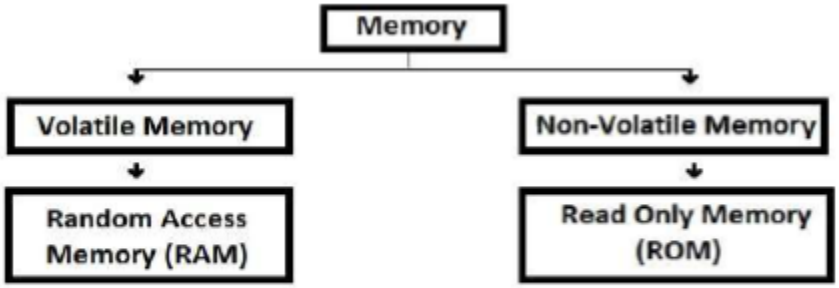


Fig: Types of Memory

A. Program Storage Memory (ROM)

The program memory or code storage memory of an embedded system stores the program instructions and it can be classified into different types as per the block diagram representation given in Figure.

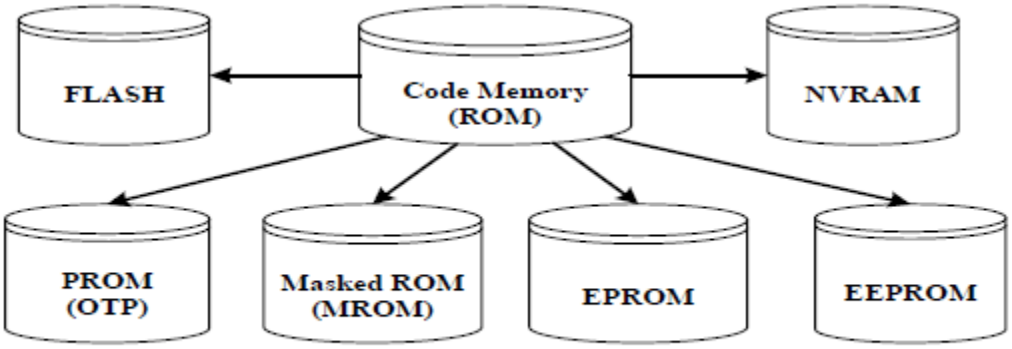


Fig: Classification of Program Memory (ROM)

The code memory retains its contents even after the power to it is turned off. It is generally known as non-volatile storage memory. Depending on the fabrication, erasing and programming techniques they are classified into the following types.

1. Masked ROM (MROM)

- Masked ROM is a one-time programmable device.
- Masked ROM makes use of the hardwired technology for storing data.
- The device is factory programmed by masking and metallization process at the time of production itself, according to the data provided by the end user.
- The primary advantage of MROM is low cost for high volume production.
- They are the least expensive type of solid state memory.
- Different mechanisms are used for the masking process of the ROM, like

1. Creation of an enhancement or depletion mode transistor through channel implant.
2. By creating the memory cell either using a standard transistor or a high threshold transistor.

- In the high threshold mode, the supply voltage required to turn ON the transistor is above the normal ROM IC operating voltage. This ensures that the transistor is always off and the memory cell stores always logic 0.

- Masked ROM is a good candidate for storing the embedded firmware for low cost embedded devices.

- Once the design is proven and the firmware requirements are tested and frozen, the binary data corresponding to it can be given to the MROM fabricator.

- The limitation with MROM based firmware storage is the inability to modify the device firmware against firmware upgrades. Since the MROM is permanent in bit storage, it is not possible to alter the bit information.

2. Programmable Read Only Memory (PROM) / (OTP)

- Unlike Masked ROM Memory, One Time Programmable Memory (OTP) or PROM is not pre-programmed by the manufacturer.

- The end user is responsible for programming these devices.

- This memory has nichrome or polysilicon wires arranged in a matrix. These wires can be functionally viewed as fuses.

- It is programmed by a PROM programmer which selectively burns the fuses according to the bit pattern to be stored.

- Fuses which are not blown/burned representlogic “1” whereas fuses which are blown/burned representa logic “0”.

- The default state is logic “1”.

- OTP is widely used for commercial production of embedded systems whose prototyped versions are proven and the code is finalized.

- It is a low cost solution for commercial production.

- OTPs cannot be reprogrammed.

3. Erasable Programmable Read Only Memory (EPROM)

- OTPs are not useful and worth for development purpose. During the development phase the code is subject to continuous changes and using an OTP each time to load the code is not economical.

- Erasable Programmable Read Only Memory (EPROM) gives the flexibility to re-program the same chip.

- EPROM stores the bit information by charging the floating gate of an FET.Bit information is stored by using an EPROM programmer, which applies high voltage to charge the floating gate.

- EPROM contains a quartz crystal window for erasing the stored information. If the window is exposed to ultraviolet rays for a fixed duration, the entire memory will be erased.

- Even though the EPROM chip is flexible in terms of re-programmability, it needs to be taken out of the circuit board and put in a UV eraser device for 20 to 30 minutes. So it is a tedious and time-consuming process.

4. Electrically Erasable Programmable Read Only Memory (EEPROM)

- As the name indicates, the information contained in the EEPROM memory can be altered by using electrical signals at the register/Byte level.

- They can be erased and reprogrammed in-circuit.

- These chips include a chip erase mode and in this mode they can be erased in a few milliseconds.

- It provides greater flexibility for system design. The only limitation is their capacity is limited when compared with the standard ROM (A few kilobytes).

5. FLASH

- FLASH is the latest ROM technology and is the most popular ROM technology used in today's embedded designs.
- FLASH memory is a variation of EEPROM technology. It combines the re-programmability of EEPROM and the high capacity of standard ROMs.
- FLASH memory is organized as sectors (blocks) or pages.
- FLASH memory stores information in an array of floating gate MOS- FET transistors.
- The erasing of memory can be done at sector level or page level without affecting the other sectors or pages.
- Each sector/page should be erased before re-programming. The typical erasable capacity' of FLASH is 1000 cycles.

B. Read-Write Memory/Random Access Memory (RAM)

- RAM is the data memory or working memory of the controller/processor.
- Controller/processor can read from it and write to it.
- RAM is volatile, meaning when the power is turned off, all the contents are destroyed.
- RAM is a direct access memory, meaning we can access the desired memory location directly without the need for traversing through the entire memory locations to reach the desired memory position.
- This is in contrast to the Sequential Access Memory (SAM), where the desired memory location is accessed by either traversing through the entire memory or through a 'seek' method.
- Magnetic tapes, CD ROMs, etc. are examples of sequential access memories.
- RAM generally falls into three categories: Static RAM (SRAM), dynamic RAM (DRAM) and non-volatile RAM (NVRAM).

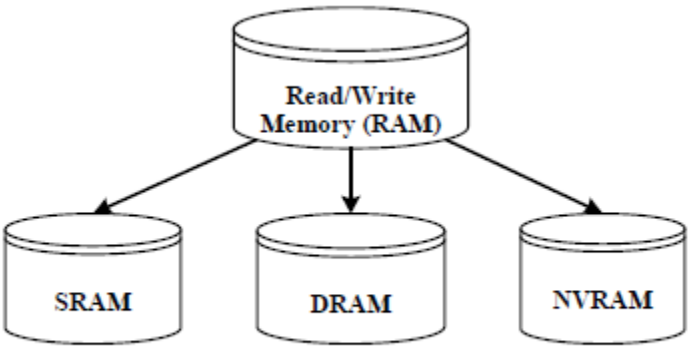


Fig: Types of Random Access Memory (ROM)

1. Static RAM (SRAM)

- Static RAM stores data in the form of voltage. They are made up of flip-flops.

- Static RAM is the fastest form of RAM available.

- In typical implementation, an SRAM cell (bit) is realized using six transistors (or MOSFETs). Four of the transistors are used for building the latch (flip-flop) part of the memory cell and two for controlling the access.

- SRAM is fast in operation due to its resistive networking and switching capabilities. In its simplest representation an SRAM cell can be visualized as shown in Figure.

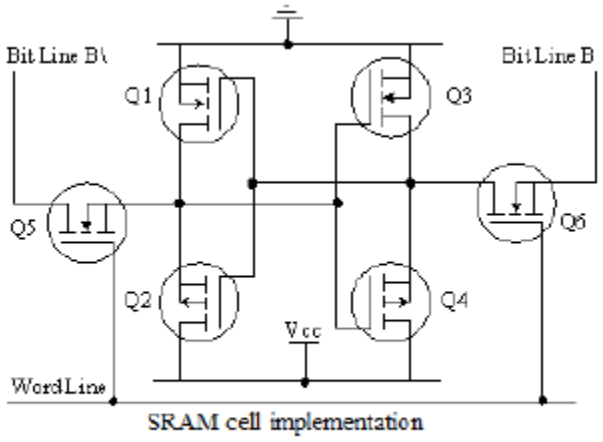


Fig: SRAM cell Implementation

• This implementation in its simpler form can be visualized as two-cross coupled inverters with read/ write control through transistors.

• The four transistors in the middle form the cross-coupled inverters. This can he visualized as shown in Figure.

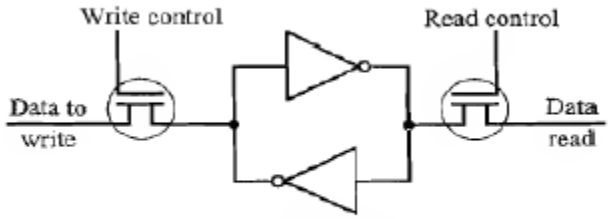


Fig: Visualization of SRAM

• From the SRAM implementation diagram, it is clear that access to the memory cell is controlled by the line Word Line, which controls the access transistors (MOSFETs) Q5 and Q6.

• The access transistors control the connection to bit lines B & B\ In order to write a value to the memory cell.

• Apply the desired value to the bit control lines (For writing 1, make B = 1 and B\ =0; For writing 0, make B = 0 and B\ =1) and assert the Word Line (Make Word line high).

• This operation latches the bit written in the flip-flop. For reading the content of the memory cell, assert both B and B\ bit lines to 1 and set the Word line to 1.

• The major limitations of SRAM are low capacity and high cost. Since a minimum of six transistors are required to build a single memory cell, imagine how many memory cells we can fabricate on a silicon wafer.

2. Dynamic RAM (DRAM)

• Dynamic RAM stores data in the form of charge. They are made up of MOS transistor gates.

• The advantages of DRAM are its high density and low cost compared to SRAM.

• The disadvantage is that since the information is stored as charge it gets leaked off with time and to prevent this they need to be refreshed periodically.

• Special circuits called DRAM controllers are used for the refreshing operation. The refresh operation is done periodically in milliseconds interval. Figure illustrates the typical implementation of a DRAM cell.

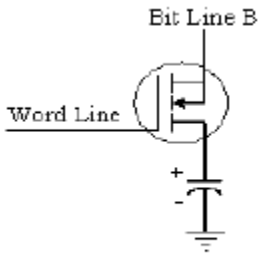


Fig:DRAM cell implementation

- The MOSFET acts as the gate for the incoming and outgoing data whereas the capacitor acts as the bit storage unit.

- Table given below summarizes the relative merits and demerits of SRAM and DRAM technology.

SRAM Cell	DRAM Cell
Made up of 6 CMOS transistors (MOSFET)	Made up of a MOSFET and a capacitor
Doesn't Require refreshing	Requires refreshing
Low capacity (Less dense)	High Capacity (Highly dense)
More expensive	Less Expensive
Fast in operation. Typical access time is 10ns	Slow in operation due to refresh requirements. Typical access time is 60ns. Write operation is faster than read operation.

3. NVRAM

- Non-volatile RAM is a random access memory with battery backup.

- It contains 5 static RAM based memory and a minute battery for providing supply to the memory in the absence of external power supply.

- The memory and battery are packed together in a single package. The life span of NVRAM is expected to be around 10 years.

- DS1644 from Maxim/Dallas is an example of 32KB i NVRAM.

C. Memory According to the Type of Interface

- The interface (connection) of memory with the processor/controller can be of various types.

- It may be a parallel or the interface may be a serial interface like I2C (Pronounced as I Square C. It is a 2 line serial interface) or it may be an SPI (Serial peripheral interface, 2+n line interface where n stands for the total number of SPI bus devices in the system). It can also be of a single wire interconnection.

- Serial interface is commonly used for data storage memory like EEPROM. The memory density of a serial memory is usually expressed in terms of kilobits, whereas that of a parallel interface memory is expressed in terms of kilobytes.

- Atmel Corporations AT24C512 is an example for serial memory with capacity 512 kilobits and 2-wire interface.

D. Memory Shadowing

- Generally the execution of a program or a configuration from a Read Only Memory (ROM) is very slow (120 to 200 ns) compared to the execution from a random access memory (40 to 70 ns).

- From the timing parameters it is obvious that RAM access is about three times as fast as ROM access.

- Shadowing of memory is a technique adopted to solve the execution speed problem in processor-based systems.

- In computer systems and video systems there will be a configuration holding ROM called Basic Input Output Configuration ROM or simply BIOS.

- In personal computer systems BIOS stores the hardware configuration information like the address assigned for various serial ports and other non-plug V play devices, etc. Usually it is read and the system is configured according to it during system boot up and it is time consuming.

- Now the manufactures included a RAM behind the logical layer of BIOS at its same address as a shadow to the BIOS and the first step that happens during the boot up is copying the BIOS to the shadowed RAM and write protecting the RAM then disabling the BIOS reading.

- Because RAM is volatile and it cannot hold the configuration data which is copied from the BIOS when the power supply is switched off. Only a ROM can hold it permanently. But for high system performance it should be accessed from a RAM instead of accessing from a ROM.

E. Memory Selection for Embedded Systems

- Embedded systems require a program memory for holding the control algorithm or embedded OS and the applications designed to run on top of it.

- Data memory for holding variables and temporary data during task execution.

- Memory for holding nonvolatile data (like configuration data, look up table etc) which are modifiable by the application (Unlike program memory, which is non-volatile as well unalterable by the end user).

- The memory requirement for an embedded system in terms of RAM and ROM (EEPROM/FLASH/NVRAM) is solely dependent on the type of the embedded system and the applications for which it is designed.

- There is no hard and fast rule for calculating the memory requirements. Lot of factors need to be considered when selecting the type and size of memory for embedded system.

- For example, if the embedded system is designed using SoC or a microcontroller with on-chip RAM and ROM (FLASH/EEPROM),depending on the application need the on-chip memory may be sufficient for designing the total system.

- Let's consider a simple electronic toy design as an example. As the complexity of requirements are less and data memory requirement are minimal, we can think of a microcontroller with a few bytes of internal RAM, a few bytes or kilobytes (depending on the number of tasks and the complexity of tasks) of FLASH memory and a few bytes of EEPROM (if required) for designing the system. Hence there is no need for external memory at all. A PIC microcontroller device which satisfies the I/O and memory requirements can be used in this case.

- If the embedded design is based on an RTOS, the RTOS requires certain amount of RAM for its execution and ROM for storing the RTOS image. Normally the binary code for RTOS kernel containing all the services is stored in a non-volatile memory (Like FLASH) as either compressed or non-compressed data.

- During boot-up of the device,the RTOS files are copied from the program storage memory, decompressed if required and then loaded to the RAM for execution. The supplier of the RTOS usually gives a rough estimate on the run time RAM requirements and program memory' requirements for the RTOS.

- On top of this add the RAM requirements for executing user tasks and ROM for storing user applications. On a safer side, always add a buffer value to the total estimated RAM and ROM size requirements.

- A smart phone device with Windows mobile operating system is a typical example for embedded device with OS.

- There are two parameters for representing a memory. The first one is the size of the memory chip (Memory density expressed in terms of number of memory bytes per chip). There is no option to get a memory chip with the exact required number of bytes.

- Memory chips come in standard sizes like 512bytes, 1024bytes (1 kilobyte), 2048bytes (2 kilobytes), 4Kb,f 8Kb, 16Kb, 32Kb, 64Kb, 128Kb, 256Kb, 512Kb, 1024Kb (1Mbytes), etc.

- The second parameter that needs to be considered in selecting a memory is the word size of the memory. The word size refers to the number of memory bits that can be read/write together at a time. 4, 8, 12, 16, 24, 32, etc. are the word sizes supported by memory chips.

- Ensure that the word size supported by the memory chip matches with the data bus width of the processor/controller.

- FLASH memory is the popular choice for ROM (program storage memory) in embedded applications. It is a powerful and cost-effective solid-state storage technology for mobile electronics devices and other consumer applications.

- FLASH memory comes in two major variants, namely, NAND and NOR FLASH. NAND FLASH is a high-density low cost non-volatile storage memory.' On the other hand, NOR FLASH is less dense and slightly expensive. But it supports the Execute in Place (XIP) technique for program execution.

- The XIP technology allows the execution of code memory from ROM itself without the need for copying it to the RAM as in the case of conventional execution method

- NAND FLASH doesn’t support XIP and if NAND FLASH is used for storing program code, a DRAM can be used for copying and executing the program code.

- NOR FLASH supports XIP and it can be used as the memory for bootloader or for even storing the complete program code.

- The EEPROM data storage memory is available as either serial interface or parallel interface chip.

- If the processor/controller of the device supports serial interface and the amount of data to write and read to and from the device is less, it is better to have a serial EEPROM chip.

• The serial EEPROM saves the address space of the total system. The memory capacity of the serial EEPROM is usually expressed inbits or kilobits. 512 bits, lKbits, 2Kbits, 4Kbits, etc. are examples for serial EEPROM memory representation.

• For embedded systems with low power requirements like portable devices, choose low power memory devices.

• Certain embedded devices may be targeted for operating at extreme environmental conditions like high temperature, high humid area, etc. Select an industrial grade memory chip in place of the commercial grade chip for such devices.

3.9 SENSORS AND ACTUATORS.

A. Sensors

A sensor is a transducer device that converts energy from one form to another form for any measurement or control purpose.

Eg: Hall Effect Sensor which measures the distance between the cushion and magnet in the Smart Running shoes from adidas.

B. Actuators

A form of transducer device (mechanical or electrical) which converts signals to corresponding physical action (motion). Actuator acts as an output device.

Eg: Micro motor actuator which adjusts the position of the cushioning element in the Smart Running shoes from adidas.

C. The I/O Subsystem

• The I/O subsystem of the embedded system facilitates the interaction of the embedded system with the external world.

• The interaction happens through the sensors and actuators connected to the input and output ports respectively of the embedded system.

• The sensors may not be directly interfaced to the input ports, instead they may be interfaced through signal conditioning and translating systems like ADC, optocouplers, etc

3.10 Light Emitting Diode (LED)

• Light Emitting Diode (LED) is an important output device for visual indication in any embedded system.

• LED can be used as an indicator for the status of various signals or situations.

• Examples: indicating the presence of power conditions like 'Device ON', 'Battery low' or 'Charging of battery' for a battery operated handheld embedded devices.

• Light Emitting Diode is a p-n junction diode and it contains an anode and a cathode.

• For proper functioning of the LED, the anode of it should be connected to +ve terminal of the supply voltage and cathode to the -ve terminal of supply voltage.

• The current flowing through the LED must be limited to a value below the maximum current that it can conduct. A resister is used in series between the power supply and the LED to limit the current through the LED. The ideal LED interfacing circuit is shown in Figure.

• LEDs can be interfaced to the port pin of a processor/controller in two ways.

• In the first method, the anode is directly connected to the port pin and the port pin drives the LED. In this approach the port pin 'sources' current to the LED when the port pin is at logic High (Logic '1').

• In the second method, the cathode of the LED is connected to the port pin of the processor/controller and the anode to the supply voltage through a current limiting resistor.

The LED is turned on when the port pin is at logic Low (Logic '0'). Here the port pin 'sinks' current.

• If the LED is directly connected to the port pin, depending on the maximum current that a port pin can source, the brightness of LED may not be to the required level. In the second approach, the current is directly sourced by the power supply and the port pin acts as the sink for current. Here we will get the required brightness for the LED.

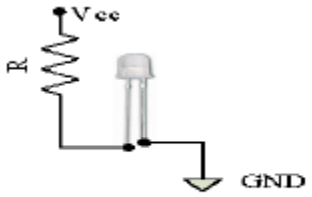


Fig: LED Interfacing

3.11 7-Segment LED Display

- The 7-segment LED display is an output device for displaying alpha numeric characters.

- It contains 8 light-emitting diode (LED) segments arranged in a special form. Out of the 8 LED segments, 7 are used for displaying alpha numeric characters and 1 is used for representing 'decimal point' in decimal number display. As shown in the figure.

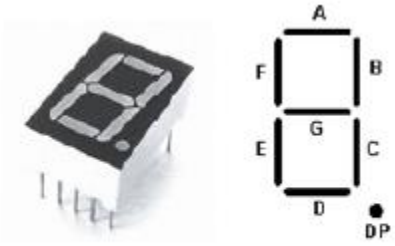


Fig: 7-segment LED display

•The LED segments are named A to G and the decimal point LED segment is named as DP.

•The LED segments A to G and DP should be lit accordingly to display numbers and characters.

For example, for displaying the number 4, the segments F, G, B and C are lit.

- All these 8 LED segments need to be connected to one port of the processor/controller for displaying alpha numeric digits.

- The 7-segment LED displays are available in two different configurations, namely; Common Anode and Common Cathode.

- In the common anode configuration, the anodes of the 8 segments are connected commonly whereas in the common cathode configuration, the 8 LED segments share a common cathode line. Figure illustrates the Common Anode and Cathode configurations.

- Based on the configuration of the 7-segment LED unit, the LED segment's anode or cathode is connected to the port of the processor/controller in the order 'A' segment to the least significant port pin and DP segment to the most significant port pin.

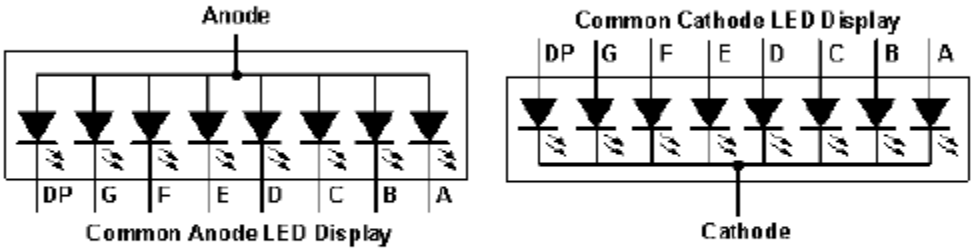


Fig: Common anode and cathode configurations of a 7-segment LED Display

- The current flow through each of the LED segments should be limited to the maximum value supported by the LED display unit.
- The typical value for the current falls within the range of 20mA.
- The current through each segment can be limited by connecting a current limiting resistor to the anode or cathode of each segment.
- The value for the current limiting resistors can be calculated using the current value from the electrical parameter listing of the LED display.
- For common cathode configurations, the anode of each LED segment is connected to the port pins of the port to which the display is interfaced. The anode of the common anode LED display is connected to the 5V supply voltage through a current limiting resistor and the cathode of each LED segment is connected to the respective port pin lines.
- For an LED segment to lit in the Common anode LED configuration, the port pin to which the cathode of the LED segment is connected should be set at logic 0.
- 7-segment LED display is a popular choice for low cost embedded applications like, Public telephone call monitoring devices, point of sale terminals, etc.

3.12 Stepper Motor

• A stepper motor is an electro-mechanical device which generates discrete displacement (motion) in response, to dc electrical signals.

• It differs from the normal dc motor in its operation. The dc motor produces continuous rotation on applying dc voltage whereas a stepper motor produces discrete rotation in response to the dc voltage applied to it.

• Stepper motors are widely used in industrial embedded applications, consumer electronic products and robotics control systems.

• The paper feed mechanism of a printer/fax makes use of stepper motors for its functioning.

• Based on the coil winding arrangements, a two-phase stepper motor is classified into two. They are:

1. **Unipolar**
2. **Bipolar**

Unipolar

• A unipolar stepper motor contains two windings per phase.

• The direction of rotation (clockwise or anticlockwise) of a stepper motor is controlled by changing the direction of current flow.

• Current in one direction flows through one coil and in the opposite direction flows through the other coil. It is easy to shift the direction of rotation by just switching the terminals to which the coils are connected. Figure illustrates the working of a two- phase unipolar stepper motor.

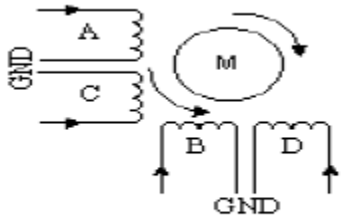


Fig: 2-Phase unipolar stepper motor

• The coils are represented as A, B, C and D. Coils A and C carry current in opposite directions for phase 1 (only one of them will be carrying current at a time). Similarly, B and D carry current in opposite directions for phase 2 (only one of them will be carrying current at a time).

Bipolar

• A bipolar stepper motor contains single winding per phase.

• For reversing the motor rotation the current flow through the windings is reversed dynamically.

• It requires complex circuitry for current flow reversal. The stator winding details for a two phase unipolar stepper motor is shown in Figure.

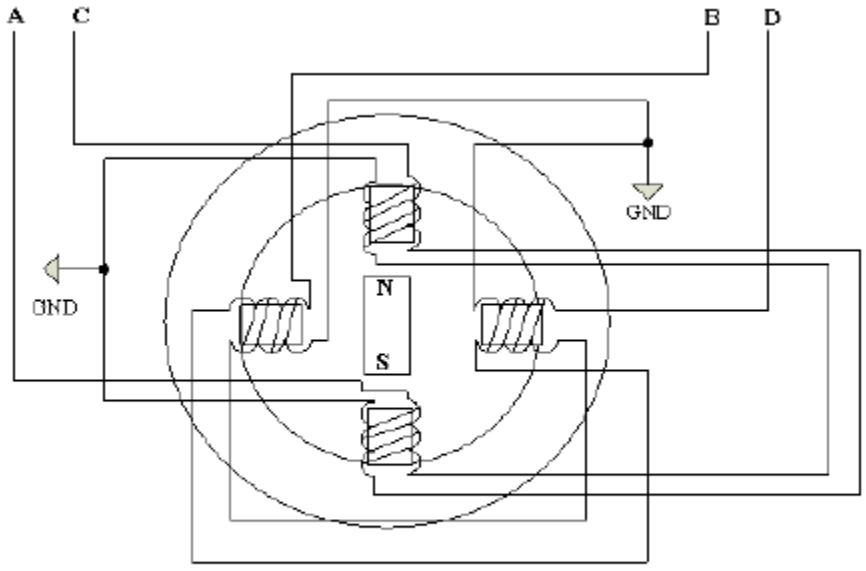


Fig:Stator Winding details for a 2 Phase unipolar stepper motor

The stepping of stepper motor can be implemented in different ways by changing the sequence of activation of the stator windings. The different stepping modes supported by stepper motor are explained below.

Full Step

In the full step mode both the phases are energized simultaneously. The coils A, B, C and D are energized in the following order:

Step	Coil A	Coil B	Coil C	Coil D
1	H	H	L	L
2	L	H	H	L
3	L	L	H	H
4	H	L	L	H

It should be noted that out of the two windings, only one winding of a phase is energized at a time.

Wave Step

In the wave step mode only one phase is energized at a time and each coils of the phase is energized alternatively. The coils A, B, C and D are energized in the following order:

Step	Coil A	Coil B	Coil C	Coil D
1	H	L	L	L
2	L	H	L	L
3	L	L	H	L
4	L	L	L	H

Half Step

It uses the combination of wave and full step. It has the highest torque and stability. The coil energizing sequence for half step is given below.

Step	Coil A	Coil B	Coil C	Coil D
1	H	L	L	L
2	H	H	L	L
3	L	H	L	L
4	L	H	H	L
5	L	L	H	L
6	L	L	H	H
7	L	L	L	H
8	H	L	L	H

- The rotation of the stepper motor can be reversed by reversing the order in which the coil is energized.
- Two-phase unipolar stepper motors are the popular choice for embedded applications.

• The current requirement for stepper motor is little high and hence the port pins of a microcontroller/processor may' not be able to drive them directly. Also the supply voltage required to operate stepper motor varies normally in the range 5V to 24 V.

• Depending on the current and voltage requirements, special driving circuits are required to interface the stepper motor with microcontroller/processors.

• Commercial off- the-shelf stepper motor driver ICs are available in the market and they can be directly interfaced to the microcontroller port. ULN2803 is an octal peripheral driver array for driving a 5V stepper motor.

• Simple driving circuit can also be built using transistors.

• The following circuit diagram illustrates the interfacing of a stepper motor through a driver circuit connected to the port pins of a microcontroller/processor

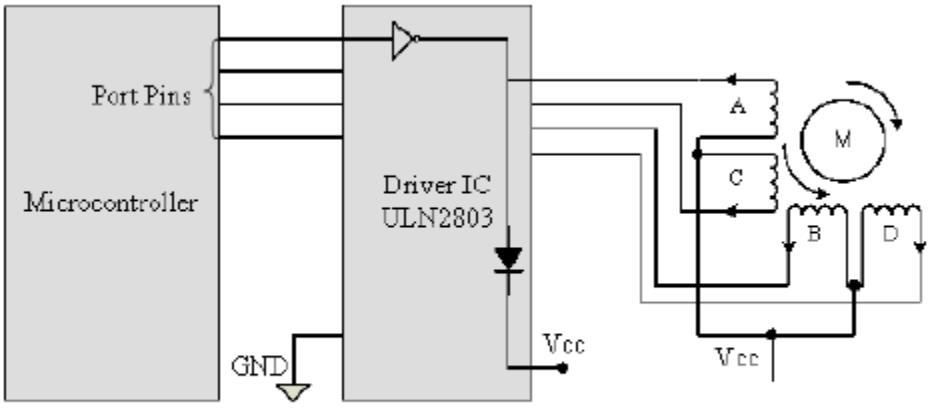


Fig: Interfacing of stepper motor through driver circuit

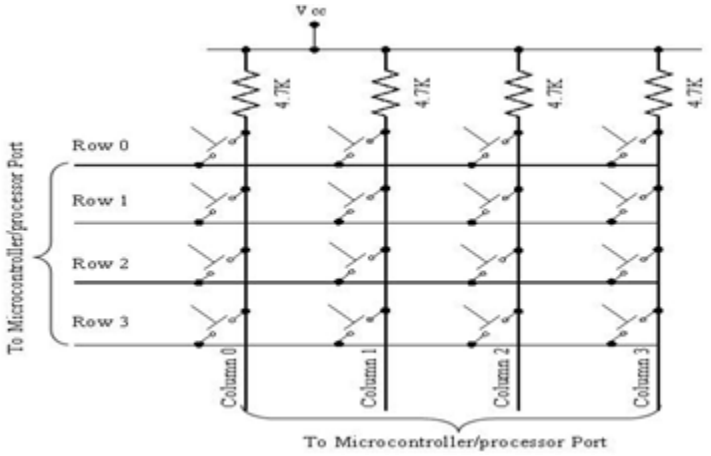
3.13 Keyboard

• Keyboard is an input device for user interfacing.

• If the number of keys required is very limited, push button switches-can be used and they can be directly interfaced to the port pins for reading.

• However, there may be situations demanding a large number of keys for user input (e.g. PDA device with alpha-numeric keypad for user data entry). In such situations it may not be possible to interface each keys to a port pin due to the limitation in the number of general purpose port pins available for the processor/controller in use and moreover it is wastage of port pins.

• Matrix keyboard is an optimum solution for handling large key requirements. It greatly reduces the number of interface connections.



- For example, for interfacing 16 keys, in the direct interfacing technique 16 port pins are required, whereas in the matrix keyboard only 8 lines are required. The 16 keys are arranged in a 4 column x 4 Row matrix. Figure illustrates the connection of keys in a matrix keyboard.

- In a matrix keyboard, the keys are arranged in matrix fashion (i.e. they are connected in a row and column style).

- For detecting a key press, the keyboard uses the scanning technique, where each row of the matrix is pulled low and the columns are read.

- After reading the status of each columns corresponding to a row, the row is pulled high and the next row is pulled low and the status of the columns are read. This process is repeated until the scanning for all rows are completed.

- When a row is pulled low and if a key connected to the row is pressed, reading the column to which the key is connected will give logic 0.

- Since keys are mechanical devices, there is a possibility for de-bounce issues, which may give multiple key press effect for a single key press. To prevent this, a proper key de-bouncing technique should be applied.

- Hardware key de-bouncer circuits and software key de-bounce techniques are the key de¬ bouncing techniques available.

- The software key de-bouncing technique doesn't require any additional hardware and is easy to implement.

- In the software de-bouncing technique, on detecting a key-press, the key is read again after a de-bounce delay. If the key press is a genuine one, the state of the key will remain as 'pressed' on the second read also.

• Pull-up resistors are connected to the column lines to limit the current that flows to the Row line on a key press.

3.14 Push Button Switch

• It is an input device.

• Push button switch comes in two configurations, namely 'Push to Make' & 'Push to Break'.

• In the 'Push to Make' configuration, the switch is normally in the open state and it makes a circuit contact when it is pushed or pressed.

• In the 'Push to Break' configuration, the switch is normally in the closed state and it breaks the circuit contact when it is pushed or pressed.

• The push button stays in the 'closed' (For Push to Make type) or 'opens' (For Push to Break type) state as long as it is kept in the pushed state and it breaks/makes the circuit connection when it is released.

• Push button is used for generating a momentary pulse.

• In embedded application push button is generally used as reset and start switch and pulse generator.

• The Push button is normally connected to the port pin of the host processor/controller. Depending on the way in which the push button interfaced to the controller, it can generate either a 'HIGH' pulse or a 'LOW' pulse.

• Figure illustrates how the push button can be used for generating 'LOW' and 'HIGH' pulses.

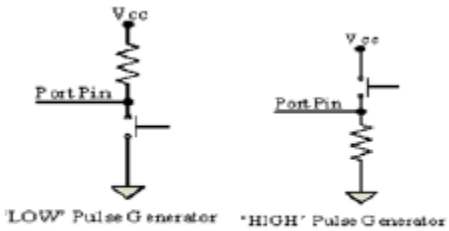


Fig: Push button switch configurations

3.15 COMMUNICATION INTERFACE

• Communication interface is essential for communicating with various subsystems of the embedded system and with the external world.

• For an embedded product, the communication interface can be viewed in two different perspectives, namely; Device/board level communication interface (Onboard Communication Interface) Product level communication, interface (External Communication Interface).

• Embedded product is a combination of different types of components (chips/devices) arranged on a printed circuit board (PCB).

• The communication channel which interconnects the various components within an embedded product is referred as device/board level communication interface (onboard communication interface).

Examples: Serial interfaces like I2C, SPI, UART, 1-Wire, etc and parallel bus interface.

• Some embedded systems are self-contained units and they don't require any interaction and data transfer with other sub-systems or external world.

• Certain embedded systems may be a part of a large distributed system and they require interaction and data transfer between various devices and sub-modules.

• The 'Product level communication interface' (External Communication Interface.) is responsible for data transfer between the embedded system and other devices or modules.

• The external communication interface can be either a wired media or a wireless media and it can be a serial or a parallel interface.

Ex: Infrared(IR), Bluetooth (BT), Wireless LAN (Wi-Fi), Radio Frequency waves (RF), GPRS, etc. for wireless communication interface. RS-232C/RS-422/RS-485, USB, Ethernet IEEE 1394 port, Parallel port, CF-II interface, SDIO, PCMCIA, etc, for wired interfaces.

• It is not mandatory that an embedded system should contain an external communication interface. Mobile communication equipment is an example for embedded system with external communication interface.

A. Onboard Communication Interfaces

Onboard Communication Interface refers to the different communication channels/buses for interconnecting the various integrated circuits and other peripherals within the embedded system. The following section gives an overview of the various interfaces for onboard communication.

1. Inter Integrated Circuit (I2C) Bus

• Inter Integrated Circuit Bus (I2C - Pronounced 'I square C') is a synchronous bi-directional half duplex (one-directional communication at a given point of time) two wire serial interface bus.

• The concept of I2C bus was developed by 'Philips Semiconductors' in the early 1980's. The original intention of I2C was to provide an easy way of connection between a microprocessor/microcontroller system and the peripheral chips in Television sets.

• The I2C bus is comprised of two bus lines, namely; **Serial Clock – SCL** and **Serial Data – SDA**. SCL line is responsible for generating synchronization clock pulses and SDA is responsible for transmitting the serial data across devices.

• I2C bus is a shared bus system to which many number of I2C devices can be connected. Devices connected to the I2C bus can act as either 'Master' device or 'Slave' device

• The 'Master' device is responsible for controlling the communication by initiating/terminating data transfer, sending data and generating necessary synchronization clock pulses.

• 'Slave' devices wait for the commands from the master and respond upon receiving the commands.

• 'Master' and 'Slave' devices can act as either transmitter or receiver.

• Regardless whether a master is acting as transmitter or receiver, the synchronization clock signal is generated by the 'Master' device only.

• I2C supports multi masters on the same bus.

• The following bus interface diagram shown in Figure illustrates the connection of master and slave devices on the I2C bus.

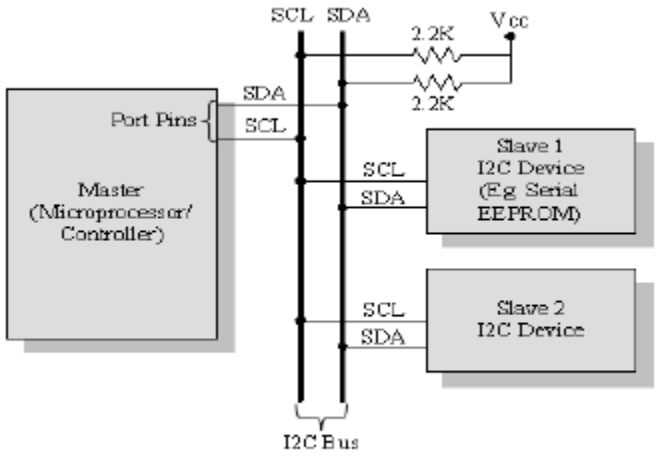


Fig: I2C Bus Interfacing.

- The I2C bus interface is built around an input buffer and an open drain or collector transistor.

- When the bus is in the idle state, the open drain/collector transistor will be in the floating state and the output lines (SDA and SCL) switch to the 'High Impedance' state.

- For proper operation of the bus, both the bus lines should be pulled to the supply voltage (+5V for TTL family and +3.3V for CMOS family devices) using pull-up resistors.

- The typical value of resistors used in pull-up is 2.2K. With pull-up resistors, the output lines of the bus in the idle state will be 'HIGH'.

- The address of a I2C device is assigned by hardwiring the address lines of the device to the desired logic level. The address to various I2C devices in an embedded device is assigned and hardwired at the time of designing the embedded hardware.

- The sequence of operation for communicating with an I2C slave device is:

1. Master device pulls the clock line (SCL) of the bus to 'HIGH'
2. Master device pulls the data line (SDA) 'LOW', when the SCL line is at logic 'HIGH' (This is the 'Start' condition for data transfer)
3. Master sends the address (7 bit or 10 bit wide) of the 'Slave' device to which it wants to communicate, over the SDA line. Clock pulses are generated at the SCL line for synchronizing the bit reception by the slave device. The MSB of the data is always transmitted first. The data in the bus is valid during the 'HIGH' period of the clock signal

4. Master sends the Read or Write bit (Bit value = 1 Read Operation; Bit value = 0 Write Operation) according to the requirement

5. Master waits for the acknowledgement bit from the slave device whose address is sent on the bus along with the Read/Write operation command. Slave devices connected to the bus compares the address received with the address assigned to them

6. The Slave device with the address requested by the master device responds by sending an acknowledge bit (Bit value =1) over the SDA line

7. Upon receiving the acknowledge bit, master sends the 8bit data to the slave device over

SDA line, if the requested operation is 'Write to device'. If the requested operation is 'Read from device', the slave device sends data to the master over the SDA line

8. Master waits for the acknowledgement bit from the device upon byte transfer complete for a write operation and sends an acknowledge bit to the slave device for a read operation

9. Master terminates the transfer by pulling the SDA line 'HIGH' when the clock line SCL is at logic 'HIGH' (Indicating the 'STOP' condition).

2. Serial Peripheral Interface (SPI) Bus

• The Serial Peripheral Interface Bus (SPI) is a synchronous bi-directional full duplex four-wire serial interface bus.

• The concept of SPI was introduced by Motorola.

• SPI is a single master multi-slave system.

• It is possible to have a system where more than one SPI device can be master, provided the condition only one master device is active at any given point of time, is satisfied.

• SPI requires four signal lines for communication. They are:

Master Out Slave In (MOSI): Signal line carrying the data from master to slave device. It is also known as Slave Input/Slave Data In (SI/SDI).

Master In Slave Out (MISO): Signal line carrying the data from slave to master device. It is also known as Slave Output (SO/SDO).

Serial Clock (SCLK): Signal line carrying the clock signals.

Slave Select (SS): Signal line for slave device select. It is an active low signal.

- The bus interface diagram shown in Figure illustrates the connection of master and slave devices on the SPI bus.

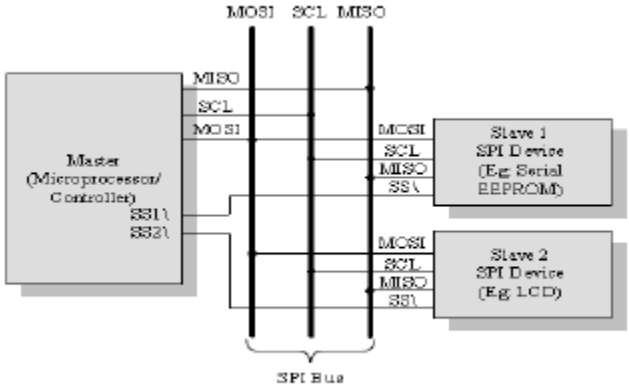


Fig:SPI bus interfacing

- The master device is responsible for generating the clock signal.
- It selects the required slave device by asserting the corresponding slave device's slave select signal 'LOW'. The data out line (MISO) of all the slave devices when not selected floats at high impedance state.
- The serial data transmission through SPI bus is fully configurable.
- SPI devices contain a certain set of registers for holding these configurations.
- The serial peripheral control register holds the various configuration parameters like master/slave selection for the device, baudrate selection for communication, clock signal control, etc.
- The status register holds the status of various conditions for transmission and reception.
- SPI works on the principle of 'Shift Register'.
- The master and slave devices contain a special shift register for the data to transmit or receive.
- The size of the shift register is device dependent. Normally it is a multiple of 8.

• During transmission from the master to slave, the data in the master's shift register is shifted out to the MOSI pin and it enters the shift register of the slave device through the MOSI pin of the slave device. At the same time the shifted out data bit from the slave device's shift register entersthe shift register of the master device through MISO pin.

• In summary, the shift registers of 'master' and 'slave' devices form a circular buffer. For some devices, the decision on whether the LS/MS bit of data needs to be sent out first is configurable through configuration.

• When compared to I2C, SPI bus is most suitable for applications requiring transfer of data in 'streams'. The only limitation is SPI doesn't support an acknowledgement mechanism.

3. Universal Asynchronous Receiver Transmitter (UART)

• Universal Asynchronous Receiver Transmitter (UART) based data transmission is an asynchronous form of serial data transmission.

• UART based serial data transmission doesn't require a clock signal to synchronize the transmitting end and receiving end for transmission.

• The serial communication settings (Baud rate, No. of bits per byte, parity, No. of start bits and stop bit and flow control) for both transmitter and receiver should be set as identical.

• The start and stop of communication is indicated through inserting special bits in the data stream.

• While sending a byte of data, a start bit is added first and a stop bit is added at the end of the bit stream. The least significant bit of the data byte follows the start bit.

• The 'Start' bit informs the receiver that a data byte is about to arrive. The receiver device starts polling it's 'receive line' as per the baudrate settings.

• If the baudrate is 'A' bits per second, the time slot available for one bit is l/A seconds. The receiver unit polls the receiver line at exactly half of the time slot available for the bit.

• If parity is enabled for communication, the UART of the transmitting device adds a parity bit. (Bit value is 1 for odd number of 1's in the transmitted bit stream and 0 for even number of 1's).

• The UART of the receiving device calculates the parity of the bits received and compares it with the received parity bit for error checking.

• The UART of the receiving device discards the 'Start', 'Stop' and 'Parity' bit from the received bit stream and converts the received serial bit data to a word.

• For proper communication, the 'Transmit line' of the sending device should be connected to the 'Receive line' of the receiving device. Figure illustrates the same.

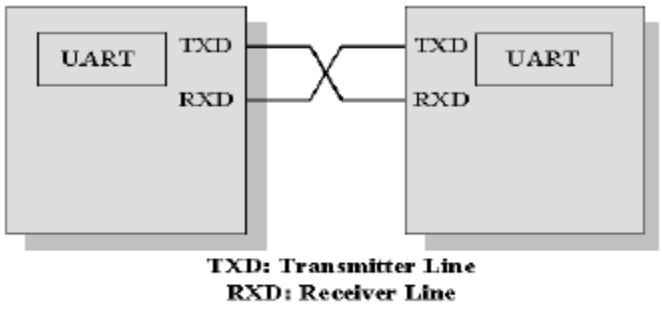


Fig: UART Interfacing

• In addition to the serial data transmission function, UART provides hardware handshaking signal support for controlling the serial data flow.

• UART chips are available from different semiconductor manufacturers. National

Semiconductor's 8250 UART chip is considered as the standard setting UART. It was used in the original IBM PC.

• Nowadays most of the microprocessors/controllers are available with integrated UART functionality and they provide built-in instruction support for serial data transmission and reception.

4. 1-Wire Interface

• 1-wire interface is an asynchronous half-duplex communication protocol developed by Maxim Dallas Semiconductor.

• It is also known as Dallas 1-Wire® protocol. It makes use of only a single signal line (wire) called DQ for communication and follows the master-slave communication model.

• One of the key features of 1-wire bus is that it allows power to be sent along the signal wire as well. Thel2C slave devices incorporate internal capacitor (typically of the order of 800 pF) to power the device from the signal line.

• The 1-wire interface supports a single master and one or more slave devices on the bus. The bus interface diagram shown in Figure illustrates the connection of master and slave devices on the 1-wire bus.

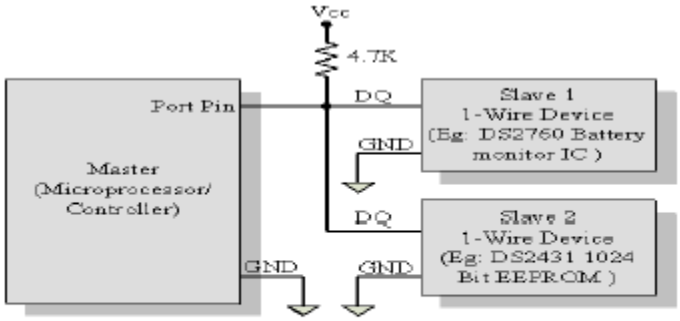


Fig:1-Wire Interface bus

• Every 1-wire device contains a globally unique 64bit identification number stored within it. This unique identification number can be used for addressing individual devices present on the bus in case there are multiple slave devices connected to the 1 -wire bus.

• The identifier has three parts: an 8bit family code, a 48bit serial number and an 8bit CRC computed from the first 56 bits.

• The sequence of operation for communicating with a 1-wire slave device is listed below.

1. Master device sends a ‘Reset’ pulse on the 1-Wire bus.
2. Slave device(s) present on the bus respond with a ‘Presence’ pulse.
3. Master device sends a ROM Command (Net Address Command followed by the 64 bit address of the device). This addresses the slave device(s) to which it wants to initiate a communication
4. Master device sends a read/write function command to read/write the internal memory or register of the slave device.
5. Master initiates a Read data /Write data from the device or to the device

- All communication over the 1-Wire bus is master initiated
- The communication over the 1-Wire bus is divided into timeslots of 60 microseconds
- The 'Reset' pulse occupies 8 time slots. For starting a communication, the master asserts the reset pulse by pulling the 1-Wire bus 'LOW' for at least 8 time slots (480µs)
- If a 'Slave' device is present on the bus and is ready for communication it should respond to the master with a 'Presence' pulse, within 60µs of the release of the 'Reset' pulse by the master
- The slave device(s) responds with a 'Presence' pulse by pulling the 1-Wire bus 'LOW' for a minimum of 1 time slot (60µs)
- For writing a bit value of 1 on the 1-Wire bus, the bus master pulls the bus for 1 to 15µs and then releases the bus for the rest of the time slot
- A bit value of '0' is written on the bus by master pulling the bus for a minimum of 1 time slot (60µs) and a maximum of 2 time slots (120µs)
- To Read a bit from the slave device, the master pulls the bus 'LOW' for 1 to 15µs
- If the slave wants to send a bit value '1' in response to the read request from the slave, it simply releases the bus for the rest of the time slot
- If the slave wants to send a bit value '0', it pulls the bus 'LOW' for the rest of the time slot.

5. Parallel Interface

- The on-board parallel interface is normally used for communicating with peripheral devices which are memory mapped to the host of the system.
- The host processor/controller of the embedded system contains a parallel bus and the device which supports parallel bus can directly connect to this bus system.
- The communication through the parallel bus is controlled by the control sig¬ nal interface between the device and the host.
- The 'Control Signals' for communication includes 'Read/ Write' signal and device select signal.
- The device normally contains a device select line and the device becomes active only when this line is asserted by the host processor.

• The direction of data transfer (Host to Device or Device to Host) can be controlled through the control signal lines for 'Read' and 'Write'. Only the host processor has control over the 'Read' and 'Write' control signals.

• The device is normally memory mapped to the host processor and a range of address is assigned to it. An address decoder circuit is used for generating the chip select signal for the device.

• When the address selected by the processor is within the range assigned for the device, the decoder circuit activates the chip select line and thereby the device becomes active. The processor then can read or write from or to the device by asserting the corresponding control line (RD\ and WR\ respectively).

• Strict timing characteristics are followed for parallel communication.As mentioned earlier, parallel communication is host processor initiated.

• If a device wants to initiate the communication, it can inform the same to the processor through interrupts. For this, the interrupt line of the device is connected to the interrupt line of the processor and the corresponding interrupt is enabled in the host processor.

• The width of the parallel interface is determined by the data bus width of the host processor. It can be 4bit, 8bit, 16bit, 32bit or 64bit etc.

• The bus width supported by the device should be same as that of the host processor. The bus interface diagram shown in Figure illustrates the interfacing of devices through parallel interface.

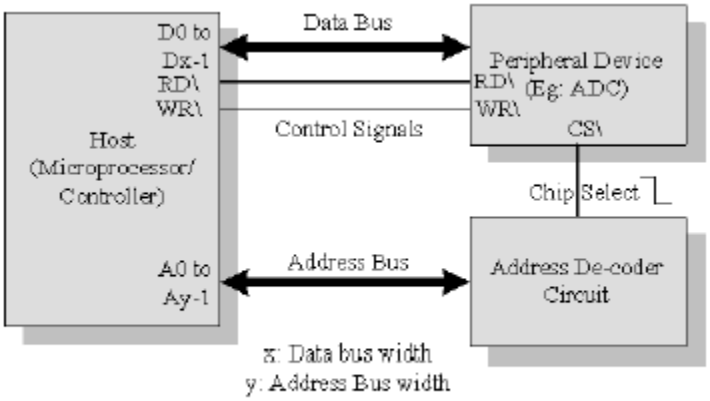


Fig: Parallel Interface bus

B. External Communication Interfaces

The External Communication Interface refers to the different communication channels/buses used by the embedded system to communicate with the external world. The following section gives an overview of the various interfaces for external communication.

1. RS-232 C & RS-485

- RS-232 C (Recommended Standard number 232, revision C from the Electronic Industry Association) is a legacy, full duplex, wired, asynchronous serial communication interface
- RS-232 extends the UART communication signals for external data communication.
- UART uses the standard TTL/CMOS logic (Logic 'High' corresponds to bit value 1 and Logic 'LOW' corresponds to bit value 0) for bit transmission whereas RS232 use the EIA standard for bit transmission. As per EIA standard, a logic '0' is represented with voltage between +3 and +25V and a logic '1' is represented with voltage between -3 and -25V.
- In EIA standard, logic '0' is known as 'Space' and logic '1' as 'Mark'.
- The RS232 interface define various handshaking and control signals for communication apart from the 'Transmit' and 'Receive' signal lines for data communication. RS-232 supports two different types of connectors, namely; DB-9: 9-Pin connector and DB-25: 25-Pin connector

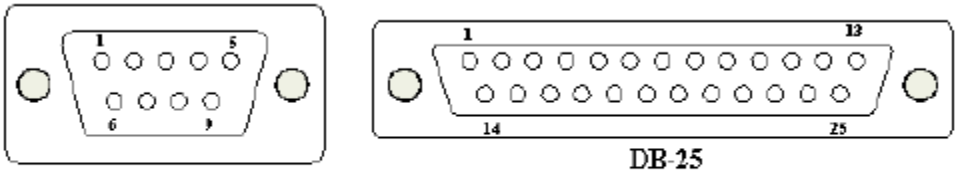


Fig:DB-9 and DB-25 RS 232 connector interface

- The pin details for the two connectors are explained in the following table:

Pin Name	Pin No: (For DB-9 Connector)	Description
TXD	3	Transmit Pin. Used for Transmitting Serial Data
RXD	2	Receive Pin. Used for Receiving serial Data
RTS	7	Request to send.
CTS	8	Clear To Send
DSR	6	Data Set ready
GND	5	Signal Ground
DCD	1	Data Carrier Detect
DTR	4	Data Terminal Ready
RI	9	Ring Indicator

- RS-232 is a point-to-point communication interface and the devices involved in RS-232 communication are called 'Data Terminal Equipment (DTE)' and 'Data Communication Equipment (DCE)'.

- If no data flow control is required, only TXD and RXD signal lines and ground line (GND) are required for data transmission and reception. The RXD pin of DCE should be connected to the TXD pin of DTE and vice versa for proper data transmission.

- If hardware data flow control is required for serial transmission, various control signal lines of the RS-232 connection are used appropriately. The control signals are implemented mainly for modem communication and some of them may be irrelevant for other type of devices.

- The Request To Send (RTS) and Clear To Send (CTS) signals co-ordinate the communication between DTE and DCE. Whenever the DTE has a data to send, it activates the RTS line and if the DCE is ready to accept the data, it activates the CTS line.

- The Data Terminal Ready (DTR) signal is activated by DTE when it is ready to accept data. The Data Set Ready (DSR) is activated by DCE when it is ready for establishing a communication link. DTR should be in the activated state before the activation of DSR.

- The Data Carrier Detect (DCD) is used by the DCE to indicate the DTE that a good signal is being received.

- Ring Indicator (RI) is a modem specific signal line for indicating an incoming call on the telephone line.

- As per the EIA standard RS-232 C supports baudrates up to 20Kbps (Upper limit 19.2Kbps) The commonly used baudrates by devices are 300bps, 1200bps, 2400bps, 9600bps, 11.52Kbps and 19.2Kbps

- The maximum operating distance supported in RS-232 communication is 50 feet at the highest supported baudrate.

- Embedded devices contain a UART for serial communication and they generate signal levels conforming to TTL/CMOS logic. A level translator IC like MAX 232 from Maxim Dallas semiconductor is used for converting the signal lines from the UART to RS-232 signal lines for communication. On the receiving side the received data is converted back to digital logic level by a converter IC. Converter chips contain converters for both transmitter and receiver

- RS-232 uses single ended data transfer and supports only point-to-point communication and not suitable for multi-drop communication.

- RS-422 is another serial interface standard from EIA for differential data communication. It supports data rates up to 100Kbps and distance up to 400 ft.

- RS-422 supports multi-drop communication with one transmitter device and receiver devices up to 10.

- RS-485 is the enhanced version of RS-422 and it supports multi-drop communication with up to 32 transmitting devices (drivers) and 32 receiving devices on the bus. The communication between devices in the bus makes use of the 'addressing' mechanism to identify slave devices.

2. Universal Serial Bus (USB)

- Universal Serial Bus (USB) is a wired high speed serial bus for data communication

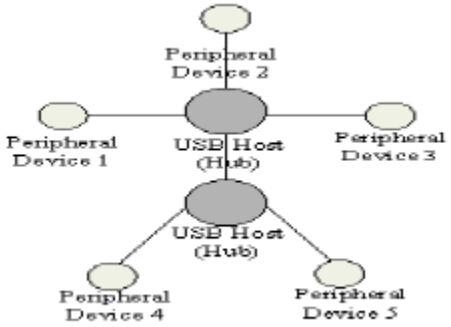
- The USB communication system follows a star topology with a USB host at the center and one or more USB peripheral devices/USB hosts connected to it

- A USB host can support connections up to 127, including slave peripheral devices and other USB hosts

- USB transmits data in packet format. Each data packet has a standard format. The USB communication is a host initiated one

• The USB Host contains a host controller which is responsible for controlling the data communication, including establishing connectivity with USB slave devices, packetizing and formatting the data packet.

• There are different standards for implementing the USB Host Control interface; namely Open Host Control Interface (OHCI) and Universal Host Control Interface (UHCI).



• The Physical connection between a USB peripheral device and master device is established with a USB cable.

• The USB cable supports communication distance of up to 5 meters.

• The USB standard uses two different types of connectors namely 'Type A' and 'Type B' at the ends of the USB cable for connecting the USB peripheral device and host device.

• 'Type A' connector is used for upstream connection (connection with host) and 'Type B' connector is used for downstream connection (connection with slave device).

• The Pin details for the connectors are listed in the table given below.

Pin No:	Pin Name	Description
1	V_{BUS}	Carries power (5V)
2	D-	Differential data carrier line
3	D+	Differential data carrier line
4	GND	Ground signal line

• Each USB device contains a Product ID (PID) and a Vendor ID (VID).

• The PID and VID are embedded into the USB chip by the USB device manufacturer.

• The VID for a device is supplied by the USB standards forum.

- PID and VID are essential for loading the drivers corresponding to a USB device for communication.

- USB supports four different types of data transfers, namely; Control, Bulk, Isochronous and Interrupt.

- Control transfer is used by USB system software to query, configure and issue commands to the USB device.

- Bulk transfer is used for sending a block of data to a device. Bulk transfer supports error checking and correction. Transferring data to a printer is an example for bulk transfer.

- Isochronous data transfer is used for real time data communication. In Isochronous transfer, data is transmitted as streams in real time. Isochronous transfer doesn't support error checking and re-transmission of data in case of any transmission loss.

- Interrupt transfer is used for transferring small amount of data. Interrupt transfer mechanism makes use of polling technique to see whether the USB device has any data to send.

- The frequency of polling is determined by the USB device and it varies from 1 to 255 milliseconds. Devices like Mouse and Keyboard, which transmits fewer amounts of data, uses interrupt transfer.

- USB.ORG Cwww.usb.org) is the standards body for defining and controlling the standards for USB communication.

- Presently USB supports four different data rates namely; Low Speed (1.5Mbps), Full Speed (12Mbp's), High Speed (480Mbps) and Super Speed (4.8Gbps). The Low Speed and Full Speed specifications are defined by USB 1.0 and the High Speed specification is defined by USB 2.0, USB 3.0defines the specifications for Super Speed.

3. IEEE 1394 (Firewire)

- A wired, isochronous high speed serial communication bus. It is also known as High Performance Serial Bus (HPSB)

- The research on 1394 was started by Apple Inc in 1985 and the standard for this was coined by IEEE.

- The Apple Inc's (www.apple.com) implementation of 1394 protocol is popularly known as Firewire.

- i.LINK is the 1394 implementation from Sony Corporation (www.sony.net) and Lynx is the implementation from Texas Instruments (www.ti.com).

• 1394 supports peer-to-peer connection and point-to-multipoint communication allowing 63 devices to be connected on the bus in a tree topology.

• The 1394 standard supports a data rate of 400 to 3200Mbits/Second.

• IEEE 1394 uses differential data transfer and the interface cable supports 3 types of connectors, namely; 4-pin connector, 6-pin connector (alpha connector) and 9 pin connector (beta connector).

• The 6 and 9 pin connectors carry power also to support external devices. It can supply unregulated power in the range of 24 to 30V (The Apple implementation is for battery operated devices and it can supply a voltage in the range 9 to 12V).

• The table given below illustrates the pin details for 4, 6 and 9 pin connectors.

Pin Name	Pin No: (4 Pin Connector)	Pin No: (6 Pin Connector)	Pin No: (9 Pin Connector)	Description
Power		1	8	Unregulated DC supply. 24 to 30V
Signal Ground		2	6	Ground connection
TPB-	1	3	1	Differential Signal line for Signal Line B
TPB+	2	4	2	Differential Signal line for Signal Line B
TPA-	3	5	3	Differential Signal line for Signal Line A
TPA+	4	6	4	Differential Signal line for Signal Line A
TPA(S)			5	Shield for the differential signal line A. Normally grounded
TPB(S)			9	Shield for the differential signal line B. Normally grounded
NC			7	No connection

• The IEEE 1394 connector contains two differential data transfer lines namely A and B.

•The differential lines of A are connected to B (TPA+ to TPB+ and TPA- to TPB-) and vice versa.

• Unlike USB interface (Except USB OTG), IEEE 1394 doesn't require a host for communicating between devices. Example, a scanner can be directly connected to a printer for printing.

• The data rate supported by 1394 is far higher than the one supported by USB2.0 interface.

- 1394 is a popular communication interface for connecting embedded devices like 'Digital Camera', 'Camcorder', 'Scanners' with desktop Computers for data transfer and storage.

- Unlike USB interface (Except USB OTG), IEEE 1394 doesn't require a host for communicating between devices.

- For example, you can directly connect a scanner with a printer for printing. The data rate supported by 1394 is far higher than the one supported by USB2.0 interface.

- The 1394 hardware implementation is much costlier than USB implementation.

4. Infrared (IrDA)

- A serial, half duplex, line of sight based wireless technology for data communication between devices.

- Infrared communication technique makes use of Infrared waves of the electromagnetic spectrum for transmitting the data.

- IrDA supports point-point and point-to-multipoint communication, provided all devices involved in the communication are within the line of sight.

- The typical communication range for IrDA lies in the range 10cm to 1 m.

- IR supports data rates ranging from 9600bits/second to 16Mbps. Depending on the speed of data transmission IR is classified into Serial IR (SIR), Medium IR (MIR), Fast IR (FIR), Very Fast IR (VFIR) and Ultra Fast IR (UFIR).

- SIR supports transmission rates ranging from 9600bps to 115.2kbps. MIR supports data rates of 0.576Mbps and 1.152Mbps. FIR supports data rates up to 4Mbps. VFIR is designed to support high data rates up to 16Mbps. The UFIR specs are under development and it is targeting a data rate up to 100Mbps.

- IrDA communication involves a transmitter unit for transmitting the data over IR and a receiver for receiving the data. Infrared Light Emitting Diode (LED) is used as the IR source for transmitter and at the receiving end a photodiode is used as the receiver.

- Both transmitter and receiver unit will be present in each device supporting IrDA communication for bidirectional data transfer. Such IR units are known as 'Transceiver'.

- Certain devices like a TV remote control always require unidirectional communication and so they contain either the transmitter or receiver unit (The remote control unit contains the transmitter unit and TV contains the receiver unit).

- 'Infra-red Data Association' is the regulatory body responsible for defining and licensing the specifications for IR data communication.

- IrDA communication has two essential parts; a physical link part and a protocol part.

- The physical link is responsible for the physical transmission of data between devices supporting IR communication.

- Protocol part is responsible for defining the rules of communication.

- The physical link works on the wireless principle making use of Infrared for communication. The IrDA specifications include the standard for both physical link and protocol layer.

- The IrDA control protocol contains implementations for Physical Layer (PHY), Media Access Control (MAC) and Logical Link Control (LLC). The Physical Layer defines the physical characteristics of communication like range, data rates, power, etc.

- IrDA is a popular interface for file exchange and data transfer in low cost devices.

- IrDA was the prominent communication channel in mobile phones before Bluetooth's existence. Even now most of the mobile phone devices support IrDA.

5. Bluetooth (BT)

- Bluetooth is a low cost, low power, short range wireless technology for data and voice communication. Bluetooth was first proposed by 'Ericsson' in 1994.

- Bluetooth operates at 2.4GHz of the Radio Frequency spectrum and uses the Frequency Hopping Spread Spectrum (FHSS) technique for communication. Literally it supports a data rate of up to 1Mbps and a range of approximately 30 feet for data communication.

- Like IrDA, Bluetooth communication also has two essential parts; a physical link part and a protocol part.

- The physical link is responsible for the physical transmission of data between devices supporting Bluetooth communication and protocol part is responsiblefor defining the rules of communication.

- The physical link works on the wireless principle making use of RF waves for communication.

- Bluetooth enabled devices essentially contain a Bluetooth wireless radio for the transmission and reception of data.

- The rules governing the Bluetooth communication is implemented in the 'Bluetooth protocol stack'. The Bluetooth communication IC holds the stack. Each Bluetooth device will have a

48 bit unique identification number. Bluetooth communication follows packet based data transfer.

- Bluetooth supports point-to-point (device to device) and point-to-multipoint (device to multiple device broadcasting) wireless communication.

- The point-to-point communication follows the master- slave relationship. A Bluetooth device can function as either master or slave.

- When a network is formed with one Bluetooth device as master and more than one device as slaves, it is called a Piconet.

- A Piconet supports a maximum of seven slave devices.

- Bluetooth is the favorite choice for short range data communication in handheld embedded devices. Bluetooth technology is very popular among cell phone users as they are the easiest communication channel for transferring ringtones, music files, pictures, media files, etc. between neighboring Bluetooth enabled phones.

- The Bluetooth standard specifies the minimum requirements that a Bluetooth device must support for a specific usage scenario. The Generic Access Profile (GAP) defines the requirements for detecting a Bluetooth device and establishing a connection with it. All other specific usage profiles are based on GAP.

- Serial Port Profile (SPP) for serial data communication, File Transfer Profile (FTP) for file transfer between devices, Human Interface Device (HID) for supporting human interface devices like keyboard and mouse are examples for Bluetooth profiles.

- The specifications for Bluetooth communication is defined and licensed by the standards body 'Bluetooth Special Interest Group' (SIG).

6. Wi-Fi

- The popular wireless communication technique for networked communication of devices.
- Wi-Fi follows the IEEE 802.11 standard.
- Wi-Fi is intended for network communication and it supports Internet Protocol (IP) based communication.
- Wi-Fi based communications require an intermediate agent called Wi-Fi router/Wireless Access point to manage the communications.
- The Wi-Fi router is responsible for restricting the access to a network, assigning IP address to devices on the network, routing data packets to the intended devices on the network.
- Wi-Fi enabled devices contain a wireless adaptor for transmitting and receiving data in the form of radio signals through an antenna.
- Wi-Fi operates at 2.4GHZ or 5GHZ of radio spectrum and they co-exist with other ISM band devices like Bluetooth.
- A Wi-Fi network is identified with a Service Set Identifier (SSID). A Wi-Fi device can connect to a network by selecting the SSID of the network and by providing the credentials if the network is security enabled.
- Wi-Fi networks implements different security mechanisms for authentication and data transfer.
- Wireless Equivalency Protocol (WEP), Wireless Protected Access (WPA) etc are some of the security mechanisms supported by Wi-Fi networks in data communication.
- Wi-Fi supports data rates ranging from 1Mbps to 150Mbps (Growing towards higher rates as technology progresses) depending on the standards (802.11 a/b/g/n) and access/modulation method.
- Depending On the type of antenna and usage location (indoor/outdoor), Wi-Fi offers a range of 100 to 300 feet.

Fig: Wi-Fi network

7. ZigBee

- ZigBee is a low power, low cost, wireless network communication protocol based on the IEEE 802.15.4-2006 standard.

- ZigBee is targeted for low power,low data rate and secure applications for Wireless Personal Area Networking (WPAN).

- The ZigBee specifications support a robust mesh network containing multiple nodes. This networking strategy makes the network reliable by permitting messages to travel through a number of different paths to get from one node to another.

- ZigBeeoperates worldwide at the unlicensed bands of Radio spectrum, mainly at 2.400 to 2.484 GHz, 902 to 928 MHz and 868.0 to 868.6 MHz.

- ZigBee Supports an operating distance of up to 100 metres and a data rate of 20 to 250Kbps.

- In the ZigBee terminology, each ZigBee device falls under any one of the following ZigBee device category.

ZigBee Coordinator (ZC)/Network Coordinator: The ZigBee coordinator acts as the root of the ZigBee network. The ZC is responsible for initiating the ZigBee network and it has the capability to store information about the network

ZigBee Router (ZR)/Full function Device (FFD): Responsible for passing information from device to another device or to another ZR

ZigBee End Device (ZED)/Reduced Function Device (RFD): End device containing ZigBee functionality for data communication. It can talk only with a ZR or ZC and doesn't have the capability to act as a mediator for transferring data from one device to another.

• The diagram shown in Figure gives an overview of ZC, ZED and ZR in a ZigBee network.

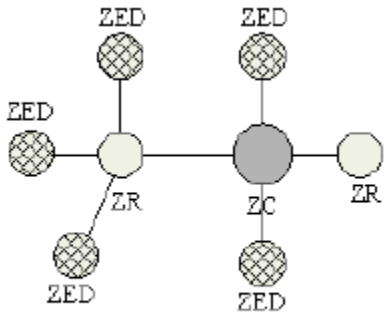


Fig: A ZigBee network model

• ZigBee is primarily targeting application areas like home & industrial automation, energy management, home control/ security, medical/patient tracking, logistics & asset tracking and sensor networks & active RFID.

• Automatic Meter Reading (AMR), smoke detectors, wireless telemetry, HVAC control, heating control, lighting controls, environmental controls, etc. are examples for applications which can make use of the ZigBee technology.

• The specifications for ZigBee is developed and managed by the ZigBee alliance (www.zigbee.org). a non-profit consortium of leading semiconductor manufacturers, technology providers, OEMs and end-users worldwide.

8. General Packet Radio Service (GPRS), 3G,4G, LTE

• General Packet Radio Service (GPRS) is a communication technique for transferring data over a mobile communication network like GSM.

• Data is sent as packets in GPRS communication. The transmitting device splits the data into several related packets. At the receiving end the data is re-constructed by combining the received data packets.

• GPRS supports a theoretical maximum transfer rate of 171.2kbps.

• In GPRS communication, the radio channel is concurrently shared between several users instead of dedicating a radio channel to a cell phone user. The GPRS communication divides the channel into 8 timeslots and transmits data over the available channel.

• GPRS supports Internet Protocol (IP), Point to Point Protocol (PPP) and X.25 protocols for communication.

• GPRS is mainly used by mobile enabled embedded devices for data communication. The device should support the necessary GPRS hardware like GPRS modem and GPRS radio.

• To accomplish GPRS based communication, the carrier network also should have support for GPRS communication.

• GPRS is an old technology and it is being replaced by new generation data communication techniques like EDGE, High Speed Downlink Packet Access (HSDPA), etc. which offers higher bandwidths for communication.

3.16 EMBEDDED FIRMWARE

• Embedded firmware refers to the control algorithm (Program instructions) and or the configuration settings that an embedded system developer dumps into the code (Program) memory of the embedded system.

• It is an un-avoidable part of an embedded system. There are various methods available for developing the embedded firmware. They are listed below.

1) Write the program in high level languages like Embedded C/C++ using an Integrated Development Environment (The IDE will contain an editor, compiler, linker, debugger, simulator, etc. IDEs are different for different family of processors/controllers.
   For example, Keil micro vision3 IDE is used for all family members of 8051 microcontroller, since it contains the generic 8051 compiler C51).
2) Write the program in Assembly language using the instructions supported by your application's target processor/controller.

• The instruction set for each family of processor/controller is different and the program written in either of the methods given above should be converted into a processor understandable machine code before loading it into the program memory.

• The process of converting the program written in either a high level language or processor/controller specific Assembly code to machine readable binary code is called 'HEX File Creation'.

• The methods used for 'HEX File Creation' is different depending on the programming techniques used. If the program is written in Embedded C/C++ using an IDE, the cross compiler

included in the IDE converts it into corresponding processor/controller understandable 'HEXFile'.

• If you are following the Assembly language based programming technique (method 2), you can use the utilities supplied by the processor/controller vendors to convert the source code into 'HEXFile'. Also third party tools are available, which may be of free of cost, for this conversion.

3.17 OTHER SYSTEM COMPONENTS

• The other system components refer to the components/circuits/ICs which are necessary for the proper functioning of the embedded system. Some of these circuits may be essential for the proper functioning of the processor/controller and firmware execution.

• Watchdog timer, Reset IC (or passive circuit), brown-out protection IC (or passive circuit), etc. are examples of circuits/ICs which are essential for the proper functioning of the processor/controllers.

• Some of the controllers or SoCs integrate these components within a single IC and doesn't require such components externally connected to the chip for proper functioning.

• Depending on the system requirement, the embedded system may include other integrated circuits for performing specific functions, level translator ICs for interfacing circuits with different logic levels, etc.

A. Reset Circuit

• The Reset circuit is essential to ensure that the device is not operating at a voltage level where the device is not guaranteed to operate, during system power ON

• The Reset signal brings the internal registers and the different hardware systems of the processor/controller to a known state and starts the firmware execution from the reset vector (Normally from vector address 0x0000 for conventional processors/controllers

• The reset vector can be relocated to an address for processors/controllers supporting boot loader

• The reset signal can be either active high (The processor undergoes reset when the reset pin of the processor is at logic high) or active low (The processor undergoes reset when the reset pin of the processor is at logic low).

• Since the processor operation is synchronized to a clock signal, the reset pulse should be wide enough to give time for the clock oscillator to stabilize before the internal reset state starts.

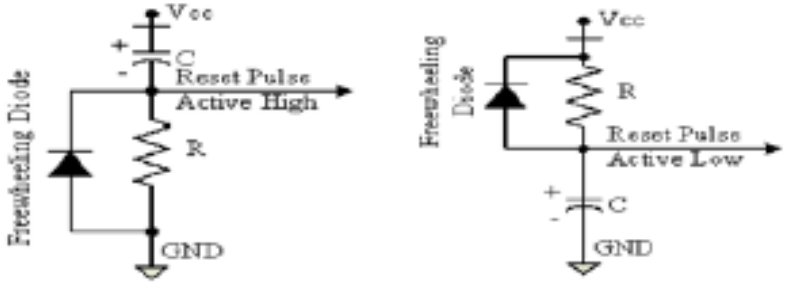


Fig: RC based RESET Circuit

• The reset signal to the processor can be applied at power ON through an external passive reset circuit comprising a Capacitor and Resistor or through a standard Reset IC .

• Select the reset IC based on the type of reset signal and logic level (CMOS/TTL) supported by the processor/controller in use.

• Some microprocessors/controllers contain built-in internal reset circuitry and they don't require external reset circuitry.

• Figure illustrates a resistor capacitor based passive reset circuit for active high and low configurations. The reset pulse width can be adjusted by changing the resistance value R and capacitance value C.

B. Brown-out Protection Circuit

• Brown-out protection circuit prevents the processor/controller from unexpected program execution behaviour when the supply voltage to the processor/controller falls below a specified voltage.

• It is essential for battery powered devices since there are greater chances for the battery voltage to drop below the required threshold.

• The processor behaviour may not be predictable if the supply voltage falls below the recommended operating voltage. It may lead to situations like data corruption.

• A brown-out protection circuit holds the processor/controller in reset state, when the operating voltage falls below the threshold until it rises above the threshold voltage.

•Certain processors/controllers support built in brown-out protection circuit which monitors the supply voltage internally.

• If the proeessor/controller doesn't integrate a built-in brown-out protection circuit, the same can be implemented using external passivecircuits or supervisor ICs.

• Figure illustrates a brown-outcircuit implementation using Zener diode and transistor for processor/controller with active low Reset logic.

• The Zener diode Dz and transistor Q forms the heart of this circuit. The transistor conducts always when the supply voltage Vcc is greater than that of the sum of VBE and V7 (Zener voltage).

• The transistor stops conducting when the supply voltage falls below the sum of VBE and Vz. Select the Zener diode with required voltage for setting the low threshold value for Fee.

• The values of Rl, R2, and R3 can be selected based on the electrical characteristics of the transistor in use. Microprocessor Supervisor ICs like DS1232 from Maxim Dallas also provides Brown-out protection.

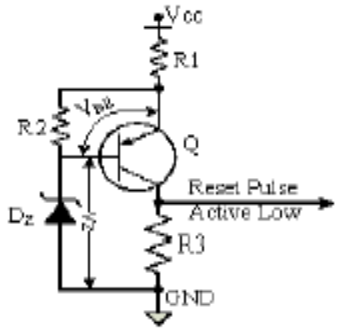


Fig:Brown-out protection circuit with Active low output

C. Oscillator Unit

• A microprocessor/microcontroller is a digital device made up of digital combinational and sequential circuits.

• The instruction execution of a microprocessor/controller occurs in sync with a clock signal. It is analogous to the heartbeat of a living being which synchronizes the execution of life.

• For a living being, the heart is responsible for the generation of the beat whereas the oscillator unit of the embedded system is responsible for generating the precise clock for the processor.

- Certain processors/controllers integrate a built-in oscillator unit and simply require an external ceramic resonator/quartz crystal for producing the necessary clock signals.

- Quartz crystals and ceramic resonators are equivalent in operation, however they possess physical difference.

- A quartz crystal is normally mounted in a hermetically sealed metal case with two leads protruding out of the case.

- Certain devices may not contain a built-in oscillator unit and require the clock pulses to be generated and supplied externally.

- Quartz crystal Oscillators are available in the form chips and they can be used for generating the clock pulses in such a cases.

- The speed of operation of a processor is primarily dependent on the clock frequency. However we cannot increase the clock frequency blindly for increasing the speed of execution.

- The logical circuits lying inside the processor always have an upper threshold value for the maximum clock at which the system can run, beyond which the system becomes unstable and non-functional.

- The total system power consumption is directly proportional to the clock frequency. The power consumption increases with increase in clock frequency.

- The accuracy of program execution depends on the accuracy of the clock signal. The accurracy of the crystal oscillator or ceramic resonator is normally expressed in terms of +/-ppm (Parts per million).

- Figure illustrates the usage of quartz crystal/ceramic resonator and external oscillator chip for clock generation.

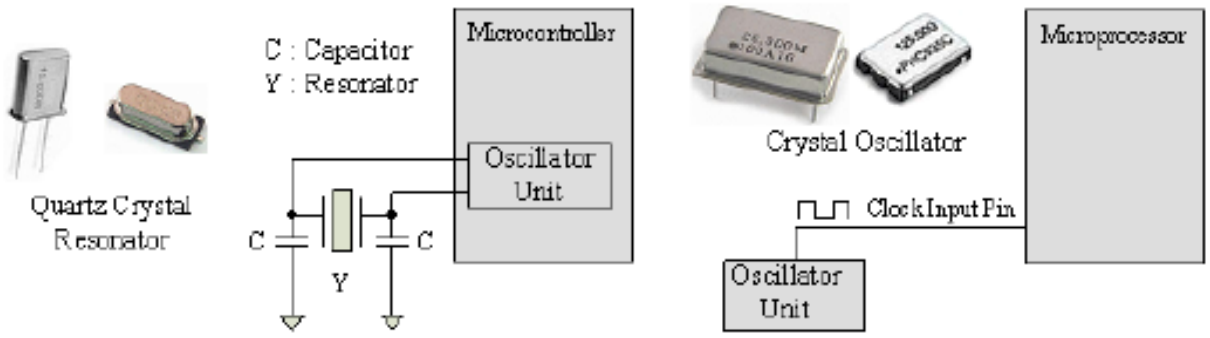


Fig: Oscillator circuitry using quartz crystal and quartz crystal oscillator

D. Real-Time Clock (RTC)

- Real-Time Clock (RTC) is a system component responsible for keeping track of time.
- RTC holds information like current time (In hours, minutes and seconds) in 12 hour/24 hour format, date, month, year, day of the week, etc. and supplies timing reference to the system.
- RTC is intended to function even in the absence of power.
- RTCs are available in the form of Integrated Circuits from different semiconductor manufacturers like Maxim/Dallas, ST Microelectronics etc.
- The RTC chip contains a microchip for holding the time and date related information and backup battery cell for functioning in the absence of power, in a single IC package.
- The RTC chip is interfaced to the processor or controller of the embedded system.
- For Operating System based embedded devices, a timing reference is essential for synchronizing the operations of the OS kernel.
- The RTC can interrupt the OS kernel by asserting the interrupt line of the processor/controller to which the RTC interrupt line is connected.
- The OS kernel identifies the interrupt in terms of the Interrupt Request (IRQ) number generated by an interrupt controller.
- One IRQ can be assigned to the RTC interrupt and the kernel can perform necessary operations like system date time updation, managing software timers etc.

- When an RTC timer tick interrupt occurs. The RTC can be configured to interrupt the processor at predefined intervals or to interrupt the processor when the RTC register reaches a specified value (used as alarm interrupt).

E. Watchdog Timer

- A watchdog timer, or simply a watchdog, is a hardware timer for monitoring the firmware execution.

- Depending on the internal implementation, the watchdog timer increments or decrements a free running counter with each clock pulse and generates a reset signal to reset the processor if the count reaches zero for a down counting watchdog, or the highest count value for an upcounting watchdog.

- If the watchdog counter is in the enabled state, the firmware can write a zero (for upcounting watchdog implementation) to it before starting the execution of a piece of code (subroutine or portion of code which is susceptible to execution hang up) and the watchdog will start counting.

- If the firmware execution doesn't complete due to malfunctioning, within the time required by the watchdog to reach the maximum count, the counter will generate a reset pulse and this will reset the processor (if it is connected to the reset line of the processor).

- If the firmware execution completes before the expiration of the watchdog timer you can reset the count by writing a 0 (for an up counting watchdog timer) to the watchdog timer register.

- Most of the processors implement watchdog as a built-in component and provides status register to control the watchdog timer (like enabling and disabling watchdog functioning) and watchdog timer register for writing the count value.

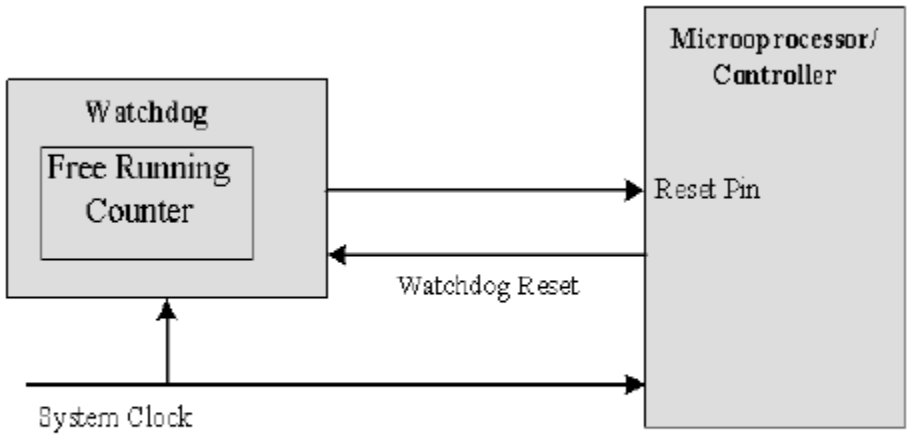
- If the processor/controller doesn't contain a built in watchdog timer, the same can be implemented using an external watchdog timer IC circuit.

- The external watchdog timer uses hardware logic for enabling/disabling, resetting the watch dog count, etc instead of the firmware based 'writing' to the status and watchdog timer register.

- The Microprocessor supervisor IC DS1232 integrates a hardware watchdog timer in it.

• In modem systems running on embedded operating systems, the watchdog can be implemented in such a way that when a watchdog timeout occurs, an interrupt is generated instead of resetting the processor.

• The interrupt handler for this handles the situation in an appropriate fashion. Figure illustrates the implementation of an external watchdog timer based microprocessor supervisor circuit for a small scale embedded system.



External Watch Dog Timer Unit Interfacing with Processor