

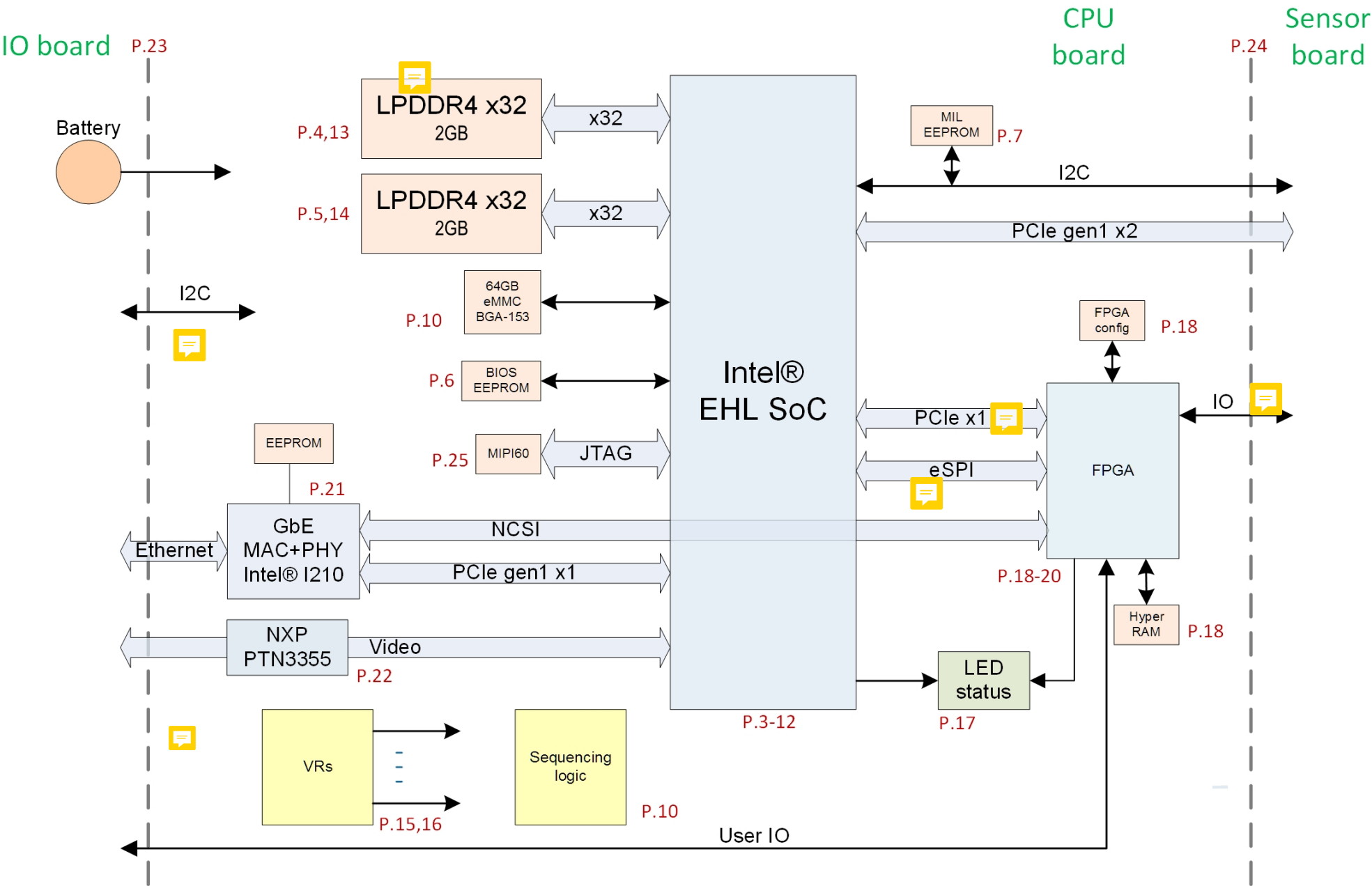
IRIS4 CPU Board


REVISIONS					
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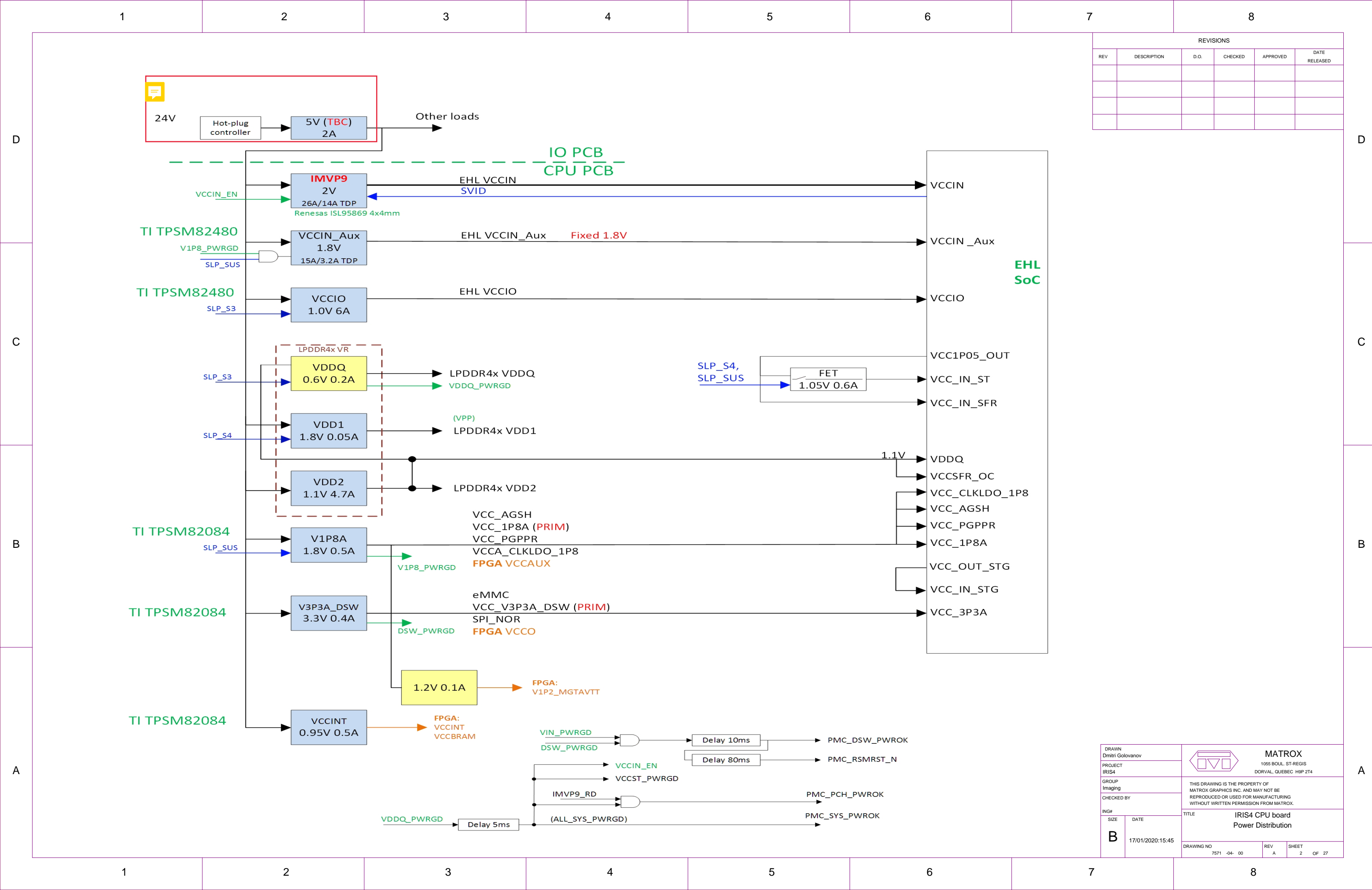
MATROX CONFIDENTIAL

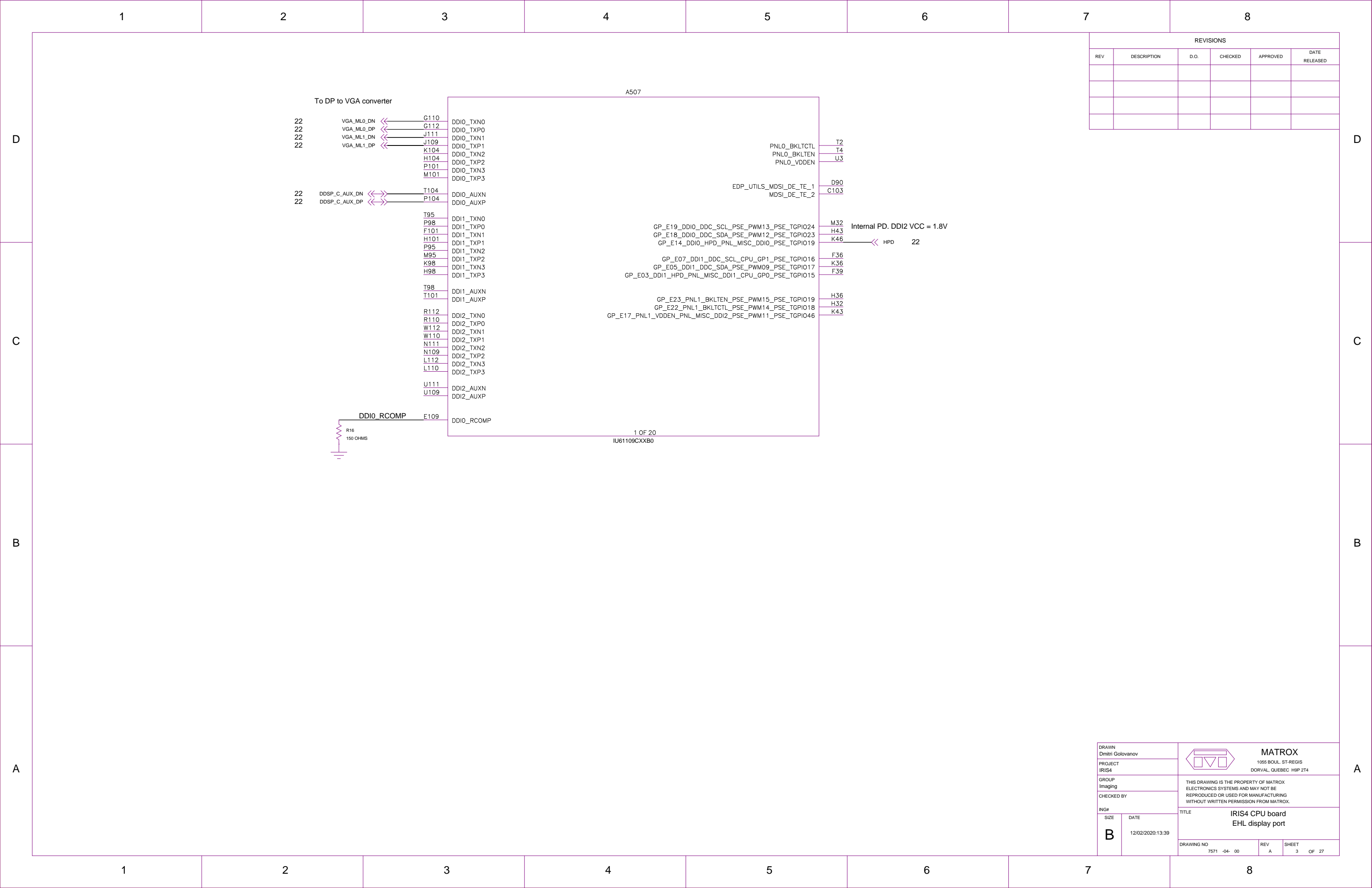
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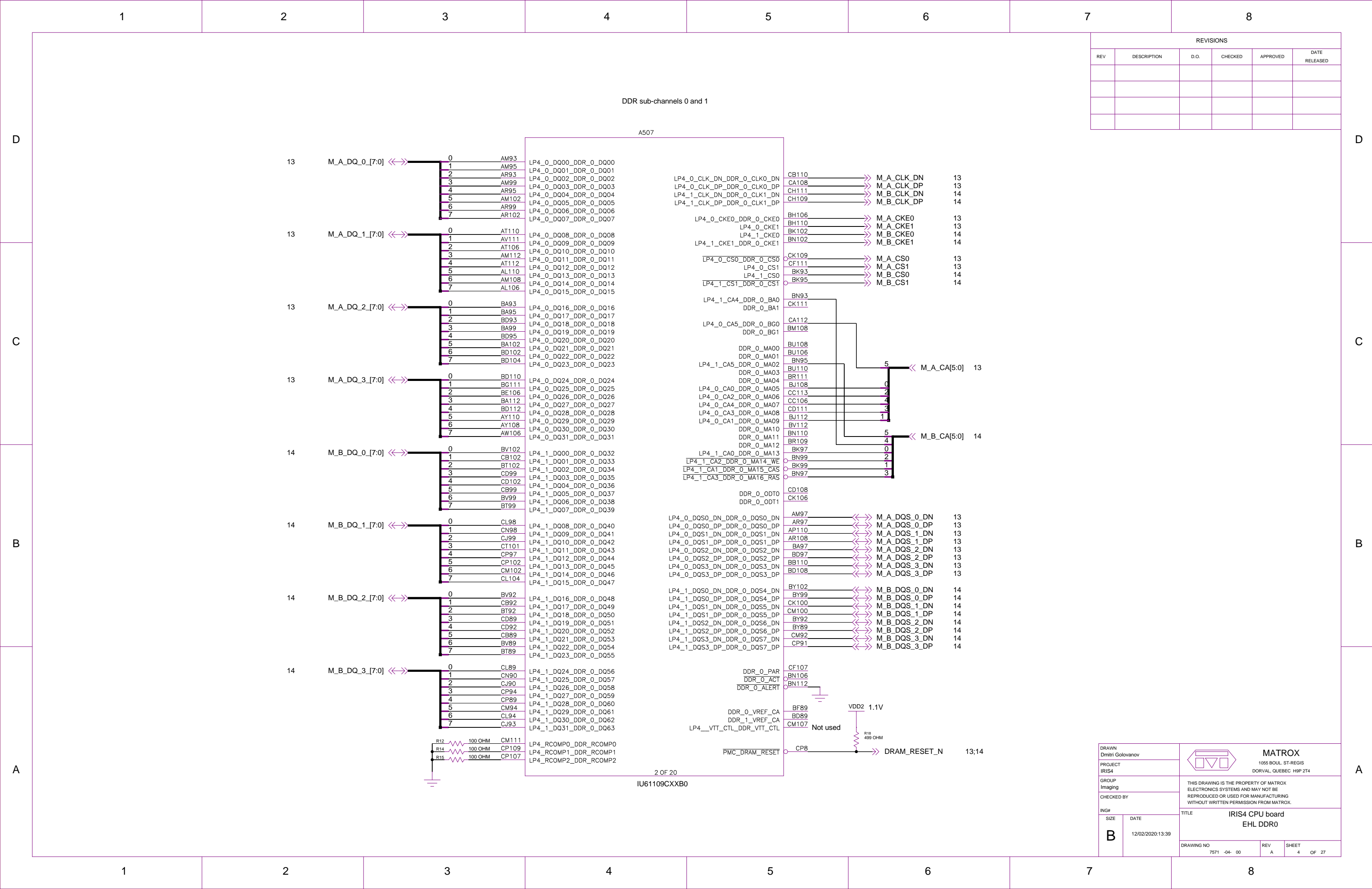
- p.1 BLOCK_DIAGRAM
- p.2 POWER DISTRIBUTION
- p.3 EHL display port
- p.4 EHL DDR0
- p.5 EHL DR1
- p.6 EHL SPI
- p.7 EHL I2C IO
- p.8 EHL GPIO
- p.9 EHL PCIe USB
- p.10 EHL eMMC PMC
- p.11 EHL power
- p.12 EHL GND pins
- p.13 LPDDR4x channel A1
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- p.15 VR VCCIN IMVP9
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DRAWN Dmitri Golovanov		 <div>MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4</div>	
PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
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DRAWING NO 7571 -04- 00		REV A	SHEET 1 OF 27

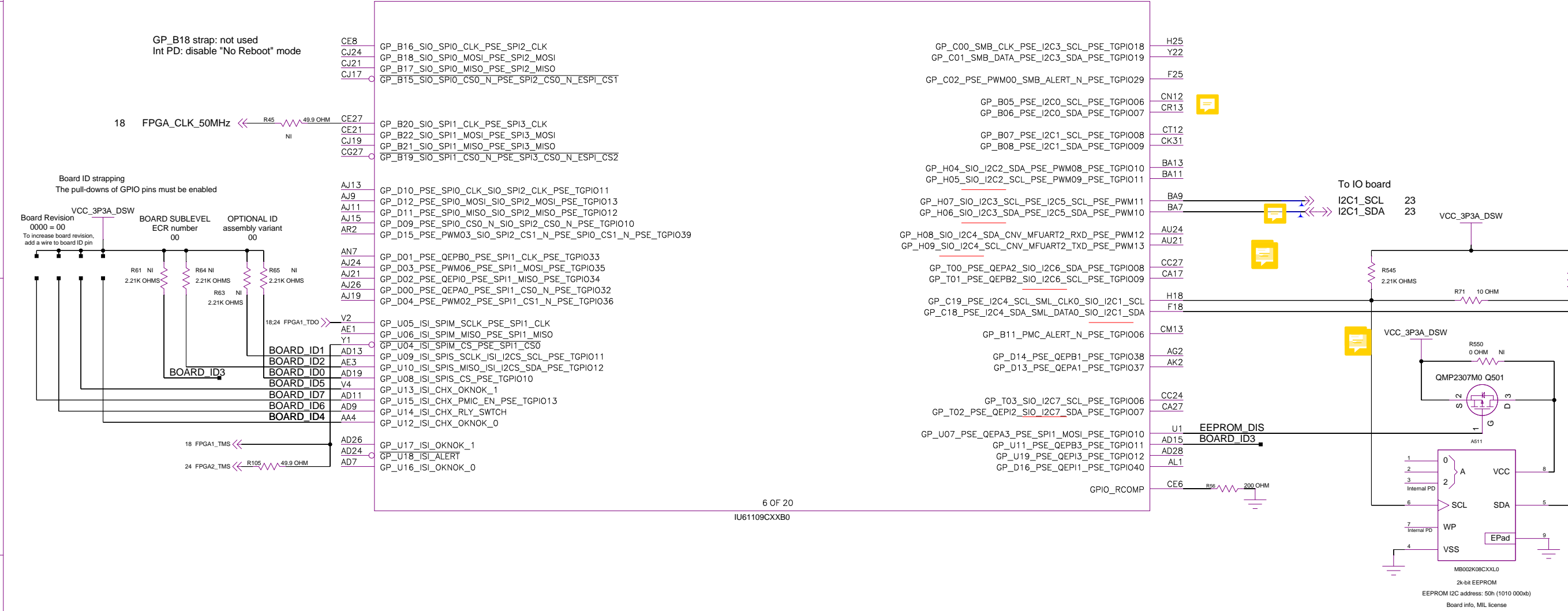





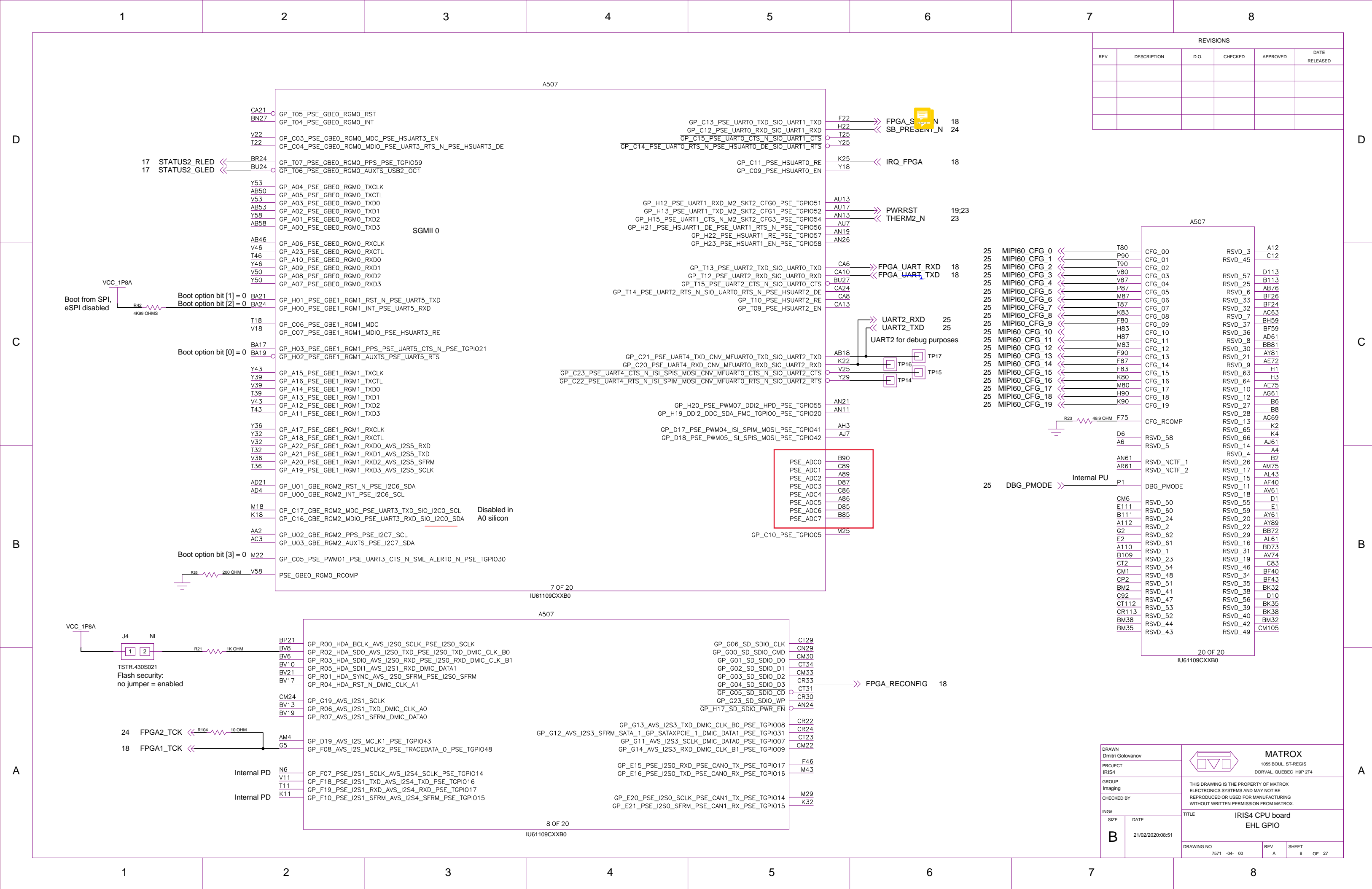


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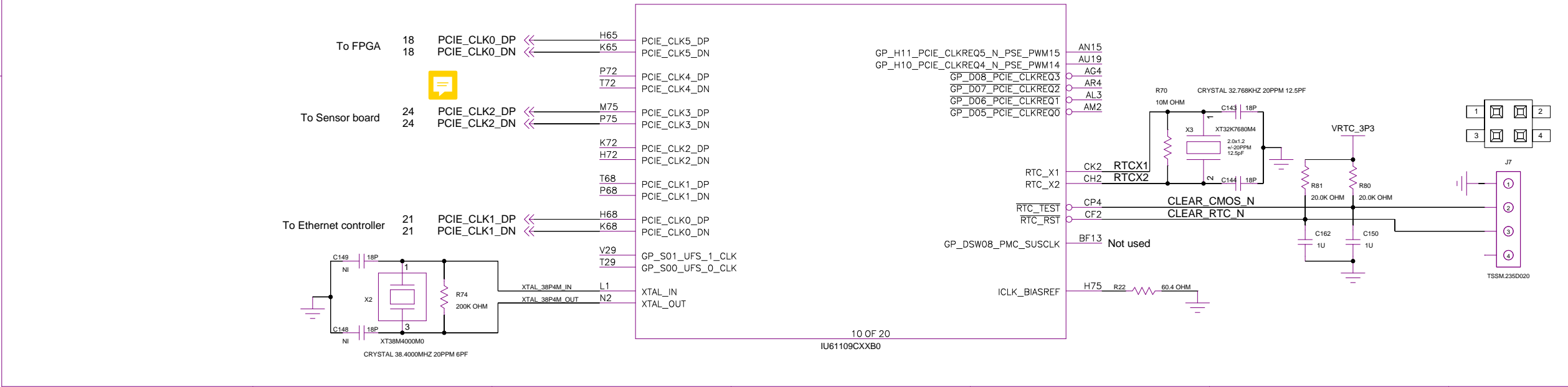
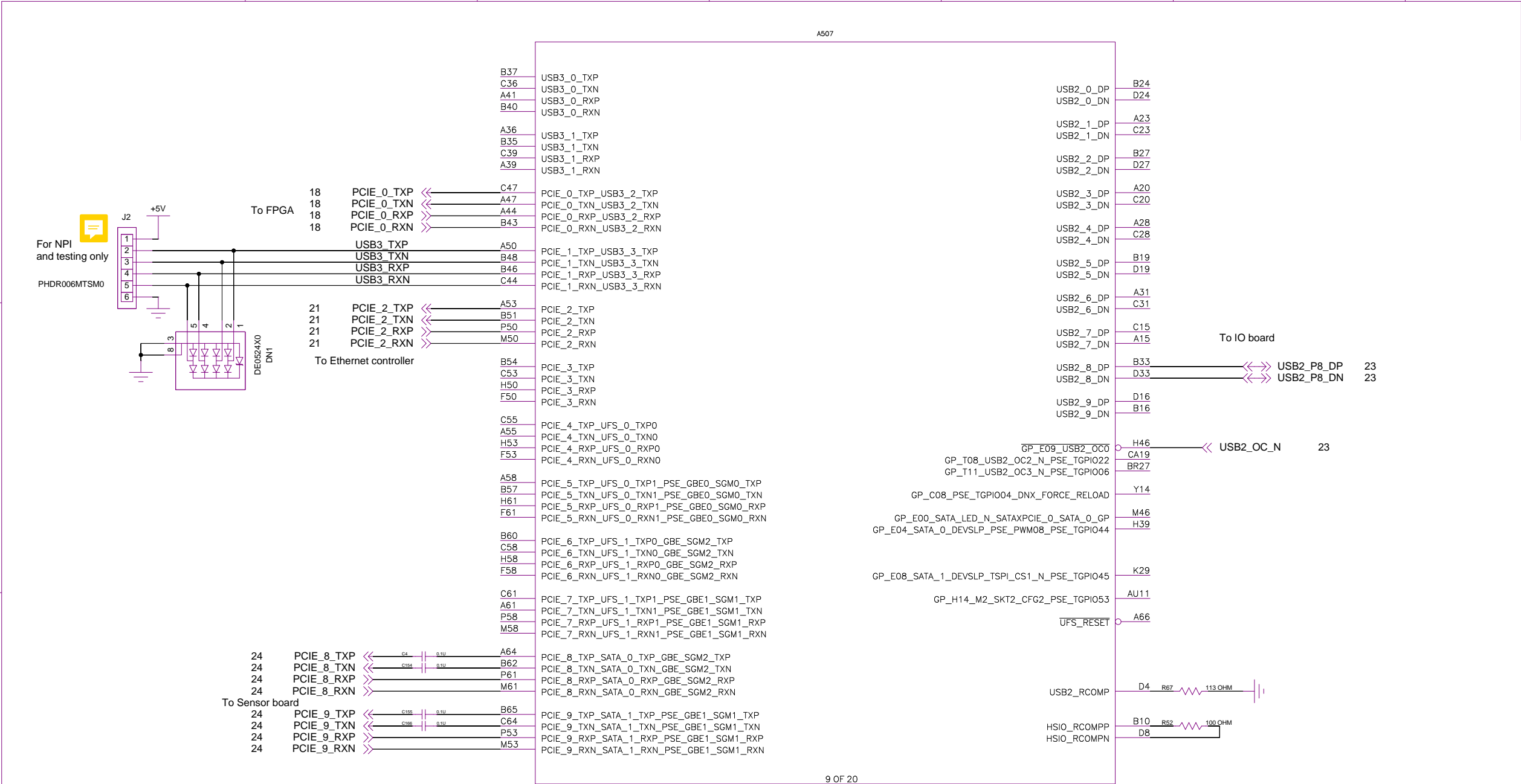
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SIZE B	DATE 21/02/2020:08:26		
DRAWING NO 7571 -04- 00		REV A	SHEET 7 OF 27



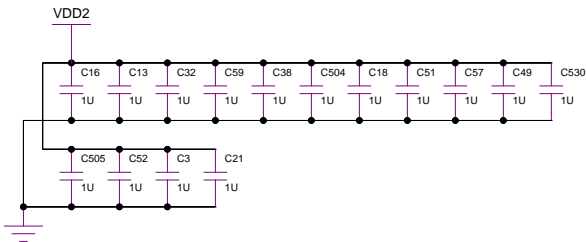
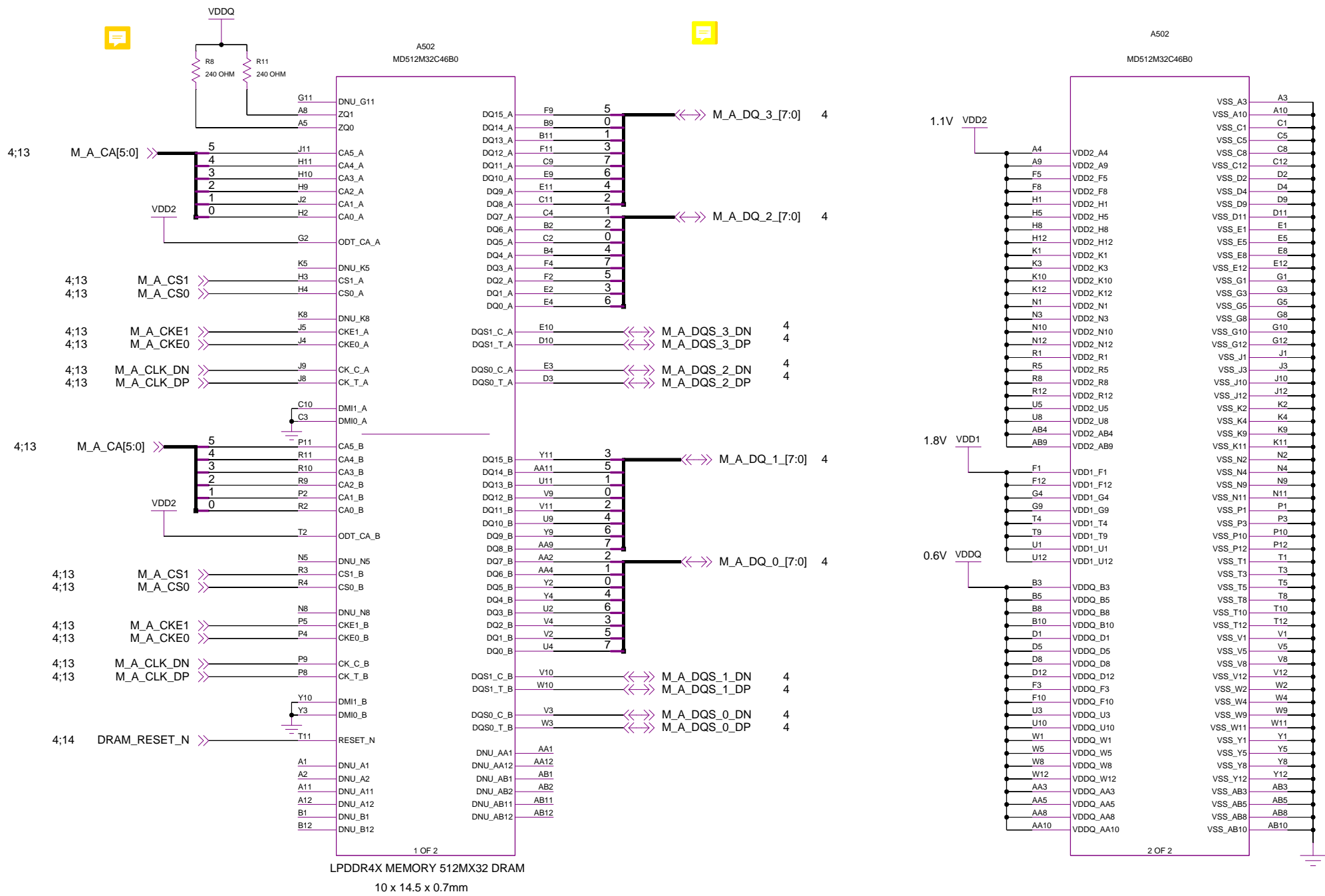
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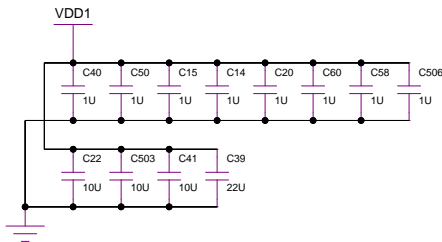
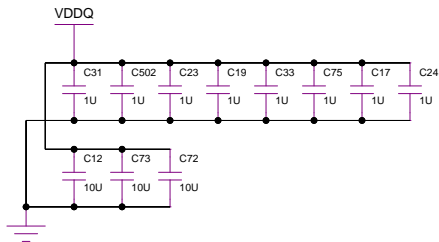
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PROJECT IRIS4			
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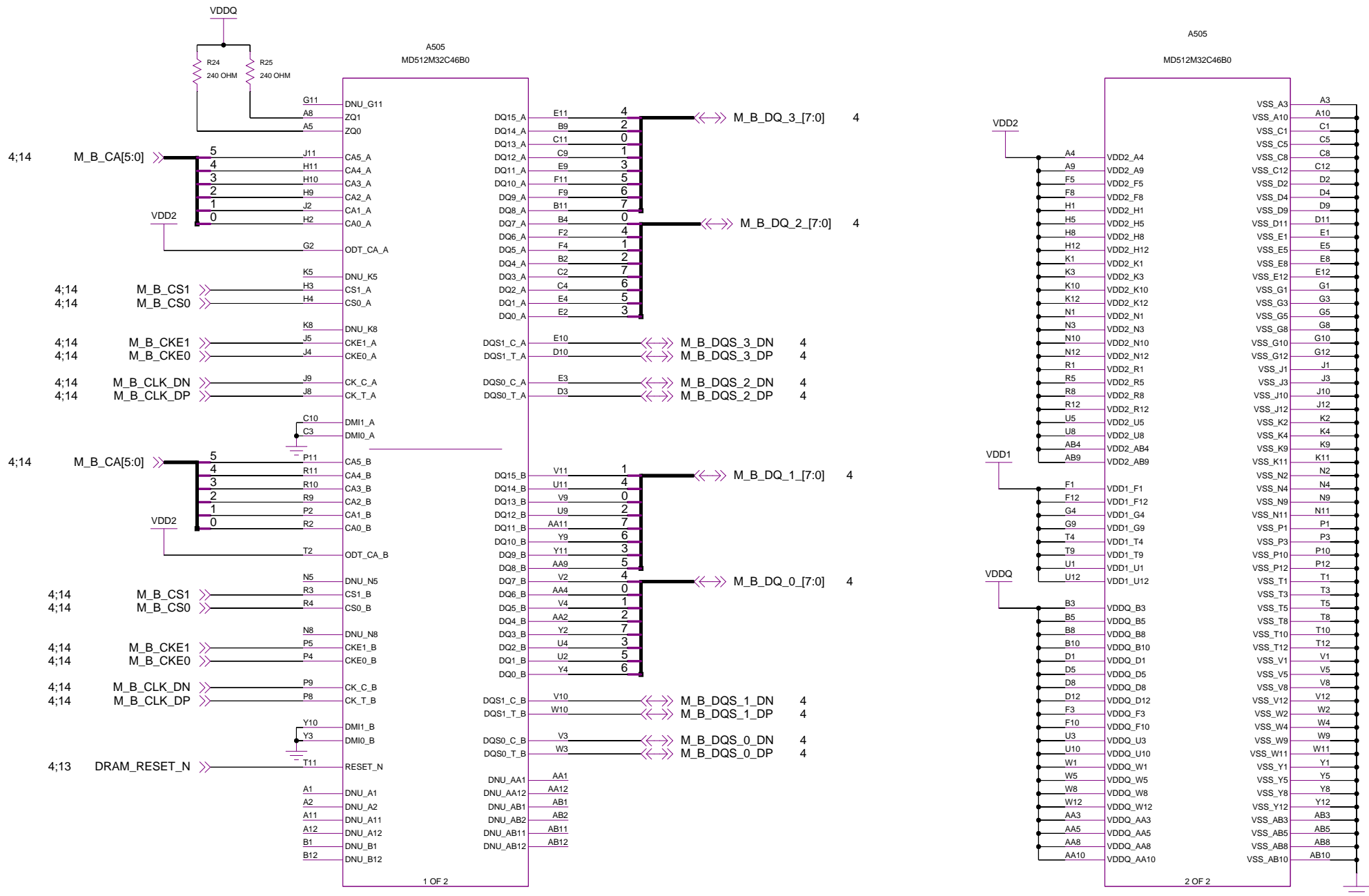



LPDDR4x decoupling for 2 devices




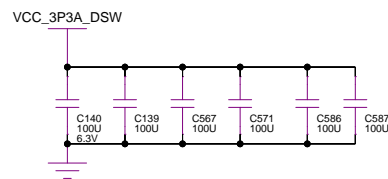
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PROJECT IRIS4				1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
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PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
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			SHEET 14 OF 27

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SIZE B	DATE 21/02/2020/07:44		
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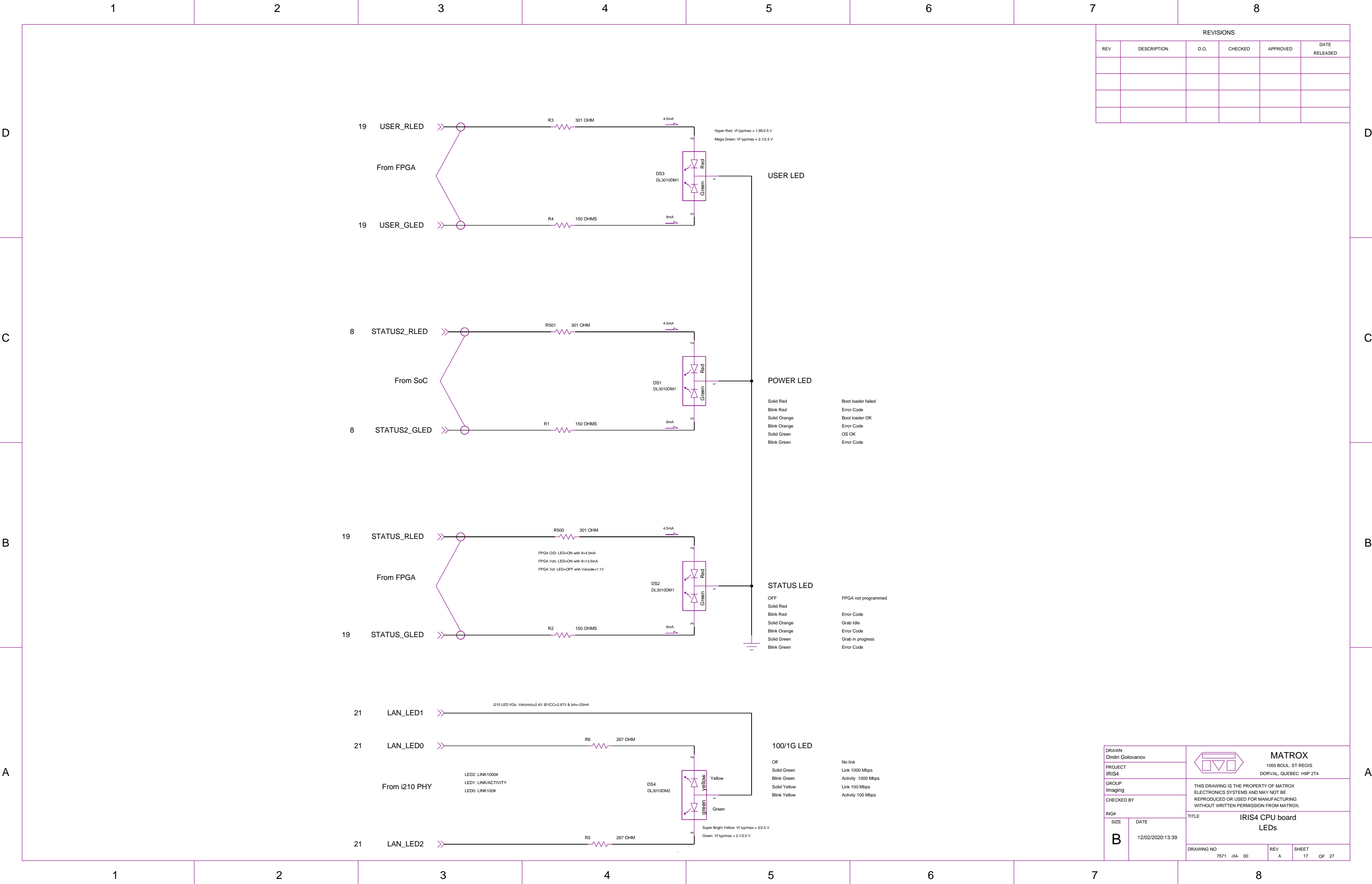
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21

LAN_LED1

»

From i210 PHY

21

LAN_LED0

»

R6

267 OHM

R5

267 OHM

DS4

DL3010DM2

i210 LED I/Os: Voh(min)=2.4V @VCC=2.97V & Ioh=-20mA

Super Bright Yellow: Vf typ/max = 2/2.5 V

Green: Vf typ/max = 2.1/2.5 V

2

1

3

100/1G LED

Off

Solid Green

Blink Green

Solid Yellow

Blink Yellow

No link

Link 1000 Mbps

Activity 1000 Mbps

Link 100 Mbps

Activity 100 Mbps

21

LAN_LED2

»

From i210 PHY

21

LAN_LED0

»

R6

267 OHM

R5

267 OHM

DS4

DL3010DM2

LED2: LINK100#

LED1: LINK/ACTIVITY

LED0: LINK100#

Super Bright Yellow: Vf typ/max = 2/2.5 V

Green: Vf typ/max = 2.1/2.5 V

2

1

3

100/1G LED

Off

Solid Green

Blink Green

Solid Yellow

Blink Yellow

No link

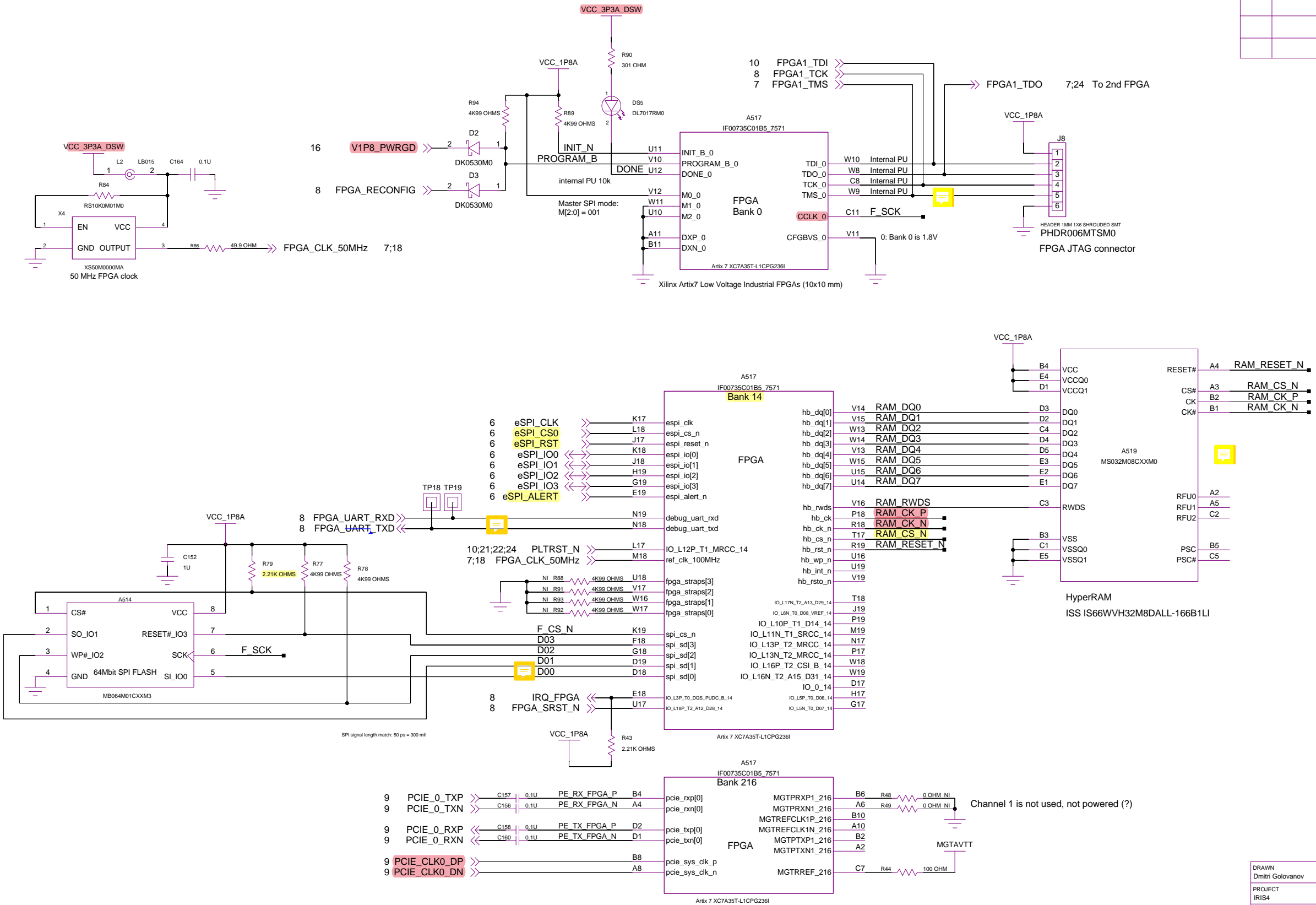
Link 1000 Mbps


Activity 1000 Mbps

Link 100 Mbps

Activity 100 Mbps

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PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
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ING#		DRAWING NO	
SIZE B	DATE 14/02/2020:11:41	7571 -04- 00	REV A
			SHEET 18 OF 27

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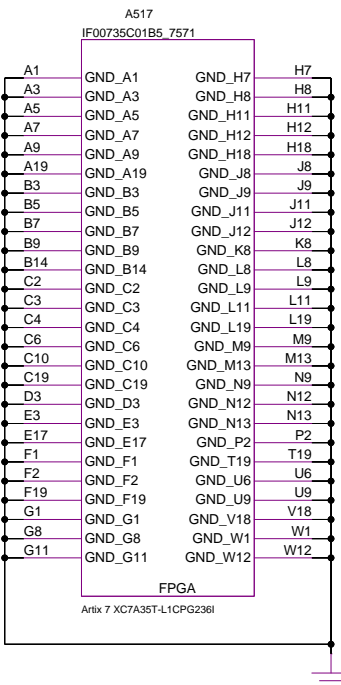
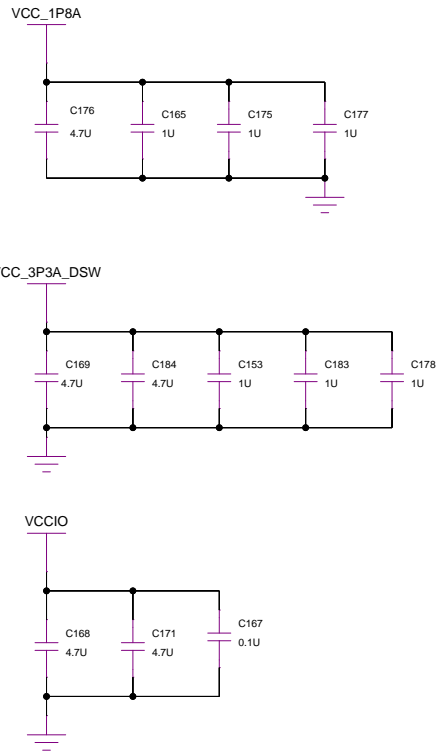
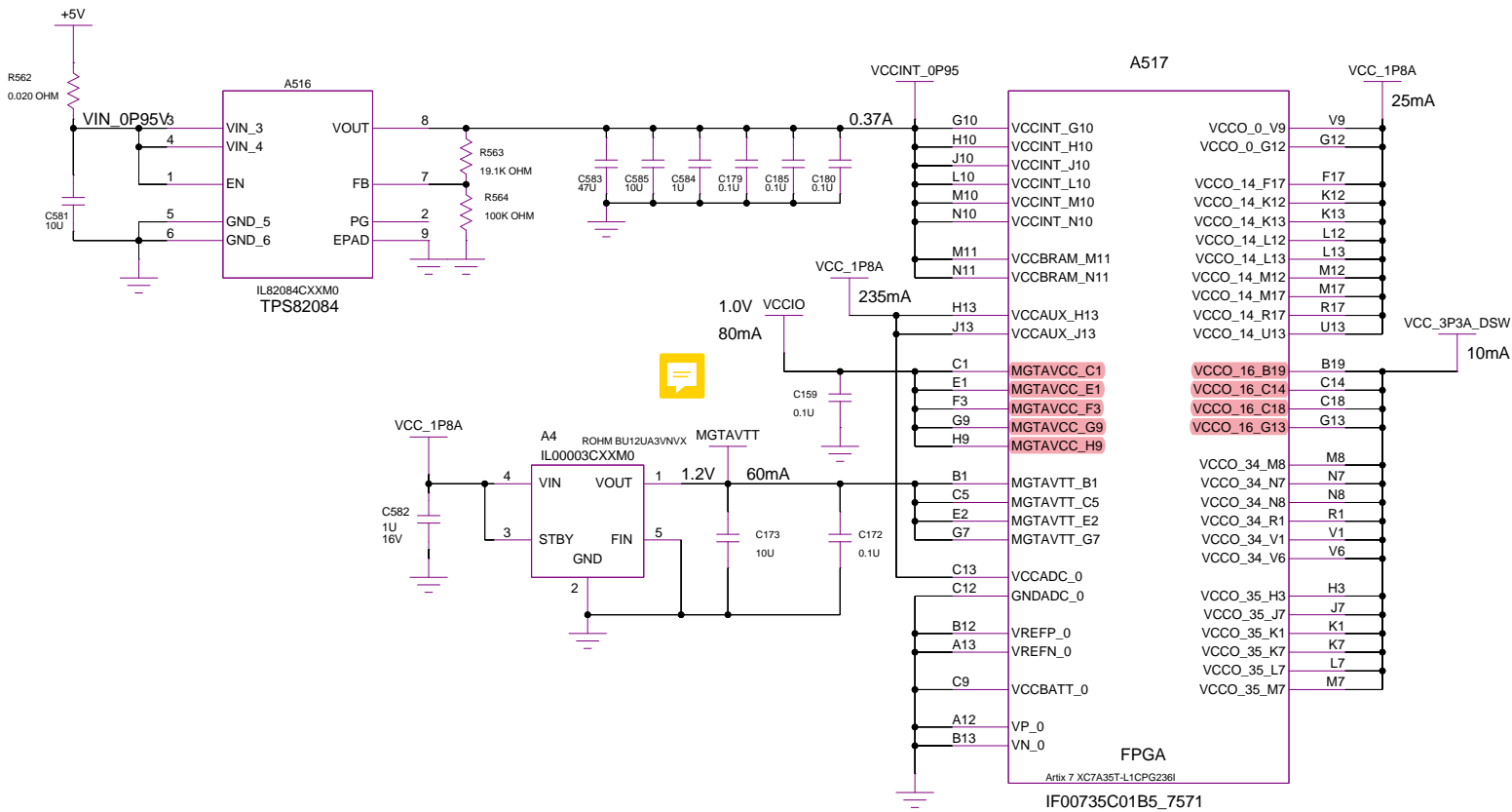
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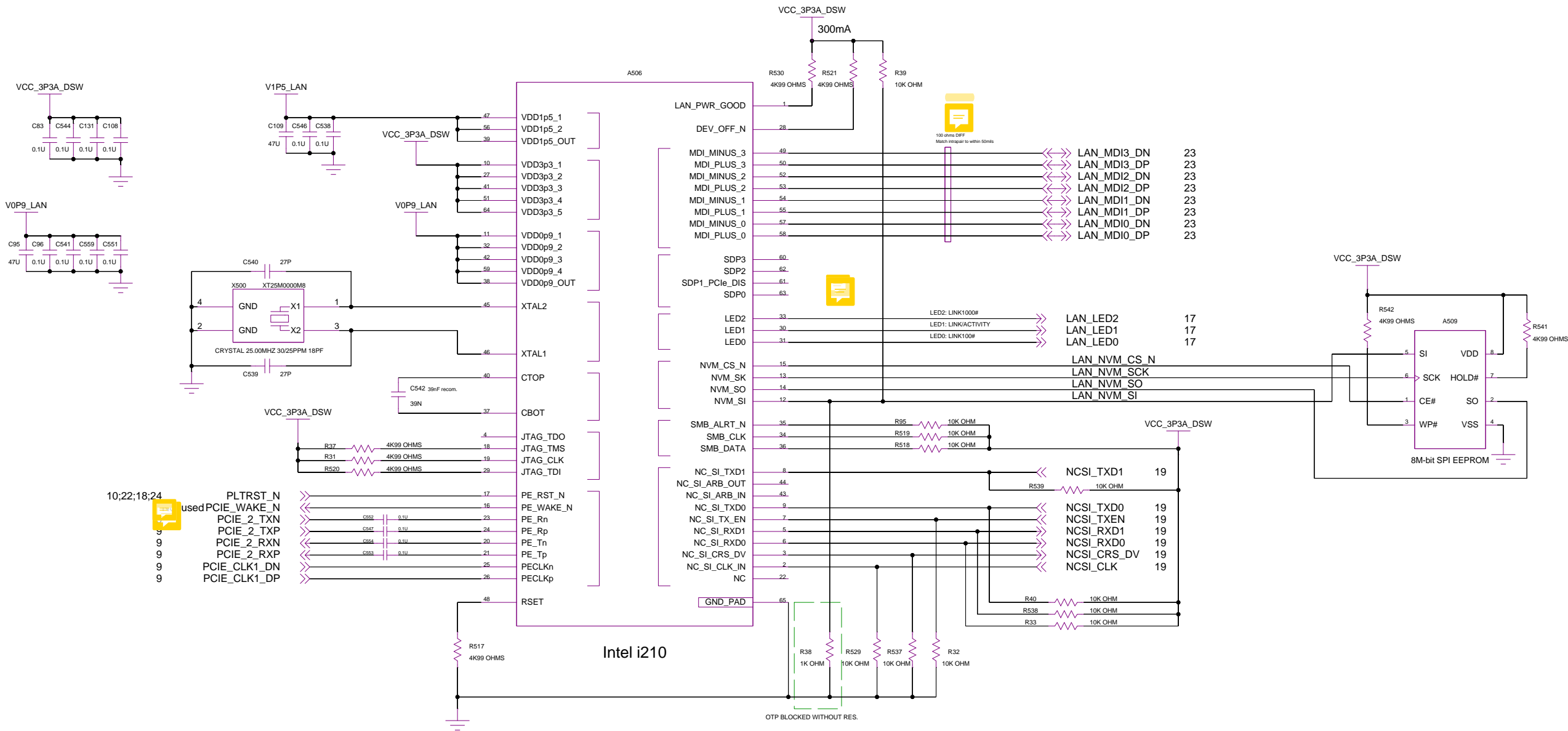
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			SHEET 21 OF 27

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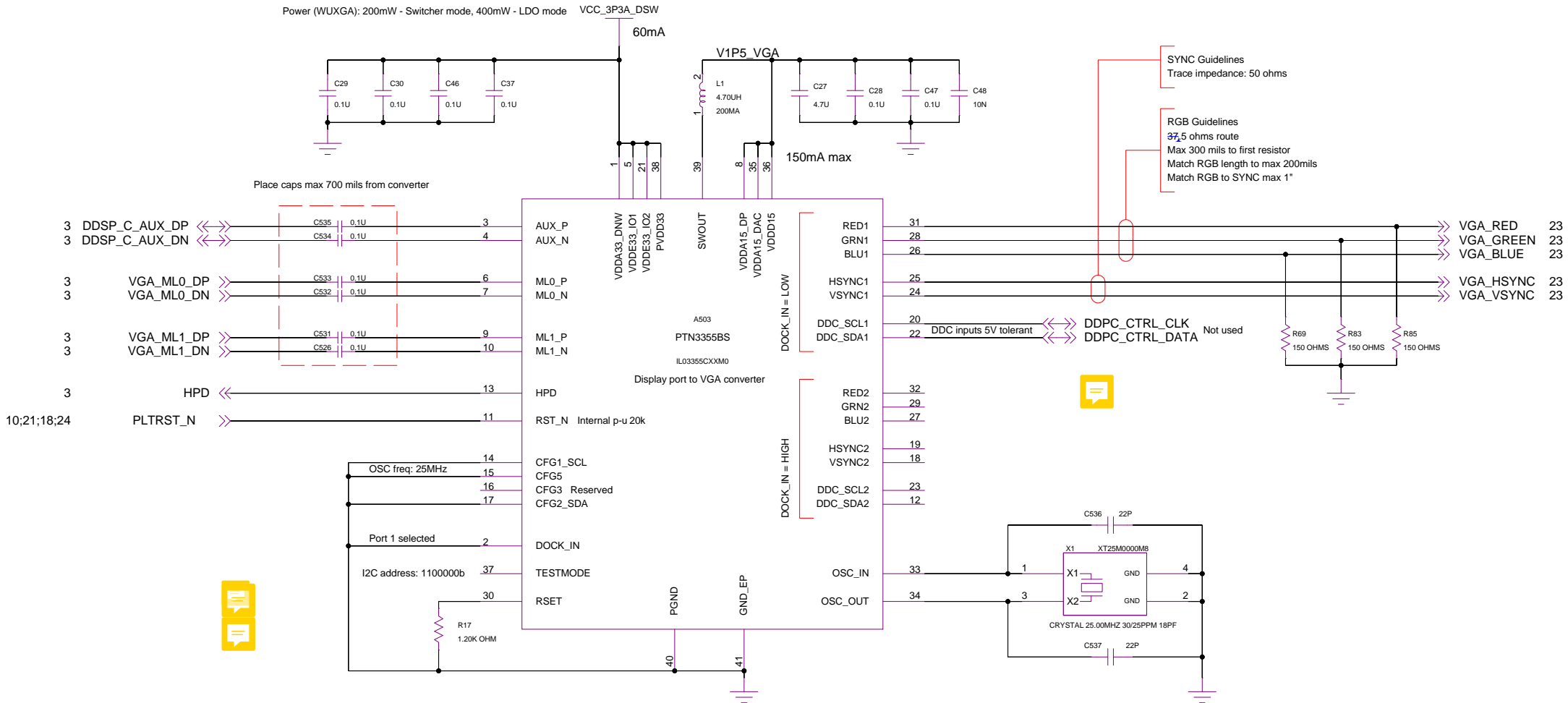
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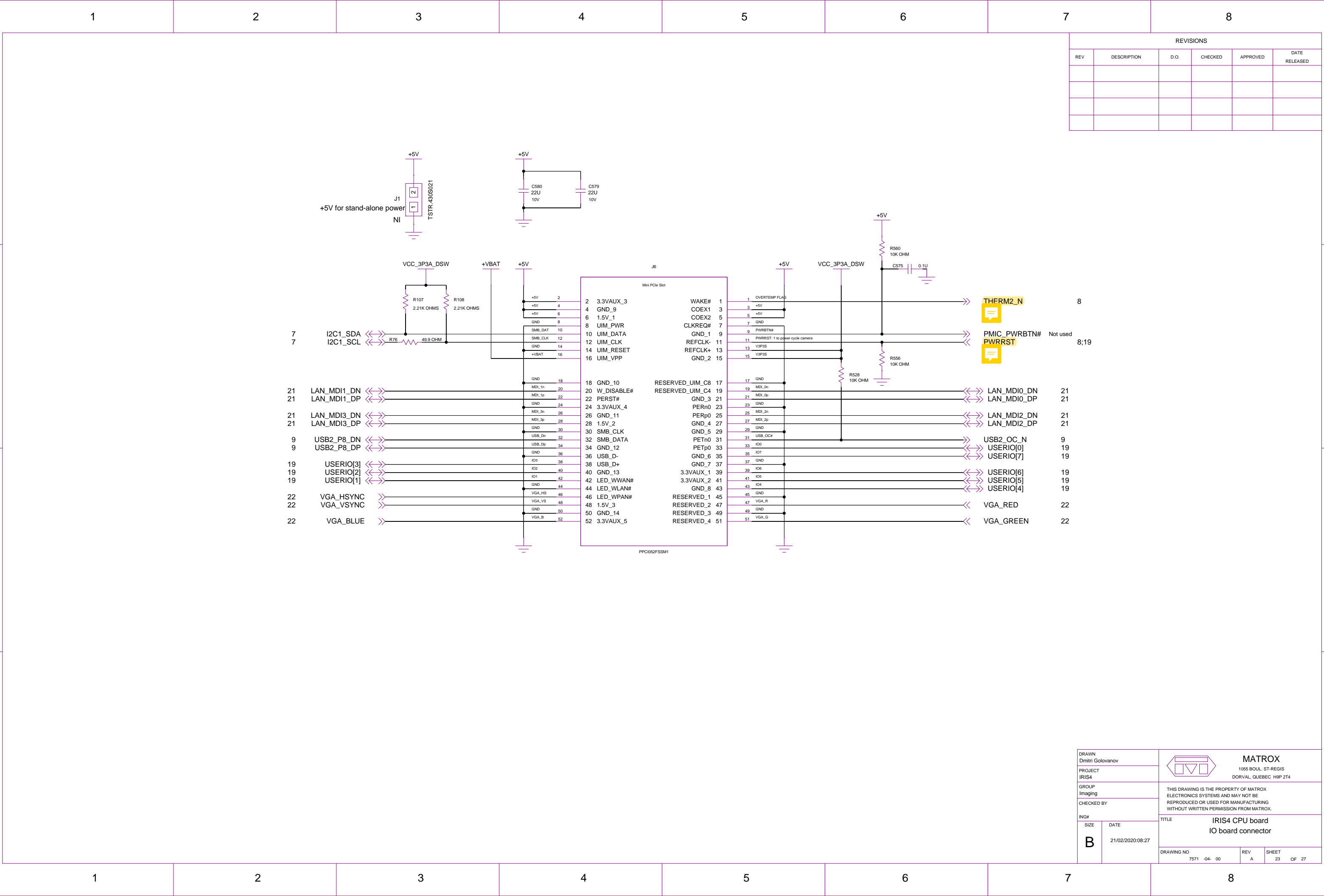
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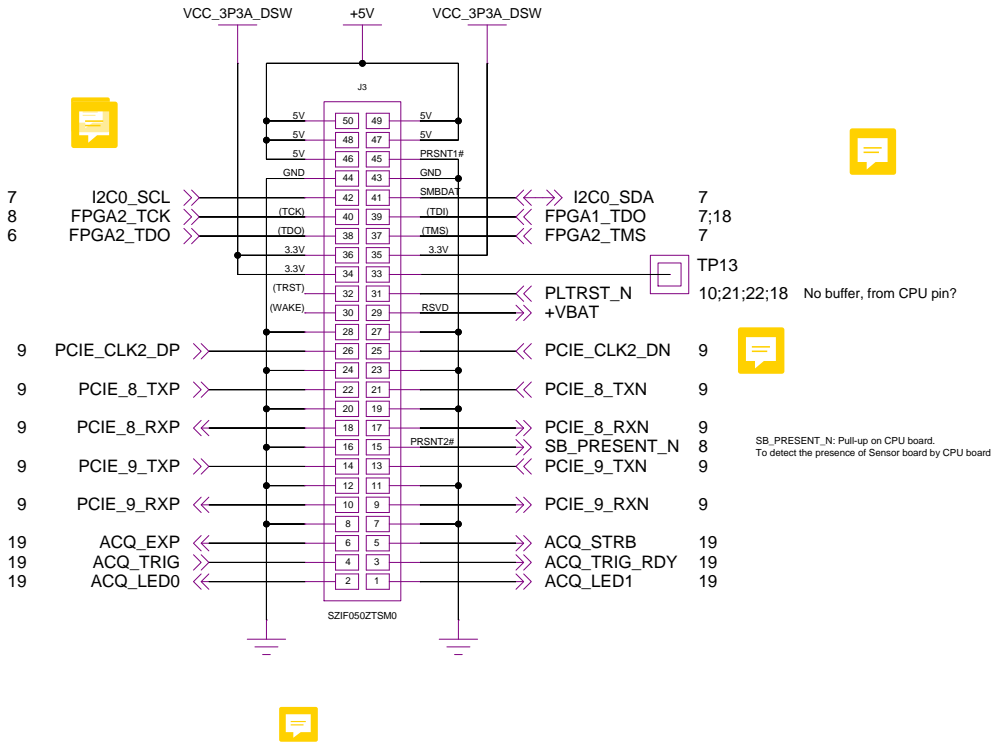
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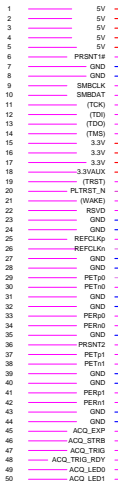
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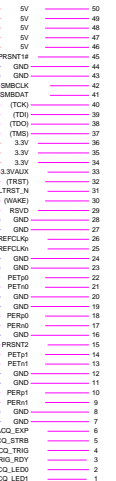
CPU Board ZIF pinout is inverted
Sensor board pos 1 aligned with CPU board pos 50
Connectors are head-to-head with latch on same side




Sensor board connector



CPU board connector



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SIZE B	DATE 20/02/2020:15:21		
DRAWING NO 7571 -04- 00		REV A	SHEET 24 OF 27

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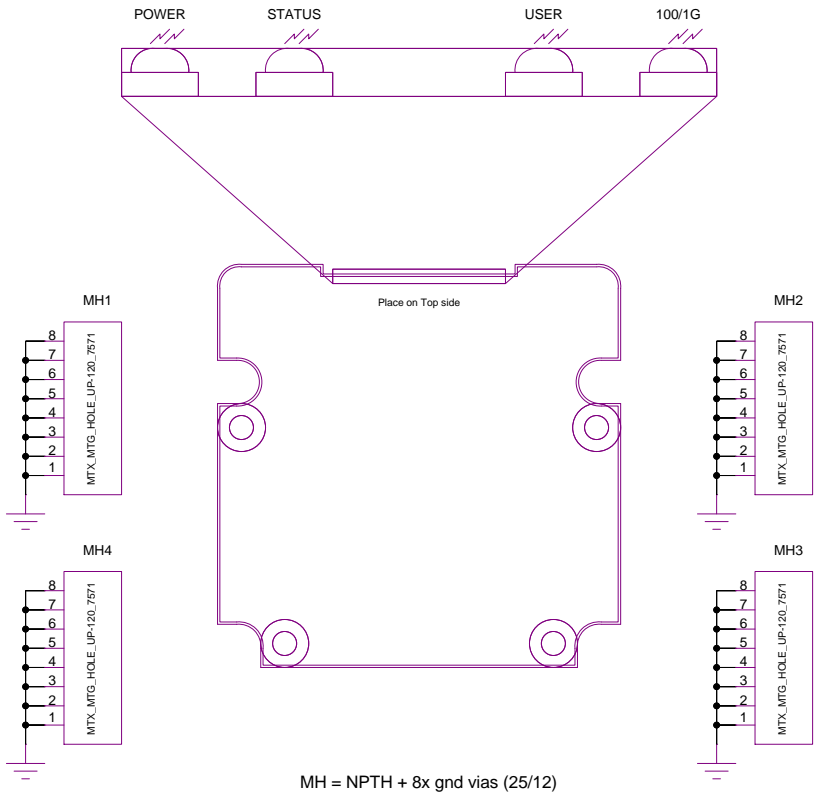
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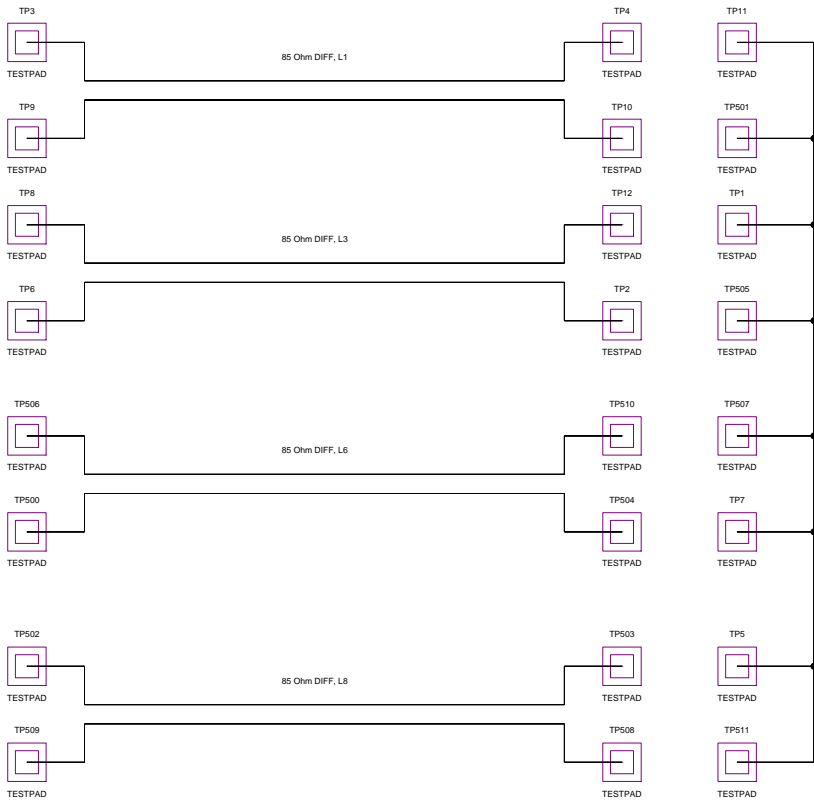
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REVISIONS

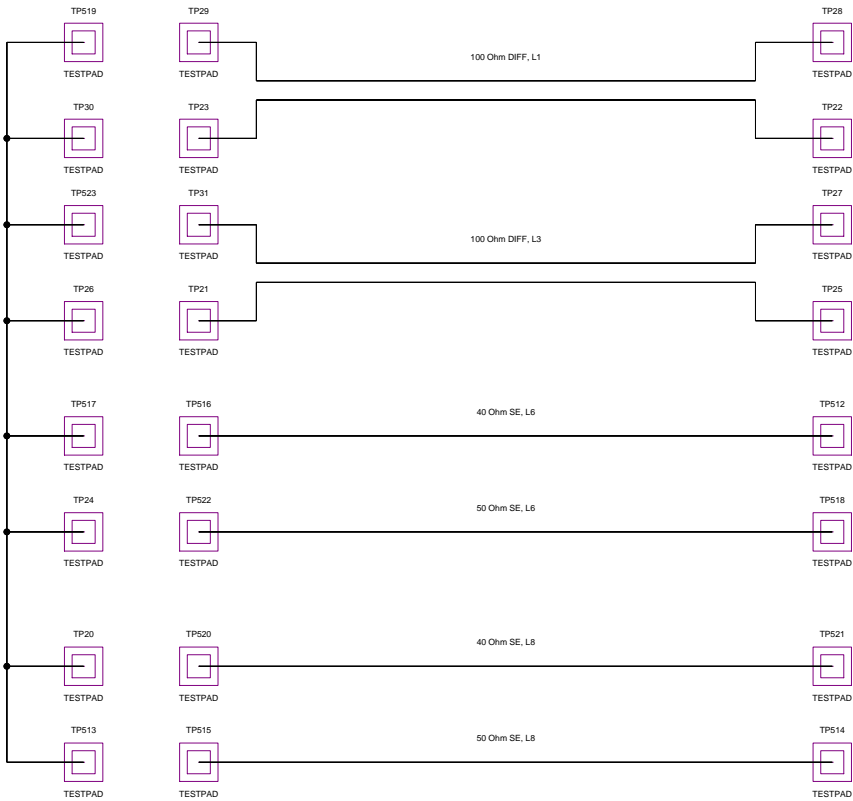
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Test coupons on panel upper cracker section
Route straight on full cracker length



Test coupons on panel lower cracker section
Route straight on full cracker length



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SIZE B	DATE 31/01/2020:09:29		
		DRAWING NO 7571 -04- 00	REV A
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