Register file structure : regfile_i2c.pdf
Created by imaval on 2020/09/03 13:59:35
Register file CRC32 : 0x5A5B9037

1. Main Parameters

Register file endianness: little endian
Address bus width: 12 bits
Data bus width: 32 bits

2. Memory Map

Section name	Address(es) / Address Ranges	Register name	Access Type
I2C	0x000	I2C_ID	R
	0x008	I2C_CTRL0	RW
	0x010	I2C_CTRL1	RW

Section: I2C

Address Range: [0x000 - 0x014]

I2C_ID

Address: section "I2C" base address + 0x000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						CLOCK_STRETCHING	NI_ACCESS
15	14	13	12	11	10	9	8
Reserved				ID(11:8)			
7	6	5	4	3	2	1	0
ID(7:0)							

CLOCK_STRETCHING		
RO	When this field is set to 1, the clock streching is supported by the I2C core.	
Possible Values:	0x0	Clock stretching not supported
	0x1	Clock stretching supported

NI_ACCESS		
RO	When this field is set to 1, write to I2C device without address cycle is supported	
Possible Values:	0x0	Write to I2C device without address cycle is NOT supported
	0x1	Write to I2C device without address cycle is supported

ID (11:0)	
STATIC	
Value at Reset:	0x012C

I2C_CTRL0 I2C Control Register 0

Address: section "I2C" base address + 0x008

31	30	29	28	27	26	25	24
I2C_INDEX(7:0)							
23	22	21	20	19	18	17	16
NI_ACC	Reserved				BUS_SEL(1:0)		TRIGGER
15	14	13	12	11	10	9	8
I2C_DATA_READ(7:0)							
7	6	5	4	3	2	1	0
I2C_DATA_WRITE(7:0)							

I2C_INDEX (7:0)	I2C Index	
RW	This is the register address in the target device	
Value at Reset:	0x0	

NI_ACC	Non Indexed I2C access	
RW	This fiels specifies if the access on the I2C bus is a Non indexed Access. This kind of access sends the Device ID and data phases without an address to the target I2C device. To DO a NI access set this bit to '1' and set the I2C_R/W bit to Read or Write, to select the operation.	
Value at Reset:	0x0	
Possible Values:	0x0	Indexed Read/write operation on I2C bus
	0x1	Non indexed Read/Write

BUS_SEL (1:0)	I2C BUS selection
STATIC	This field selects which I2C bus is targetted by the current access when Trigger is written. Note: There is a single I2C bus on this product, so this field is hardwired to 0.
Value at Reset:	0x0

TRIGGER	Trigger
WO/AutoClr	Triggers the whole access. Must be written last (or in the same access) as all the other parameters.

I2C_DATA_READ (7:0)	I2C Data Read
RO	Data read by the automatic I2C interface from the I2C_DEVICE_ID with the I2C_DEVICE_INDEX.

I2C_DATA_WRITE (7:0)	I2C Data Write
RW	Data to be written by the automatic I2C interface to the I2C_DEVICE_ID with the I2C_DEVICE_INDEX.
Value at Reset:	0x0

I2C_CTRL1 I2C Control Register 1

Address: section "I2C" base address + 0x010

31	30	29	28	27	26	25	24
Reserved			I2C_ERROR	BUSY	WRITING	READING	Reserved
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
I2C_DEVICE_ID(6:0)							I2C_RW

I2C_ERROR	Error	
RO	Specifies an error occurred during an I2C access. This bit is automatically reset by a new I2C cycle.	
Possible Values:	0x0	Normal operation
	0x1	An error Ocured

BUSY	Busy	
RO	I2C Interface is currently busy, either polling, reading or writing.	
Possible Values:	0x0	Not Currently Busy
	0x1	Currently Busy

WRITING	Writing	
RO	I2C Interface is currently writing the I2C_DEVICE_ID with the I2C_INDEX.	
Possible Values:	0x0	Not currently writing
	0x1	Currently writing

READING	Reading	
RO	I2C Interface is currently reading the I2C_DEVICE_ID with the I2C_INDEX.	
Possible Values:	0x0	Not currently reading
	0x1	Currently reading

I2C_DEVICE_ID (6:0)	I2C Device ID
RW	This is a static register that holds the 7-bit I2C_DEVICE_ID of the I2C device to be accessed.
Value at Reset:	0x44

I2C_RW	I2C Read/Write	
RW	When set, current cycle will be a read and will be a write when reset.	
Value at Reset:	0x1	
Possible Values:	0x0	Write cycle
	0x1	Read cycle