DEVICES: 28 nm DEVICE PORTFOLIO

Cyclone V FPGA Features

	Product Line	Cyclone V E FPGAs[1]					Cyclone V GX FPGAs[1]					Cyclone V GT FPGAs[1]		
		5CEA2	5CEA4	5CEA5	5CEA7	5CEA9	5CGXC3	5CGXC4	5CGXC5	5CGXC7	5CGXC9	5CGTD5	5CGTD7	5CGTD9
Resources	LEs (K)	25	49	77	149.5	301	35.5	50	77	149.5	301	77	149.5	301
	ALMs	9,434	18,480	29,080	56,480	113,560	13,460	18,868	29,080	56,480	113,560	29,080	56,480	113,560
	Registers	37,736	73,920	116,320	225,920	454,240	53,840	75,472	116,320	225,920	454,240	116,320	225,920	454,240
	M10K memory blocks	176	308	446	686	1,220	135	250	446	686	1,220	446	686	1,220
	M10K memory (Kb)	1,760	3,080	4,460	6,860	12,200	1,350	2,500	4,460	6,860	12,200	4,460	6,860	12,200
	MLAB memory (Kb)	196	303	424	836	1,717	291	295	424	836	1,717	424	836	1,717
	Variable-precision DSP blocks	25	66	150	156	342	57	70	150	156	342	150	156	342
	18 x 18 multipliers	50	132	300	312	684	114	140	300	312	684	300	312	684
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	16	16	16	16	16	16	16	16	16	16	16	16	16
	PLLs[2] (FPGA)	4	4	6	7	8	4	6	6	7	8	6	7	8
	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5,3.3												
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12, HiSpi, SLVS, Sub-LVDS												
	LVDS channels (receiver/transmitter)	56/56	56/56	60/60	120/120	120/120	52/52	84/84	84/84	120/120	140/140	84/84	120/120	140/140
	Transceiver count (3.125 Gbps)	–	–	–	–	–	3	6	6	9	12	–	–	–
	Transceiver count (6.144 Gbps)[3]	–	–	–	–	–	–	–	–	–	–	6[4]	9[4]	12[4]
	PCIe hardened IP blocks (Gen1)[5]	–	–	–	–	–	1	2	2	2	2	–	–	–
	PCIe hardened IP blocks (Gen2)	–	–	–	–	–	–	–	–	–	–	2	2	2
	Hard memory controllers[6] (FPGA)	1	1	2	2	2	1	2	2	2	2	2	2	2
	Memory devices supported	DDR3, DDR2, LPDDR2												
Package Options and I/O Pins: GPIO Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count														
M301 pin (11 mm, 0.5 mm pitch)								129 4	129 4			129 4		
M383 pin (13 mm, 0.5 mm pitch)		223	223	175				175 6	175 6			175 6		
M484 pin (15 mm, 0.5 mm pitch)					240					240 3			240 3	
U324 pin (15 mm, 0.8 mm pitch		176	176				144 3							
U484 pin (19 mm, 0.8 mm pitch)		224	224	224	240	240	208 3	224 6	224 6	240 6	240 5	224 6	240 6	240 5
F256 pin (17 mm, 1.0 mm pitch)		128	128											
F484 pin (23 mm, 1.0 mm pitch)		224	224	240	240	224	208 3	240 6	240 6	240 6	224 6	240 6	240 6	224 6
F672 pin (27 mm, 1.0 mm pitch					336	336		336 6	336 6	336 9	336 9	336 6	336 9	336 9
F896 pin (31 mm, 1.0 mm pitch					480	480				480 9	480 12		480 9	480 12
F1152 pin (35 mm, 1.0 mm pitch											560 12			560 12

Notes:

1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.altera.com.
2. The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.
3. Automotive grade Cyclone V GT FPGAs include a 5 Gbps transceiver.
4. Transceiver counts shown are for ≤ 5 Gbps. The 6 Gbps channel count support depends on package and channel usage. Refer to Cyclone V Device Handbook Volume 2: Transceivers for guidelines.
5. One PCIe hard IP block in U672 package.
6. Includes 16 and 32 bit error correction code ECC support.

129 / 4 — Values on top indicate available user I/O pins; values at the bottom indicate the 3.125 Gbps, 5 Gbps, or 6.144 Gbps transceiver count.

Pin migration (same V_{CC}, GND, ISP, and input pins). User I/O pins may be less than labelled for pin migration.

For FPGAs: Pin migration is only possible if you use only up to 175 GPIOs.

DEVICES: 28 nm DEVICE PORTFOLIO

Cyclone V SoC Features

	Product Line	Cyclone V SE SoCs[1]				Cyclone V SX SoCs[1]				Cyclone V ST SoCs[1]	
		5CSEA2	5CSEA4	5CSEA5	5CSEA6	5CSXC2	5CSXC4	5CSXC5	5CSXC6	5CSTD5	5CSTD6
Resources	LEs (K)	25	40	85	110	25	40	85	110	85	110
	ALMs	9,434	15,094	32,075	41,509	9,434	15,094	32,075	41,509	32,075	41,509
	Registers	37,736	60,376	128,300	166,036	37,736	60,376	128,300	166,036	128,300	166,036
	M10K memory blocks	140	270	397	557	140	270	397	557	397	557
	M10K memory (Kb)	1,400	2,700	3,970	5,570	1,400	2,700	3,970	5,570	3,970	5,570
	MLAB memory (Kb)	138	231	480	621	138	231	480	621	480	621
	Variable-precision DSP blocks	36	84	87	112	36	84	87	112	87	112
	18 x 18 multipliers	72	168	174	224	72	168	174	224	174	224
Clocks, Maximum I/O Pins, and Architectural Features	Processor cores (ARM Cortex-A9)	Single or dual	Single or dual	Single or dual	Single or dual	Dual	Dual	Dual	Dual	Dual	Dual
	Maximum CPU clock frequency (MHz)	925	925	925	925	925	925	925	925	925	925
	Global clock networks	16	16	16	16	16	16	16	16	16	16
	PLLs[2] (FPGA)	5	5	6	6	5	5	6	6	6	6
	PLLs (HPS)	3	3	3	3	3	3	3	3	3	3
	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5,3.3									
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12, HiSpi, SLVS, Sub-LVDS									
	LVDS channels (receiver/transmitter)	37/32	37/32	72/72	72/72	37/32	37/32	72/72	72/72	72/72	72/72
	Transceiver count (3.125 Gbps)	–	–	–	–	6	6	9	9	–	–
	Transceiver count (6.144 Gbps)[3]	–	–	–	–	–	–	–	–	9[4]	9[4]
	PCIe hardened IP blocks (Gen1)[5]	–	–	–	–	2	2	2	2	–	–
	PCIe hardened IP blocks (Gen2)	–	–	–	–	–	–	–	–	2	2
	GPIOs (FPGA)	145	145	288	288	145	145	288	288	288	288
	GPIOs (HPS)	181	181	181	181	181	181	181	181	181	181
	Hard memory controllers[6] (FPGA)	1	1	1	1	1	1	1	1	1	1
	Hard memory controllers[6] (HPS)	1	1	1	1	1	1	1	1	1	1
	Memory devices supported	DDR3, DDR2, LPDDR2									
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count											
	U484 pin (19 mm, 0.8 mm pitch)	66, 151 0	66, 151 0	66, 151 0	66, 151 0						
	U672 pin (23 mm, 0.8 mm pitch)	145, 181 0	145, 181 0	145, 181 0	145, 181 0	145, 181 6	145, 181 6	145, 181 6	145, 181 6		
	F896 pin (31 mm, 1.0 mm pitch			288, 181 0	288, 181 0			288, 181 9	288, 181 9	288, 181 9	288, 181 9

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3. Automotive grade Cyclone V GT FPGAs include a 5 Gbps transceiver.
4. Transceiver counts shown are for ≤ 5 Gbps.
   The 6 Gbps channel count support depends on package and channel usage.
   Refer to Cyclone V Device Handbook Volume 2: Transceivers for guidelines.
5. One PCIe hard IP block in U672 package.
6. With 16 and 32 bit ECC support.

66, 151 / 0 — Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 3.125 Gbps or 5 Gbps transceiver count.

Pin migration (same V_{cc}, GND, ISP, and input pins). User I/O pins may be less than labelled for pin migration.

For SoCs: Pin migration is only possible if you use only up to 138 GPIOs.