

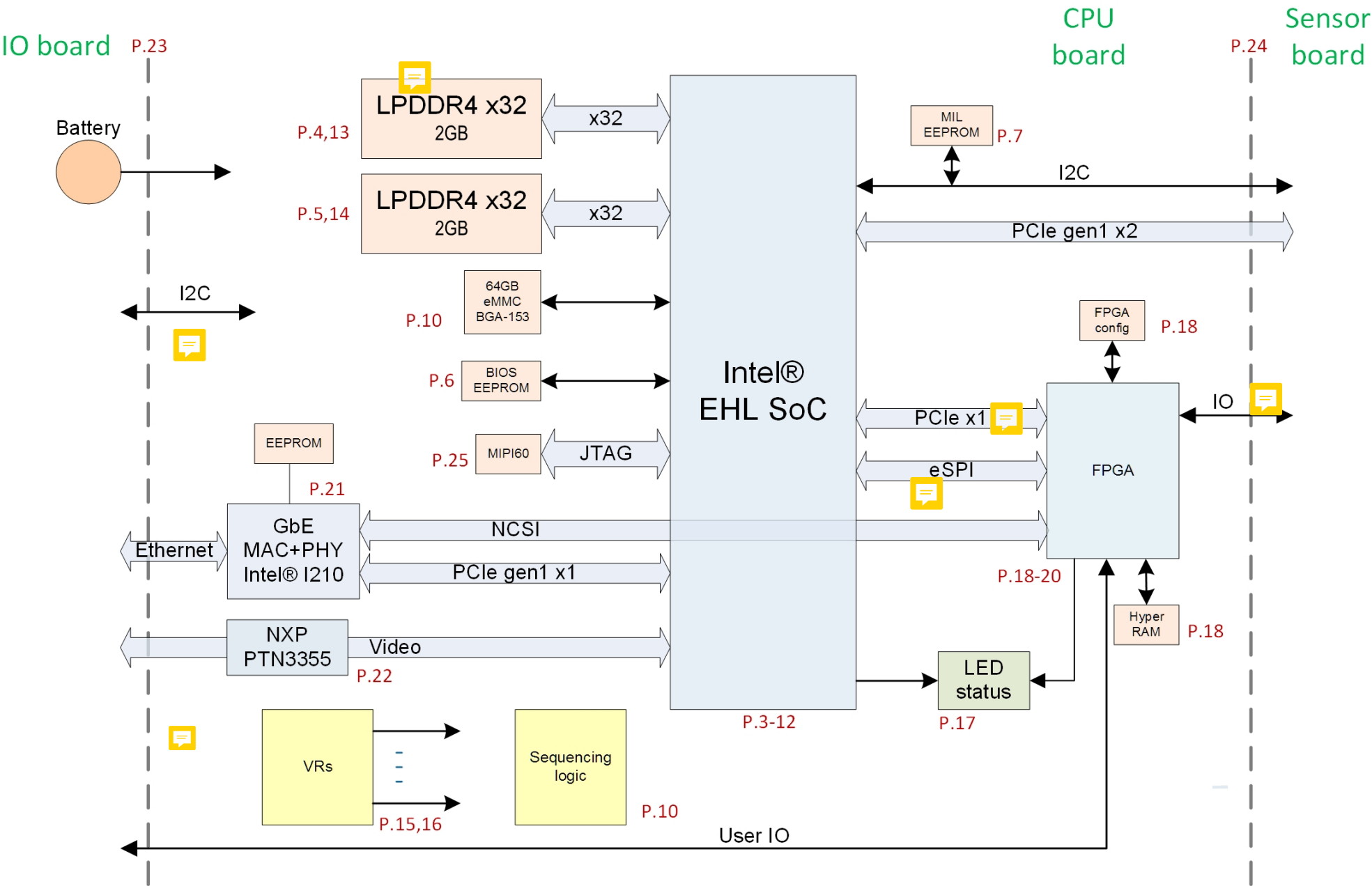
IRIS4 CPU Board


REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

MATROX CONFIDENTIAL

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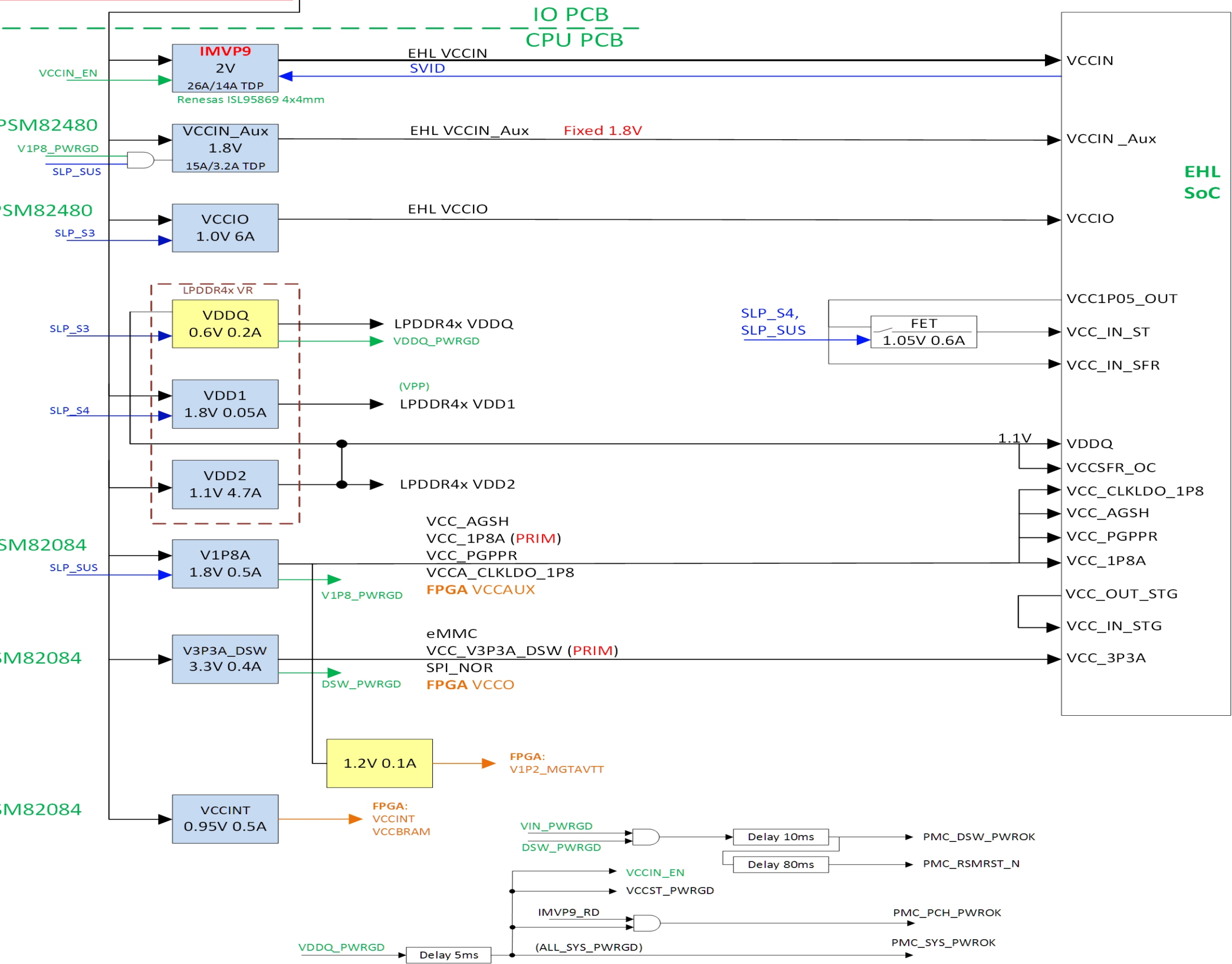
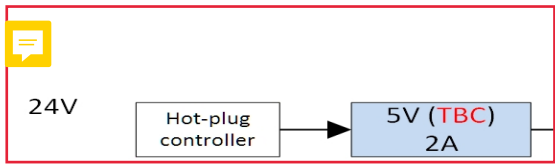
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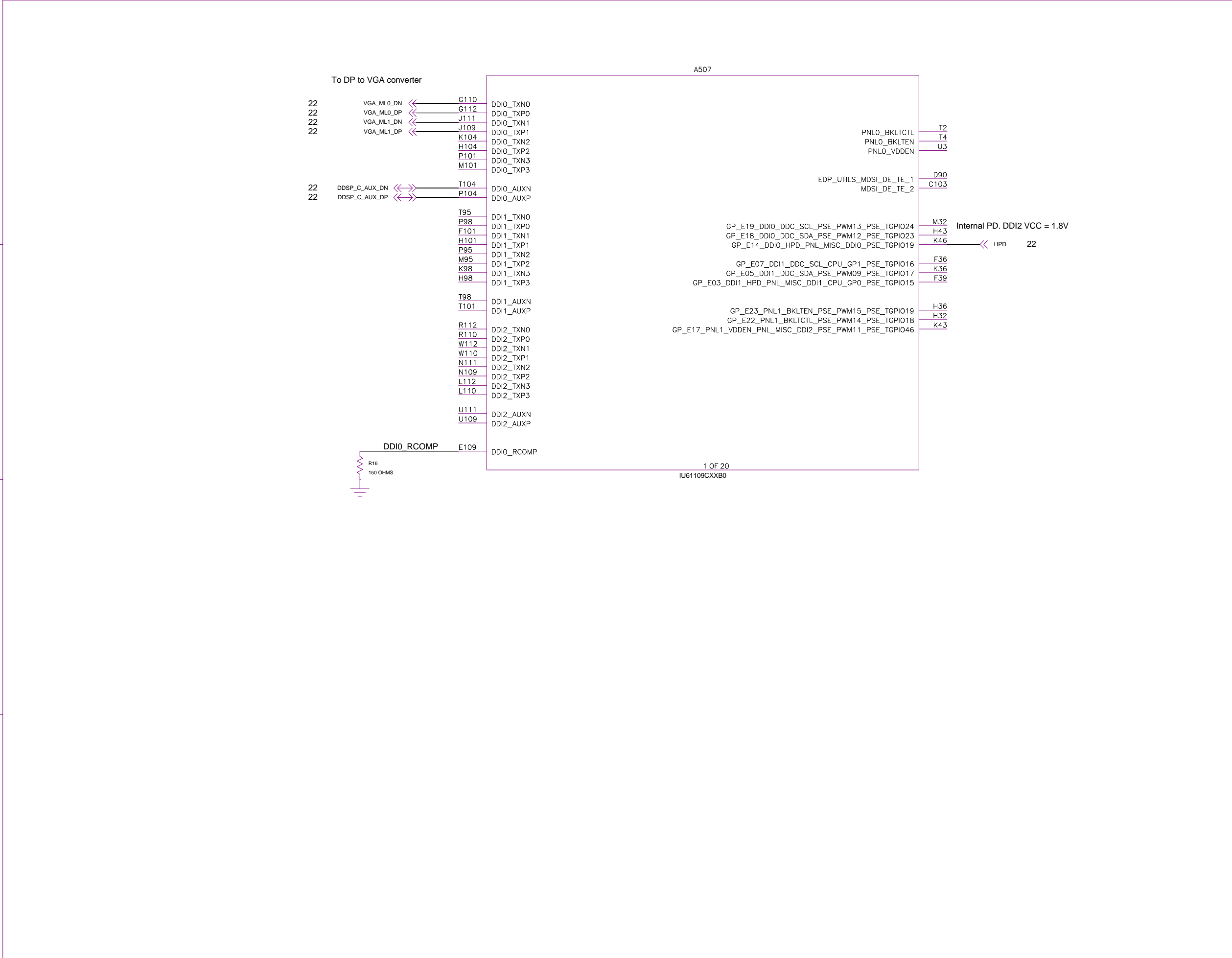
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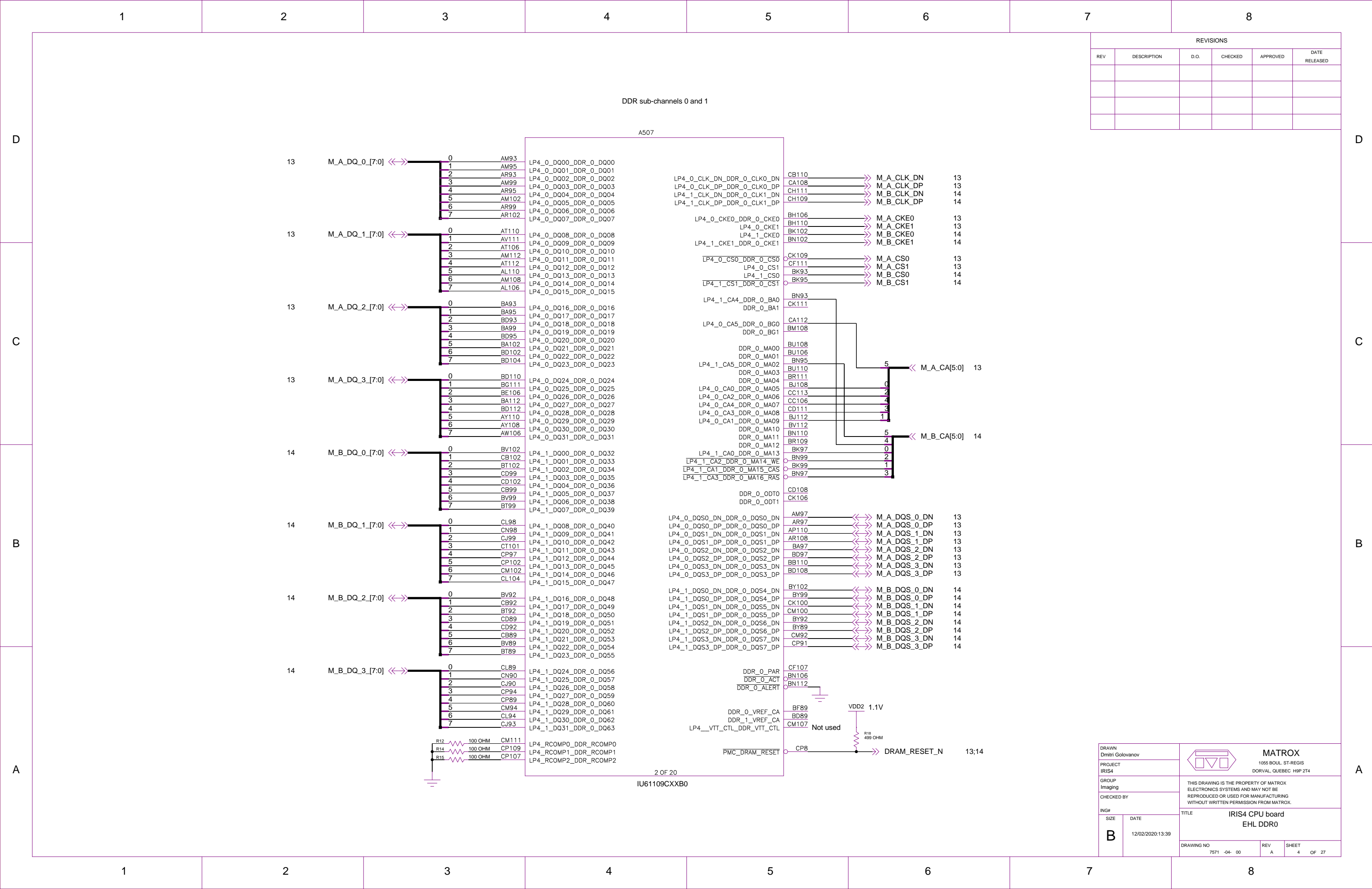
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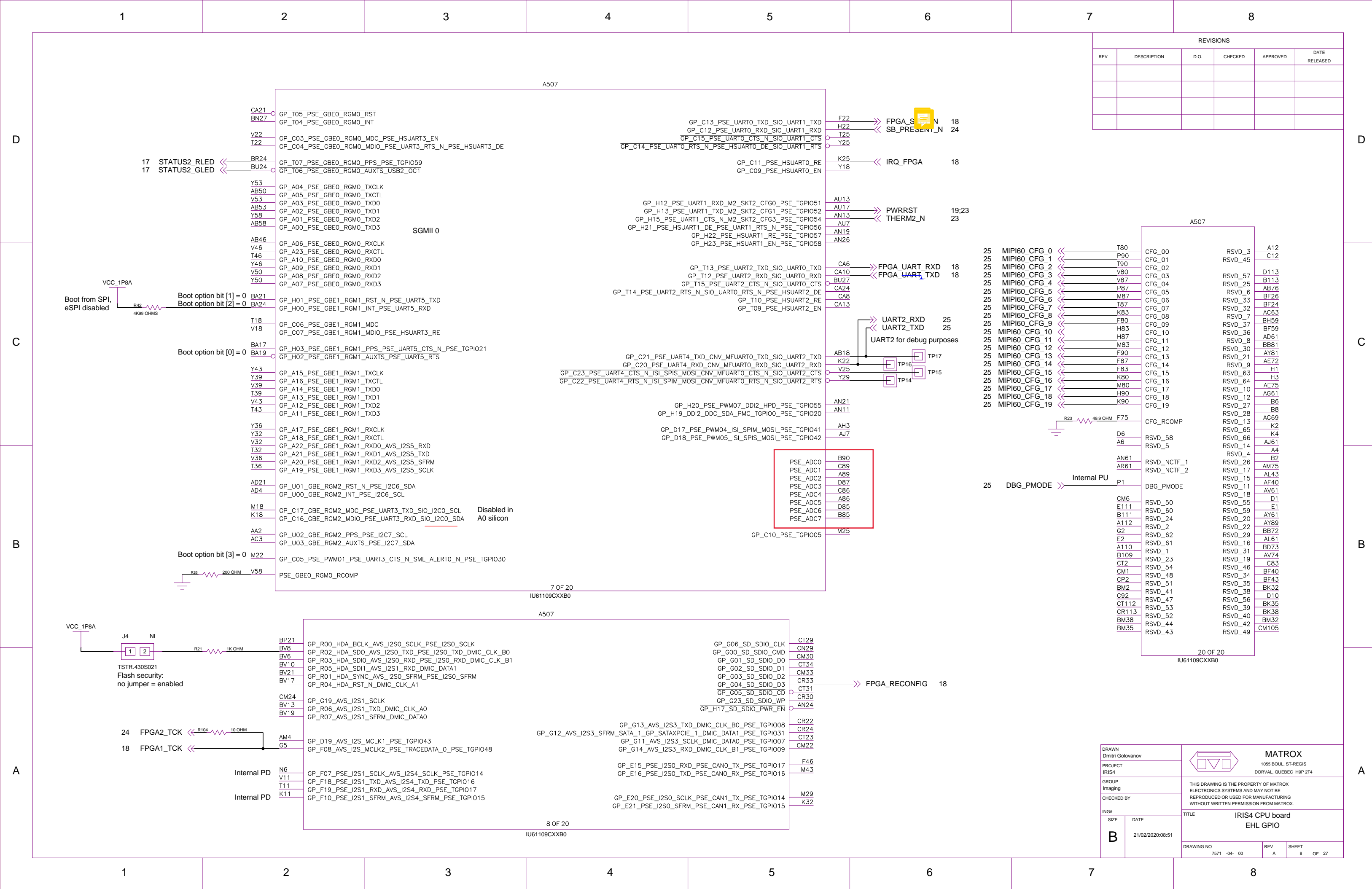






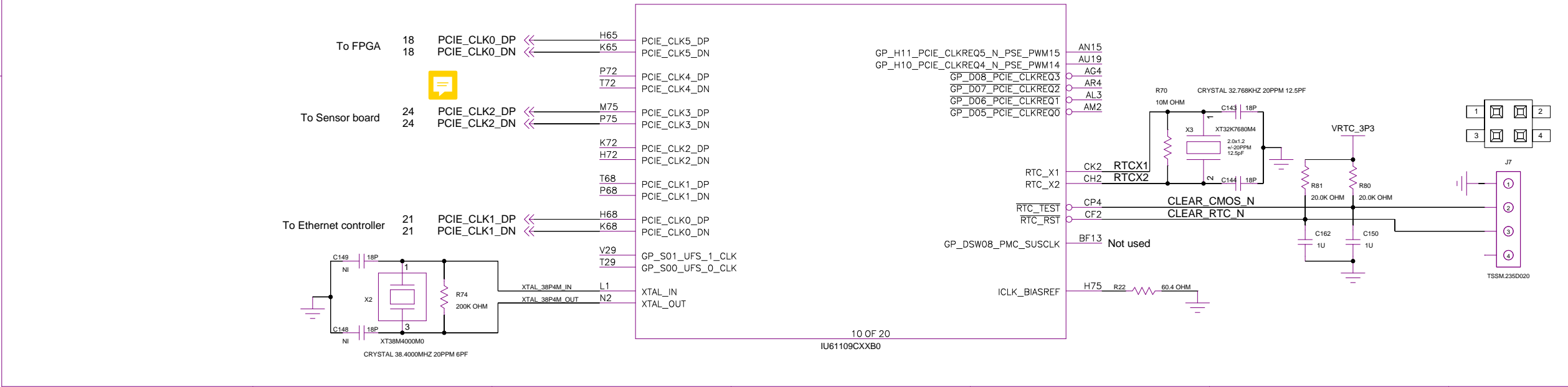
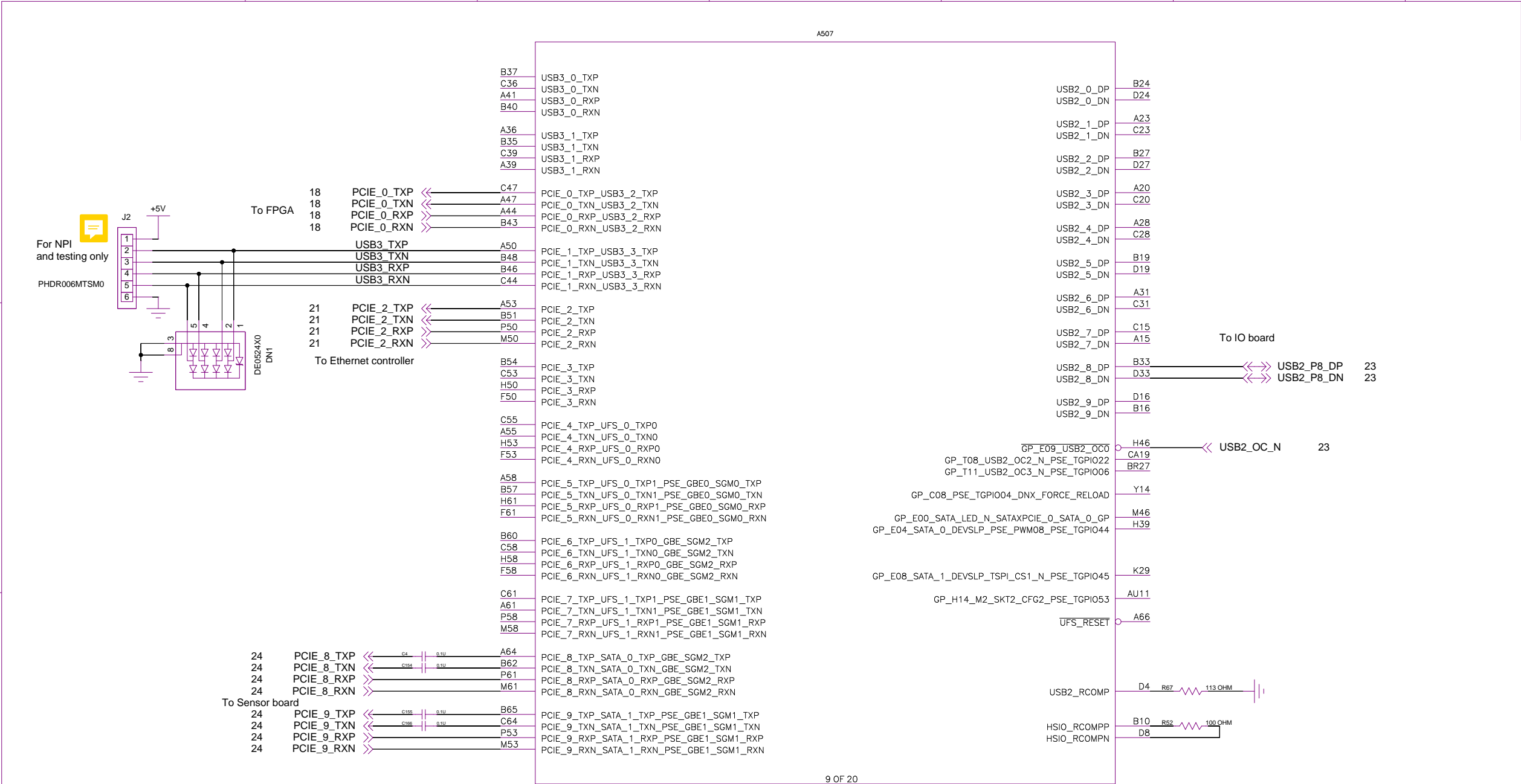







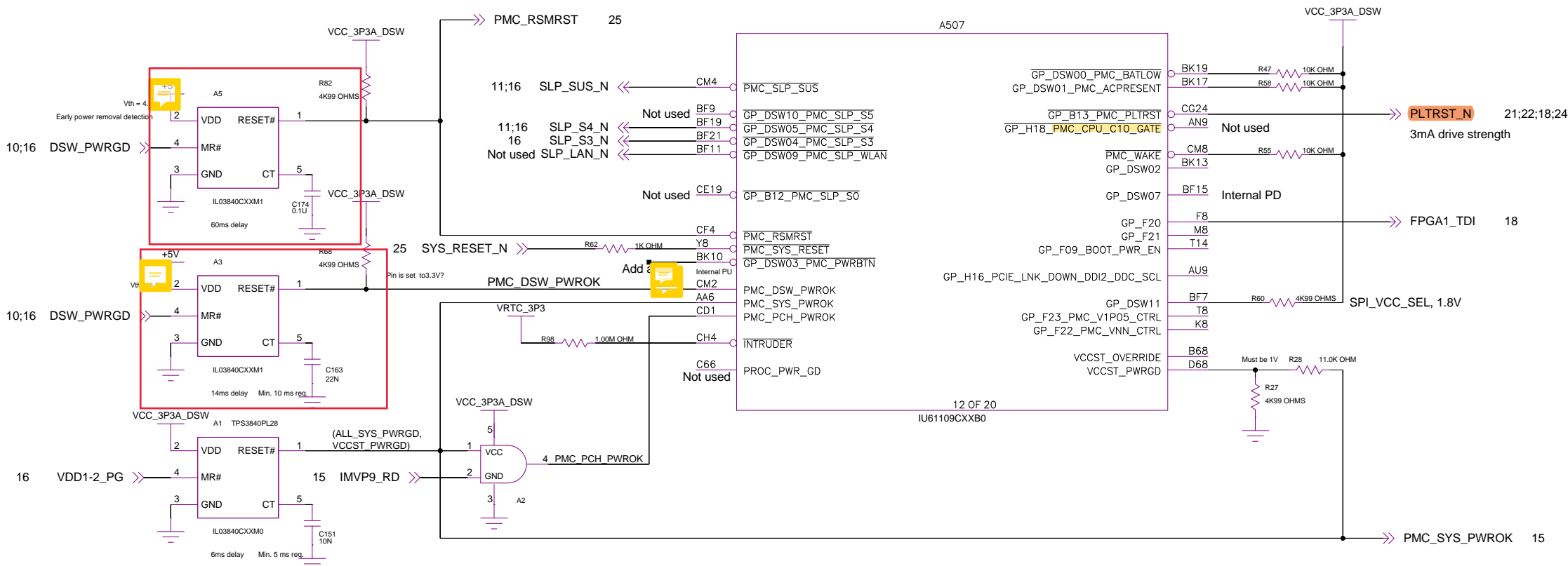
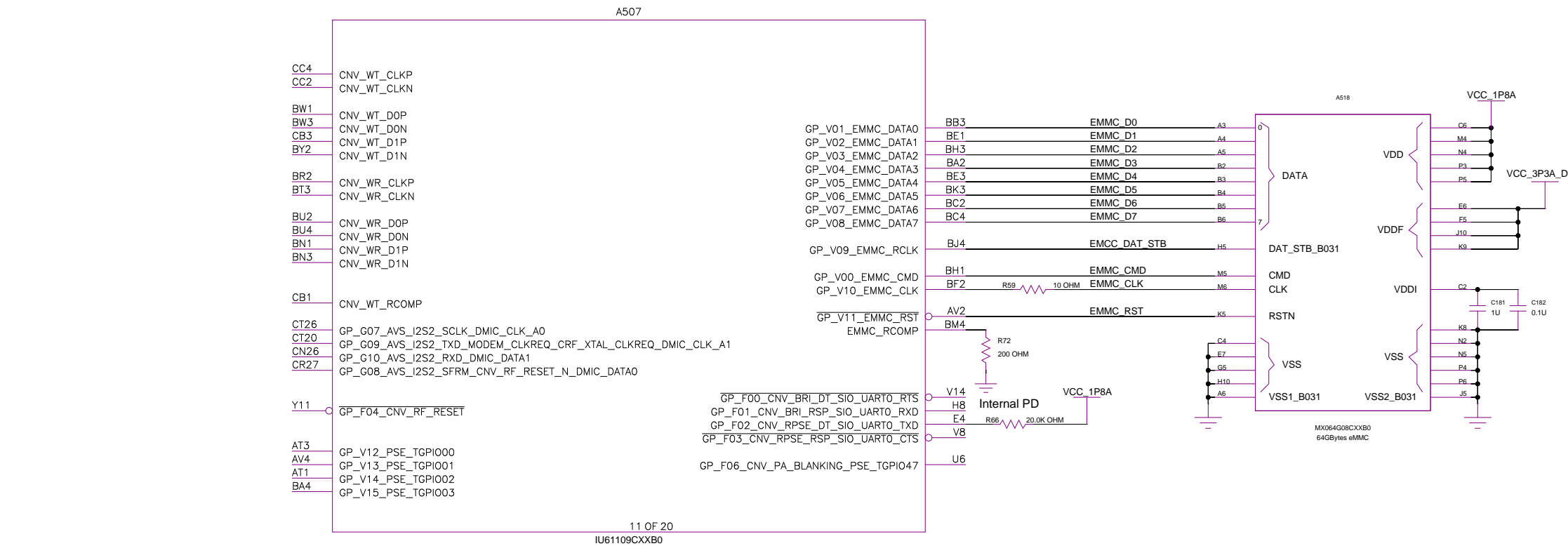



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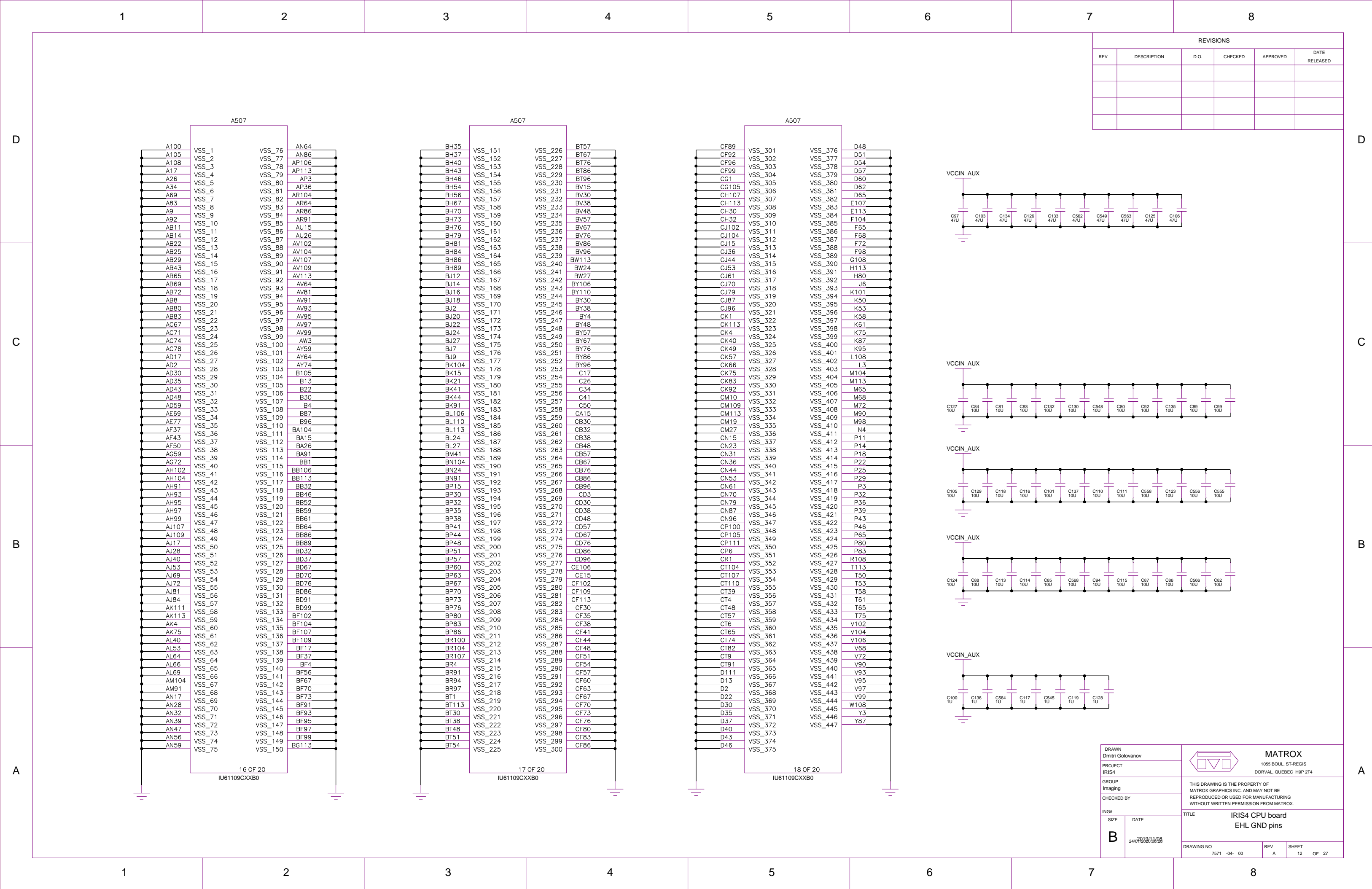
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SIZE  <b>B</b>	DATE  21/02/2020:08:18	7571 -04- 00	REV A
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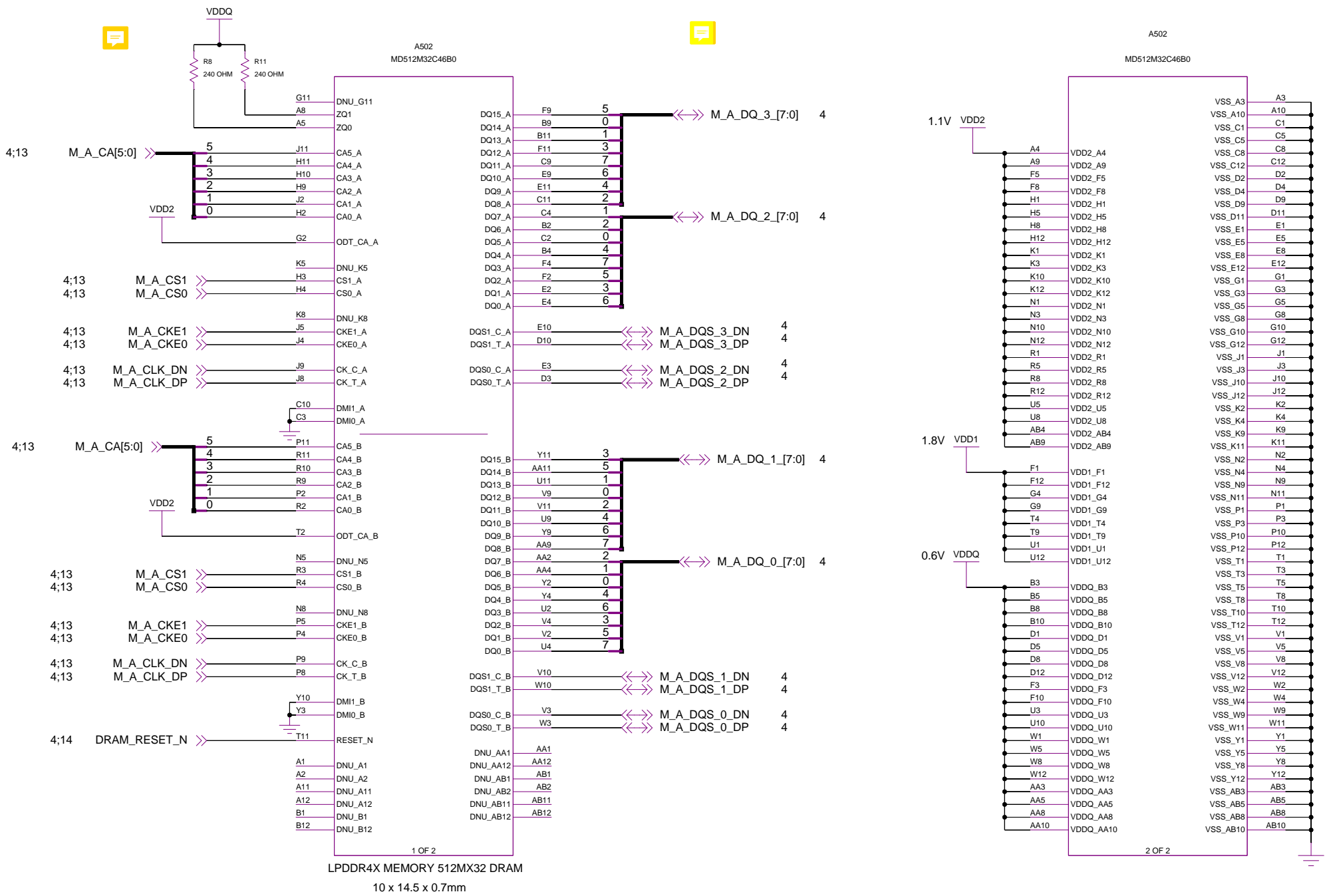



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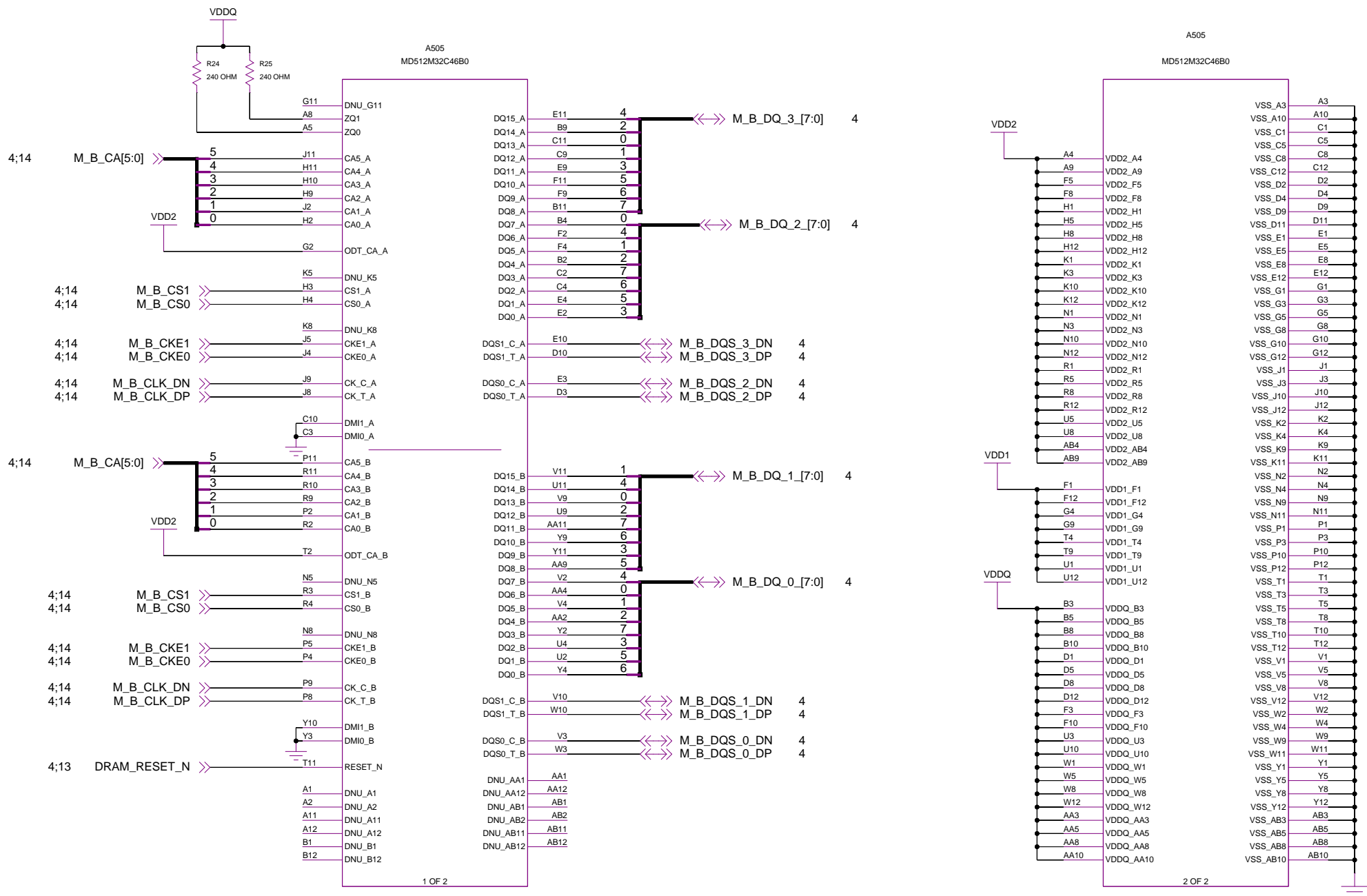
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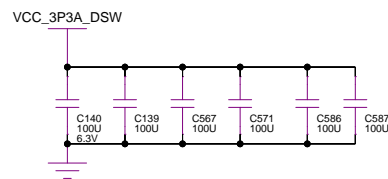


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GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
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SIZE <div>B</div>	DATE 12/02/2020:13:39	DRAWING NO 7571 -04- 00	
		REV A	SHEET 14 OF 27





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DRAWING NO  7571 -04- 00		REV  A	SHEET  16 OF 27



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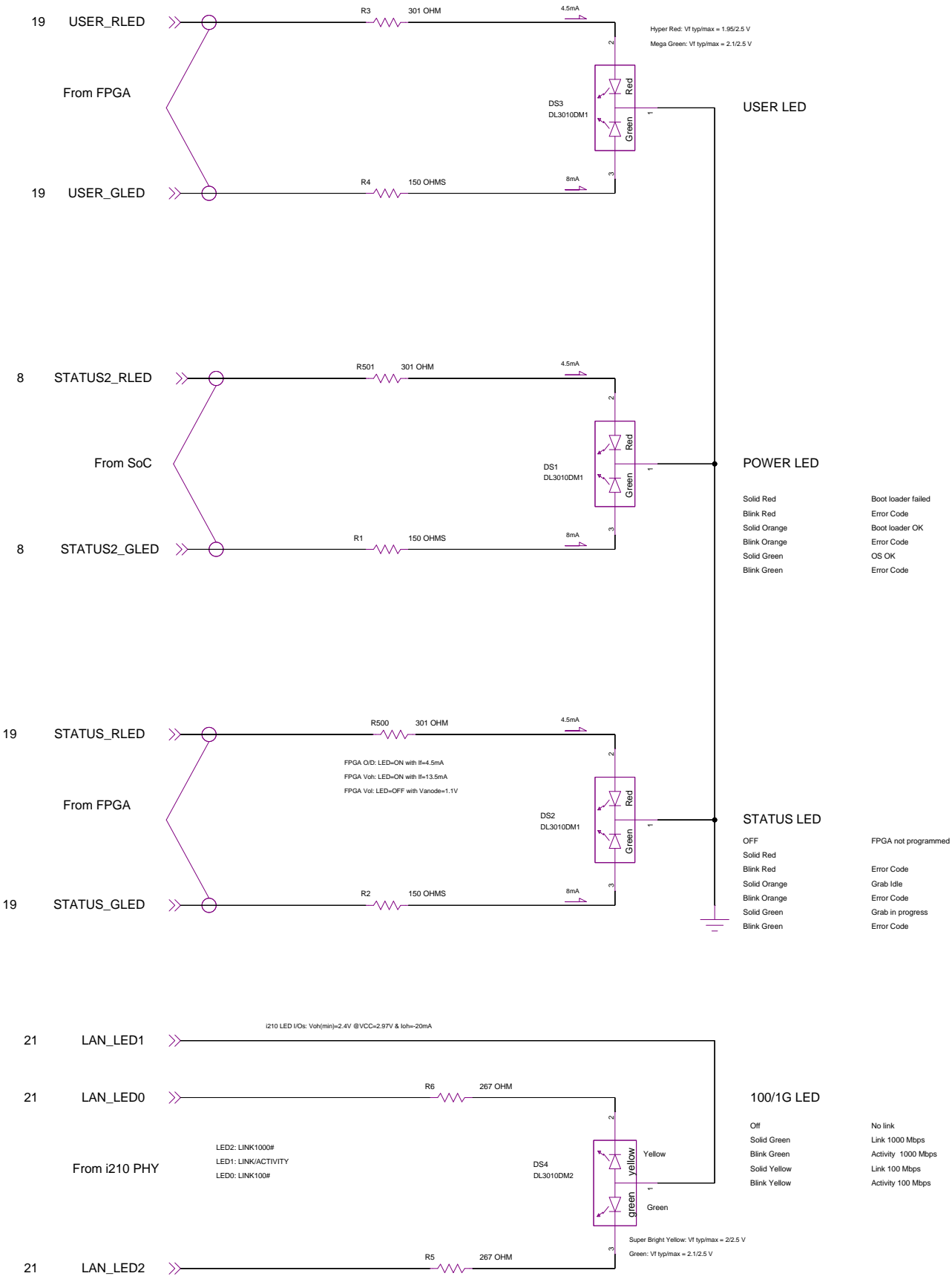
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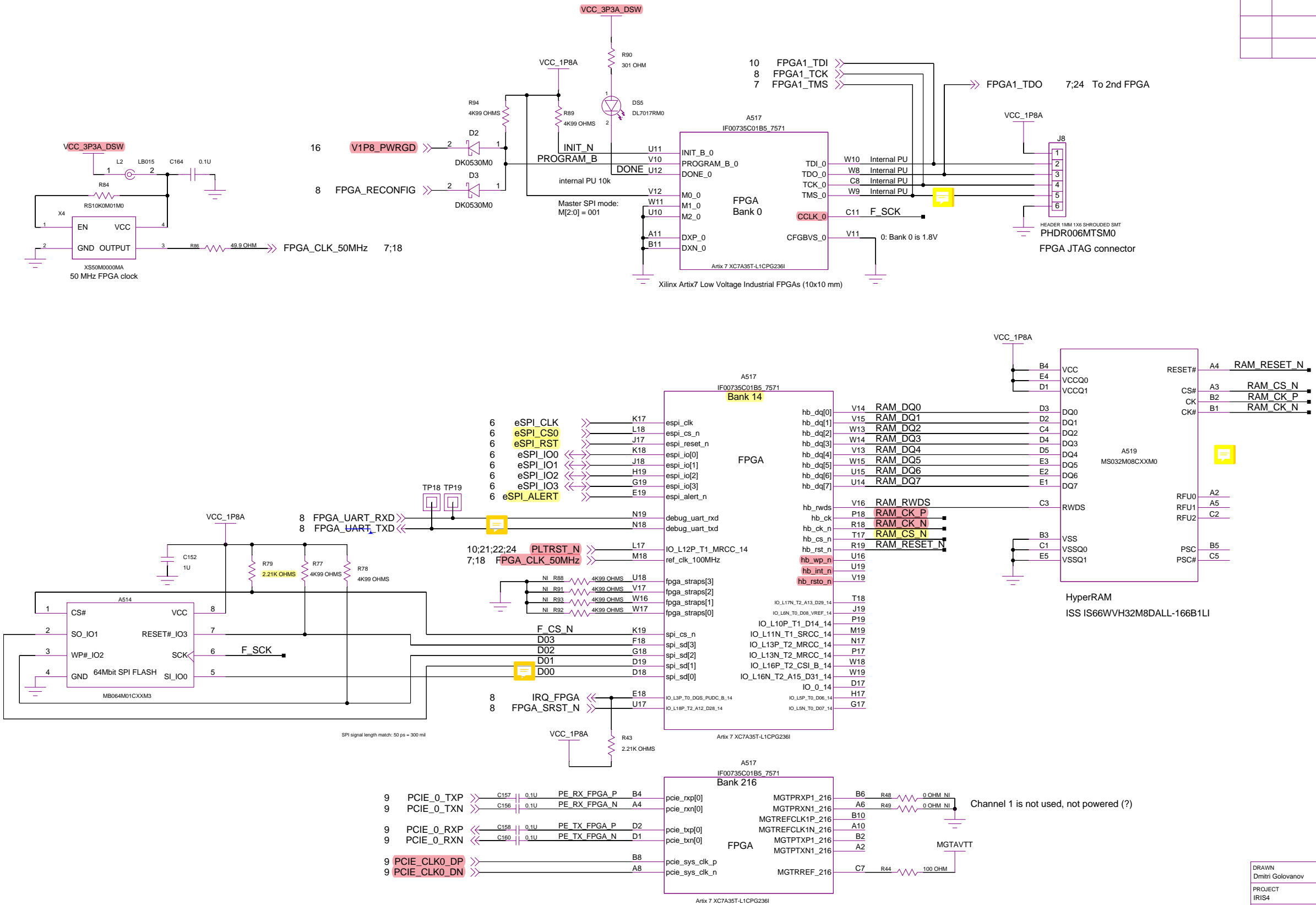
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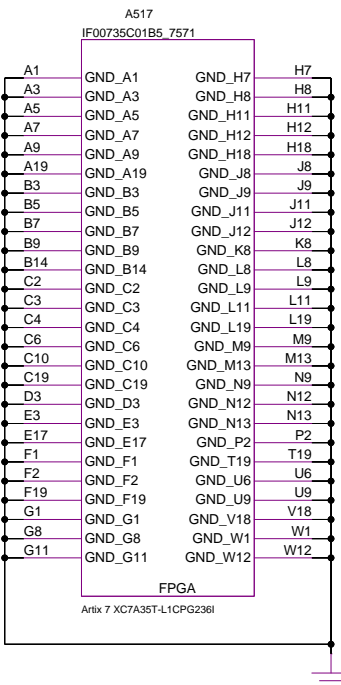
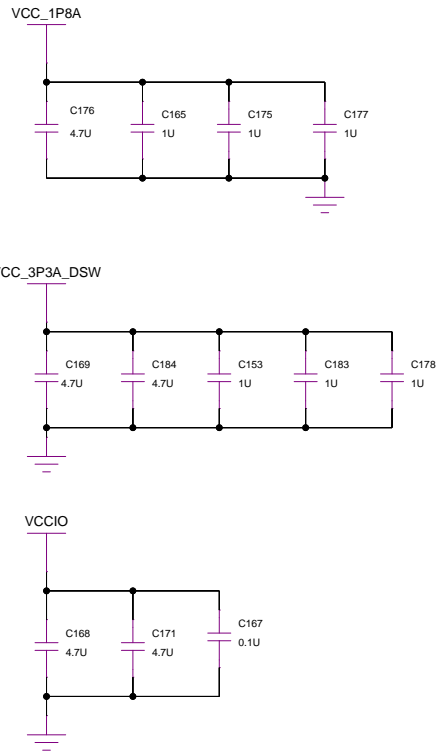
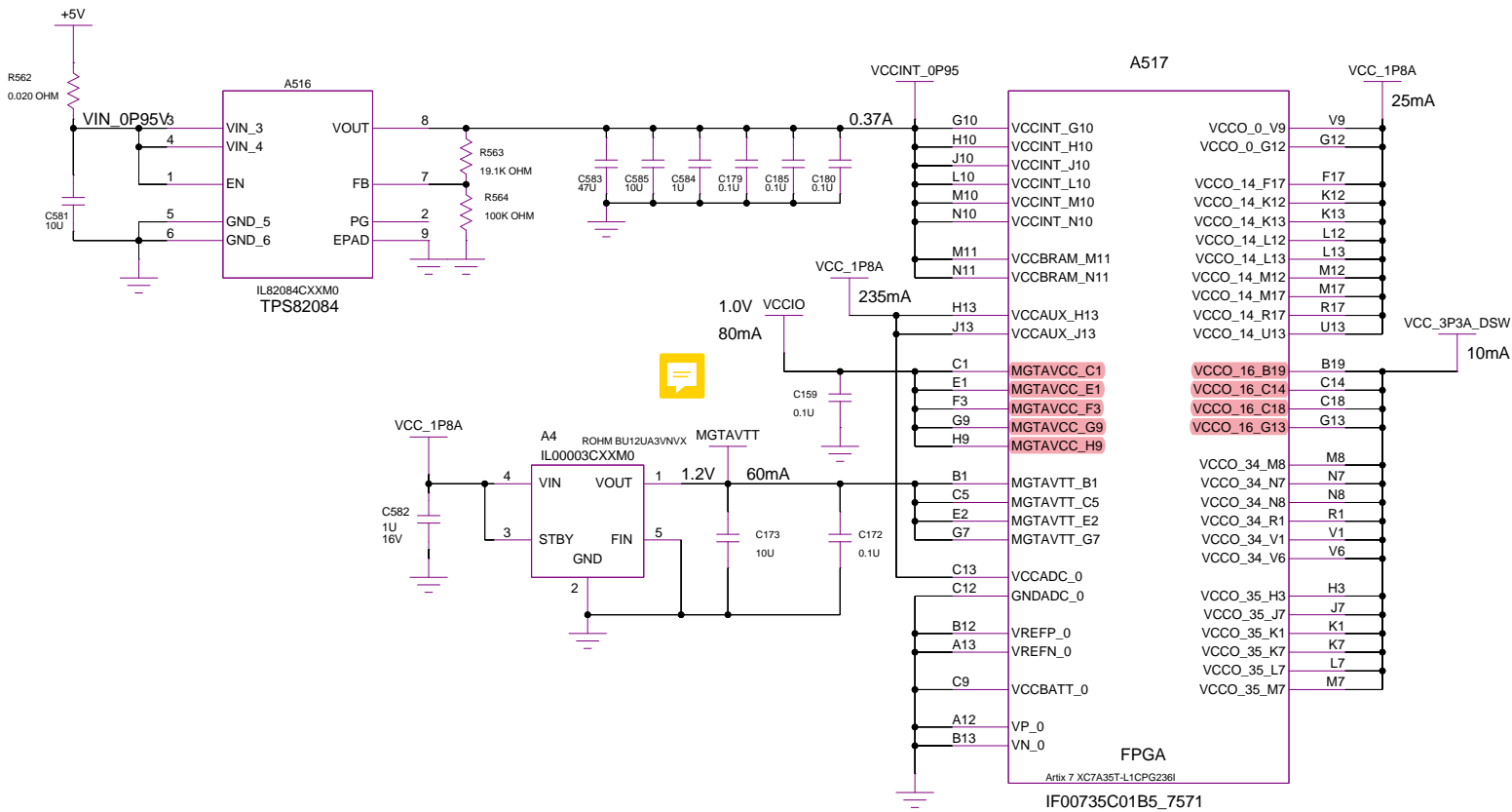
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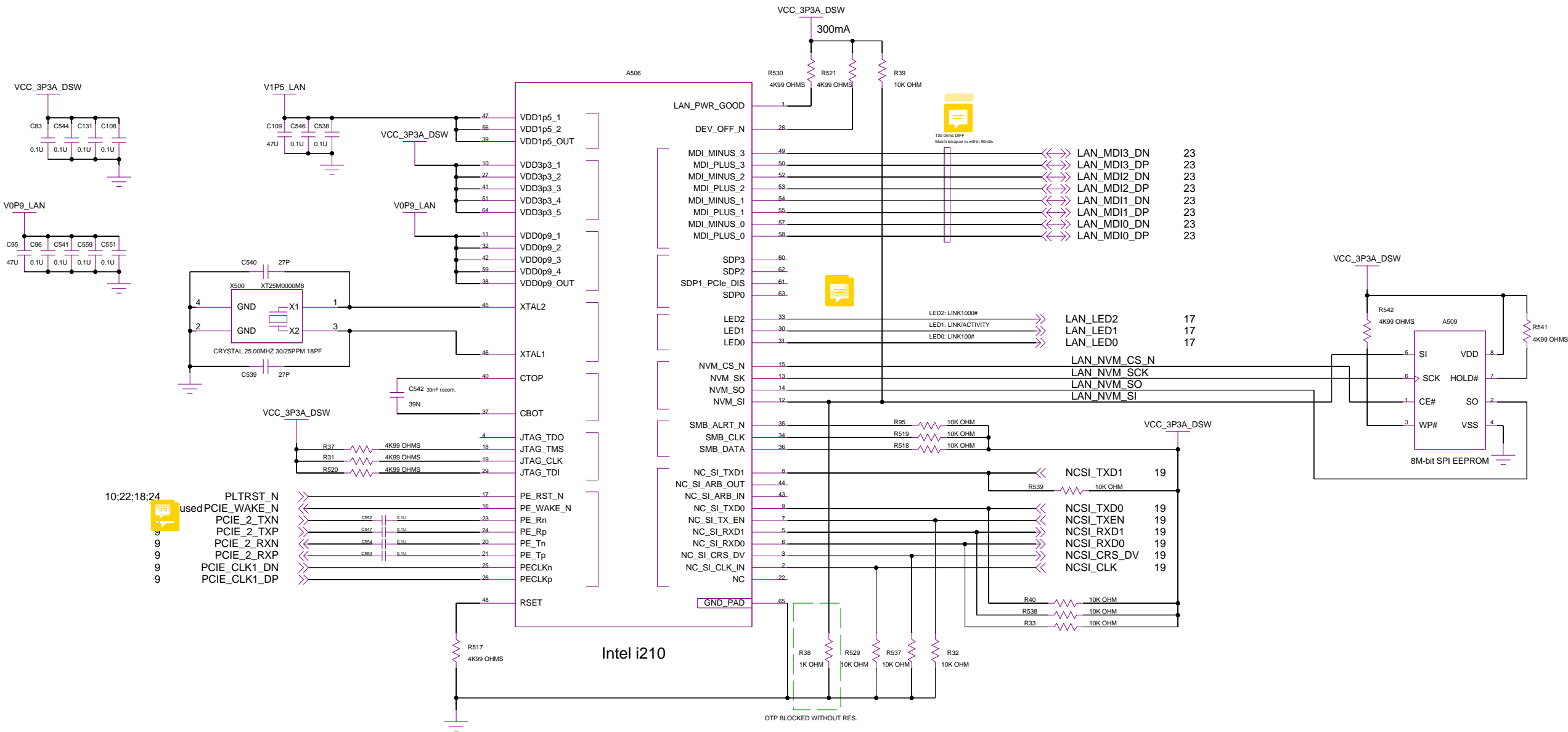
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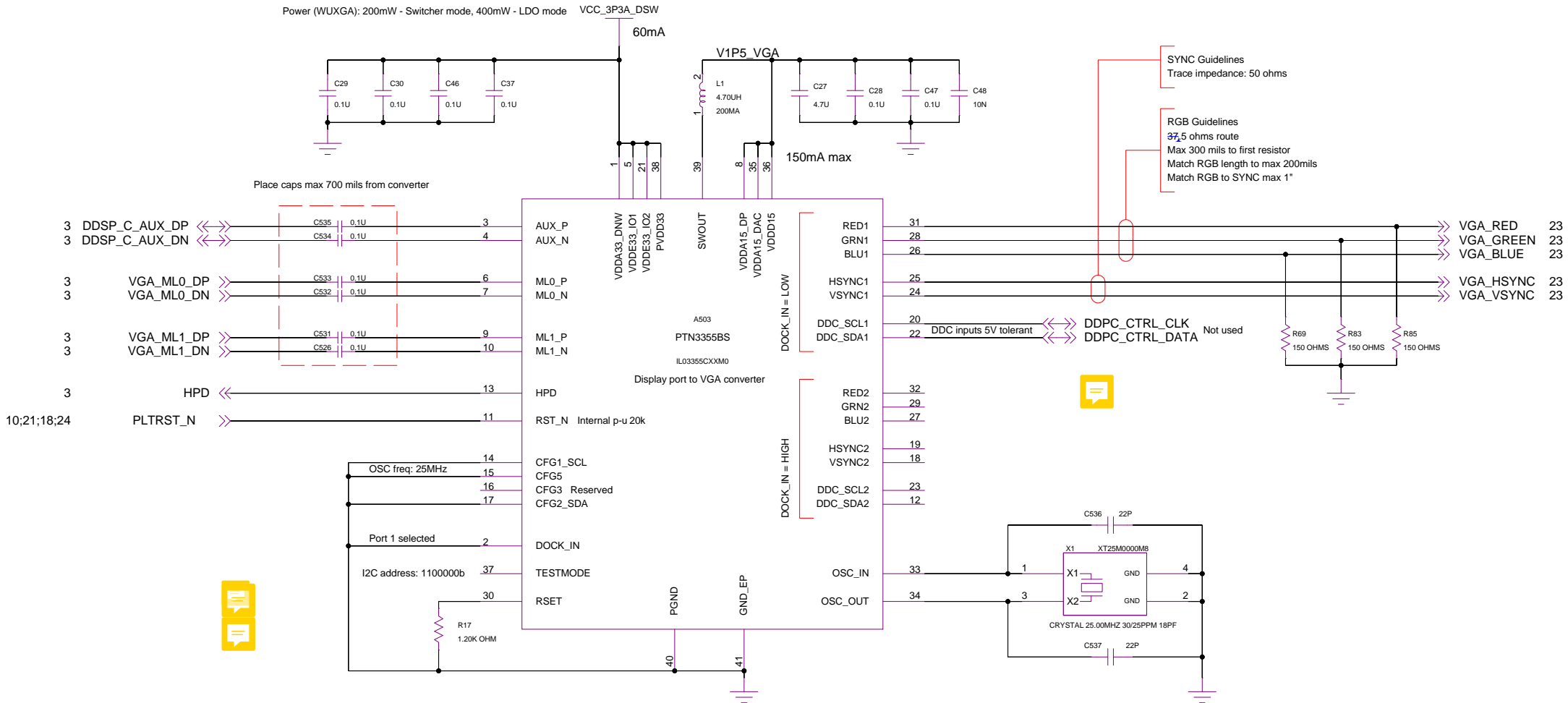
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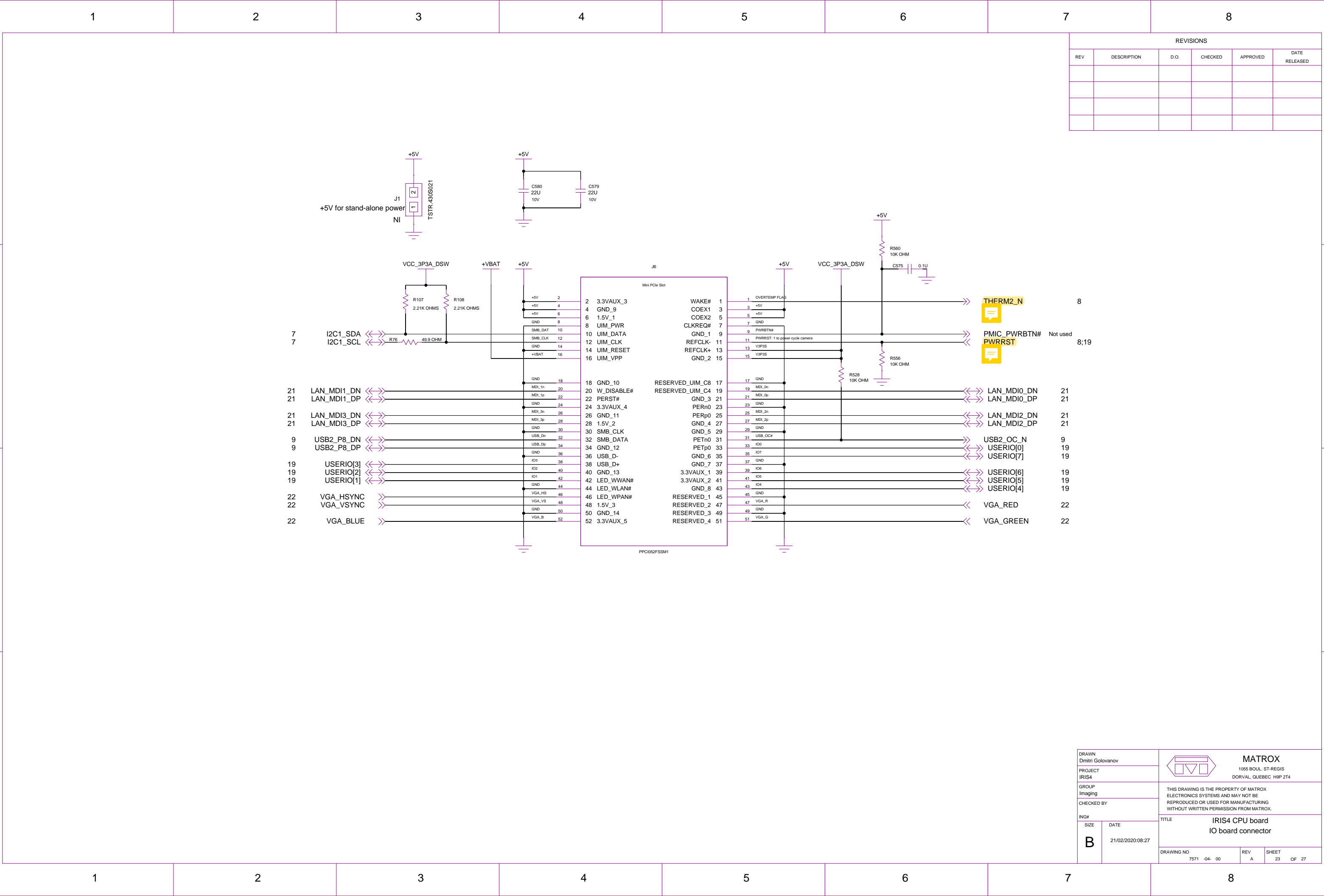
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		REV A	SHEET 23 OF 27

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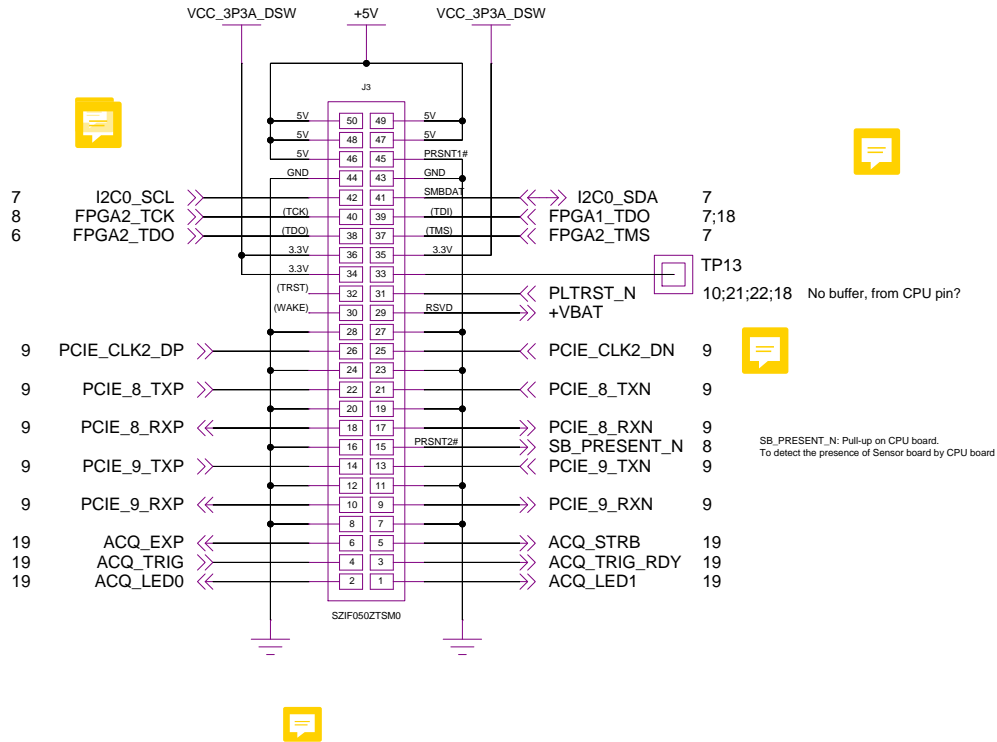
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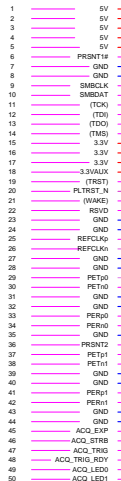
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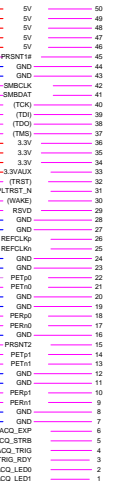
CPU Board ZIF pinout is inverted  
Sensor board pos 1 aligned with CPU board pos 50  
Connectors are head-to-head with latch on same side




Sensor board connector



CPU board connector



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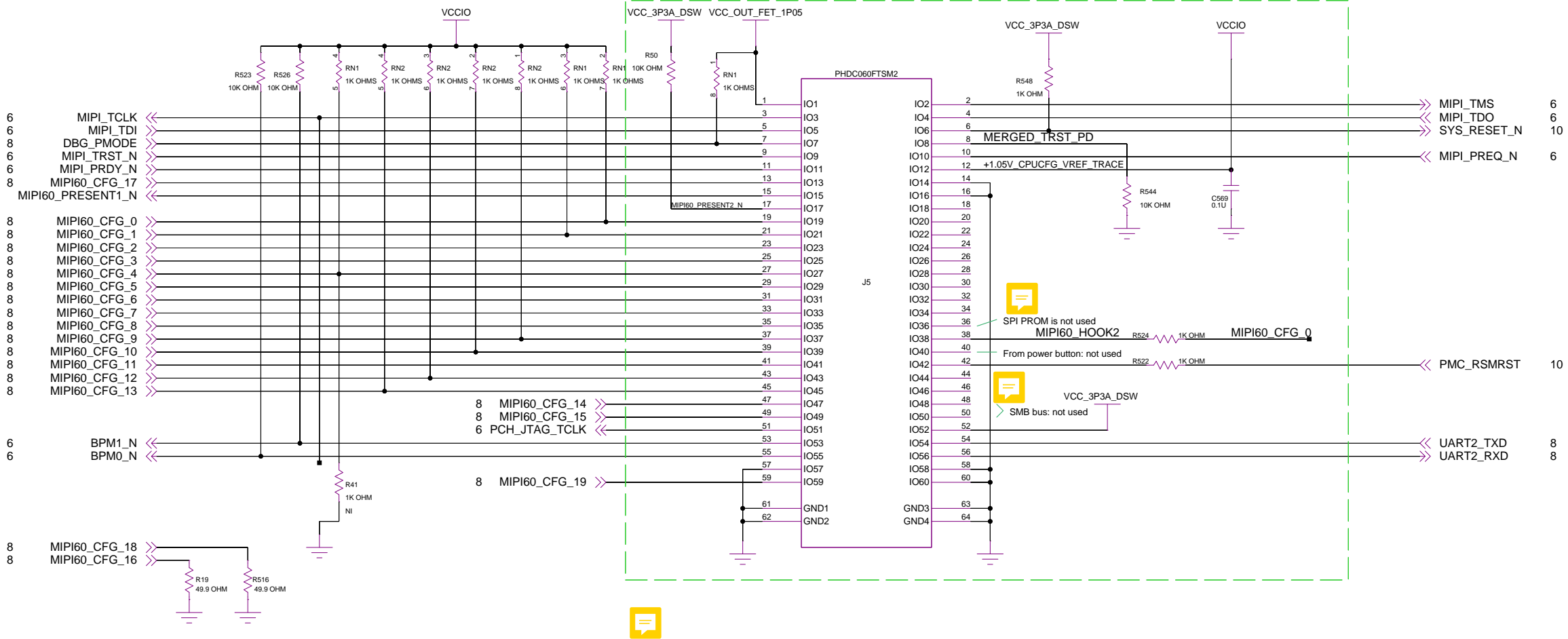
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The MIPI 60 debug connector could be implemented on a break-away extension of the PCB, on prototype version only.  
In this case, all components inside this outline will be disconnected from EHL SoC pins on production revision



SUB=XDP

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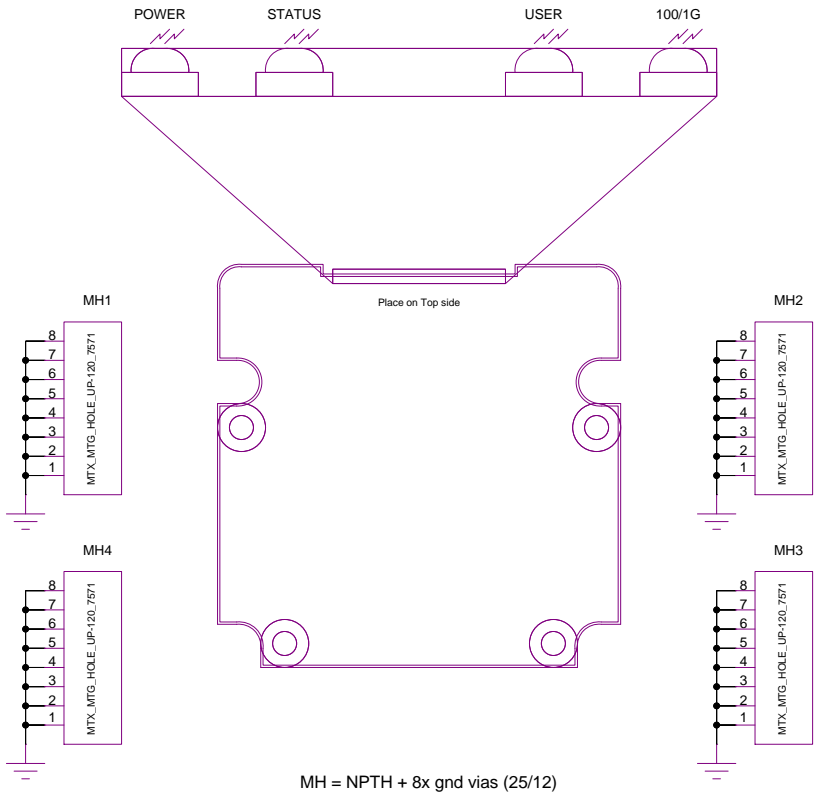
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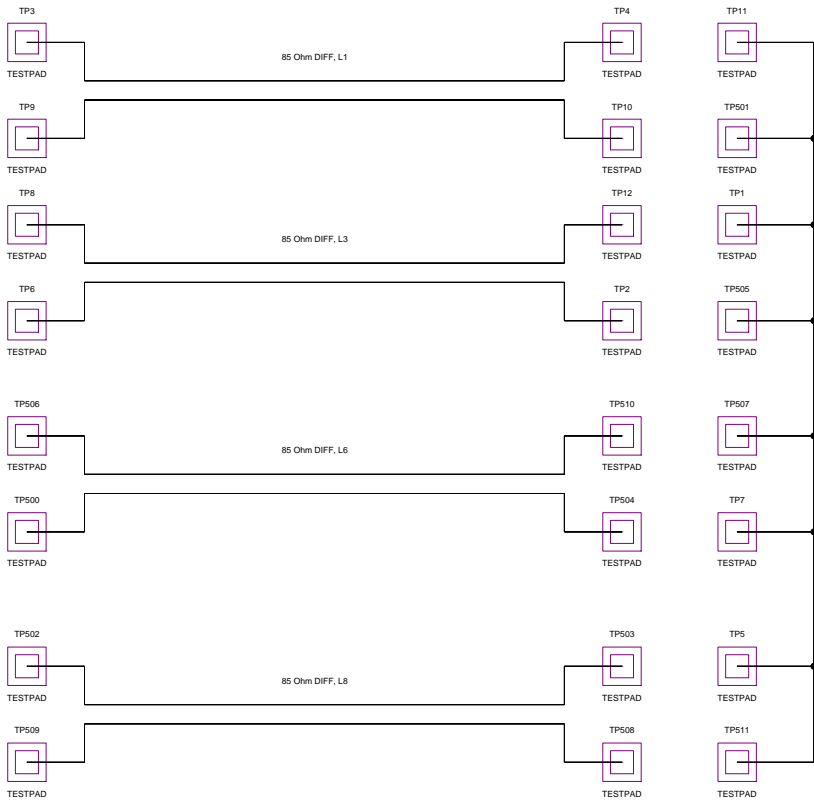
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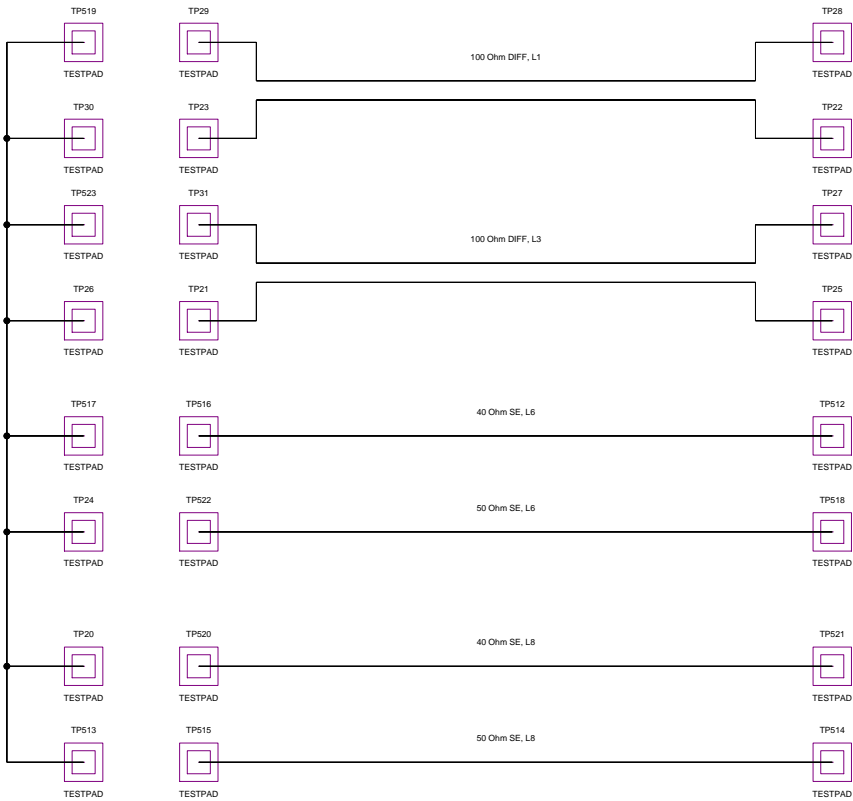
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Test coupons on panel upper cracker section  
Route straight on full cracker length



Test coupons on panel lower cracker section  
Route straight on full cracker length



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