IRIS3 ByT CPU Board

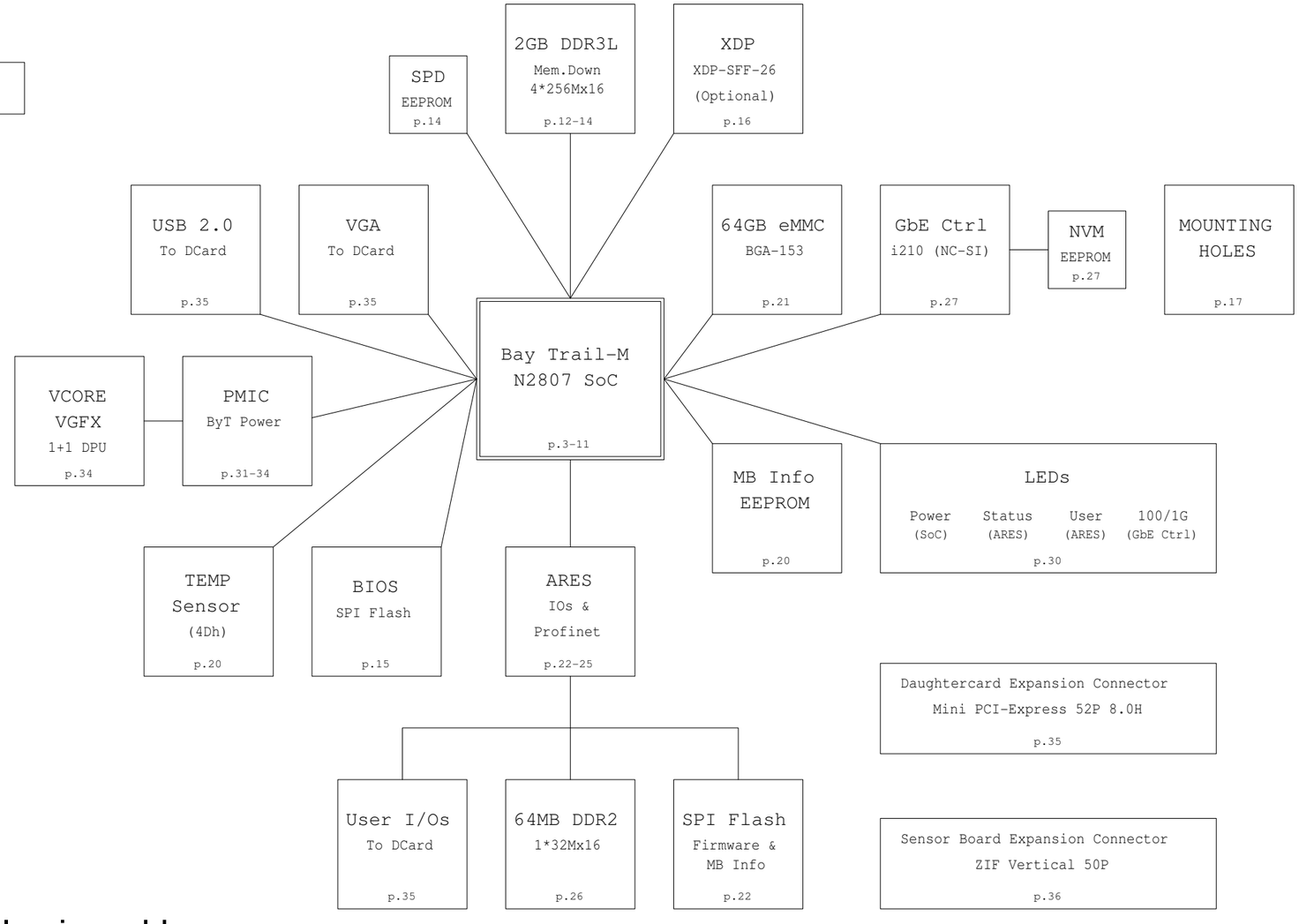
Revision 1.30 (Official Release)

December 21, 2016

MATROX CONFIDENTIAL

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			

INDEX



Digitally signed by Jean-Philippe Gagnon
Date: 2016.12.21 07:52:00 -05'00'

CC1U0WMM5: 0402 (1.0x0.5), 16V, 0.64mm max thickness (Venkel)
CC2U2WMM3: 0402 (1.0x0.5), 16V, 0.6mm max thickness
CC2U2WMM1: 0603 (1.6x0.8), 16V, 1.02mm max thickness (Venkel)
CC4U7WMM3: 0402 (1.0x0.5), 6.3V, 0.64mm max thickness (Venkel)
CC10UWMM6: 0603 (1.6x0.8), 6.3V, 1.02mm max thickness (Venkel)
CC10UWMM8: 0402 (1.0x0.5), 10V, 0.7mm max thickness
CC22UWMM7: 0805 (2.0x1.25), 6.3V, 1.52mm max thickness (Venkel)
CC47UWMM2: 0805 (2.0x1.25), 6.3V, 1.4mm max thickness

PCU SMBus	Refdes	Page	Address
DDR3L SPD EEPROM	A501	14	1010000b (50h)
MB Temperature sensor	A505	20	1001101b (4Dh)
DC Temperature sensor	Axxx	xx	1001100b (4Ch)
MB Info EEPROM	A2	20	1010100b (54h)
DC Info EEPROM	Axxx	xx	1010101b (55h)
SIO I2C	**Refdes**	**Page**	**Address**
PMIC	A515	32	1011110b (5Eh)

DRAWN P-O.Lessard
PROJECT IRIS3
GROUP Imaging
CHECKED Jean-Philippe Gagnon
ING# 127861
SIZE B
DATE 2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: BLOCK DIAGRAM

DRAWING NO 7478-04-01 | REV A | SHEET 1 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			

+5V
5.00V @2.5A
(From Daughtercard)

VCORE
PMIC DCD0+DPU
SVID @ 4A

VGFX
PMIC DCD1+DPU
SVID @ 7A

N2807 (2C ByT-M) EDS

VCC Icc Max = 4A, VNN Icc Max = 7A
TDP(SDP) = 4.3(2.5) W, Tj=105C
Core HFM(Turbo) = 1.58(2.16) GHz, GFX Normal(Burst) = 311(756)
LFM = 533 MHz, DDR = 1333 MT/s

For non-Turbo/Burst operation, expected to stay within the current capability of the PMIC alone (i.e. without DPUs)
Measurements taken with 4GPm-N2807 indicate that it would also be possible to support Turbo/Burst operation for CPU and GFX without DPUs
PMIC DCD0-2 Iout: 4A min cont. and 5A typ pulsed
DPU Iout: 4.5A max cont. and 6A typ pulsed

PMIC DCD5-6 Iout: 2A min cont. and 2.3A typ pulsed
PMIC LDO1-2 Iout: 425mA min cont. with 440mA min current limit

V1P80_A
PMIC DCD6
1.80V @ 1.2A

V1P00_A
PMIC DCD4+DPU
1.00V @ 1.5A

V3P30_A
PMIC DCD3+DPU
3.30V @ 1.2A

VSM
PMIC DCD2
1.35V @ 2A

V5P0_S
LS
5.00V @ 0.1A

VTT
PMIC LDO5
0.625V @ 0.5A (s/s)

V1P80_S
LS
1.80V @ 0.7A

V1P35_S
PMIC LDO2
1.35V @ 0.1A

VSFR
PMIC LDO1
1.35V @ 0.4A

V1P00_S
LS
1.00V @ 1.0A

V3P30_S
LS
3.30V @ 0.9A

V1P05_S
PMIC DCD5
1.05V @ 1.0A

MGTAVCC
LDO
1.00V @ 0.1A

MGTAVTT
LDO
1.20V @ 0.1A

LEGEND:

DC INPUT

PMIC

OTHERS

DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
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TITLE: Power Distribution

DRAWING NO	REV	SHEET
7478-04-01	A	2 OF 38

See DDR3L Memory Down TWP #521656
5.1.3 ODT recommendations (reduced power mode)
2.3 Daisy-chain memory routing guidelines
2.4 T-topology memory routing guidelines

See Micron TN-41-13 DDR3 Point-to-Point Design Support Introduction
ODT, Output Drive Levels

REVISIONS					
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12:13:14 SOC_DDR0_A[15:0] — 40 ohms SE

Consult E3800 colaterals for trace length matching guidelines
(Issue ID #6000108315)

0	K45	0
1	H47	
2	L41	
3	H44	
4	H50	
5	G53	
6	H49	
7	D50	7
8	G52	8
9	E52	DRAM0_MA
10	K48	
11	E51	
12	F47	
13	J51	
14	B49	
15	B50	15

12:13 SOC_DDR0_DM[7:0] — 50 ohms SE

0	G36	0
1	B36	
2	F38	
3	B42	
4	P51	DRAM0_DM
5	V42	
6	Y50	
7	Y52	7

A512-A

DDR0

12:13:14	SOC_DDR0_RAS# — 40 ohms SE	M45 — DRAM0_RAS#
12:13:14	SOC_DDR0_CAS# — 40 ohms SE	M44 — DRAM0_CAS#
12:13:14	SOC_DDR0_WE# — 40 ohms SE	H51 — DRAM0_WE#
12:13:14	SOC_DDR0_BA[2:0] — 40 ohms SE	K47 — DRAM0_BS0
		K44 — DRAM0_BS1
		D52 — DRAM0_BS2
12:13:14	SOC_DDR0_CS0# — 40 ohms SE	P44 — DRAM0_CS0#
12:13:14	SOC_DDR0_CS2# — 40 ohms SE	P45 — DRAM0_CS2#
12:13:14	SOC_DDR0_CKE0 — 40 ohms SE	C47 — DRAM0_CKE0
		D48 — RESERVED_1
12:13:14	SOC_DDR0_CKE2 — 40 ohms SE	F44 — DRAM0_CKE2
		E46 — RESERVED_2
12:13:14	SOC_DDR0_ODT0 — 40 ohms SE	T41 — DRAM0_ODT0
12:13:14	SOC_DDR0_ODT2 — 40 ohms SE	P42 — DRAM0_ODT2
12:13:14	SOC_DDR0_CLKp — 85 ohms DIFF	M50 — DRAM0_CKp0
12:13:14	SOC_DDR0_CLKn — 85 ohms DIFF	M48 — DRAM0_CKn0
		P50 — DRAM0_CKp2
		P48 — DRAM0_CKn2
12:13	SOC_DDR0_RST# — 50 ohms SE	P41 — DRAM0_DRAMRST#
	SOC_DRAM_VREF	AF44 — DRAM_VREF
		AF42 — ICLK_DRAM_TERM0
		AH42 — ICLK_DRAM_TERM1
31	VSM_PGOOD — V1P35U	AD42 — DRAM_VDD_S4_PWROK
32	DRAM_CORE_PWROK	AB42 — DRAM_CORE_PWROK
		AD44 — DRAM_RCOMP0
		AF45 — DRAM_RCOMP1
		AD45 — DRAM_RCOMP2
		AF40 — RESERVED_3
		AF41 — RESERVED_4
		AD40 — RESERVED_5
		AD41 — RESERVED_6

IU80653C15B0

12:13	SOC_DDR0_DQ[63:0] — 50 ohms SE	M36 — 0
		J36 — 1
		P40 — 2
		M40 — 3
		P36 — 4
		N36 — 5
		K40 — 6
		K42 — 7
		B32 — 8
		C32 — 9
		C36 — 10
		A37 — 11
		C33 — 12
		A33 — 13
		C37 — 14
		B38 — 15
		F36 — 16
		G38 — 17
		F42 — 18
		J42 — 19
		G40 — 20
		C38 — 21
		G44 — 22
		D42 — 23
		A41 — 24
		C41 — 25
		A45 — 26
		B46 — 27
		C40 — 28
		B40 — 29
		B48 — 30
		B47 — 31
	DRAM0_DQ	K52 — 32
		K51 — 33
		T52 — 34
		T51 — 35
		L51 — 36
		L53 — 37
		R51 — 38
		R53 — 39
		T47 — 40
		T45 — 41
		Y40 — 42
		V41 — 43
		T48 — 44
		T50 — 45
		Y42 — 46
		AB40 — 47
		V45 — 48
		V47 — 49
		AD48 — 50
		AD50 — 51
		V48 — 52
		V50 — 53
		AB44 — 54
		Y45 — 55
		V52 — 56
		W51 — 57
		AC53 — 58
		AC51 — 59
		W53 — 60
		Y51 — 61
		AD52 — 62
		AD51 — 63

	DRAM0_DQSp0 — J38	
12	DRAM0_DQSn0 — K38 — 85 ohms DIFF	SOC_DDR0_DQS0p
12	DRAM0_DQSp1 — C35	SOC_DDR0_DQS0n
12	DRAM0_DQSn1 — B34 — 85 ohms DIFF	SOC_DDR0_DQS1p
12	DRAM0_DQSp2 — D40	SOC_DDR0_DQS1n
12	DRAM0_DQSn2 — F40 — 85 ohms DIFF	SOC_DDR0_DQS2p
12	DRAM0_DQSp3 — B44	SOC_DDR0_DQS2n
12	DRAM0_DQSn3 — C43 — 85 ohms DIFF	SOC_DDR0_DQS3p
13	DRAM0_DQSp4 — N53	SOC_DDR0_DQS3n
13	DRAM0_DQSn4 — M52 — 85 ohms DIFF	SOC_DDR0_DQS4p
13	DRAM0_DQSp5 — T42	SOC_DDR0_DQS4n
13	DRAM0_DQSn5 — T44 — 85 ohms DIFF	SOC_DDR0_DQS5p
13	DRAM0_DQSp6 — Y47	SOC_DDR0_DQS5n
13	DRAM0_DQSn6 — Y48 — 85 ohms DIFF	SOC_DDR0_DQS6p
13	DRAM0_DQSp7 — AB52	SOC_DDR0_DQS6n
13	DRAM0_DQSn7 — AA51 — 85 ohms DIFF	SOC_DDR0_DQS7p
		SOC_DDR0_DQS7n

VSM
R94 RS4K02M01M0
R93 RS4K02M01M0
C178 CCU10XKM5 Place cap close to SoC
R86 RSM100M01M0
R99 RSM100M01M0
R98 RS23R2M01M0
R100 RS29R4M01M0
R97 RSK162M01M0

DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE
BAY TRAIL SoC
[1 OF 9]

DRAWING NO	REV	SHEET
7478-04-01	A	3 OF 38

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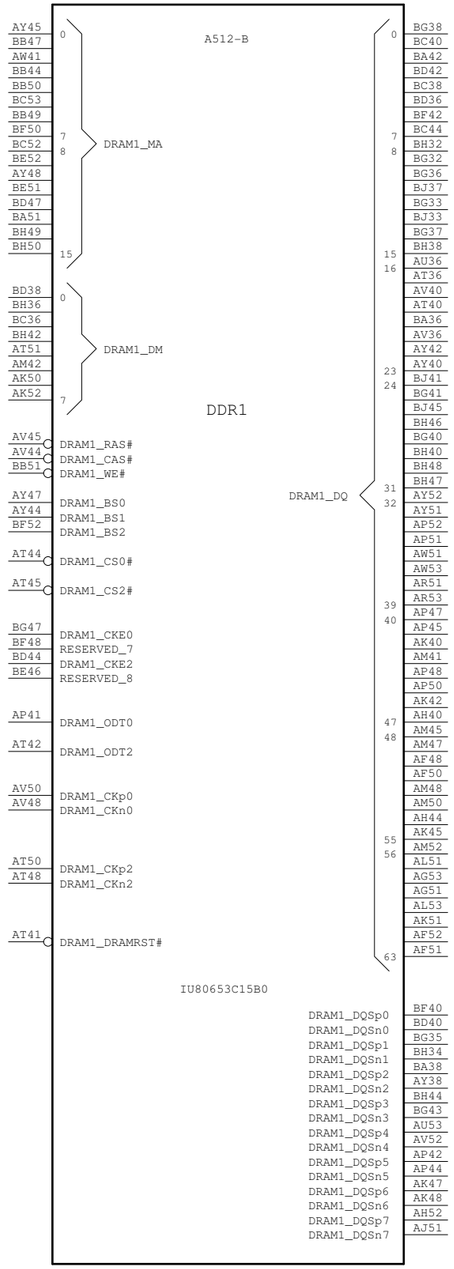
N2807 Max # of Memory Channels = 1



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7478-04-01	A	4 OF 38

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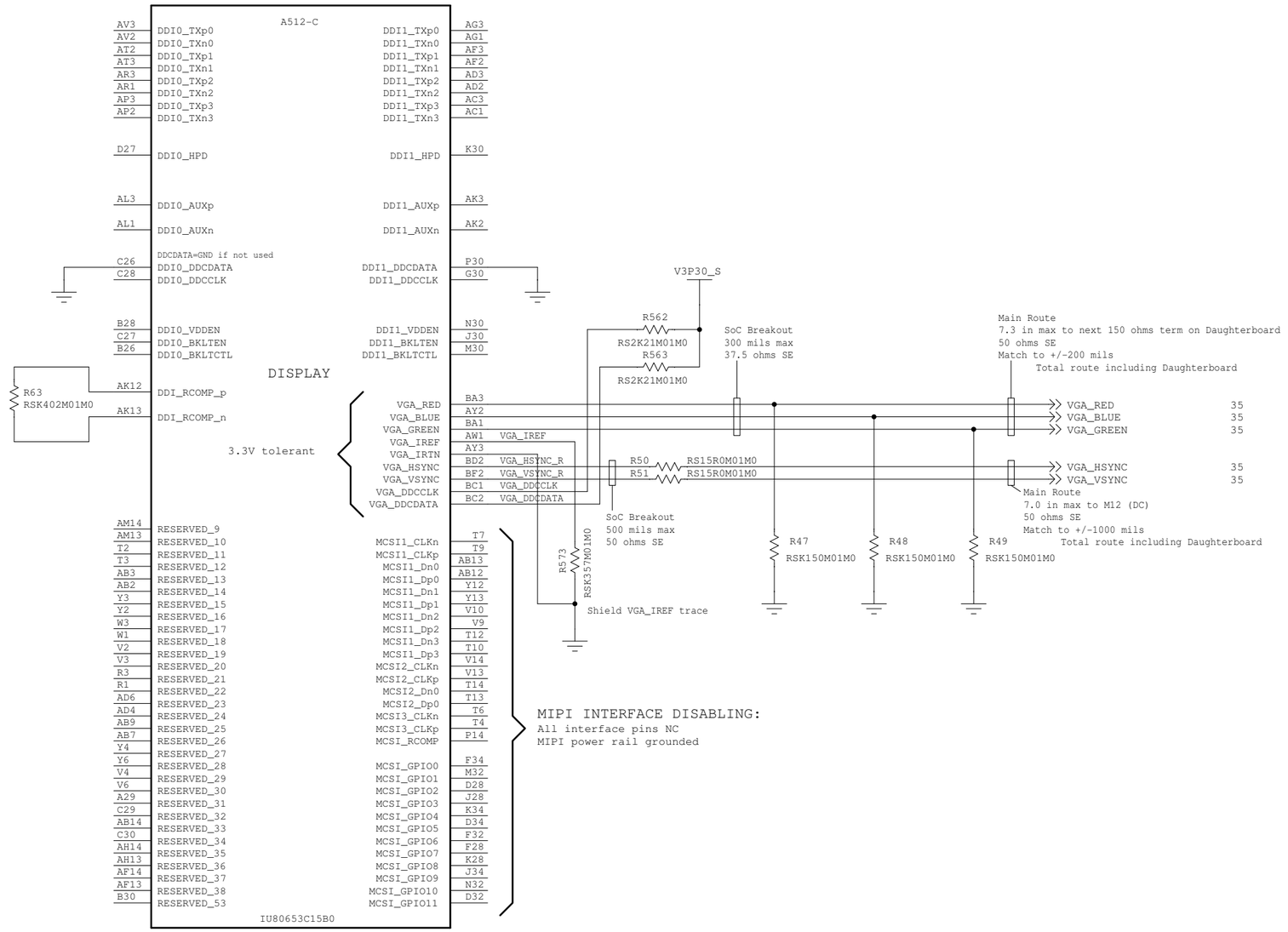

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TITLE: BAY TRAIL SoC [3 OF 9]

DRAWING NO	REV	SHEET
7478-04-01	A	5 OF 38

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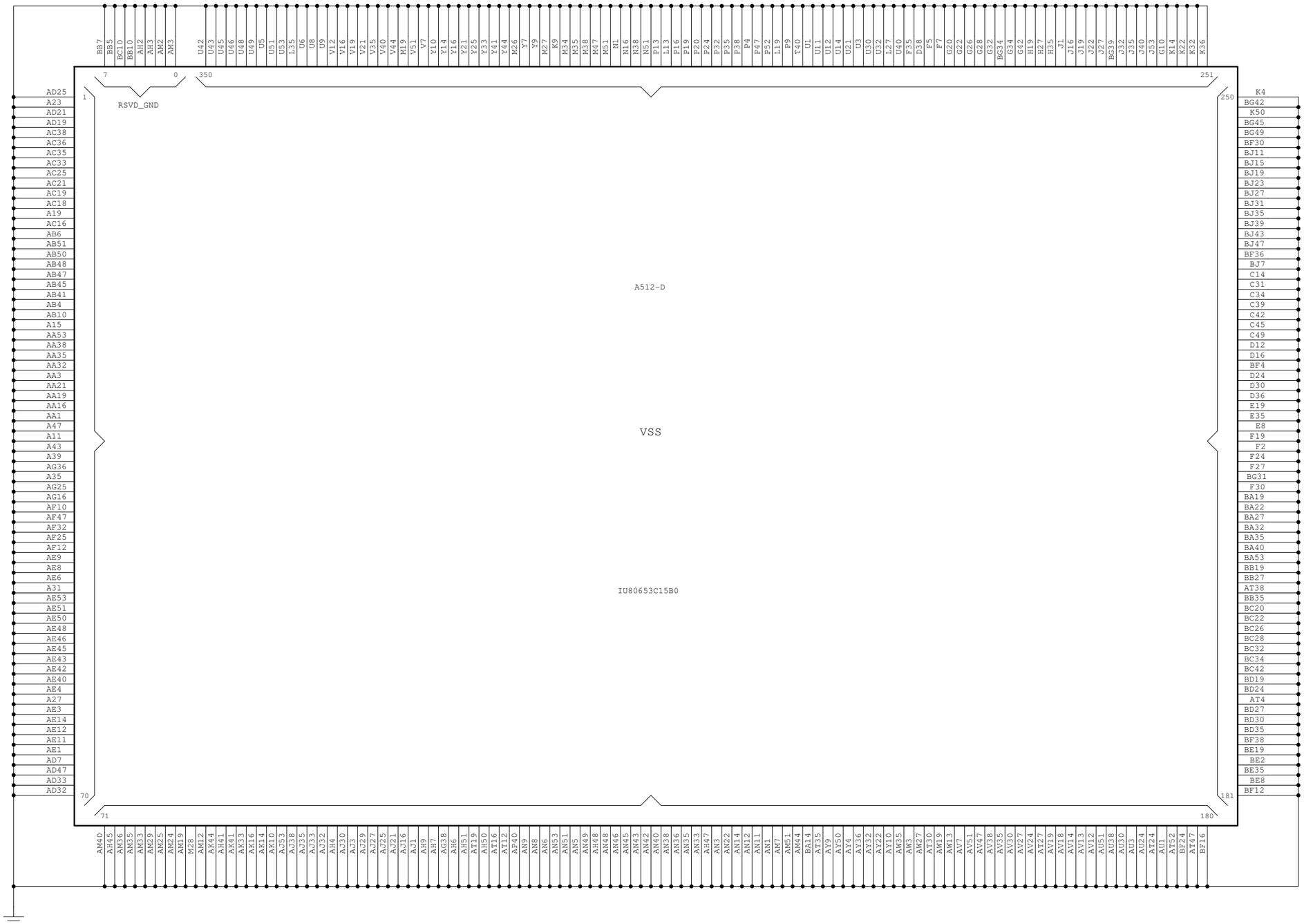

DRAWN	JP Gagnon	MATROX	
PROJECT	IRIS3	1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
GROUP	Imaging	THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED	Jean-Philippe Gagnon	TITLE	BAY TRAIL SoC [4 OF 9]
ING#	127861		
SIZE	B	DATE	2016-12-21
DRAWING NO	7478-04-01	REV	A
SHEET	6 OF 38		

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Integrated Clock Crystal Specifications:
AT cut, fundamental, parallel resonance
25MHz +/-100ppm, ESR = 100 Ohm max.
Cload = 18pF typ, Cshunt = 6pF max, Pdrive = 100uW max

C537 CC27PNFM1
X3 QUARTZCRYSTALS XT25M0000M7 2.5x2.0
C93 CC27PNFM1
R572 RS1M00M01M0
XTAL25M_IN (50 ohms SE)
XTAL25M_OUT (Min spacing to other traces is 15 mils (or shield); Match trace lengths IN-OUT to within +/-100 mils)

ICOMP/RCOMP: Min spacing to other traces is 3x width (or shield)
R570 RS4K02M01M0 ICLK_ICOMP
R571 RS47R5M01M0 ICLK_RCOMP
TP_ICLK_HFHPLLC
TP_ICLK_EXTBGREF

36 PE_REFCLK0_N / 36 PE_REFCLK0_P — Athena PCIe REFCLK (85 ohms DIFF)
PCIe 2.0 (5GT/s): 68-105 ohms
PDG: 85 ohms +/-15%
27 PE_REFCLK2_N / 27 PE_REFCLK2_P — i210 PCIe REFCLK (85 ohms DIFF)
24 PE_REFCLK3_N / 24 PE_REFCLK3_P — Ares PCIe REFCLK (85 ohms DIFF)

V1P80_A
R72 RS49R9M01M0 NI
R67 RS49R9M01M0 NI

16 XDP_TAP_TCK (TAP: 45-65 ohms)
16 XDP_TAP_TRST#
16 XDP_TAP_TMS
16 XDP_TAP_TDI
16 XDP_TAP_TDO
16 XDP_TAP_PRDY#
16 XDP_TAP_PREQ#

All SPI signals are 3s with 20k ohm iPU until PMC_CORE_PWROK is asserted
15 PCU_SPI_CS# (R593 RS23R2M01M0)
15 PCU_SPI_MISO
15 PCU_SPI_MOSI (R594 RS23R2M01M0)
15 PCU_SPI_CLK (R592 RS23R2M01M0)

32 H_THRMTRIP_N (iPU(20k),S0-5,V1P8A)
18 EN_MOBO
32 PM_SLP_SOIX_N

R583 NI RS49R9M01M0
R588 NI RS49R9M01M0
R596 RS49R9M01M0 — Place as close as possible to SoC

A512-E

ICLK_OSCIN	AH12	
ICLK_OSCOUT	AH10	
RESERVED_47	AD9	
ICLK_ICOMP	AD14	
ICLK_RCOMP	AD13	
RESERVED_48	AD10	
RESERVED_49	AD12	
PCIE_CLKn0	AF6	
PCIE_CLKp0	AF4	
PCIE_CLKn1	AF9	
PCIE_CLKp1	AF7	
PCIE_CLKn2	AK4	
PCIE_CLKp2	AK6	
PCIE_CLKn3	AM4	
PCIE_CLKp3	AM6	
RESERVED_50	AM9	
RESERVED_51	AM10	
PMC_PLT_CLK0	BH7	
PMC_PLT_CLK1	BH5	
PMC_PLT_CLK2	BH4	
PMC_PLT_CLK3	BH8	
PMC_PLT_CLK4	BH6	
PMC_PLT_CLK5	BJ9	
TAP_TCK	D14	
TAP_TRST#	G12	
TAP_TMS	F14	
TAP_TDI	F12	
TAP_TDO	G16	
TAP_PRDY#	D18	
TAP_PREQ#	F16	
RESERVED_52	AT34	
PCU_SPI_CS1#	C21	
PCU_SPI_CS0#	C23	
PCU_SPI_MISO	B22	
PCU_SPI_MOSI	A21	
PCU_SPI_CLK	C22	
GPIO_S5_0	B18	
GPIO_S5_1	B16	
GPIO_S5_2	C18	
GPIO_S5_3	A17	
GPIO_S5_4	C17	
GPIO_S5_5	C16	
GPIO_S5_6	B14	
GPIO_S5_7	C15	
GPIO_S5_8	C13	
GPIO_S5_9	A13	
GPIO_S5_10	C19	
GPIO_S5_13	F18	
GPIO_S5_17	J24	
GPIO_RCOMP	N26	

PMC/GPIO

SIO_UART1_RXD	AU34	
SIO_UART1_TXD	AV34	
SIO_UART1_RTS#	BA34	
SIO_UART1_CTS#	AY34	iTDO1
SIO_UART2_RXD	BF34	iTDO2
SIO_UART2_TXD	BD34	oTMS
SIO_UART2_RTS#	BD32	oTDI
SIO_UART2_CTS#	BF32	oTCK
PMC_SUSPWRDNACK	D26	
PMC_SUSCLK0	G24	
PMC_SLP_S4#	P22	
PMC_SLP_S3#	D22	
PMC_ACPRESENT	D20	iPD(20k),S0-3,V1P8A
PMC_WAKE_PCIE0#	F26	iPU(20k),S0-5.V1P8A
PMC_BATLOW#	K26	iPU(20k),S0-5.V1P8A
PMC_PWRBTN#	J26	iPU(20k),S0-5.V1P8A,dbnc=16ms
PMC_RSTBTN#	BG9	iPU(20k),S0-RST.V1P8S
PMC_PLTRST#	F20	
PMC_SUS_STAT#	G18	
PMC_RSMRST#	B10	
PMC_CORE_PWROK	B7	
ILB_RTC_X1	C9	
ILB_RTC_X2	A9	
ILB_RTC_RST#	C12	
ILB_RTC_TEST#	C11	
ILB_RTC_EXTPAD	B8	
SVID_ALERT#	B24	
SVID_DATA	A25	
SVID_CLK	C25	
SIO_PWM0	AU32	
SIO_PWM1	AT32	
GPIO_S5_22	K24	
GPIO_S5_23	N24	
GPIO_S5_24	M20	
GPIO_S5_25	J18	
GPIO_S5_26	M18	
GPIO_S5_27	K18	
GPIO_S5_28	K20	
GPIO_S5_29	M22	
GPIO_S5_30	M24	

IU80653C15B0

SIO_SPI_CS#	AV32	
SIO_SPI_MISO	BA28	
SIO_SPI_MOSI	AY28	
SIO_SPI_CLK	AY30	

V1P80_A, V1P80_S
R605 RS2K21M01M0, R589 RS2K21M01M0, R603 RS20K0M01M0, R604 RS10K0M01M0, R582 RS2K21M01M0
R82 NI RSR000M00M0 — Install when Platform Cable USBII is used (located on IS Board)

GPIO_S0_SC73	FPGA_TDO	22:36		
GPIO_S0_SC74	CPU_TDO	36		
GPIO_S0_SC75	TMS	22:36		
GPIO_S0_SC76	CPU_TDI	22		
GPIO_S0_SC77	TCK	22:36		
	SOC_SUSPWRDNACK	32		
	PM_SLP_S4_N	32		
	PM_SLP_S3_N	32		
	PCIE_WAKE_N	27		
	SOC_PWRBTN#	32		
	SYS_RST_N	16:23		
	PM_PLTRST_N	16:18:32		
	PM_RSMRST_N	16:32		
	SOC_CORE_PWROK	16:32		

iPU(20k).S0-RST.V1P8S.Vil/Vih=0.35/0.65*VREF.Vol=0.45V,Voh=VREF-0.45V
TP_PM_SUSCLK
VREF=V1P8A.Vol/Voh=0.1/0.9*VREF
V1P8A.Vol/Voh=0.1/0.9*VREF
TP_PM_SUS_STAT_N
VRTC.Vil/Vih=0.78/2.0V
Vil/Vih=0.5/0.8*VREF

R637 RSM100M01M0
R575 RSM100M01M0
R579 RS10M0M01M0
VRTC_3P3
R66 RS20K0M01M0, R65 RS20K0M01M0
C547 CC1U0WNM5, C546 CC1U0WNM5

CLEAR_RTC_N 7
CLEAR_CMOS_N 7:16
RTC_EXTPAD 7
V1P00_S
Place within 0.5" of SoC
R597 70-ohm RS68R0R05M0
R598 RS20R0M01M0, R606 RS16R9M01M0
H_CPU_SVIDALRT_N 31
H_CPU_SVIDDAT 31
H_CPU_SVIDCLK 31

XDP_OBSDATA_A0 16
XDP_OBSDATA_A1 16
XDP_OBSDATA_A2 16
XDP_OBSDATA_A3 16

ILB RTC Crystal Specifications:
32.768 kHz +/-10ppm (1.7s per day tol.)
ESR = 50 kOhm max.
Place close to SoC
X500 XT32K7680M4 2.0x1.2 +/-20PPM 12.5pF
RTCX1, RTCX2
C543 CC18PNJM2, C544 CC18PNJM2
C541 CCU10XKM5
RTC_EXTPAD

2mm 2x2
J2 TSSM.235D020
CLEAR_CMOS_N 7:16
CLEAR_RTC_N 7
OVRD_DESC 10

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1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: BAY TRAIL SoC [5 OF 9]

DRAWING NO	REV	SHEET
7478-04-01	A	7 OF 38

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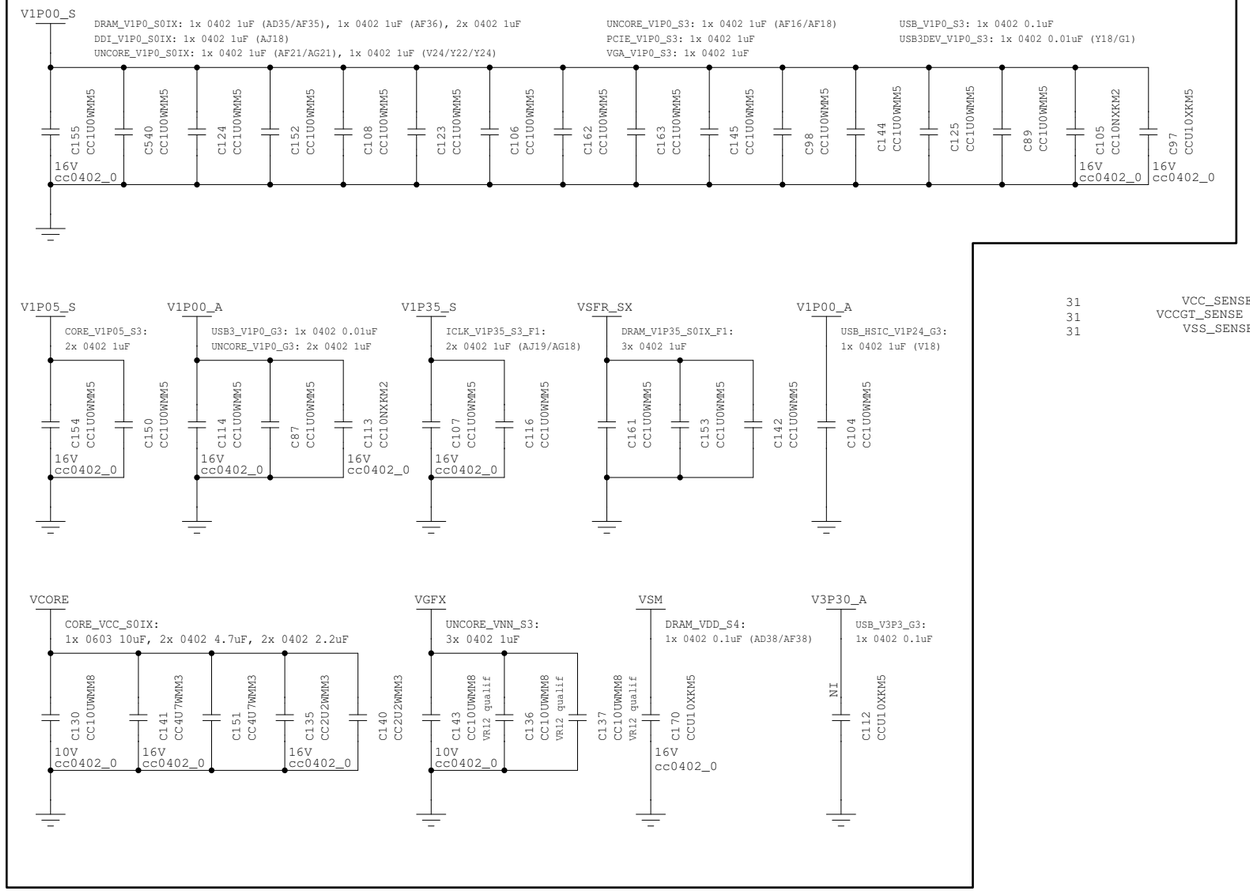
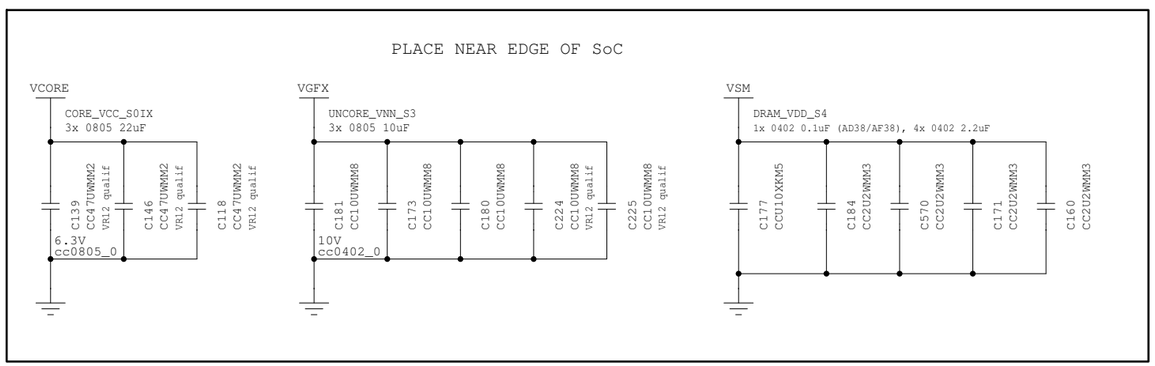
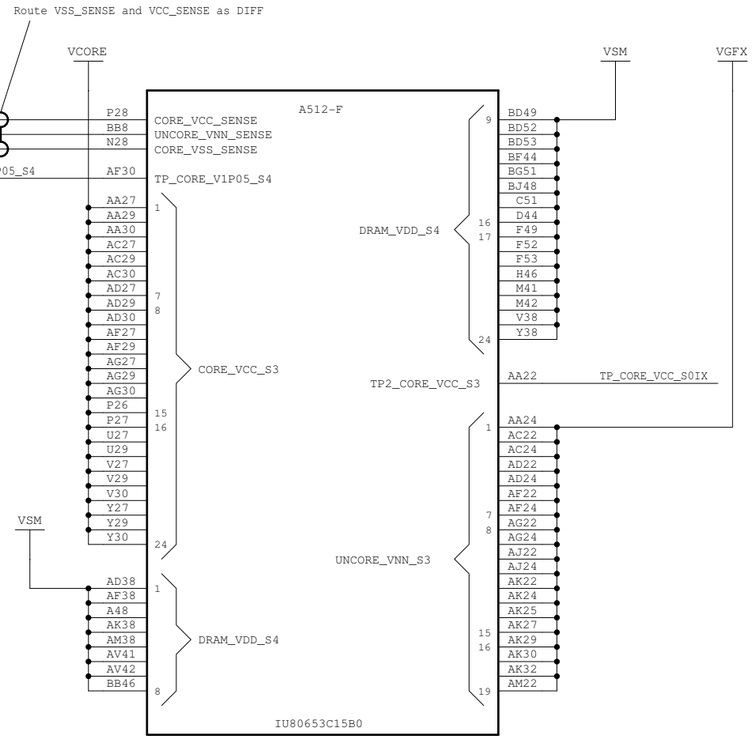
A	7478-91-0100	POL			

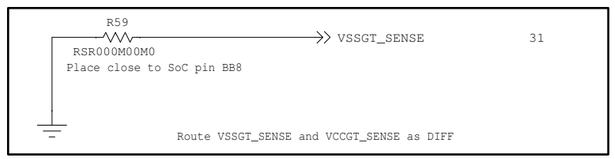
PLACE UNDER PACKAGE SHADOW



PLACE NEAR EDGE OF SoC







DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE
BAY TRAIL SoC
[6 OF 9]

DRAWING NO	REV	SHEET
7478-04-01	A	8 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			

RTC_VCC : 2-3V 100uA Max (6uA avg in G3 @ 27degC)

YBR2032-40+85C : 3V, 195mAh

VF: 0.35V-0.5V (85-25degC) for 100uA

Chosen for higher VF. Battery Manuf spec avoid using schottky diode

CSA considerations:
D2 Vf protects against short-circuit between D3-1 and D3-2 pins

PLACE NEAR EDGE OF SoC

V1P00_S

DDI_V1P0_S0IX: 1x 0402 1uF (AM16)
UNCORE_V1P0_S0Ix: 3x 0805 22uF (AF21/AG21/V24/Y22/Y24)
PCIE_SATA_V1P0_S3: 1x 0402 1uF

C542 CC1U0WNM5 16V cc0402_0
C91 CC1U0WNM5
C92 CC1U0WNM5
C172 CC1U0WNM5
C111 CC22UWNM7 16V cc0805_0
C164 CC22UWNM7
C99 CC22UWNM7

GPIO_V1P0_S3: 1x 0402 1uF
SVID_V1P0_S3: 1x 0402 1uF

V1P00_A

UNCORE_V1P0_G3:
2x 0402 1uF

C88 CC1U0WNM5 16V cc0402_0
C122 CC1U0WNM5

V3P30_S

VGA_V3P3_S3:
1x 0402 1uF

C126 CC1U0WNM5 16V cc0402_0

V1P80_A

UNCORE_V1P8_G3: 1x 0402 1uF
PMC_V1P8_G3: 1x 0402 1uF

C131 CC1U0WNM5
C133 CC1U0WNM5

V3P30_A

PCU_V3P3_G3:
1x 0402 1uF

C132 CC1U0WNM5

V1P80_S

UNCORE_V1P8_S3:
1x 0402 1uF (U38), 3x 0402 1uF (AM30/AN32)

C156 CC1U0WNM5
C158 CC1U0WNM5
C138 CC1U0WNM5
C167 CC1U0WNM5

V1P80_S

HDA_LPE_V1P5V1P8_S3:
1x 0402 1uF

C157 CC1U0WNM5 16V cc0402_0

VSFR_SX

DRAM_V1P35_S0IX_F1: 2x 0402 1uF
UNCORE_V1P35_S0IX_F1: 1x 0402 1uF
UNCORE_V1P35_S0Ix_F5: 1x 0402 1uF
UNCORE_V1P35_S0Ix_F6: 1x 0402 1uF

C168 CC1U0WNM5
C134 CC1U0WNM5
C169 CC1U0WNM5
C115 CC1U0WNM5
C559 CC1U0WNM5

USB_HSIC_V1P24_G3 can be connected to
V1P0A platform rail if USB HSIC is not used

A512-G

P22	RTC_VCC	USB_HSIC_V1P24_G3	V18
		USB_ULPI_V1P8_G3	AA18
		USB_V1P8_G3	N20
		PMC_V1P8_G3	U25
		UNCORE_V1P8_G3	U24
		PCU_V1P8_G3	V25
		PCU_V3P3_G3	N22
		USB_V3P3_G3_1	N18
		USB_V3P3_G3_2	P18
U22	UNCORE_V1P0_G3_1	MIPI_V1P24_S3_1	AD16
V22	UNCORE_V1P0_G3_2	MIPI_V1P24_S3_2	AD18
C5	UNCORE_V1P0_G3_3		
B6	UNCORE_V1P0_G3_4	HDA_LPE_V1P5V1P8_S3	AM32
C3	USB3_V1P0_G3_1		
Y19	USB3_V1P0_G3_2	UNCORE_V1P8_S3_1	AM30
		UNCORE_V1P8_S3_2	AN32
		MIPI_V1P8_S3	U38
V32	SVID_V1P0_S3		
BJ6	VGA_V1P0_S3	LPC_V1P8V3P3_S3	AM27
AD35	DRAM_V1P0_S3_1	SD3_V1P8V3P3_S3	AN27
AF35	DRAM_V1P0_S3_2		
AF36	DRAM_V1P0_S3_3	VGA_V3P3_S3	AN24
AA36	DRAM_V1P0_S3_4		
AJ36	DRAM_V1P0_S3_5	CORE_V1P05_S3_1	AA33
AK35	DRAM_V1P0_S3_6	CORE_V1P05_S3_2	AF33
AK36	DRAM_V1P0_S3_7	CORE_V1P05_S3_3	AG33
Y35	DRAM_V1P0_S3_8	CORE_V1P05_S3_4	AG35
Y36	DRAM_V1P0_S3_9	CORE_V1P05_S3_5	U33
AK19	DDI_V1P0_S3_1	CORE_V1P05_S3_6	U35
AK21	DDI_V1P0_S3_2	CORE_V1P05_S3_7	V33
AJ18	DDI_V1P0_S3_3	CORE_V1P05_S3_8	AC32
AM16	DDI_V1P0_S3_4	CORE_V1P05_S3_9	Y32
AN29	UNCORE_V1P0_S3_1		
AN30	UNCORE_V1P0_S3_2		A3
AF16	UNCORE_V1P0_S3_3		A49
AF18	UNCORE_V1P0_S3_4		A5
V24	UNCORE_V1P0_S3_5		A51
Y22	UNCORE_V1P0_S3_6		A52
Y24	UNCORE_V1P0_S3_7		A6
AF21	UNCORE_V1P0_S3_8		B2
AG21	UNCORE_V1P0_S3_9		B52
Y18	USB3DEV_V1P0_S3_1		B53
G1	USB3DEV_V1P0_S3_2		BE1
AK18	PCIE_V1P0_S3_1		BE53
AM18	PCIE_V1P0_S3_2		BG1
AM21	PCIE_V1P0_S3_3		BG53
AN21	PCIE_V1P0_S3_4		BH1
AN18	PCIE_SATA_V1P0_S3		BH2
AN19	SATA_V1P0_S3		BH52
M14	USB_V1P0_S3_1		BH53
U18	USB_V1P0_S3_2		BJ2
U19	USB_V1P0_S3_3		BJ3
AN25	GPIO_V1P0_S3		BJ49
			BJ5
AG19	UNCORE_V1P35_S3_F1		BJ51
AG32	UNCORE_V1P35_S3_F2		BJ52
V36	UNCORE_V1P35_S3_F3		C1
U36	UNCORE_V1P35_S3_F4		C53
AA25	UNCORE_V1P35_S3_F5		E1
AF19	UNCORE_V1P35_S3_F6		E53
BD1	VGA_V1P35_S3_F1		
AJ19	ICLK_V1P35_S3_F1		
AG18	ICLK_V1P35_S3_F2		
AD36	DRAM_V1P35_S3_F1		
F1	RESERVED_62		
AN16	VSSA		
U16	USB_VSSA		

VSS: 351 – 377

IU80653C15B0

V1P00_S V1P00_A V1P80_A V3P30_A

V1P00_S VRTC_3P3 V1P00_A

C121 CC1U0WMM5

V1P80_S V3P30_S V1P05_S

MIPI interface disabled

If the VGA interface is used,
VLPC must have a nominal voltage of 3.3V
No restrictions apply to VSDIO (3.3V or 1.8V)

VSFR_SX

VGA_V1P35

L500 LB015

C538 CC1U0WNM8 10V cc0402_0

NI

C532 CC1U0WNM5 16V cc0402_0

V1P35_S

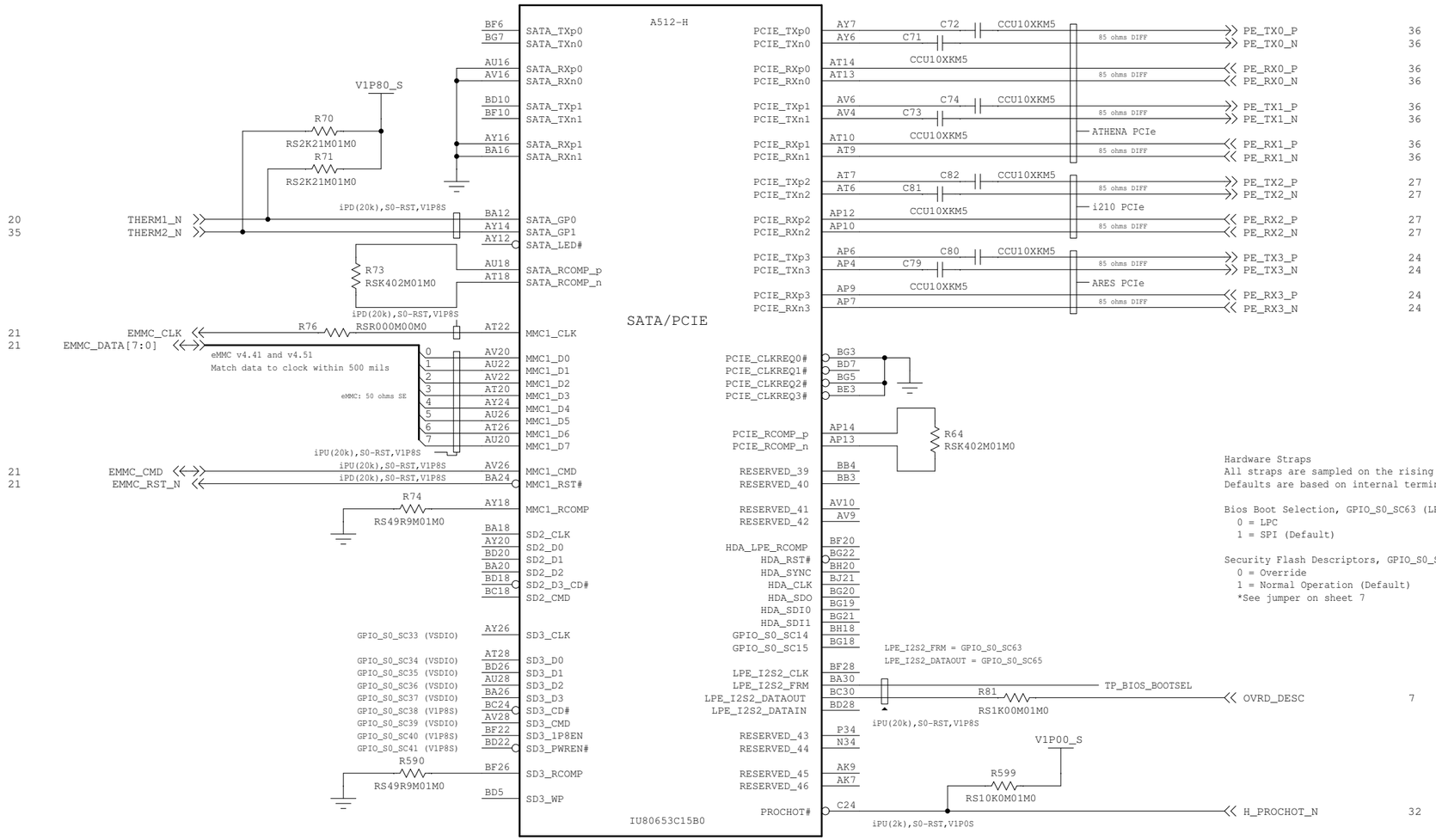
DRAWN	P-O.Lessard
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE
BAY TRAIL SoC
[7 OF 9]

DRAWING NO	REV	SHEET
7478-04-01	A	9 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			



DRAWN	JP Gagnon
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ING#	127861
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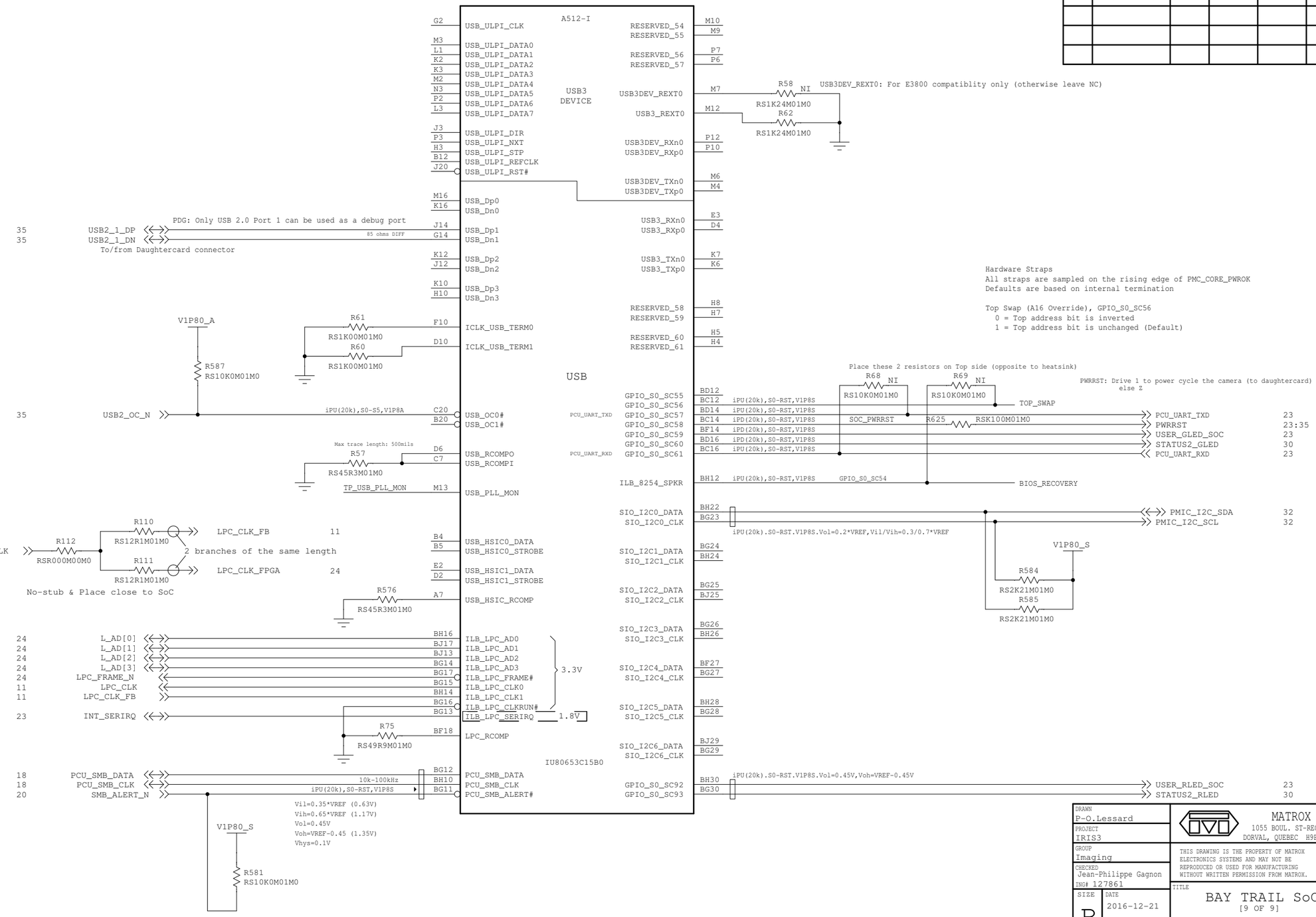
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: BAY TRAIL SoC [8 OF 9]

DRAWING NO	REV	SHEET
7478-04-01	A	10 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			



DRAWN	P-O.Lessard
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: BAY TRAIL SoC [9 OF 9]

DRAWING NO	REV	SHEET
7478-04-01	A	11 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			

3:13:14 SOC_DDR0_CLKp
3:13:14 SOC_DDR0_CLKn
3:13:14 SOC_DDR0_CKE0
3:13:14 SOC_DDR0_CKE2
3:13:14 SOC_DDR0_CS0#
3:13:14 SOC_DDR0_CS2#
3:13:14 SOC_DDR0_RAS#
3:13:14 SOC_DDR0_CAS#
3:13:14 SOC_DDR0_WE#
3 SOC_DDR0_DQS2p
3 SOC_DDR0_DQS2n
3 SOC_DDR0_DQS3p
3 SOC_DDR0_DQS3n
3 SOC_DDR0_DQS0p
3 SOC_DDR0_DQS0n
3 SOC_DDR0_DQS1p
3 SOC_DDR0_DQS1n
3:13 SOC_DDR0_DM[7:0]
3:13:14 SOC_DDR0_BA[2:0]

Single Die Package (SDP): CKE0, CS0#, ODT0, ZQ0
Dual Die Package (DDP): CKE[1:0], CS[1:0]#, ODT[1:0], ZQ[1:0]

See Bay Trail-M/D Platform DDR3L Memory Down technical white paper (521656)
for decoupling recommendations (6x 1uF-0402 per DRAM device and total of 6x 10uF-0603).

VSM
C592 CC1U0WMM5 16V
C618 CC1U0WMM5
C608 CC1U0WMM5
C607 CC1U0WMM5
C591 CC1U0WMM5
C604 CC1U0WMM5

VSM
C189 CC1U0WMM5 16V
C201 CC1U0WMM5
C198 CC1U0WMM5
C206 CC1U0WMM5
C192 CC1U0WMM5
C211 CC1U0WMM5

VSM
C578 CC10UWMM8 10V
C579 CC10UWMM8
C613 CC10UWMM8
C188 CC10UWMM8
C207 CC10UWMM8

A7
4Gb/8Gb
MD256M16C11B0

A518
4Gb/8Gb
MD256M16C11B0

VSM
R102 RS4K02M01M0
R101 RS4K02M01M0
VREF_DQ
C594 CCU10XKM5
C195 CCU10XKM5 16V

VSM
R635 RS4K02M01M0
R636 RS4K02M01M0
VREF_CA
C202 CCU10XKM5
C612 CCU10XKM5 16V

VREF_DQ
VREF_CA
R103 RSK243M01M0
R105 RSK243M01M0
R629 RSK243M01M0
R633 RSK243M01M0

3:13:14 SOC_DDR0_ODT0
3:13:14 SOC_DDR0_ODT2
3:13 SOC_DDR0_RST#
3:13:14 SOC_DDR0_A[15:0]
3:13 SOC_DDR0_DQ[63:0]

DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE
SoC DDR3L
Memory Down B0-3

DRAWING NO	REV	SHEET
7478-04-01	A	12 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			

3:12:14 SOC_DDR0_CLKp
3:12:14 SOC_DDR0_CLKn
3:12:14 SOC_DDR0_CKE0
3:12:14 SOC_DDR0_CKE2
3:12:14 SOC_DDR0_CS0#
3:12:14 SOC_DDR0_CS2#
3:12:14 SOC_DDR0_RAS#
3:12:14 SOC_DDR0_CAS#
3:12:14 SOC_DDR0_WE#
3 SOC_DDR0_DQS6p
3 SOC_DDR0_DQS6n
3 SOC_DDR0_DQS7p
3 SOC_DDR0_DQS7n
3 SOC_DDR0_DQS4p
3 SOC_DDR0_DQS4n
3 SOC_DDR0_DQS5p
3 SOC_DDR0_DQS5n
3:12 SOC_DDR0_DM[7:0]
3:12:14 SOC_DDR0_BA[2:0]

VSM
C581 CC1U0WMM5 16V
C605 CC1U0WMM5
C619 CC1U0WMM5
C614 CC1U0WMM5
C593 CC1U0WMM5
C610 CC1U0WMM5

VSM
C193 CC1U0WMM5 16V
C191 CC1U0WMM5
C186 CC1U0WMM5
C187 CC1U0WMM5
C203 CC1U0WMM5
C208 CC1U0WMM5

VSM
C209 CC10UWMM8 10V
C584 CC10UWMM8
C615 CC10UWMM8
C580 CC10UWMM8
C190 CC10UWMM8

A519
4Gb/8Gb
J7 CK
K7 CK#
K9 CKE0
J9 CKE1_NC
L2 CS0#
L1 CS1#_NC
J3 RAS#
K3 CAS#
L3 WE#
F3 LDQS
G3 LDQS#
C7 UDQS
B7 UDQS#
E7 LDM
D3 UDM
M2 BA0
N8 BA1
M3 BA2
K1 ODT0
J1 ODT1_NC
T2 RESET#
N3 A0
P7 A1
P3 A2
N2 A3
P8 A4
P2 A5
R8 A6
R2 A7
T8 A8
R3 A9
L7 A10_AP
R7 A11
N7 A12_BC#
T3 A13
T7 A14
M7 A15_NC
VDD: B2 D9 G7 K2 K8 N1 N9 R1 R9
VDDQ: A1 A8 C1 C9 D2 E9 F1 H2 H9
VSS: A9 B3 E1 G8 J2 J8 M1 M9 P1 P9 T1 T9
VSSQ: B1 B9 D1 D8 E2 E8 F9 G1 G9
DQ: E3 F7 F2 F8 H3 H8 G2 H7 D7 C3 C8 C2 A7 A2 B8 A3
DQ_0 DQ_1 DQ_2 DQ_3 DQ_4 DQ_5 DQ_6 DQ_7 DQ_8 DQ_9 DQ_10 DQ_11 DQ_12 DQ_13 DQ_14 DQ_15
VREF_DQ H1
VREF_CA M8
ZQ0 L8
ZQ1_NC L9
MD256M16C11B0

A8
4Gb/8Gb
J7 CK
K7 CK#
K9 CKE0
J9 CKE1_NC
L2 CS0#
L1 CS1#_NC
J3 RAS#
K3 CAS#
L3 WE#
F3 LDQS
G3 LDQS#
C7 UDQS
B7 UDQS#
E7 LDM
D3 UDM
M2 BA0
N8 BA1
M3 BA2
K1 ODT0
J1 ODT1_NC
T2 RESET#
N3 A0
P7 A1
P3 A2
N2 A3
P8 A4
P2 A5
R8 A6
R2 A7
T8 A8
R3 A9
L7 A10_AP
R7 A11
N7 A12_BC#
T3 A13
T7 A14
M7 A15_NC
VDD: B2 D9 G7 K2 K8 N1 N9 R1 R9
VDDQ: A1 A8 C1 C9 D2 E9 F1 H2 H9
VSS: A9 B3 E1 G8 J2 J8 M1 M9 P1 P9 T1 T9
VSSQ: B1 B9 D1 D8 E2 E8 F9 G1 G9
DQ: E3 F7 F2 F8 H3 H8 G2 H7 D7 C3 C8 C2 A7 A2 B8 A3
DQ_0 DQ_1 DQ_2 DQ_3 DQ_4 DQ_5 DQ_6 DQ_7 DQ_8 DQ_9 DQ_10 DQ_11 DQ_12 DQ_13 DQ_14 DQ_15
VREF_DQ H1
VREF_CA M8
ZQ0 L8
ZQ1_NC L9
MD256M16C11B0

VREF_DQ
C595 CCU10XKM5
C196 16V CCU10XKM5

VREF_CA
C204 CCU10XKM5
C609 16V CCU10XKM5

R630 RSK243M01M0
R634 RSK243M01M0
R104 RSK243M01M0
R106 RSK243M01M0

3:12:14 SOC_DDR0_ODT0
3:12:14 SOC_DDR0_ODT2
3:12 SOC_DDR0_RST#
3:12:14 SOC_DDR0_A[15:0]
3:12 SOC_DDR0_DQ[63:0]

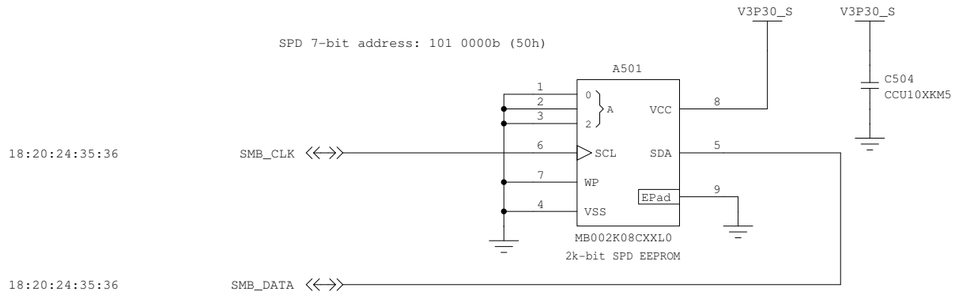
DRAWN JP Gagnon
PROJECT IRIS3
GROUP Imaging
CHECKED Jean-Philippe Gagnon
ING# 127861
SIZE B
DATE 2016-12-21

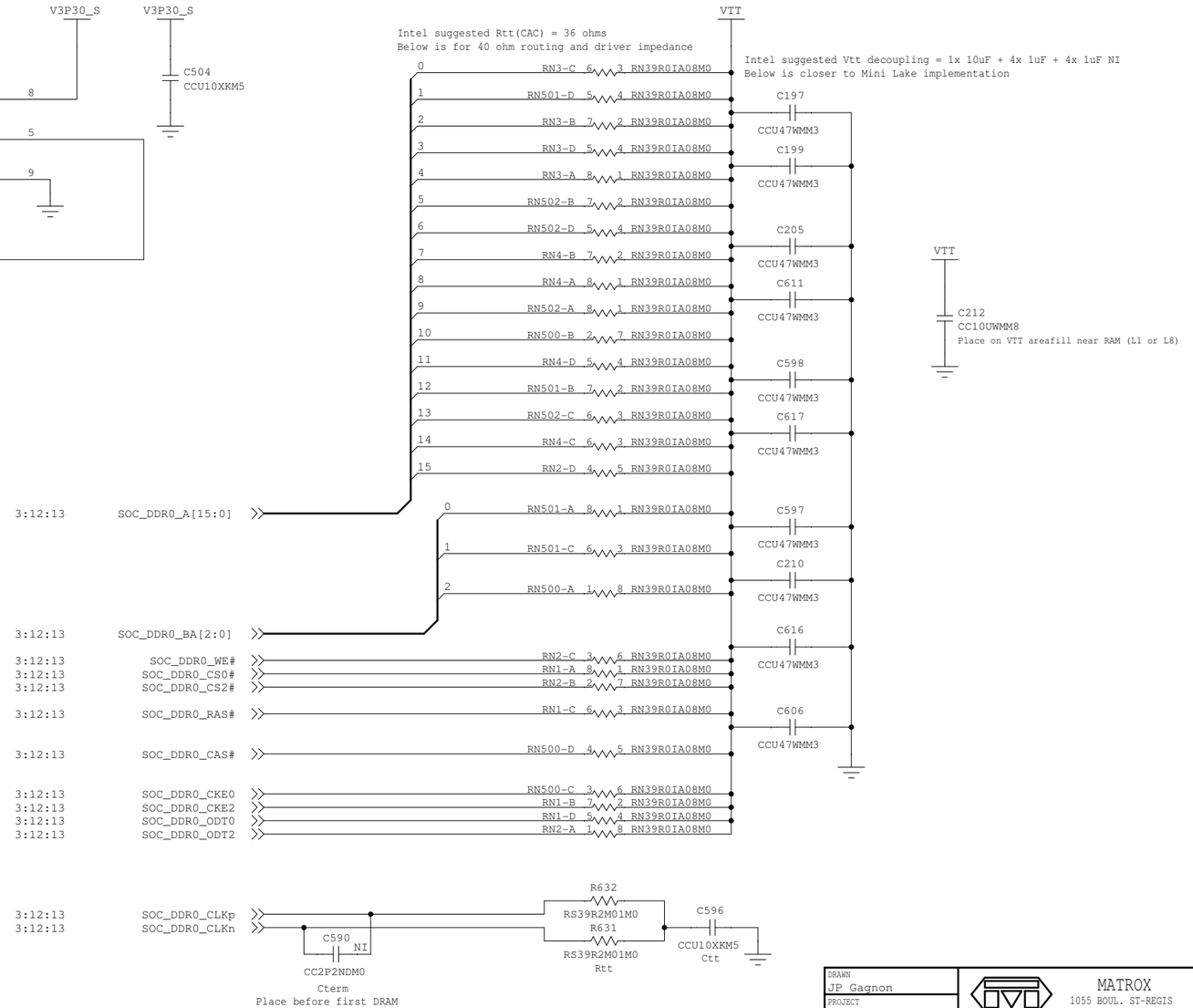
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE
SoC DDR3L
Memory Down B4-7

DRAWING NO 7478-04-01
REV A
SHEET 13 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			





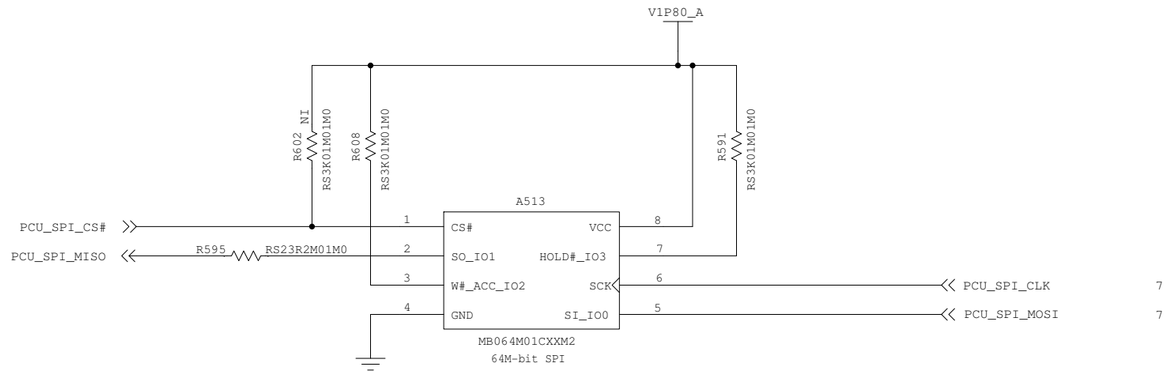
DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

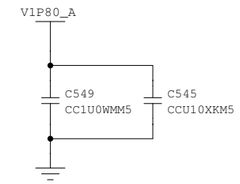
TITLE: SoC DDR3L CAC Terminations

DRAWING NO	REV	SHEET
7478-04-01	A	14 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			



Socket for protos: SSOIC008XTSM0
Do not install EEPROM for protos



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PROJECT	IRIS3
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ING#	127861
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MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: BIOS SPI FLASH

DRAWING NO	REV	SHEET
7478-04-01	A	15 OF 38

REVISIONS					
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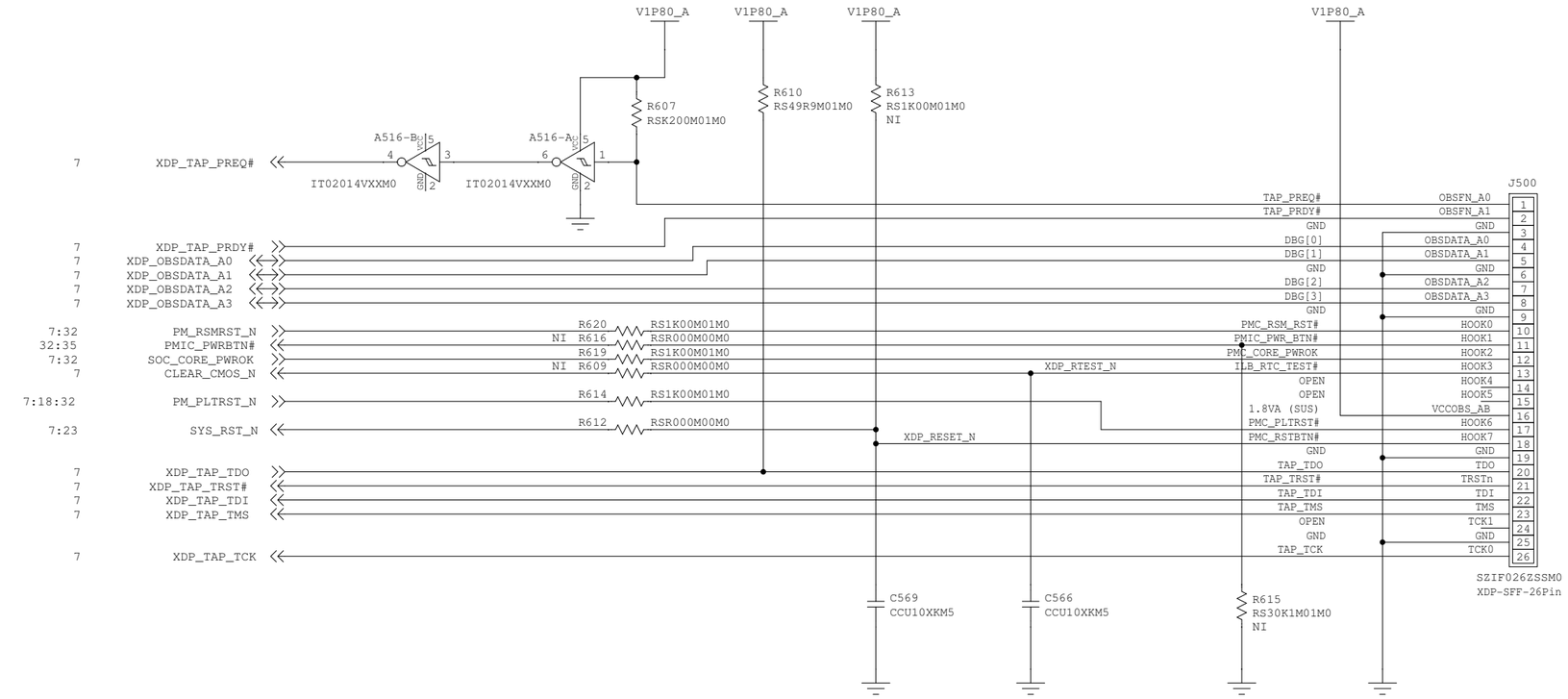
A	7478-91-0100	POL			

Depopulating Debug Port: Debug Port Design Guide (DPDG) Revision 2.1 p.8



DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

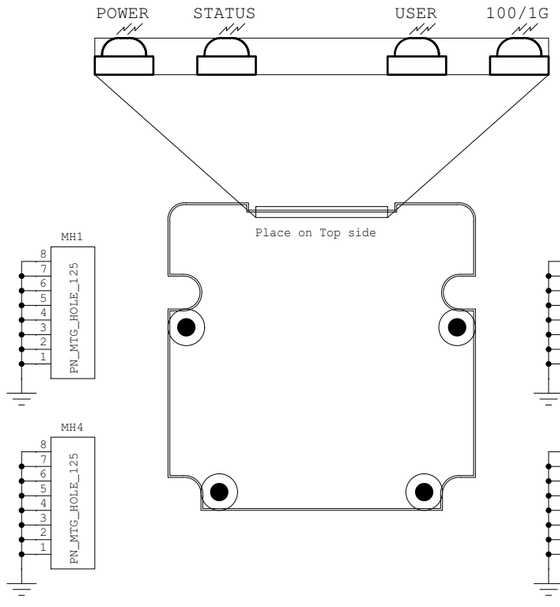
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: XDP DEBUG PORT

DRAWING NO	REV	SHEET
7478-04-01	A	16 OF 38

SUB=XDP

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			



MH = NPTH + 8x gnd vias (25/12)

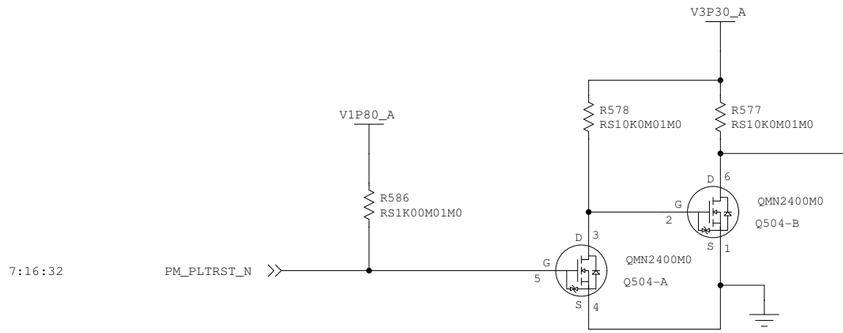
DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: Mounting Holes

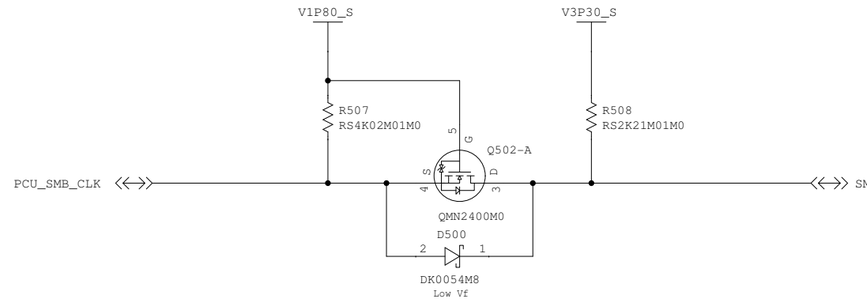
DRAWING NO	REV	SHEET
7478-04-01	A	17 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			



7:16:32 PM_PLTRST_N

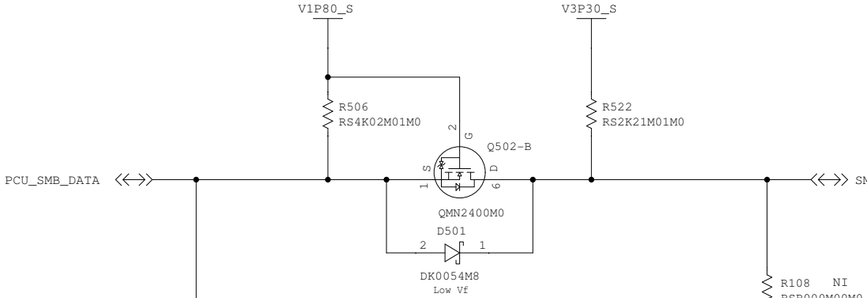
PLTRST_N 24:27:36



11 PCU_SMB_CLK

SMB_CLK 14:20:24:35:36

To SPD, MoBo Info, DCard and SBoard

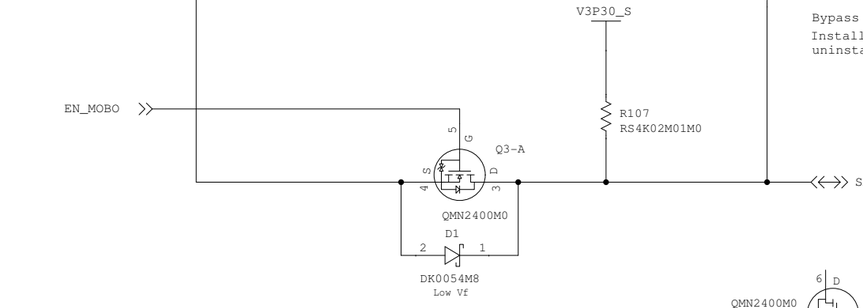


11 PCU_SMB_DATA

SMB_DATA 14:20:24:35:36

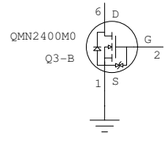
R108 NI
RSR000M00M0

Bypass MoBo info license protection
Install R108
uninstall R107, Q3 and D1



7 EN_MOBO

SMB_DATA_MOBO 20



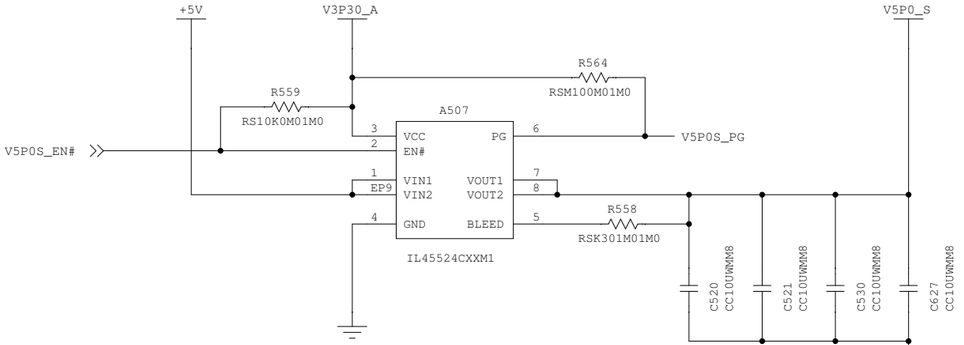
DRAWN	P-O.Lessard
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

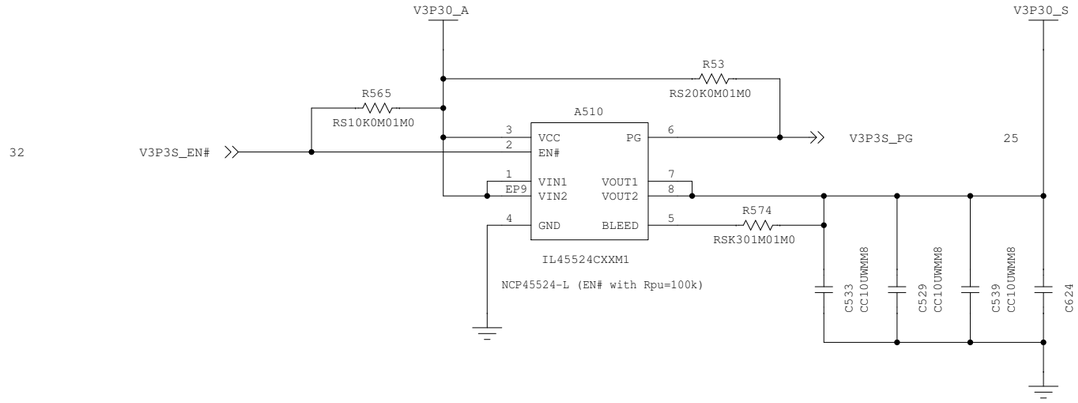
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

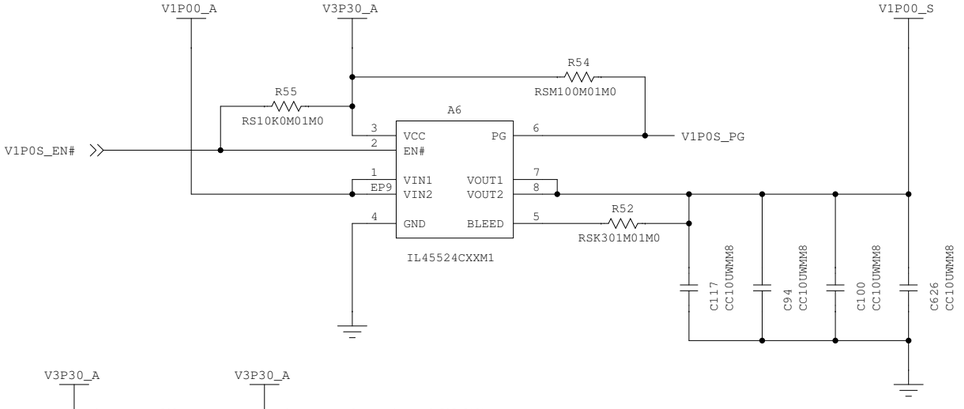
TITLE: LEVEL SHIFTERS

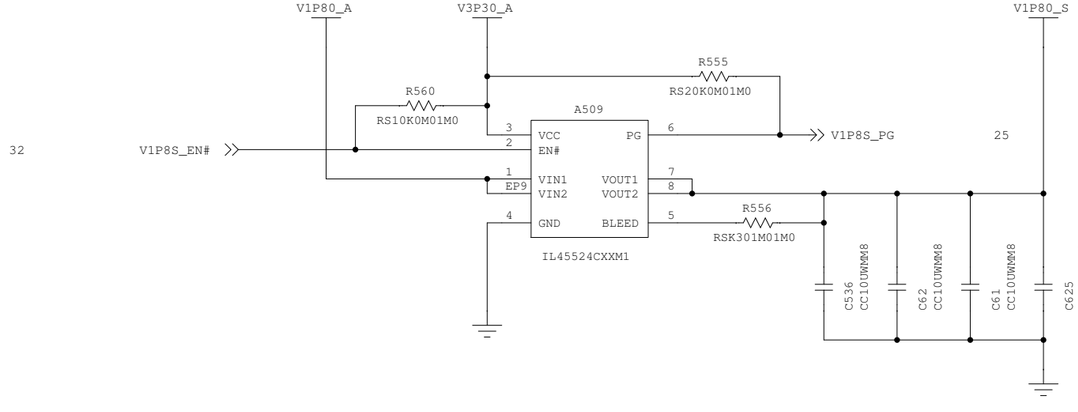
DRAWING NO	REV	SHEET
7478-04-01	A	18 OF 38

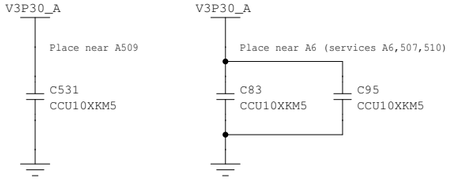
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			











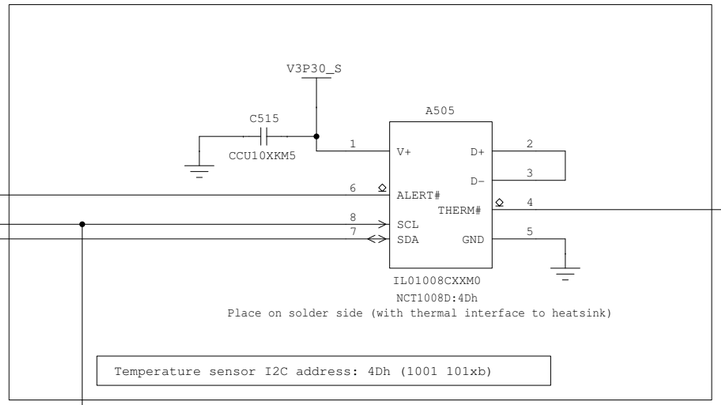
DRAWN: P-O.Lessard
PROJECT: IRIS3
GROUP: Imaging
CHECKED: Jean-Philippe Gagnon
ING# 127861
SIZE: B
DATE: 2016-12-21

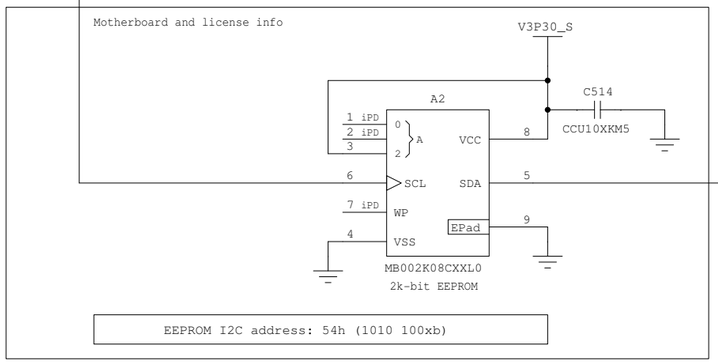
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: SLEEP CONTROL

DRAWING NO: 7478-04-01
REV: A
SHEET: 19 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			





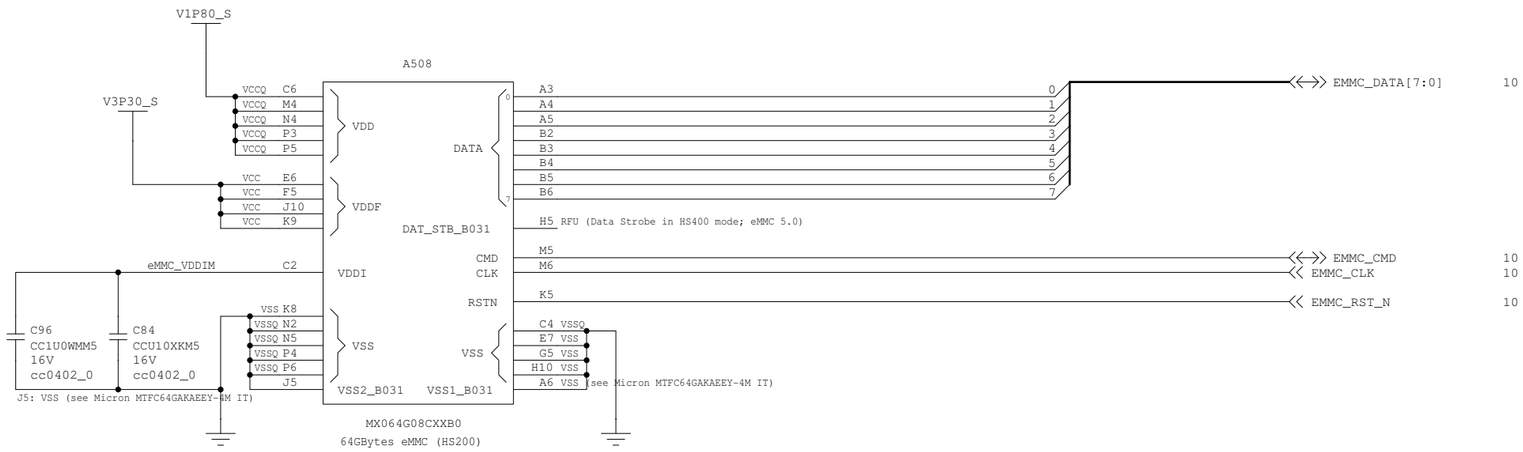
DRAWN	P-O.Lessard
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

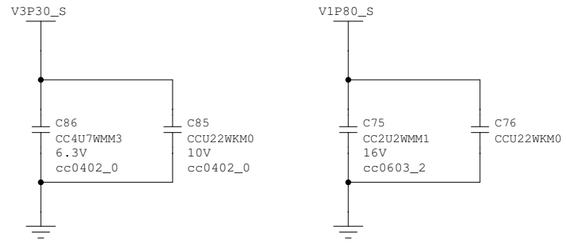
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: MoBo INFO

DRAWING NO	REV	SHEET
7478-04-01	A	20 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			





DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: eMMC

DRAWING NO	REV	SHEET
7478-04-01	A	21 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			

Locate LED on CS (opposite side of Heatsink)

V3P30_S

DS5 — DL7017RM0

R37 — RSK100M01M0

R38 — RSM100M01M0

Q503-A — QMN2400M0

Q503-B — QMN2400M0

V1P80_S

When VCCBAT is not used, connect to ground or VCCAUX

R566 — RS4K99M01M0 — FPGA_INIT#

FPGA_DONE — iPU-10k

A506-A

C13	VCCADC_0	CCLK_0	C11 FW_CCLK_R
C9	VCCBATT_0	M0_0	V12
B12	VREFP_0	M1_0	W11
A13	VREFN_0	M2_0	U10
U11	INIT_B_0	PROGRAM_B_0	V10 FPGA_PROG#
	BANK 0	TDI_0	W10 iPU
A12	VP_0	TDO_0	W8 iPU
B13	VN_0	TCK_0	C8 iPU
U12	DONE_0	TMS_0	W9 iPU
A11	DXP_0	CFGBVS_0	V11
B11	DXN_0	GNDADC_0	C12

SUB=FPGA35T

IF00735C01B2_7478

R11 — RS23R2M01M0 — FW_CCLK

Master SPI: M[2:0] = 001

R567 — RS4K99M01M0

R568 — RS49R9M01M0

CPU_TDI — 7

FPGA_TDO — 7:36

TCK — 7:36

TMS — 7:36

JTAG inputs are not 3.3V tolerant

CFGBVS: Set low for 1.8V/1.5V IO operation (Banks 0,14)

Artix-7 decoupling guide (ug483 table 2-1)

V1P80_S — VCCADC — C22 CCU47WMM3, C63 CCU10XKM5

V1P00_S — VCCINT — C90 CC47UWMM2 6.3V cc0805_0, C57 CCU47WMM3 16V cc0402_0, C58 CCU47WMM3, C47 CCU47WMM3, C70 CCU47WMM3, C34 CCU47WMM3

V1P00_S — VCCBRAM — C65 CCU47WMM3, C36 CCU47WMM3

V1P80_S — VCCAUX — C17 CC47UWMM2, C45 CCU47WMM3, C33 CCU47WMM3

A506-H

G10	VCCINT_1	VCCO_0_1	V9
H10	VCCINT_2	VCCO_0_2	G12
J10	VCCINT_3	VCCO_14_1	F17
L10	VCCINT_4	VCCO_14_2	K12
M10	VCCINT_5	VCCO_14_3	K13
N10	VCCINT_6	VCCO_14_4	L12
		VCCO_14_5	L13
		VCCO_14_6	M12
		VCCO_14_7	M17
		VCCO_14_8	R17
		VCCO_14_9	U13
	POWER	VCCO_16_1	B19
		VCCO_16_2	C14
		VCCO_16_3	C18
		VCCO_16_4	G13
M11	VCCBRAM_1	VCCO_34_1	M8
N11	VCCBRAM_2	VCCO_34_2	N7
		VCCO_34_3	N8
		VCCO_34_4	R1
H13	VCCAUX_1	VCCO_34_5	V1
J13	VCCAUX_2	VCCO_34_6	V6
		VCCO_35_1	H3
		VCCO_35_2	J7
		VCCO_35_3	K1
		VCCO_35_4	K7
		VCCO_35_5	L7
		VCCO_35_6	M7

IF00735C01B2_7478

V1P80_S — VCCO_14 — C64 CC47UWMM2, C18 CCU47WMM3, C54 CCU47WMM3, C46 CCU47WMM3, C55 CCU47WMM3, C24 CCU47WMM3, C32 CCU47WMM3

Power sequencing: VCCINT (1.0V), VCCBRAM (1.0V), VCCAUX (1.8V) and VCCO (3.3V)
Power sequencing GTP: VCCINT, MGTAVCC, MGTAVTT or MGTAVCC, VCCINT, MGTAVTT

V1P80_S — VCCO_16 — C19 CCU47WMM3, C20 CCU47WMM3, C23 CCU47WMM3, C21 CCU47WMM3

V3P30_S — VCCO_34 — C528 CCU47WMM3, C524 CCU47WMM3, C38 CCU47WMM3, C60 CCU47WMM3, C49 CCU47WMM3, C48 CCU47WMM3

V3P30_S — VCCO_35 — C66 CCT10WMM5 R1.30, C59 CCU47WMM3, C39 CCU47WMM3, C37 CCU47WMM3, C67 CCU47WMM3, C526 CCU47WMM3, C68 CCU47WMM3

V1P80_S — VCCO_0 — C43 CCU47WMM3, C56 CCU47WMM3

23 FW_SI_IO0

FW_CCLK

23 FW_CS#

23 FW_SO_IO1

V1P80_S

R533 — RS2K21M01M0

R532 — RS4K99M01M0

C523 — CCU10XKM5

R538 — RS4K99M01M0

R512 — RS23R2M01M0

R537 — RS23R2M01M0

A1

1	CS#	VCC	8
2	SO_IO1	HOLD#_IO3	7
3	W#_ACC_IO2	SCK	6
4	GND	SI_IO0	5

MB064M01CXXM2
Vih(min)=1.26V, Vil(max)=0.54V
ARES Golden and Upgrade firmwares
MoBo Info
MIL license information

A506-G

A1	1	27	H7
A3			H8
A5			H11
A7			H12
A9			H18
A19			J8
B3			J9
B5			J11
B7			J12
B9			K8
B14			L8
C2			L9
C3			L11
C4	GROUND		L19
C6			M9
C10			M13
C19			N9
D3			N12
E3			N13
E17			P2
F1			T19
F2			U6
F19			U9
G1			V18
G8			W1
G11	26	52	W12

IF00735C01B2_7478

DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: Ares FPGA [1 of 3]

DRAWING NO	REV	SHEET
7478-04-01	A	22 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			

V1P80_S

R539 RS1K00M01M0

R540 NI RS1K00M01M0

A506-B

26	DDR2_CKE	D17	IO_0_14		IO_25_14	U14	DDR2_A0	26
22	FW_SI_IO0	D18	IO_L1P_T0_D00_MOSI_14		IO_L13P_T2_MRCC_14	N17	PCU_UART_RXD	11
22	FW_SO_IO1	D19	IO_L1N_T0_D01_DIN_14		IO_L13N_T2_MRCC_14	P17	INT_SERIRQ	11
26	DDR2_A8	G18	IO_L2P_T0_D02_14		IO_L14P_T2_SRCC_14	P18		
26	DDR2_A7	F18	IO_L2N_T0_D03_14		IO_L14N_T2_SRCC_14	R18	PCU_UART_TXD	11
	FPGA_PUDC#	E18	IO_L3P_T0_DQS_PUDC_B_14		IO_L15P_T2_DQS_RDWR_B_14	U19		
26	DDR2_BA1	E19	IO_L3N_T0_DQS_EMCCLK_14		IO_L15N_T2_DQS_DOUT_CSO_B_14	V19		
26	DDR2_BA0	H19	IO_L4P_T0_D04_14		IO_L16P_T2_CSI_B_14	W18		
26	DDR2_RAS#	G19	IO_L4N_T0_D05_14		IO_L16N_T2_A15_D31_14	W19		
26	DDR2_CAS#	H17	IO_L5P_T0_D06_14		IO_L17P_T2_A14_D30_14	T17		
26	DDR2_WE#	G17	IO_L5N_T0_D07_14		IO_L17N_T2_A13_D29_14	T18		
22	FW_CS#	K19	IO_L6P_T0_FCS_B_14	BANK 14	IO_L18P_T2_A12_D28_14	U17	FPGA_SYS_RST_N R561 RSK100M01M0 SYS_RST_N	7:16
26	ODT	J19	IO_L6N_T0_D08_VREF_14		IO_L18N_T2_A11_D27_14	U18		
26	DDR2_DM0	J17	IO_L7P_T1_D09_14		IO_L19P_T3_A10_D26_14	V16	DDR2_A12	26
26	DDR2_DQ0	J18	IO_L7N_T1_D10_14		IO_L19N_T3_A09_D25_VREF_14	V17	DDR2_A11	26
26	DDR2_DQ1	L18	IO_L8P_T1_D11_14		IO_L20P_T3_A08_D24_14	W16	DDR2_A10	26
26	DDR2_DQ2	K18	IO_L8N_T1_D12_14		IO_L20N_T3_A07_D23_14	W17	DDR2_A9	26
26	DDR2_DQS0_P	N18	IO_L9P_T1_DQS_14		IO_L21P_T3_DQS_14	V15	DDR2_A6	26
26	DDR2_DQS0_N	N19	IO_L9N_T1_DQS_D13_14		IO_L21N_T3_DQS_A06_D22_14	W15	DDR2_A5	26
26	DDR2_DQ3	P19	IO_L10P_T1_D14_14		IO_L22P_T3_A05_D21_14	W13	DDR2_CK_P	26
26	DDR2_DQ4	R19	IO_L10N_T1_D15_14		IO_L22N_T3_A04_D20_14	W14	DDR2_CK_N	26
26	DDR2_DQ5	M18	IO_L11P_T1_SRCC_14		IO_L23P_T3_A03_D19_14	U15	DDR2_A4	26
26	DDR2_DQ6	M19	IO_L11N_T1_SRCC_14		IO_L23N_T3_A02_D18_14	U16	DDR2_A3	26
11:35	PWRRST	L17	IO_L12P_T1_MRCC_14		IO_L24P_T3_A01_D17_14	V13	DDR2_A2	26
26	DDR2_DQ7	K17	IO_L12N_T1_MRCC_14	IF00735C01B2_7478	IO_L24N_T3_A00_D16_14	V14	DDR2_A1	26

R34 RSK100M01M0 FPGA_PWRRST

PWRRST: Drive 1 to power cycle the camera (to daughtercard) else Z

V1P80_S

A506-C

11	USER_RLED_SOC	A14	IO_L6P_T0_16		IO_L13P_T2_MRCC_16	C16	DEBUG_DATA_0 R519 RS1K00M01M0 NI	
11	USER_GLED_SOC	A15	IO_L6N_T0_VREF_16		IO_L13N_T2_MRCC_16	B16	DEBUG_DATA_1 R518 RS1K00M01M0 NI	
36	ACQ_EXP	C15	IO_L11P_T1_SRCC_16		IO_L14P_T2_SRCC_16	C17	DEBUG_DATA_2 R515 RS1K00M01M0 NI	
36	ACQ_STRB	B15	IO_L11N_T1_SRCC_16	BANK 16	IO_L14N_T2_SRCC_16	B17	DEBUG_DATA_3 R516 RS1K00M01M0 NI	
36	ACQ_TRIG	A16	IO_L12P_T1_MRCC_16		IO_L19P_T3_16	B18	ACQ_LED0	36
36	ACQ_TRIG_RDY	A17	IO_L12N_T1_MRCC_16	IF00735C01B2_7478	IO_L19N_T3_VREF_16	A18	ACQ_LED1	36

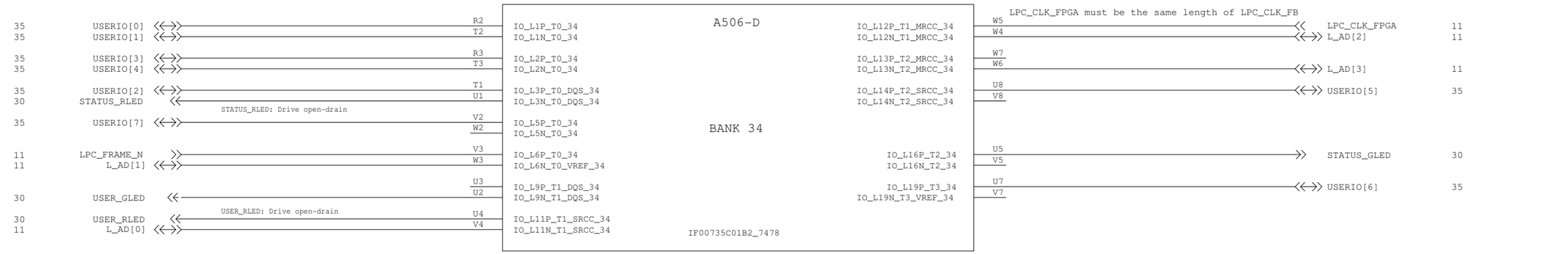
DRAWN	P-O.Lessard
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: Ares FPGA [2 of 3]

DRAWING NO	REV	SHEET
7478-04-01	A	23 OF 38

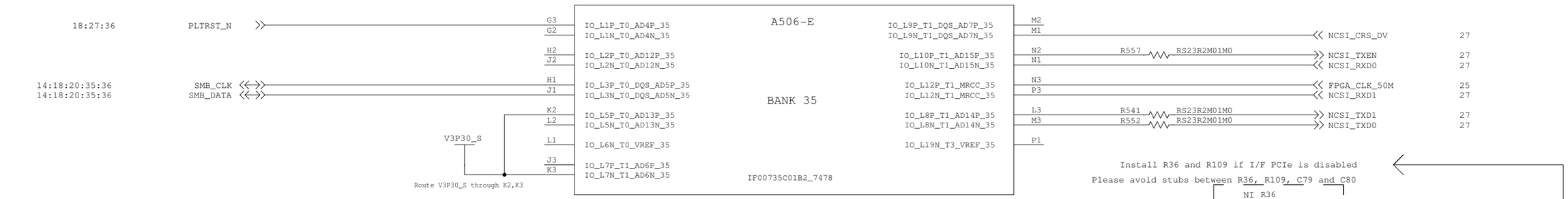
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			



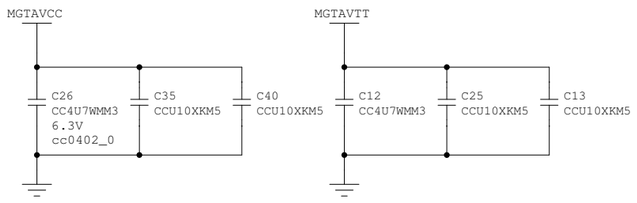
LPC_CLK_FPGA must be the same length of LPC_CLK_FB

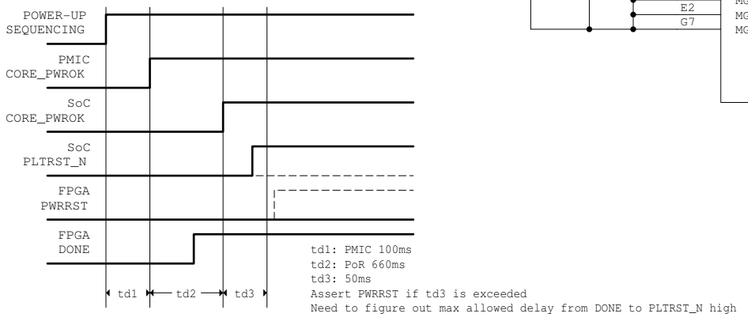
Intel sighting #4600919

FPGA shall assert PWRRST if PLTRST_N not de-asserted within allowed time

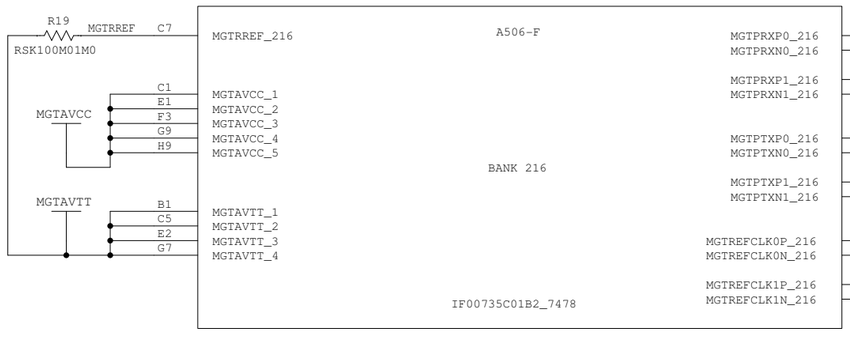


Artix-7 GTP decoupling guide (ug482 table 5-7)





td1: PMIC 100ms
td2: PoR 660ms
td3: 50ms
Assert PWRRST if td3 is exceeded
Need to figure out max allowed delay from DONE to PLTRST_N high



Install R36 and R109 if I/F PCIe is disabled

Please avoid stubs between R36, R109, C79 and C80

NI R36
RSR000M00M0
NI R109
RSR000M00M0

(ug482) MGTPRXP/N1 connection if not used: GND

PE_TX3_P 10
PE_TX3_N 10

PE_RX3_P 10
PE_RX3_N 10

(ug482) MGTPTXP/N1 connection if not used: FLOAT

PE_REFCLK3_P 7
PE_REFCLK3_N 7

(ug482) MGTREFCLK1P/N connection if not used: FLOAT

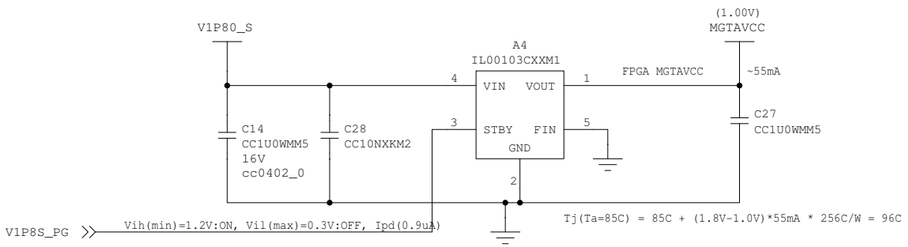
DRAWN	P-O.Lessard
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

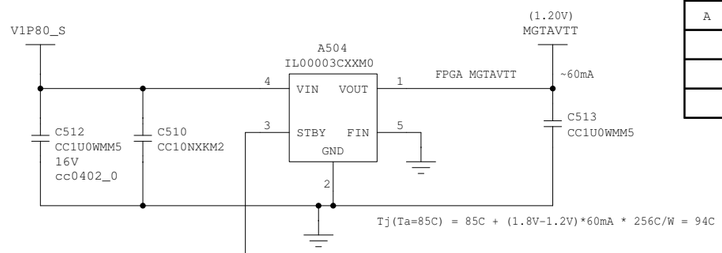
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

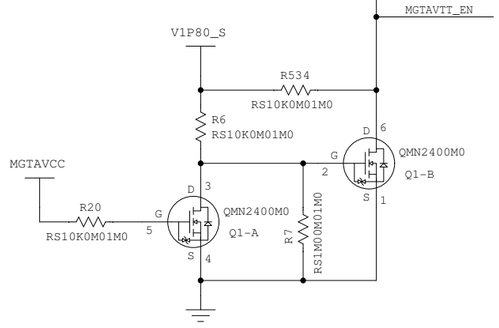
TITLE: Ares FPGA [3 of 3]

DRAWING NO	REV	SHEET
7478-04-01	A	24 OF 38

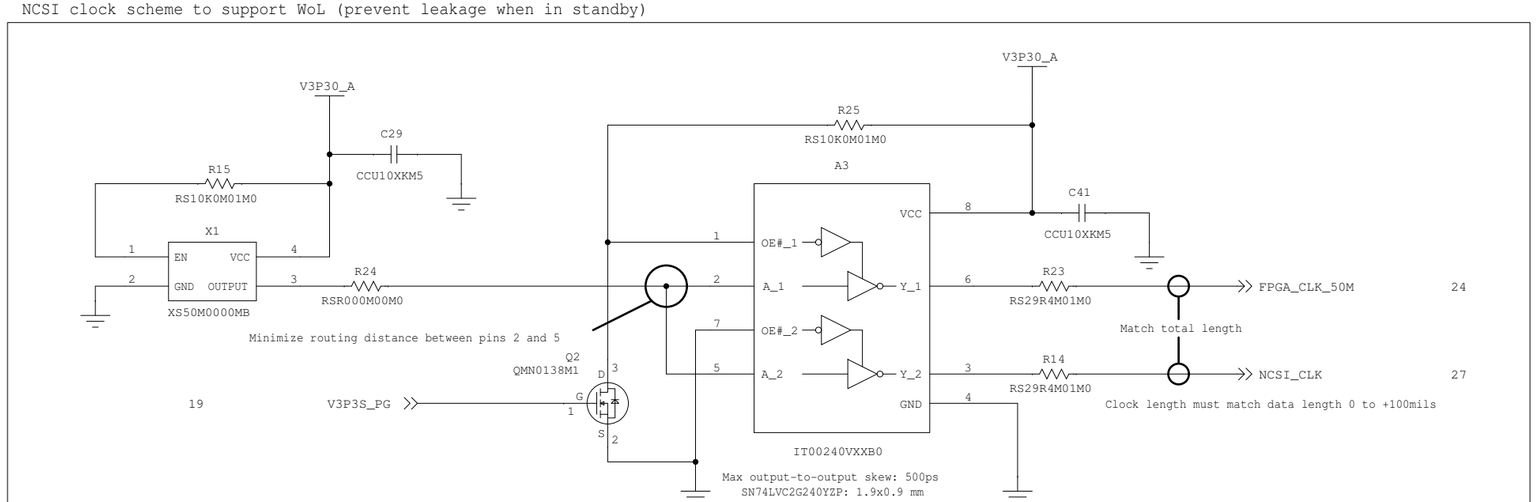
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			







NCSI clock scheme to support WoL (prevent leakage when in standby)



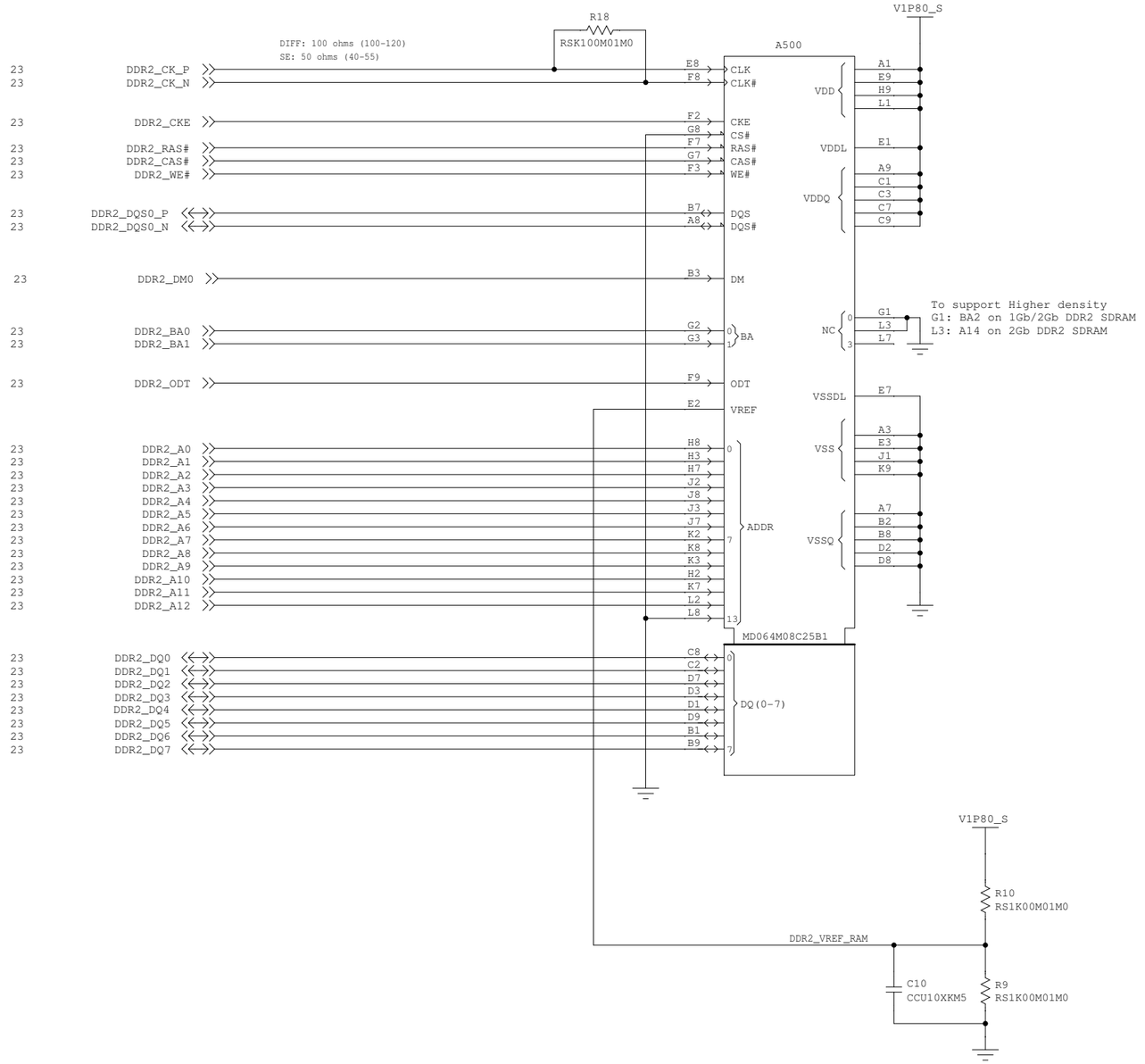
DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

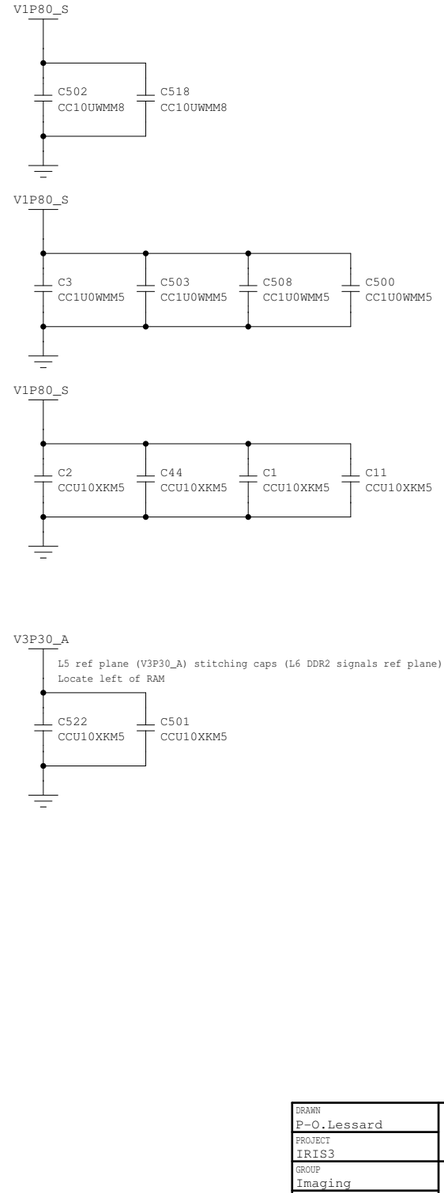
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE
Ares FPGA
MGT Power

DRAWING NO	REV	SHEET
7478-04-01	A	25 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			





DRAWN	P-O.Lessard
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

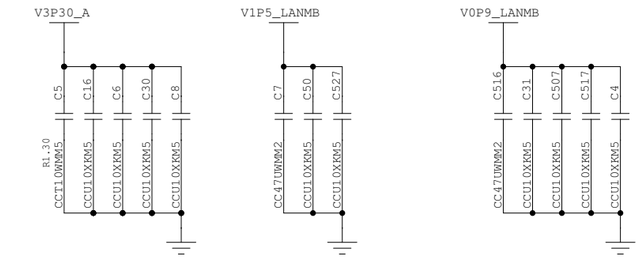
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

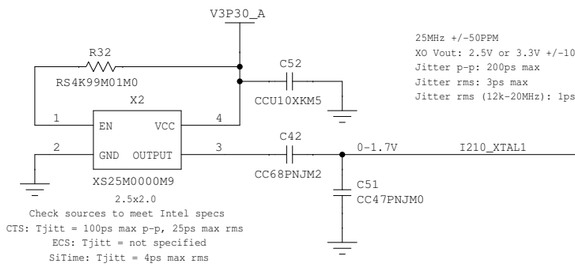
TITLE
Ares FPGA
DDR2

DRAWING NO	REV	SHEET
7478-04-01	A	26 OF 38

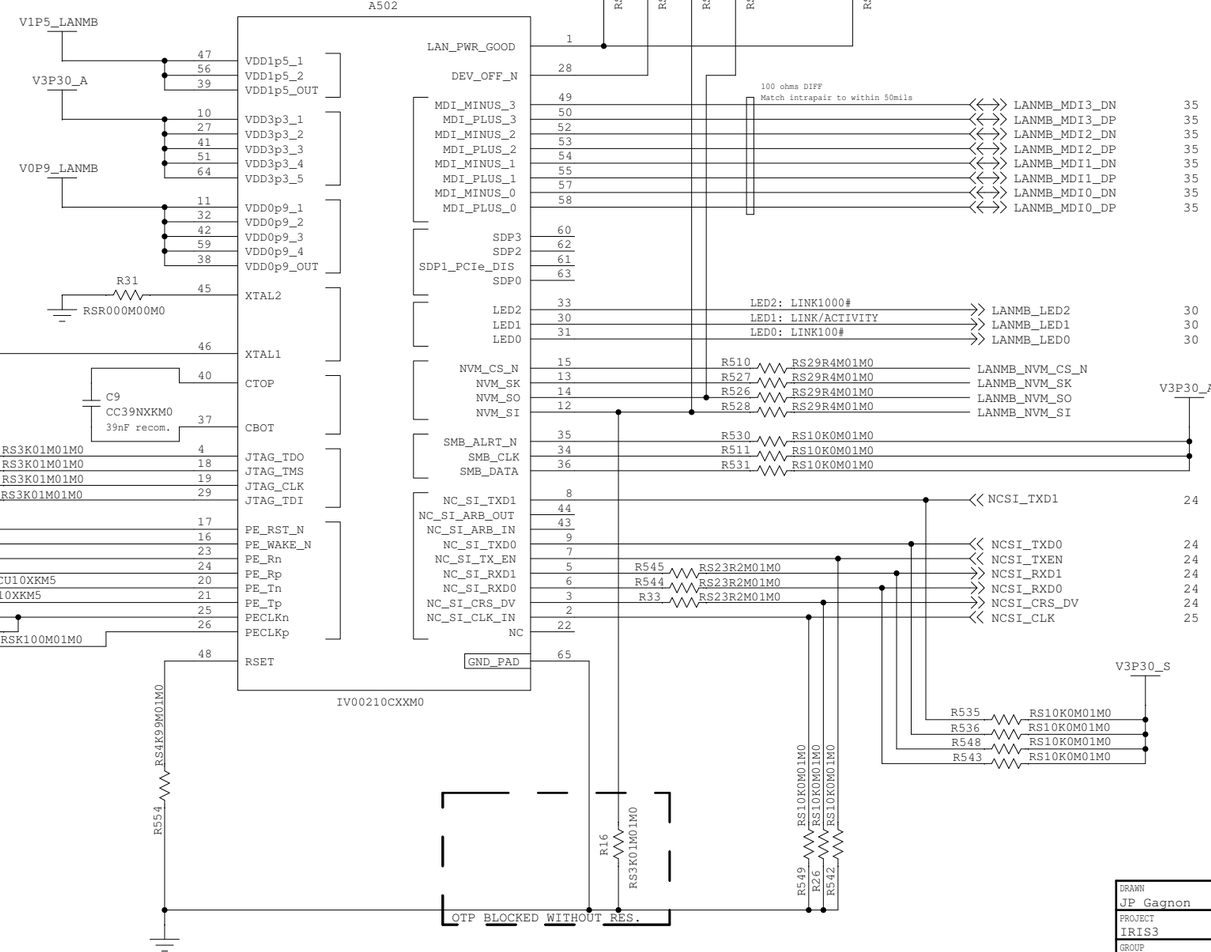
GigE Controller I210 MoBo (Springville)

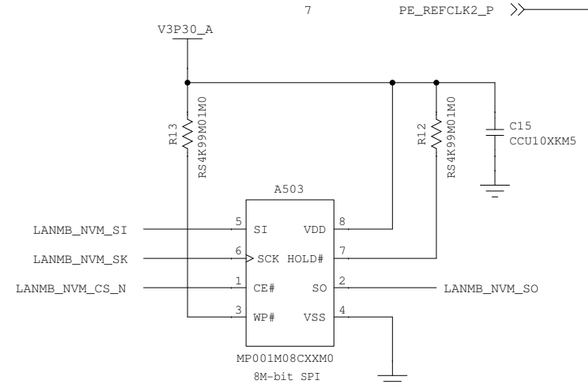
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			





25MHz +/-50PPM
XO Vout: 2.5V or 3.3V +/-10%
Jitter p-p: 200ps max
Jitter rms: 3ps max
Jitter rms (12k-20MHz): 1ps max





DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

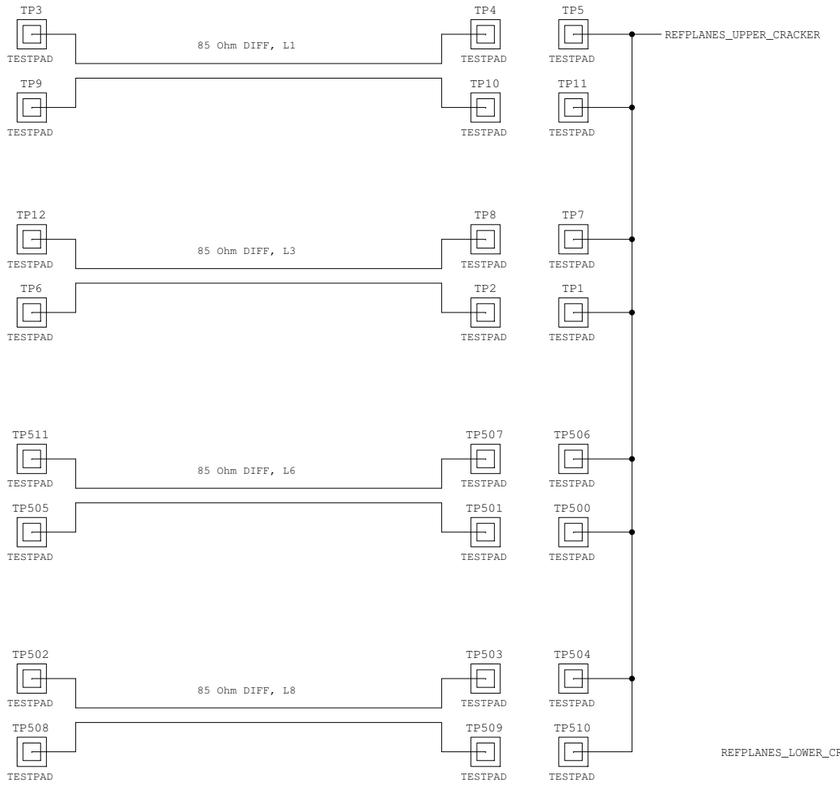
TITLE: GigE MAC & PHY MoBo

DRAWING NO	REV	SHEET
7478-04-01	A	27 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			

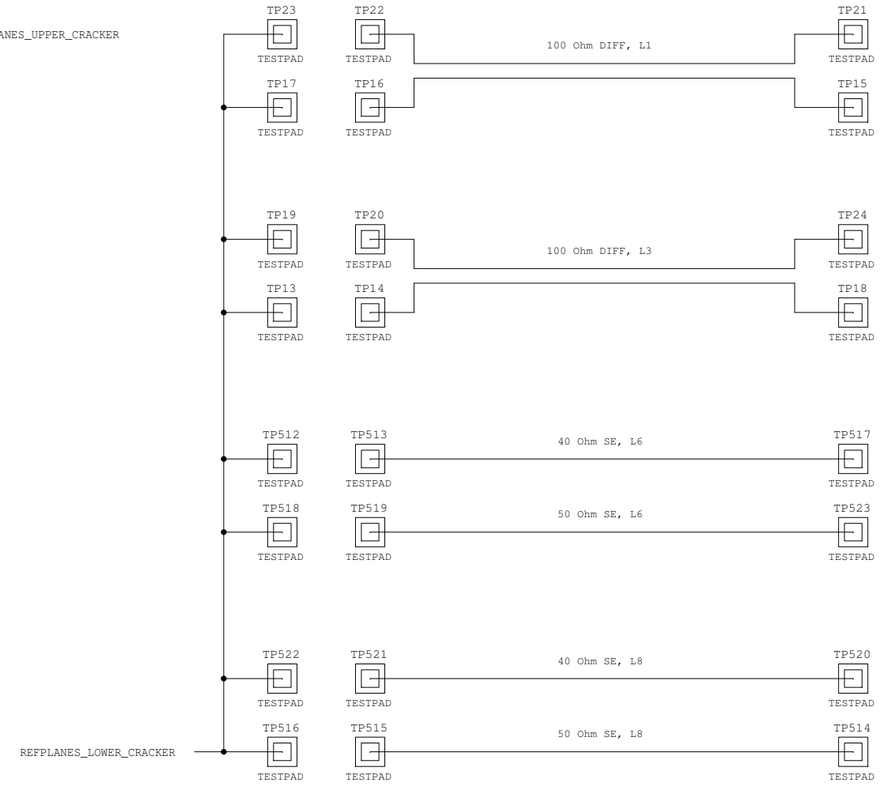
Test coupons on panel upper cracker section

Route straight on full cracker length



Test coupons on panel lower cracker section

Route straight on full cracker length

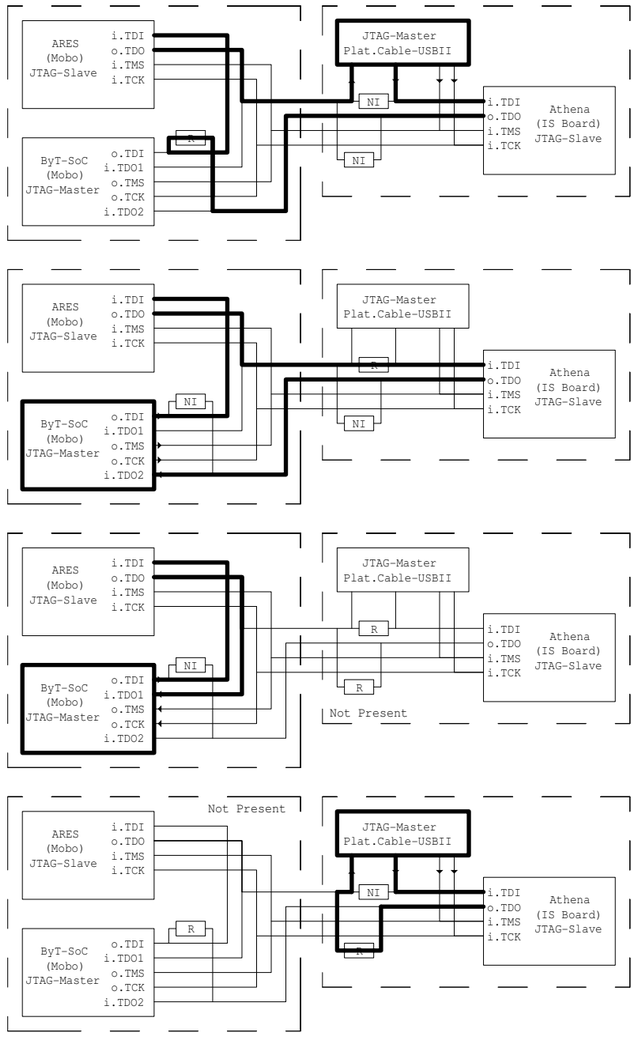


DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

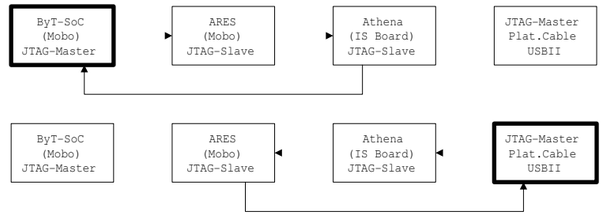
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: TEST COUPONS

DRAWING NO	REV	SHEET
7478-04-01	A	28 OF 38



JTAG Daisy Chain Routing Order:



REVISIONS

REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			

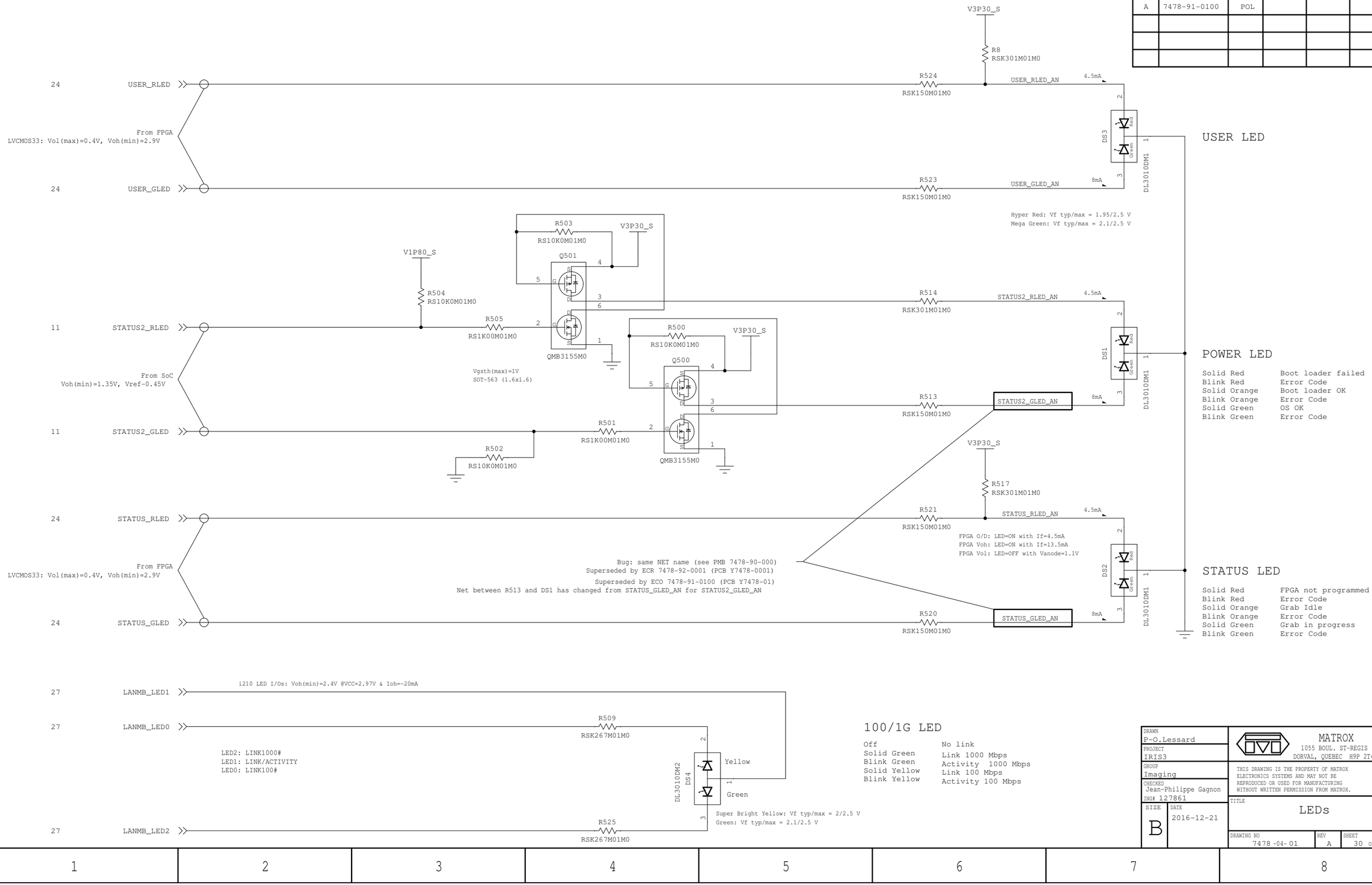
DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: JTAG scheme

DRAWING NO	REV	SHEET
7478-04-01	A	29 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			



DRAWN	P-O.Lessard
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: LEDs

DRAWING NO	REV	SHEET
7478-04-01	A	30 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			

+5V
VIN_DCD0
C159 CC10UWMM8 10V cc0402_0
C147 CC10UWMM8
+5V
VIN_DCD1
C174 CC10UWMM8
C166 CC10UWMM8
+5V
VIN_DCD2
C175 CC10UWMM8
C176 CC10UWMM8
+5V
VIN_DCD5
C148 CC10UWMM8
C222 CC10UWMM8
+5V
VIN_DCD6
C149 CC10UWMM8
C223 CC10UWMM8

VR12 qualif (N2807):
-BIOS PMIC 0xA8 = 0x01 (VCC set VID Slow Rate to 5mV/us and Fast Rate to 10mV/us)
-BIOS PMIC 0xA9 = 0x11 (VNN set VID slow to 5mV/us to respect "Max duration CSO# to Alert")

VR12 qualif (J1900):
-BIOS PMIC 0xA8 = 0x11 (VCC set VID slow to 5mV/us to respect "Max duration CSO# to Alert")
-BIOS PMIC 0xA9 = 0x11 (Changer le Slow Rate 5mV/ s)

A515-A

[OTP=A1]

VIN_DCD0_1 B41, VIN_DCD0_2 B42
DCD0/VCC
GPIO5__DCD0_DIF B24 — 34 DCD0_DIF
GPIO4__DCD0_DIO A32 — 34 DCD0_DIO
DCD0_FB B40
DCD0_LX_1 A50, DCD0_LX_2 A51, DCD0_LX_3 A52
DCD0_GSEN B43

DCD0-1: 0.47uH, 5A min, dual footprint IHLP1212+XFL4012, 1.2mm max thickness

B40 — R83 RSK100M01M0 — VCORE — L503 LCU470M9 — C127 CC47UWMM2 (VR12 qualif) — VCORE — C119 CC47UWMM2, C128 CC47UWMM2
A50/A51/A52 — L503 LCU470M9
B43 — R78 RSK100M01M0

VCC_SENSE 8
VSS_SENSE 8

Place within 0.5" of SoC

V1P00_S — R79 RS68R0M05M0 — R84 70-ohm RS68R0M05M0

VIN_DCD1_1 B36, VIN_DCD1_2 B37
DCD1/VNN
GPIO3__DCD1_DIF B25 — 34 DCD1_DIF
GPIO2__DCD1_DIO A33 — 34 DCD1_DIO
SVID_CLK B44 — 7 H_CPU_SVIDCLK — R85 RS20R0M01M0
SVID_DIO A55 — 7 H_CPU_SVIDDAT — R80 RS16R9M01M0
DCD1_FB B38
DCD1_LX_1 A47, DCD1_LX_2 A48, DCD1_LX_3 A49
DCD1_GSEN B35
SVID_ALERT_B A56 — H_CPU_SVIDALRT_N 7

B38 — R89 RSK100M01M0 — VGFX — L504 LCU470M9 — C572 CC47UWMM2 (VR12 qualif) — VGFX — C183 CC47UWMM2, C182 CC47UWMM2
A47/A48/A49 — L504 LCU470M9
B35 — R92 RSK100M01M0

VCCGT_SENSE 8
VSSGT_SENSE 8

VSM — R96 NI RS10K0M01M0 P9180 — 3 VSM_PGOOD — Voh(min)=VSM_FB-0.40

VIN_DCD2_1 B28, VIN_DCD2_2 B29
DCD2/VDDQ
DRAMPWROK B32
GPIO1__DCD2_DIF B26
GPIO0__DCD2_DIO A34
DCD2_FB B30
DCD2_LX_1 A35, DCD2_LX_2 A36, DCD2_LX_3 A37

DCD2: 0.47uH, 3.5A min, 2.5x2.0 mm footprint, 1.2mm max thickness

B30 VSM_FB — R622 RSR000M00M0 — VSM — L506 LC1U50MC R1.30 — C585 CC47UWMM2 — VSM — C179 CC47UWMM2

V1P05_S

VIN_DCD5 B5
DCD5/V1P05S
DCD5_LX_1 A6, DCD5_LX_2 A7
DCD5_FB B4

A6/A7 — L501 LC1U00MK — C550 CC47UWMM2 — V1P05_S

DCD5-6: 1.00uH, 2.5A min, 2.5x2.0 mm footprint, 1.2mm max thickness

VIN_DCD6 B6
DCD6/V1P8A
DCD6_FB B8
DCD6_LX_1 A8, DCD6_LX_2 A9

B8 — V1P80_A
A8/A9 — L502 LC1U00MK — C551 CC47UWMM2 — V1P80_A

DCD3_DIF A25 — 34 DCD3_DIF
DCD3_DIO A26 — 34 DCD3_DIO
DCD3/V3P3A
DCD3_FB A10 — V3P30_A
DCD4_DIF A27 — DCD4_DIF 34
DCD4_DIO A28 — DCD4_DIO 34
DCD4/V1P0A
DCD4_FB B9 — V1P00_A

EPAD — 101

IL09145CXXM1
IL09145CXXM0: -I0 OTP (DCD4=V1P8A,DCD6=V1P0A)
IL09145CXXM1: -A1 OTP (DCD4=V1P0A,DCD6=V1P8A)

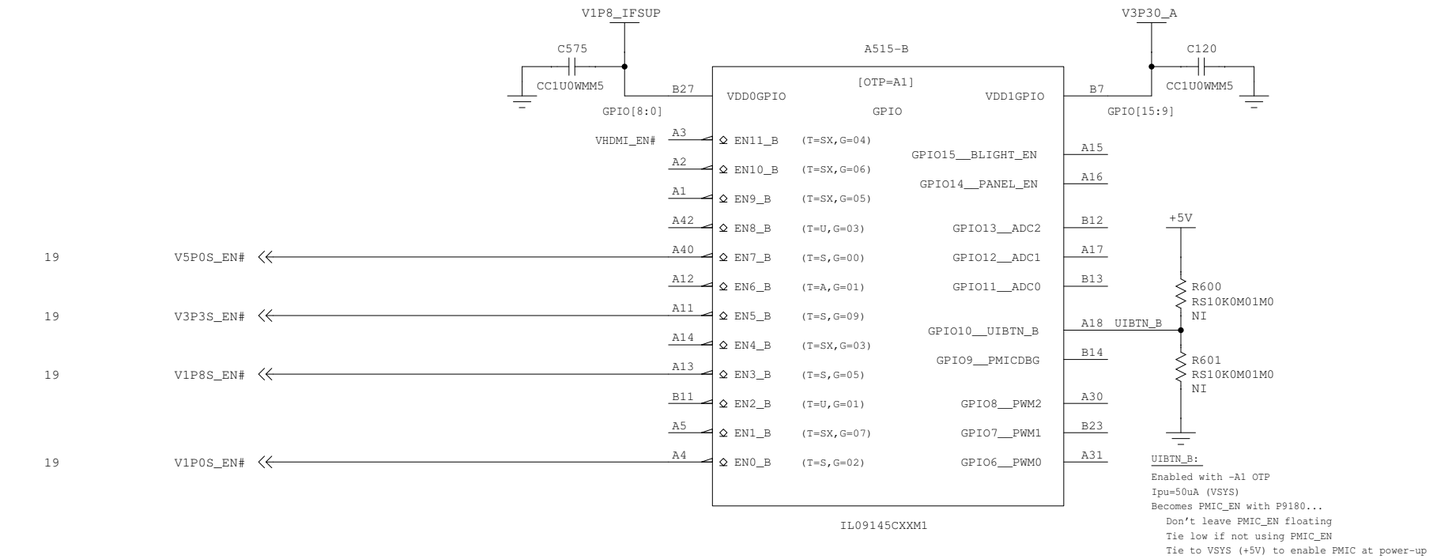
DRAWN	P-O.Lessard
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

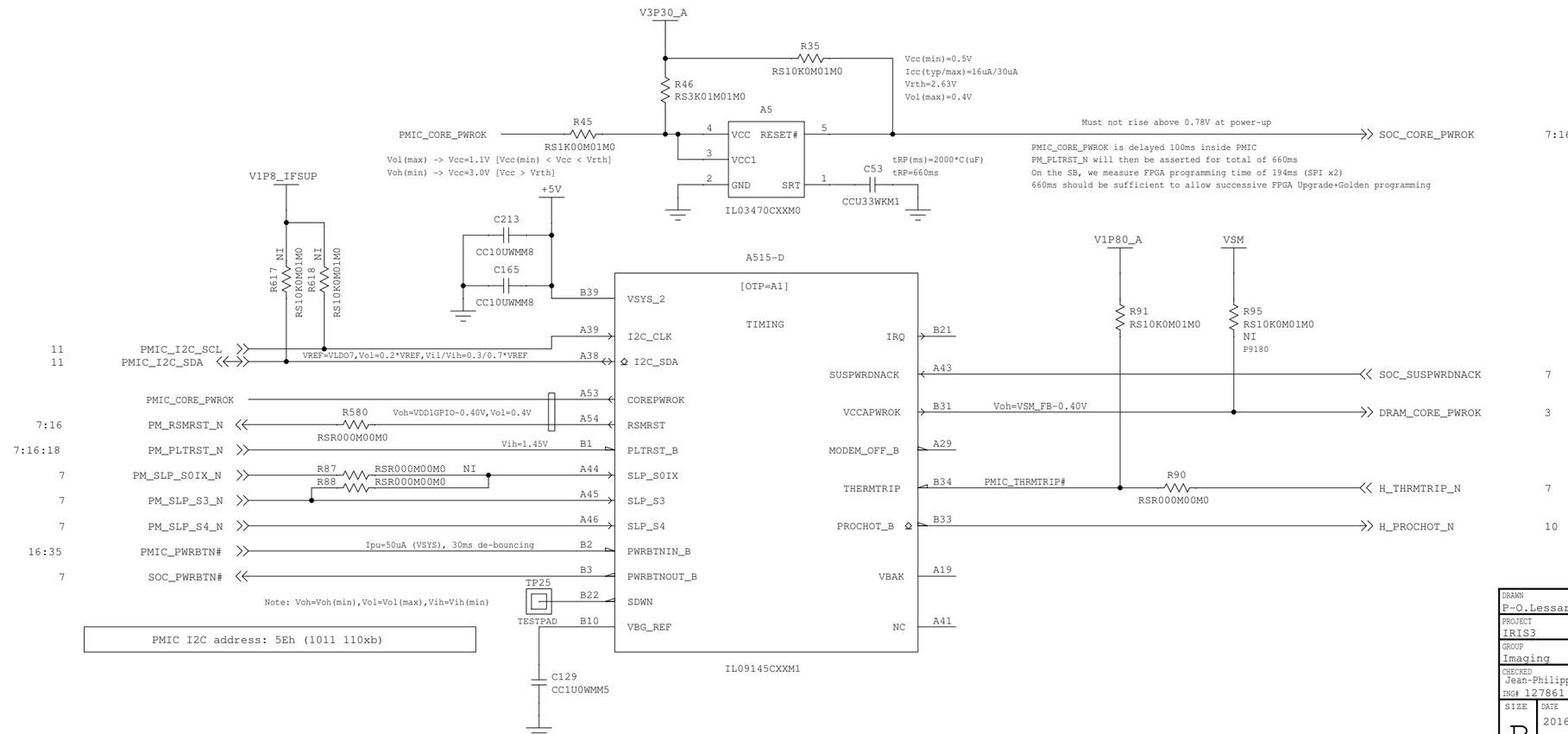
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: PMIC DCD

DRAWING NO	REV	SHEET
7478-04-01	A	31 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			





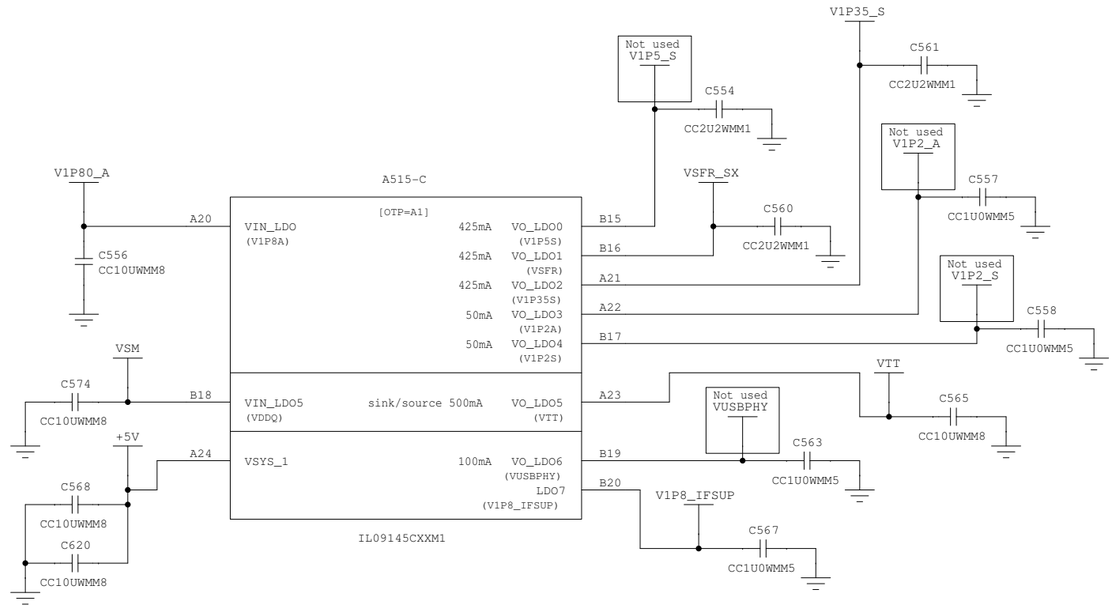
DRAWN	P-O.Lessard
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: PMIC Misc.

DRAWING NO	REV	SHEET
7478-04-01	A	32 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			



LDO0-4,6 Rdis = 10k-ohm
LDO5 Rdis = 80-ohm
DCD0-2 Rdis = 280-ohm
DCD5 Rdis = 850-ohm
DCD6 Rdis = 800-ohm

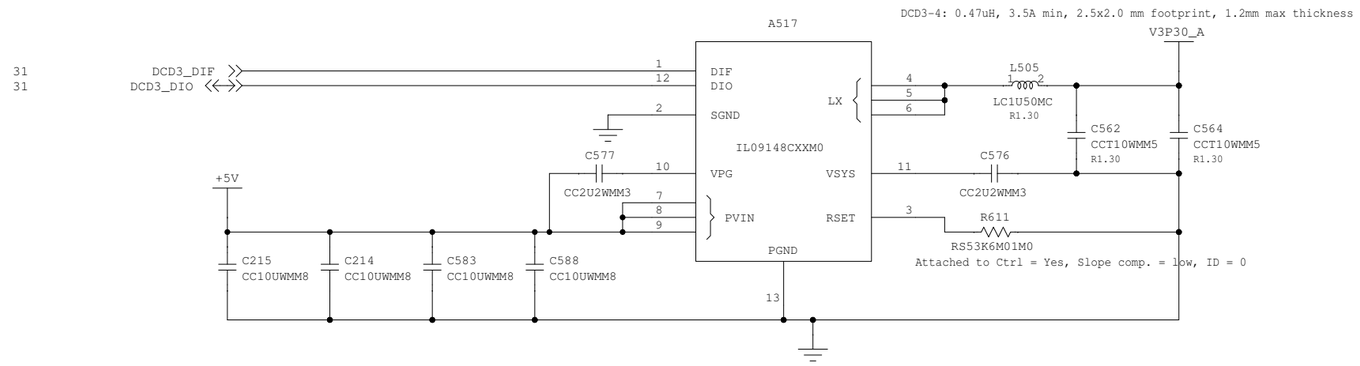
DRAWN	P-O.Lessard
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

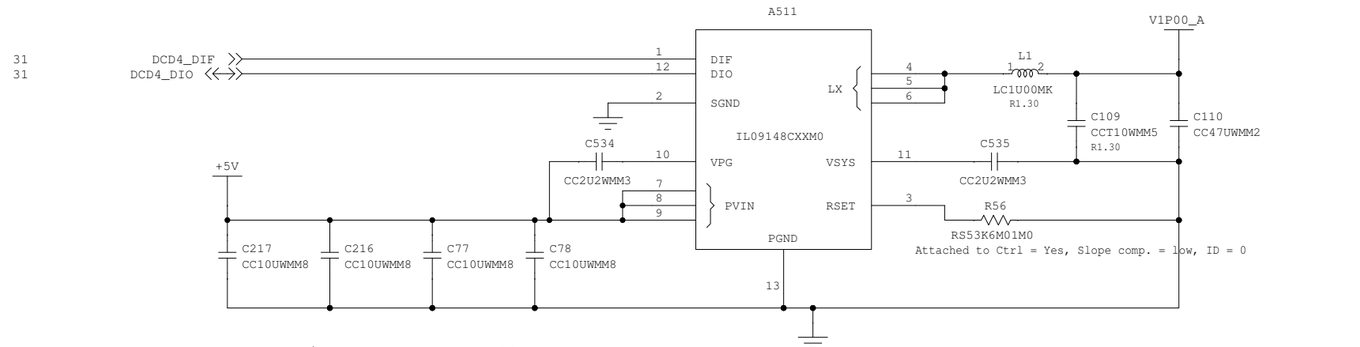
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: PMIC LDO

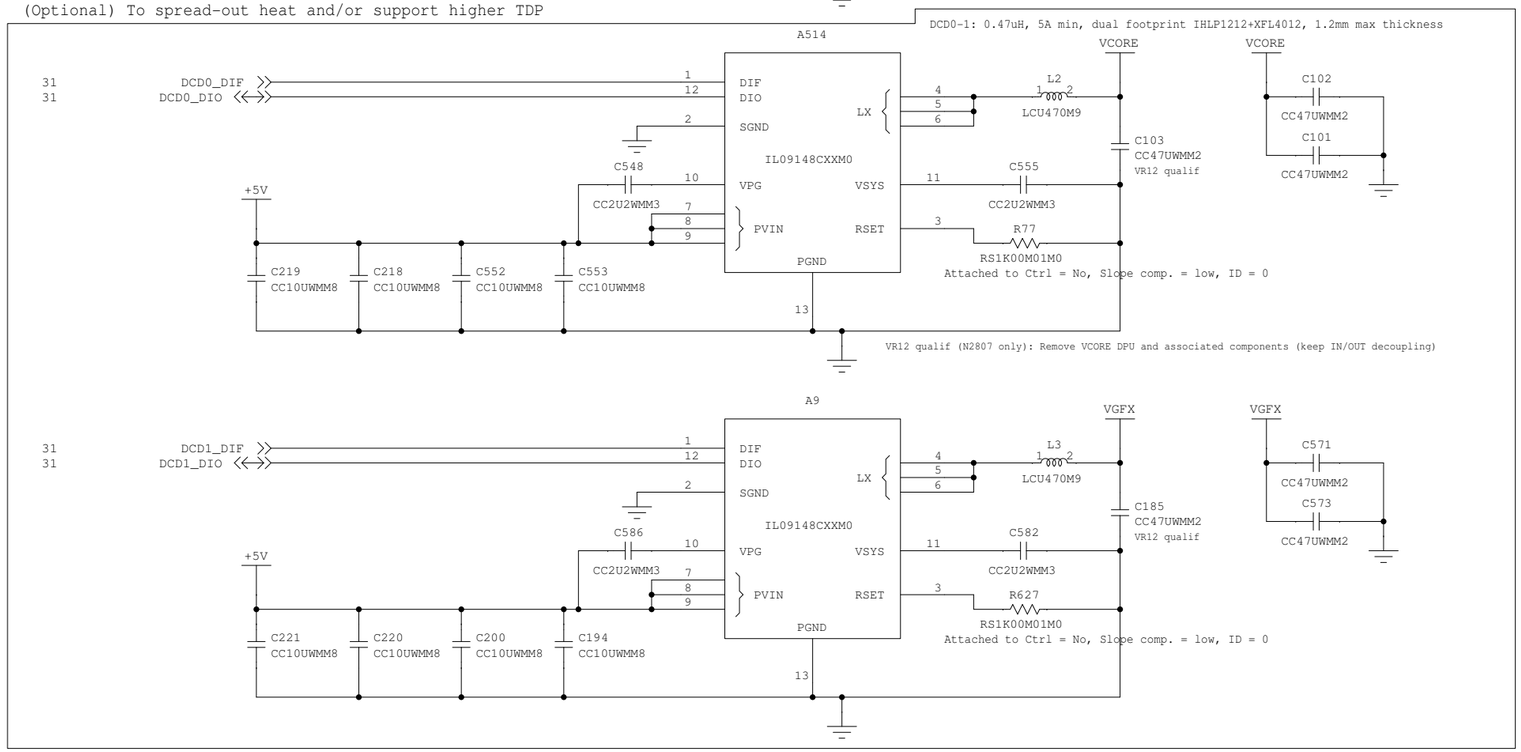
DRAWING NO	REV	SHEET
7478-04-01	A	33 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			





(Optional) To spread-out heat and/or support higher TDP



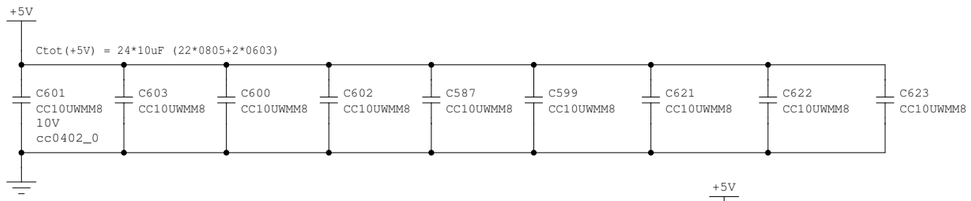
DRAWN	P-O.Lessard
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

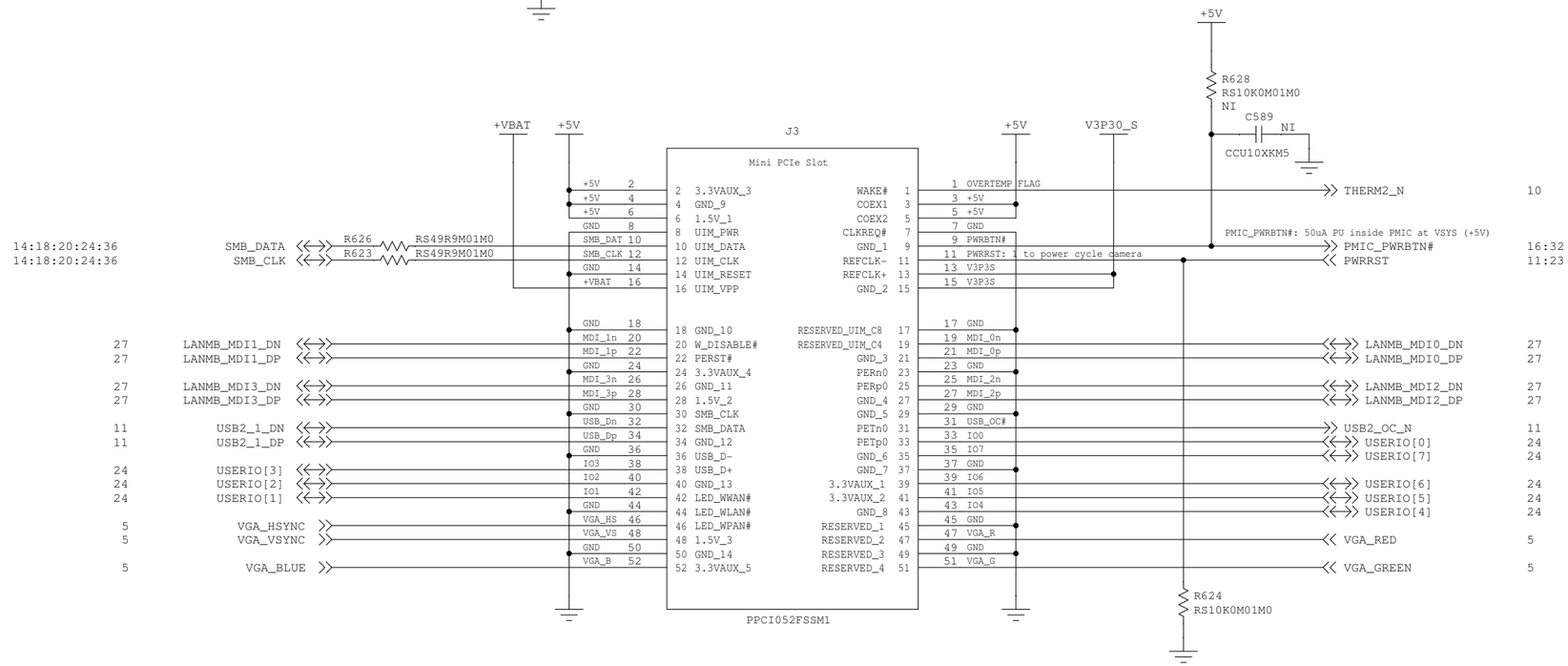
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: PMIC DPUs

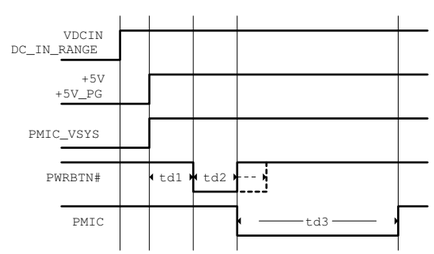
DRAWING NO	REV	SHEET
7478-04-01	A	34 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			





Daughtercard: Assert PWRBTN# with +5V PGD flag



td1: No specific requirement for td1 (suggested to use VSYS PG)
td2: Pulse duration must exceed 30ms deglitch (td2=50ms suggested)
td3: Automatic 500ms delay inserted after 30ms deglitch

DRAWN	JP Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-12-21

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: Daugthercard Expansion

DRAWING NO	REV	SHEET
7478-04-01	A	35 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			

CPU Board ZIF pinout is inverted
SB pos1 aligned with CPU Board pos50
Connectors are head2head with latch on same side

JTAG direction shown: Master is Platform Cable USBII located on ISB

14:18:20:24:35	SMB_CLK	R546 RSK100M01M0		5-12V	50 49	5-12V	R21 RSK100M01M0	SMB_DATA	14:18:20:24:35
				5-12V	48 47	5-12V			
				5-12V	46 45	PRSNT1#			
				GND	44 43	GND			
				SMBCLK	42 41	SMBDAT			
7:22	TCK (To Ares & CPU iTCK)	R40 RSR000M00M0	TCK_R	TCK	40 39	TDI	FPGA_TDO_R	R547 RSR000M00M0 (From Ares oTDO)	FPGA_TDO 7:22
			CPU_TDO_R	TDO	38 37	TMS	TMS_R		
				3.3V	36 35	3.3V			
7	CPU_TDO (To CPU iTDO)	R41 RSR000M00M0		3.3V	34 33	3.3VAUX		R22 RSR000M00M0 (To Ares & CPU iTMS)	TMS 7:22
				TRST#	32 31	PERST#			
				WAKE#	30 29	RSVD			PLTRST_N 18:24:27
				GND	28 27	GND			
7	PE_REFCLK0_P (To Athena PE_REFCLK)			REFCLKp	26 25	REFCLKn			PE_REFCLK0_N 7
				GND	24 23	GND			
10	PE_TX0_P (To Athena PE_RX0)			PETp0	22 21	PETn0			PE_TX0_N 10
				GND	20 19	GND			
10	PE_RX0_P (From Athena PE_TX0)			PERp0	18 17	PERn0			PE_RX0_N 10
				GND	16 15	PRSNT2#			
10	PE_TX1_P (To Athena PE_RX1)			PETp1	14 13	PETn1			PE_TX1_N 10
				GND	12 11	GND			
10	PE_RX1_P (From Athena PE_TX1)			PERp1	10 9	PERn1			PE_RX1_N 10
				GND	8 7	GND			
23	ACQ_EXP	R42 RSK100M01M0	ACQ_EXP_R	ACQ_EXP	6 5	ACQ_STRB	ACQ_STRB_R	R28 RSK100M01M0	ACQ_STRB 23
			ACQ_TRIG_R	ACQ_TRIG	4 3	ACQ_TRIG_RDY	ACQ_TRIG_RDY_R		
23	ACQ_TRIG	R43 RSK100M01M0	ACQ_LED0_R	ACQ_LED0	2 1	ACQ_LED1	ACQ_LED1_R	R29 RSK100M01M0	ACQ_TRIG_RDY 23
23	ACQ_LED0	R44 RSK100M01M0						R30 RSK100M01M0	ACQ_LED1 23

J1

SZIF050ZTSM0

R39 RS68R0M05M0 NI

C69 CCN10XKM1 NI

PRSNT1#: GND on Mobo
PRSNT2#: Pull-up on Mobo (use for SB detection on CPU board)

ISB	Device-side	Host-side	CPUB
1	5-12V	5-12V	50
2	5-12V	5-12V	49
3	5-12V	5-12V	48
4	5-12V	5-12V	47
5	5-12V	5-12V	46
6	PRSNT1#	PRSNT1#	45
7	GND	GND	44
8	GND	GND	43
9	SMBCLK	SMBCLK	42
10	SMBDAT	SMBDAT	41
11	TCK	TCK	40
12	TDI	TDI	39
13	TDO	TDO	38
14	TMS	TMS	37
15	3.3V	3.3V	36
16	3.3V	3.3V	35
17	3.3V	3.3V	34
18	3.3VAUX	3.3VAUX	33
19	TRST#	TRST#	32
20	PERST#	PERST#	31
21	WAKE#	WAKE#	30
22	RSVD	RSVD	29
23	GND	GND	28
24	GND	GND	27
25	REFCLKp	REFCLKp	26
26	REFCLKn	REFCLKn	25
27	GND	GND	24
28	GND	GND	23
29	PERp0	PETp0	22
30	PERn0	PETn0	21
31	GND	GND	20
32	GND	GND	19
33	PETp0	PERp0	18
34	PETn0	PERn0	17
35	GND	GND	16
36	PRSNT2#	PRSNT2#	15
37	PERp1	PETp1	14
38	PERn1	PETn1	13
39	GND	GND	12
40	GND	GND	11
41	PETp1	PERp1	10
42	PETn1	PERn1	9
43	GND	GND	8
44	GND	GND	7
45	ACQ_EXP	ACQ_EXP	6
46	ACQ_STRB	ACQ_STRB	5
47	ACQ_TRIG	ACQ_TRIG	4
48	ACQ_TRIG_RDY	ACQ_TRIG_RDY	3
49	ACQ_LED0	ACQ_LED0	2
50	ACQ_LED1	ACQ_LED1	1

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TITLE: Sensor Board Connector

DRAWING NO	REV	SHEET
7478-04-01	A	36 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7478-91-0100	POL			

Revision History

Y7478-00 Rev.A:

R1.00: First Release

R1.10: Bring-up changes

- XDP: V1P80_A Rpu on SYS_RST_N is now NI (poss.leakage V1P80_S)
- Board ID EEPROM: now installed by default
- eMMC: increased to 32GB
- +VBAT: Rs is now split MB+DC (500+500)
- Bug: same net for DS1-AN and DS2-AN (see PMB 7478-90-000)

Y7478-0001 Rev.A: ECR# 7478-92-0001

R1.20:

- XDP: When used, disconnect CLEAR_CMOS_N from XDP conn.
- PCB change:
  - Removed STATUS_GLED_AN net segment on L3 (DS1-AN/DS2-AN bug)

R1.30:

- Reduced bulk capacitance on VCORE (-2x 47uF)
- Reduced bulk capacitance on VGFX (-2x 47uF)
- Enabled SoC access to JTAG chain (ISB changes also needed)

R1.40:

- Moved to 64GB eMMC (32GB pSLC operation)

Y7478-01 Rev.A: ECO# 7478-91-0100

R1.00: First Release

R1.01:

- Changed p/n for C53 (same value, but valid part)

R1.10:

- Updated SMBus pull-up and damping values
- Removed resistor strapping on JTAG debug signals (not used)

R1.20:

- Changes following VCORE/VGFX (IMVP7/VR12) qualification

R1.30:

- Adjusted VSM, V1P00 and V3P30 (reduced ripple)

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TITLE: REVISION HISTORY [1 OF 2]

DRAWING NO	REV	SHEET
7478-04-01	A	37 OF 38

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
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REVISION HISTORY [2 OF 2]

DOCUMENT# 7478-91-0100

LEVEL# 7478-01-A

- REFERENCES -	- PAGES -	- CHANGES -	- REASON FOR CHANGES -	-TYPE-
-	-	-	-	-
i210	27	Changed CTOP/CBOT C9 for 39nF.	Intel recommendation.	schematic
Sequencing	32	Changed C53 for 0.33uF.	Improvement following bring up stage.	schematic
ECR 7478-92-0001	30	Changed the net name for DS2 to gain control on both LEDs.	Schematic error.	schematic/layout
SB_PRSNT#	7; 36	Removed connection to the SoC BA34 pin and grounded J1-15.	Feature will not be implemented.	schematic/layout
VRTC_3P3	9	Changed and separated Diodes in single package.	CSA considerations and battery manufacturer recommendation.	schematic/layout
MoBo info	18; 20	Added MIL licence protection feature.	Software security improvement.	schematic/layout
LPC	11; 23; 24	Added LPC interface between SoC and FPGA.	To reduce power consumption.	schematic/layout
DDR2 FPGA	23; 26	Changed 32Mx16 84pins to 64Mx8 64pins DDR2 module.	To reduce power consumption and facilitate LPC interface routing.	schematic/layout
SoC UART	11; 23	Connected SoC UART to FPGA.	Added access to SoC UART through FPGA/IOs.	schematic/layout
10uF capacitors	-	Changed all YCC10UWMM7 (0805) per YCC10UWMM8 (0402).	To gain board space.	schematic/layout
+5V; PMIC rails; switched rails	-	Optimized decoupling of power pins.	Decoupling was inefficient.	layout
+5V; PMIC rails; switched rails	-	Reorganized reference plane.	Switching noise was coupled to inner signals.	layout
eMMC	-	Changed VDDI routing.	Possibility of VGA_HSYNC coupling on VDDI.	layout
VGA routing	-	unmatched (M.B.+D.C.+R.F. = +/- 200mils tolerance) RGB signals.	To get more margin on radiated emissions.	layout
Via inpad	-	Added new geometry for via inpad (top; bottom and both).	To facilitate and improve PMIC decoupling.	layout
DDR2 FPGA	-	Changed reference plane V3P30_A for VDD = V1P80_S.	Per TN-46-14 Micron Technology Technical Note document.	layout

DRAWN P-O.Lessard

PROJECT IRIS3

GROUP Imaging

CHECKED Jean-Philippe Gagnon

ING# 127861

SIZE B

DATE 2016-12-21

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TITLE REVISION HISTORY [2 OF 2]

DRAWING NO 7478-04-01

REV A