Register file structure : regfile_xgs_athena.pdf
Created by jmansill on 2021/12/08 09:30:59
Register file CRC32 : 0x4F0D5164

1. Main Parameters

Register file endianness: little endian
Address bus width: 11 bits
Data bus width: 32 bits

2. Memory Map

Section name	Address(es) / Address Ranges	Register name	Access Type
SYSTEM	0x000	TAG	R
	0x004	VERSION	R
	0x008	CAPABILITY	R
	0x00C	SCRATCHPAD	RW
DMA	0x070	CTRL	RW
	0x078	FSTART	RW
	0x07C	FSTART_HIGH	RW
	0x080	FSTART_G	RW
	0x084	FSTART_G_HIGH	RW
	0x088	FSTART_R	RW
	0x08C	FSTART_R_HIGH	RW
	0x090	LINE_PITCH	RW
	0x094	LINE_SIZE	RW
	0x098	CSC	RW
	0x0A8	OUTPUT_BUFFER	RW
	0x0AC	TLP	R
	0x0B0	ROI_X	RW
	0x0BC	ROI_Y	RW
ACQ	0x100	GRAB_CTRL	RW
	0x108	GRAB_STAT	R
	0x110	READOUT_CFG1	RW
	0x114	READOUT_CFG_FRAME_LINE	RW
	0x118	READOUT_CFG2	R
	0x120	READOUT_CFG3	RW
	0x124	READOUT_CFG4	RW
	0x128	EXP_CTRL1	RW
	0x130	EXP_CTRL2	RW
	0x138	EXP_CTRL3	RW
	0x140	TRIGGER_DELAY	RW
	0x148	STROBE_CTRL1	RW
	0x150	STROBE_CTRL2	RW

Section name	Address(es) / Address Ranges	Register name	Access Type
	0x158	ACQ_SER_CTRL	RW
	0x160	ACQ_SER_ADDATA	RW
	0x168	ACQ_SER_STAT	R
	0x190	SENSOR_CTRL	RW
	0x198	SENSOR_STAT	R
	0x19C	SENSOR_SUBSAMPLING	RW
	0x1A4	SENSOR_GAIN_ANA	RW
	0x1A8	SENSOR_ROI_Y_START	RW
	0x1AC	SENSOR_ROI_Y_SIZE	RW
	0x1B8	SENSOR_M_LINES	RW
	0x1BC	SENSOR_DP_GR	RW
	0x1C0	SENSOR_DP_GB	RW
	0x1C4	SENSOR_DP_R	RW
	0x1C8	SENSOR_DP_B	RW
	0x1CC	SENSOR_GAIN_DIG_G	RW
	0x1D0	SENSOR_GAIN_DIG_RB	RW
	0x1E0	DEBUG_PINS	RW
	0x1E8	TRIGGER_MISSED	RW
	0x1F0	SENSOR_FPS	R
	0x1F4	SENSOR_FPS2	R
	0x2A0	DEBUG	RW
	0x2A8	DEBUG_CNTR1	R
	0x2B0	DEBUG_CNTR2	R
	0x2B4	DEBUG_CNTR3	R
	0x2B8	EXP_FOT	RW
	0x2C0	ACQ_SFNC	RW
	0x2D0	TIMER_CTRL	RW
	0x2D4	TIMER_DELAY	RW
	0x2D8	TIMER_DURATION	RW
HISPI	0x400	CTRL	RW
	0x404	STATUS	R
	0x408	IDELAYCTRL_STATUS	R
	0x40C	IDLE_CHARACTER	RW
	0x410	PHY	RW
	0x414	FRAME_CFG	RW
	0x418	FRAME_CFG_X_VALID	RW
	0x424, 0x428, ... ,0x438	LANE_DECODER_STATUS (5:0)	RW
	0x43C, 0x440, ... ,0x450	TAP_HISTOGRAM (5:0)	R
	0x454	DEBUG	RW
DPC	0x480	DPC_CAPABILITIES	R
	0x484	DPC_LIST_CTRL	RW
	0x488	DPC_LIST_STAT	R
	0x48C	DPC_LIST_DATA1	RW
	0x490	DPC_LIST_DATA2	RW
	0x494	DPC_LIST_DATA1_RD	R
	0x498	DPC_LIST_DATA2_RD	R

Section name	Address(es) / Address Ranges	Register name	Access Type
LUT	0x4B0	LUT_CAPABILITIES	R
	0x4B4	LUT_CTRL	RW
	0x4B8	LUT_RB	R
BAYER	0x4C0	BAYER_CAPABILITIES	R
	0x4C4	WB_MUL1	RW
	0x4C8	WB_MUL2	RW
	0x4CC	WB_B_ACC	R
	0x4D0	WB_G_ACC	R
	0x4D4	WB_R_ACC	R
	0x4D8	CCM_CTRL	RW
	0x4DC	CCM_KR1	RW
	0x4E0	CCM_KR2	RW
	0x4E4	CCM_KG1	RW
	0x4E8	CCM_KG2	RW
	0x4EC	CCM_KB1	RW
	0x4F0	CCM_KB2	RW
SYSMONXIL	0x700	TEMP	R
	0x704	VCCINT	R
	0x708	VCCAUX	R
	0x718	VCCBRAM	R
	0x780	TEMP_MAX	R
	0x790	TEMP_MIN	R

Section: SYSTEM

Address Range: [0x000 - 0x00C]

TAG

Address: section "SYSTEM" base address + 0x000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
VALUE(23:16)							
15	14	13	12	11	10	9	8
VALUE(15:8)							
7	6	5	4	3	2	1	0
VALUE(7:0)							

VALUE (23:0) *STATIC*	Tag identifier	
Value at Reset:	0x58544d	
Possible Values:	0x58544D	MTX ASCII string

VERSION — Register file version

Address: section "SYSTEM" base address + 0x004

Description:

Revisions

0.1.0 : First functionnal revision

0.2.0 : Removed tha lane_packer module

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAJOR(7:0)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MINOR(7:0)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HW(7:0)							

MAJOR (7:0)	
STATIC	
Value at Reset:	0x0

MINOR (7:0)	
STATIC	
Value at Reset:	0x2

HW (7:0)	
STATIC	
Value at Reset:	0x0

Address: section "SYSTEM" base address + 0x008

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
VALUE(7:0)							

VALUE (7:0) *STATIC*	
Value at Reset:	0x0

Address: section "SYSTEM" base address + 0x00C

31	30	29	28	27	26	25	24
VALUE(31:24)							
23	22	21	20	19	18	17	16
VALUE(23:16)							
15	14	13	12	11	10	9	8
VALUE(15:8)							
7	6	5	4	3	2	1	0
VALUE(7:0)							

VALUE (31:0) *RW*	
Value at Reset:	0x0

Section: DMA

Address Range: [0x070 - 0x0C4]

CTRL — Initial Grab Address Register

Address: section "DMA" base address + 0x000

Description:

Initial Grab Address LOW 32 bits

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							GRAB_QUEUE_EN

GRAB_QUEUE_EN *RW*		
Value at Reset:	0x0	
Possible Values:	0x0	
	0x1	

Address: section "DMA" base address + 0x008

Description:

Initial Grab Address LOW 32 bits

31	30	29	28	27	26	25	24
VALUE(31:24)							
23	22	21	20	19	18	17	16
VALUE(23:16)							
15	14	13	12	11	10	9	8
VALUE(15:8)							
7	6	5	4	3	2	1	0
VALUE(7:0)							

VALUE (31:0)	INitial GRAb ADDRess Register	
RW	This is the address in the host ram where the grab engine will start writing pixel data.	
Value at Reset:	0x0	
Possible Values:	Any Value	

Address: section "DMA" base address + 0x00C

Description:

Initial Grab Address HI 32 bits

31	30	29	28	27	26	25	24
VALUE(31:24)							
23	22	21	20	19	18	17	16
VALUE(23:16)							
15	14	13	12	11	10	9	8
VALUE(15:8)							
7	6	5	4	3	2	1	0
VALUE(7:0)							

VALUE (31:0)	INitial GRAb ADDRess Register High	
RW	This is the high 32 bits of the 64-bit addresess in the host ram where the grab engine will start writing pixel data.	
Value at Reset:	0x0	
Possible Values:	Any Value	

Address: section "DMA" base address + 0x010

Description:

Grab Address LOW 32 bits for the Green plane. Only used when grabbing in Planar mode.

31	30	29	28	27	26	25	24
VALUE(31:24)							
23	22	21	20	19	18	17	16
VALUE(23:16)							
15	14	13	12	11	10	9	8
VALUE(15:8)							
7	6	5	4	3	2	1	0
VALUE(7:0)							

VALUE (31:0)	GRAb ADDRess Register	
RW	This is the address in the host ram where the grab engine will start writing pixel data.	
Value at Reset:	0x0	
Possible Values:	Any Value	

FSTART_G_HIGH — Green Grab Address Register HIGH 32 bits

Address: section "DMA" base address + 0x014

Description:

Green Grab Address HIGH 32 bits

31	30	29	28	27	26	25	24
VALUE(31:24)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VALUE(23:16)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VALUE(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VALUE(7:0)							

VALUE (31:0) *RW*	GRAb ADDRess Register High This is the high part of the 64-bit addresess in the host ram where the grab engine will start writing pixel data.	
Value at Reset:	0x0	
Possible Values:	Any Value	Any value

FSTART_R Red Grab Address Register

Address: section "DMA" base address + 0x018

Description:

Grab Address LOW 32 bits for the Red plane. Only used when grabbing in Planar mode.

31	30	29	28	27	26	25	24
VALUE(31:24)							
23	22	21	20	19	18	17	16
VALUE(23:16)							
15	14	13	12	11	10	9	8
VALUE(15:8)							
7	6	5	4	3	2	1	0
VALUE(7:0)							

VALUE (31:0)	GRAb ADDRess Register	
RW	This is the address in the host ram where the grab engine will start writing pixel data.	
Value at Reset:	0x0	
Possible Values:	Any Value	Any value

Address: section "DMA" base address + 0x01C

Description:

Red Grab Address HIGH 32 bits

31	30	29	28	27	26	25	24
VALUE(31:24)							
23	22	21	20	19	18	17	16
VALUE(23:16)							
15	14	13	12	11	10	9	8
VALUE(15:8)							
7	6	5	4	3	2	1	0
VALUE(7:0)							

VALUE (31:0)	GRAb ADDRess Register High	
RW	This is the high part of the 64-bit addresess in the host ram where the grab engine will start writing pixel data.	
Value at Reset:	0x0	
Possible Values:	Any Value	Any value

Address: section "DMA" base address + 0x020

Description:

Grab Line Pitch Register

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
VALUE(15:8)							
7	6	5	4	3	2	1	0
VALUE(7:0)							

VALUE (15:0)	Grab LinePitch
RW	This is the line pitch when writing in ram. It is measured in bytes, not pixels.
Value at Reset:	0x0

Address: section "DMA" base address + 0x024

Description:

Host Line Size Register.

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved	VALUE(14:8)						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VALUE(7:0)							

VALUE (14:0)	Host Line size	
RW	This is the line size when writing in host ram. It is measured in bytes, not pixels. If this register is higher than the actual data provided by the sensor, stray data will be written into host memory. If this register is lower than the data provided by the sensor, image data will be cropped at the end of the line. For backward compatibility, the value of 0 indicates that the FPGA should auto-compute the line sized based on data provided by the sensor interface.	
Value at Reset:	0x0	
Possible Values:	0x1 - 0x7FFF	Written line size in host frame.
	0x0	Auto-compute line size from sensor data.

CSC

Address: section "DMA" base address + 0x028

31	30	29	28	27	26	25	24
Reserved					COLOR_SPACE(2:0)		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved		SUB_X(3:0)				REVERSE_Y	REVERSE_X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

COLOR_SPACE (2:0)		
RW	Output color space used to transfer data to the DMA engine.	
Value at Reset:	0x0	
Possible Values:	0x0	Reserved for Mono sensor operation
	0x1	BGR32
	0x2	YUV 4:2:2 in full range
	0x3	Planar 8-bits
	0x4	Y only with color sensor
	0x5	RAW color pixels (For color sensor only, 8bpp)

SUB_X (3:0)		
RW		
Value at Reset:	0x0	
Possible Values:	0x0	No subsampling
	0x1	1/2
	0x2	1/3
	0x3	1/4
	0x4	1/5

REVERSE_Y	REVERSE Y	
RW	Reverse readout	
Value at Reset:	0x0	
Possible Values:	0x0	Bottom to top readout
	0x1	Top to bottom readout

REVERSE_X	Reverse image in X direction	
RW	When this field is set each row is mirorred while streamed out. Miror process is applied on a pixel resolution. This means for multi-bytes pixels, bytes are always streamed in the right order.	
Value at Reset:	0x0	
Possible Values:	0x0	Reverse X disabled
	0x1	Reverse X enabled

Address: section "DMA" base address + 0x038

31	30	29	28	27	26	25	24
Reserved	MAX_LINE_BUFF_CNT(2:0)			Reserved		LINE_PTR_WIDTH(1:0)	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADDRESS_BUS_WIDTH(3:0)				Reserved			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			PCIE_BACK_PRESSURE	Reserved			CLR_MAX_LINE_BUFF_CNT

MAX_LINE_BUFF_CNT (2:0)	Maximum line buffer count
RO	This is an elastic line buffer. This fields records maximum number of line buffer that was used for transfering data. This field is cleared by the system reset and can also be cleared by the field registerfile.DMA.OUTPUT_BUFFER.CLR_MAX_LINE_BUFF_CNT

LINE_PTR_WIDTH (1:0)	Line pointer size (in bits)	
RW	Set the line pointer size (in bits) 3 = 3 bits wide : The full memory buffer is divided in 8 sub line buffers	
Value at Reset:	0x2	
Possible Values:	0x0	Not valid
	0x1	The buffer is divided in 2 line buffers
	0x2	The buffer is divided in 4 line buffers
	0x3	The buffer is divided in 8 line buffers

ADDRESS_BUS_WIDTH (3:0)	Line buffer address size in bits
RO	Indicate to the software the size of the DMA output line buffer address bus in bits. For example for a 11 bits address bus, the buffer size in bytes is : 2pow(11) * 8 bytes = 16KB (16384 bytes)

PCIE_BACK_PRESSURE	PCIE link back pressure detected	
RW2C	Indicates that the DMA line buffer was full while the XGS sensor was still pushing data. When this occures the Athena rely on the buffering (FiFo) along the data path as the last ressort to absorb the pcie back pressure. This should not occur.	
Value at Reset:	0x0	
Possible Values:	0x0	No effect
	0x1	Back pressure detected on PCIe

CLR_MAX_LINE_BUFF_CNT *WO/AutoClr*	Clear maximum line buffer count	
Possible Values:	0x0	No effect
	0x1	Clear the max count

Address: section "DMA" base address + 0x03C

31	30	29	28	27	26	25	24
Reserved				MAX_PAYLOAD(11:8)			
23	22	21	20	19	18	17	16
MAX_PAYLOAD(7:0)							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				BUS_MASTER_EN	CFG_MAX_PLD(2:0)		

MAX_PAYLOAD (11:0)	
RO	

BUS_MASTER_EN	
RO	

CFG_MAX_PLD (2:0)	PCIe Device Control Register (Offset 08h); bits 7 downto 5	
RO	See PCIe Baser2.1, Section 7.8.4. Device Control Register (Offset 08h) This field indicates the maximum TLP payload size allowed by the host for this Function. As a Receiver, the Function must handle TLPs as large as the set value. As a Transmitter, the Function must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register (see Section 7.8.3). Functions that support only the 128-byte max payload size are permitted to hardwire this field to 000b. System software is not required to program the same value for this field for all the Functions of a multi-Function device. Refer to Section 2.2.2 for important guidance. For ARI Devices, Max_Payload_Size is determined solely by the setting in Function 0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Default value of this field is 000b.	
Possible Values:	0x0	128 bytes max payload size
	0x1	256 bytes max payload size
	0x2	512 bytes max payload size
	0x3	1024 bytes max payload size
	Others	Not supported by Xilinx endpoint

ROI_X

Address: section "DMA" base address + 0x040

31	30	29	28	27	26	25	24
ROI_EN	Reserved		X_SIZE(12:8)				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
X_SIZE(7:0)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved			X_START(12:8)				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
X_START(7:0)							

ROI_EN	Region of interest enable	
RW	This bit activate the region of interest mechanism (cropping). If enabled, this mechanism rely on the X_START and X_SIZE parameters todetermine the valid region of a row. If ROI_EN is disabled the full sensor image is sent to the host. The first valide pixel is located at X_START and the last valid pixel is located at at X_STOP = X_START + (X_SIZE -1)	
Value at Reset:	0x0	
Possible Values:	0x0	Region of interest is disabled
	0x1	Region of interest is enabled

X_SIZE (12:0)	
RW	This register defines the size in pixels of the region of interest (On the X axis)
Value at Reset:	0x3ff

X_START (12:0)	
RW	This register defines the position of the first horizontal valid pixel (including interpolation pixels).
Value at Reset:	0x0

ROI_Y

Address: section "DMA" base address + 0x04C

31	30	29	28	27	26	25	24
ROI_EN	Reserved		Y_SIZE(12:8)				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Y_SIZE(7:0)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved			Y_START(12:8)				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Y_START(7:0)							

ROI_EN	Region of interest enable	
RW	This bit activate the region of interest mechanism (cropping)in the Y axix. If enabled, this mechanism rely on the Y_START and Y_SIZE parameters to determine the valid region of a row. If ROI_EN is disabled the full sensor image is sent to the host. The first valide line is located at Y_START and the last valid line is located at at Y_STOP = Y_START + (Y_SIZE -1)	
Value at Reset:	0x0	
Possible Values:	0x0	Region of interest is disabled
	0x1	Region of interest is enabled

Y_SIZE (12:0)	
RW	This register defines the size in lines of the region of interest .
Value at Reset:	0x3ff

Y_START (12:0)	
RW	This register defines the position of the first vertical valid line.
Value at Reset:	0x0

Section: ACQ

Address Range: [0x100 - 0x2D8]

GRAB_CTRL — GRAB ConTRoL Register

Address: section "ACQ" base address + 0x000

Description:

Grag Control Register

31	30	29	28	27	26	25	24
RESET_GRAB	Reserved	GRAB_ROI2_EN	ABORT_GRAB	Reserved			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							TRIGGER_OVERLAP_BUFFn
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TRIGGER_OVERLAP	TRIGGER_ACT(2:0)			Reserved	TRIGGER_SRC(2:0)		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			GRAB_SS	Reserved		BUFFER_ID	GRAB_CMD

RESET_GRAB		
RW	This register resets the entire XGS ctrl.	
Value at Reset:	0x0	
Possible Values:	0x0	Reset not active
	0x1	Reset active

GRAB_ROI2_EN		
RW	Enable the second ROI on the frame (KNS). This register is not DB. 1) No Y overlap is allowed 2) Xsize must be the same for the two ROI for the moment(DMA constraint). 3) EOF and SOF in between the two in-frame ROIs will be masked to the DMA. The DMA will see one frame, with the two ROI inside.	
Value at Reset:	0x0	
Possible Values:	0x0	Dual ROI disable
	0x1	Dual ROI enable

ABORT_GRAB	ABORT GRAB	
WO/AutoClr	This is the grab Abort signal, it will reset all the grab queued.	
Possible Values:	0x0	Normal operation
	0x1	Reset Grab

TRIGGER_OVERLAP_BUFFn		
RW	NOT FULLY VALIDATED. DON'T USE. SET IT TO '0'.	
Value at Reset:	0x0	
Possible Values:	0x0	Buffer the trigger received during the dead window in PET mode and execute
	0x1	The trigger will be ignored during dead window in PET mode.

TRIGGER_OVERLAP		
RW	This field enables the trigger overlap. In this mode the exposure and the readout of the sensor can be done in parallel for higher framerates.	
Value at Reset:	0x1	
Possible Values:	0x0	Trigger Overlap disable
	0x1	Trigger Overlap enable (default)

TRIGGER_ACT (2:0)	TRIGGER ACTivation	
RW	This is the trigger activation . This register selects the activation of the trigger when the trigger source is set to Hardware Snapshop mode . This register is Double Buffered, so the trigger activation may change from one grab command to another. In activation Level HI/LO with EXPOSURE_MODE register set to Timed, the camera will be triggered in continuous way if the level of the external trigger remains at the LEVEL programmed in this register. In activation Level HI/LO with EXPOSURE_MODE register set to Trigger Width, the Exposure time will be set by the level of the trigger input. The FPGA exposure regsiters will be ignored. The Dual and Triple slope are not supported in the mode.	
Value at Reset:	0x0	
Possible Values:	0x0	Rising edge
	0x1	Falling edge
	0x2	Rising or Falling edge
	0x3	Level HI
	0x4	Level LO
	0x5	Internal Programmable Timer Trigger
	0x6	RESERVED
	0x7	RESERVED

TRIGGER_SRC (2:0)	TRIGGER SouRCe	
RW	This is the trigger source. This register selects the source of the grab trigger. This register is Double Buffered, so the trigger source may change from one grab command to another. TRIGGER_SRC(1) may be seen as a TRIGGER_STATE by the software driver.	
Value at Reset:	0x0	
Possible Values:	0x0	RESERVED
	0x1	Immediate mode (Continuous)
	0x2	Hardware Snapshop mode
	0x3	Software Snapshot mode
	0x4	SFNC mode (auto trig)

GRAB_SS	GRAB Software Snapshot	
WO/AutoClr	This is the software snapshot register when the trigger source selected is Software Snapshot mode.	
Possible Values:	0x0	Idle
	0x1	Start a grab

BUFFER_ID	
RW	This is the ID of the DMA parameters to associate with this grab command.
Value at Reset:	0x0

GRAB_CMD	GRAB CoMmanD	
WO/AutoClr	This is MIL GRAB command. When the trigger source is set to Immediate mode(Continuous), an exposure sequence will be automatically executed. When the trigger source is set to Software Snapshop mode or Hardware Snapshop mode, GRAB_CMD will act as an ARM. The GRAB_CMD will take around 13 clks to reccord the grab parametters to the SPI fifo. The GRAB_CMD_DONE register may be readed to avoid fifo corruption before sending another Grab command instruction.	
Possible Values:	0x0	Idle
	0x1	Start grab command

GRAB_STAT

Address: section "ACQ" base address + 0x008

31	30	29	28	27	26	25	24
GRAB_CMD_DONE	ABORT_PET	ABORT_DELAI	ABORT_DONE	Reserved			TRIGGER_RDY
23	22	21	20	19	18	17	16
Reserved	ABORT_MNGR_STAT(2:0)			TRIG_MNGR_STAT(3:0)			
15	14	13	12	11	10	9	8
Reserved	TIMER_MNGR_STAT(2:0)			GRAB_MNGR_STAT(3:0)			
7	6	5	4	3	2	1	0
Reserved	GRAB_FOT	GRAB_READOUT	GRAB_EXPOSURE	Reserved	GRAB_PENDING	GRAB_ACTIVE	GRAB_IDLE

GRAB_CMD_DONE	GRAB CoMmanD DONE	
RO	The GRAB_CMD will take around 13 clks to reccord the grab parametters to the SPI fifo. This register may be readed to avoid fifo corruption before sending another Grab command instruction.	
Possible Values:	0x0	Grab Command in process
	0x1	Grab command idle

ABORT_PET	ABORT during PET	
RO	This is the ABORT PET flag. It is set to '1' when an abort is detected in the PETengin phase of the trigger. It is set back to '0' when ABORT_DONE is set to '1'.	
Possible Values:	0x0	Abort in PET Phase idle
	0x1	Abort in PET Phase active

ABORT_DELAI		
RO	This is the ABORT DELAI flag. It is set to '1' when an abort is detected in the delai phase of the trigger. It is set back to '0' when ABORT_DONE is set to '1'.	
Possible Values:	0x0	Abort in Delai Phase idle
	0x1	Abort in Delai Phase active

ABORT_DONE	ABORT is DONE	
RO	This read-only field indicates the RESET_GRAB command status. If 0, an abort sequence is executing.	
Possible Values:	0x0	Abort sequence not finished yet
	0x1	Abort DONE, or not started (reset value)

TRIGGER_RDY	
RO	

ABORT_MNGR_STAT (2:0)	
RO	DEBUG ABORT MANAGER STATE MACHINE

TRIG_MNGR_STAT (3:0)	
RO	DEBUG TRIGGER MANAGER STATE MACHINE

TIMER_MNGR_STAT (2:0)	
RO	DEBUG TIMER MANAGER STATE MACHINE

GRAB_MNGR_STAT (3:0)	
RO	DEBUG GRAB MANAGER STATE MACHINE

GRAB_FOT	GRAB Field Overhead Time	
RO	This is the sensor FOT (Field Overhead Time).	
Possible Values:	0x0	Not in FOT
	0x1	In FOT

GRAB_READOUT	
RO	This is the sensor readout status. It goes to '1' on the SO_FOT and goes to '0' when the datapath decoder decodes the end of frame.

GRAB_EXPOSURE		
RO	This is the sensor integration status	
Possible Values:	0x0	Idle
	0x1	Integrating

GRAB_PENDING		
RO	Grab pending status. When this register is set to one, a second grab command is queued in the fpga.	
Possible Values:	0x0	No grab pending
	0x1	Grab pending

GRAB_ACTIVE	
RO	Grab active status. When this register is set to one, at least one grab command has been received.

GRAB_IDLE		
RO	GRAB IDLE status. When this register is set to '1', The grab engin is in idle state.	
Possible Values:	0x0	Grab is in proccess
	0x1	Grab is Idle

READOUT_CFG1

Address: section "ACQ" base address + 0x010

31	30	29	28	27	26	25	24
Reserved			FOT_LENGTH_LINE(4:0)				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							EO_FOT_SEL
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FOT_LENGTH(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FOT_LENGTH(7:0)							

FOT_LENGTH_LINE (4:0) *RW*	Frame Overhead Time LENGTH LINE This is the length of the Frame Overhead Time in line_time unit.	
Value at Reset:	0x0	
Possible Values:	Any Value	Any 16 bit value

EO_FOT_SEL *RW*	This selector selects who will generate the EO_FOT in the controller. When select 0, the EO_FOT is the falling edge detection of the monitor FOT. When select 1, the EO_FOT will be generated inside the controller with programmed FOT_LENGTH.
Value at Reset:	0x0

FOT_LENGTH (15:0) *RW*	Frame Overhead Time LENGTH This is the length of the Frame Overhead Time in sys clock. This register is calculated from FOT_LENGTH_LINE and LINE_TIME. It is used when EO_FOT_SEL is set to 1.	
Value at Reset:	0x0	
Possible Values:	Any Value	Any 16 bit value

READOUT_CFG_FRAME_LINE

Address: section "ACQ" base address + 0x014

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DUMMY_LINES(7:0)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved			CURR_FRAME_LINES(12:8)				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_FRAME_LINES(7:0)							

DUMMY_LINES (7:0)	
RW	Number of lines to add in the readout (to debug XGS)
Value at Reset:	0x0

CURR_FRAME_LINES (12:0)	
RO	Current number of lines in the readout calculated by the XGS controller (without FOT).

READOUT_CFG2

Address: section "ACQ" base address + 0x018

31	30	29	28	27	26	25	24
Reserved			READOUT_LENGTH(28:24)				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
READOUT_LENGTH(23:16)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
READOUT_LENGTH(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
READOUT_LENGTH(7:0)							

READOUT_LENGTH (28:0)		
RO	This is the readout length register. This register is calculated by the FPGA in the IRIS4 projectand gives the readout lenght without the FOT. This register will depend on the ROI, and Subsampling mode. It is used in the PET engin calculations. In Sys_Clock domain.	
Possible Values:	Any Value	Any 24 bits value

READOUT_CFG3

Address: section "ACQ" base address + 0x020

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LINE_TIME(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LINE_TIME(7:0)							

LINE_TIME (15:0)	LINE TIME	
RW	This register definel the length of one line of the sensor. It includes blanking and valid time . Line Time Unit is SENSOR Clock Cycles	
Value at Reset:	0x16e	
Possible Values:	Any Value	between 1 and 255

READOUT_CFG4

Address: section "ACQ" base address + 0x024

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							KEEP_OUT_TRIG_ENA
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEEP_OUT_TRIG_START(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KEEP_OUT_TRIG_START(7:0)							

KEEP_OUT_TRIG_ENA	
RW	KEEPOUT zone TRIGger ENAble. When this register is enabled, then the trigger output will be synchronized with the line_int(monitor2) signal from the XGS sensor. To configure this keep out zone, use register READOUT_CFG4.
Value at Reset:	0x0

KEEP_OUT_TRIG_START (15:0)	
RW	During the line time, this register indicates the start of the trigger keep-out zone.
Value at Reset:	0xffff

EXP_CTRL1

Address: section "ACQ" base address + 0x028

31	30	29	28	27	26	25	24
Reserved			EXPOSURE_LEV_MODE	EXPOSURE_SS(27:24)			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EXPOSURE_SS(23:16)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXPOSURE_SS(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EXPOSURE_SS(7:0)							

EXPOSURE_LEV_MODE	EXPOSURE LEVel MODE	
RW	This is the exposure level mode selector. When selecting the TRIGGER ACTIVATION = Level Mode, this register selects the exposure method used. When this register is set to '0' the timed mode is selected; Register EXPOSURE_SS is used for the exposure time. When this register is set to '1' the external trigger width is used for the exposure time.	
Value at Reset:	0x0	
Possible Values:	0x0	Timed Mode
	0x1	Trigger Width

EXPOSURE_SS (27:0)	EXPOSURE Single Slope	
RW	This is the total exposure time in single/dual/triple slope mode. This register is double buffered.	
Value at Reset:	0x0	
Possible Values:	Any Value	Any 28 bits value

EXP_CTRL2

Address: section "ACQ" base address + 0x030

31	30	29	28	27	26	25	24
Reserved				EXPOSURE_DS(27:24)			
23	22	21	20	19	18	17	16
EXPOSURE_DS(23:16)							
15	14	13	12	11	10	9	8
EXPOSURE_DS(15:8)							
7	6	5	4	3	2	1	0
EXPOSURE_DS(7:0)							

EXPOSURE_DS (27:0)	EXPOSURE Dual	
RW	This is a new 3d profiler feature We will be able to program upto 3 diferent exposure times (using unused multiSlope registers) Then we will be able to sequence those exposure times . Selection is made with input exposure_select.	
Value at Reset:	0x0	
Possible Values:	Any Value	Any 28 bits value

EXP_CTRL3

Address: section "ACQ" base address + 0x038

31	30	29	28	27	26	25	24
Reserved				EXPOSURE_TS(27:24)			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EXPOSURE_TS(23:16)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXPOSURE_TS(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EXPOSURE_TS(7:0)							

EXPOSURE_TS (27:0)	EXPOSURE Tripple	
RW	This is a new 3d profiler feature We will be able to program upto 3 diferent exposure times (using unused multiSlope registers) Then we will be able to sequence those exposure times . Selection is made with input exposure_select.	
Value at Reset:	0x0	
Possible Values:	Any Value	Any 28 bits value

TRIGGER_DELAY

Address: section "ACQ" base address + 0x040

31	30	29	28	27	26	25	24
Reserved				TRIGGER_DELAY(27:24)			
23	22	21	20	19	18	17	16
TRIGGER_DELAY(23:16)							
15	14	13	12	11	10	9	8
TRIGGER_DELAY(15:8)							
7	6	5	4	3	2	1	0
TRIGGER_DELAY(7:0)							

TRIGGER_DELAY (27:0)	TRIGGER DELAY	
RW	This is the trigger delay. This trigger delay can be applied to HW(Only edge mode), SW and Continuous mode. In HW level mode, the trigger cannot be delayed, since the level time represents the exposure time. This register is double buffered	
Value at Reset:	0x0	
Possible Values:	Any Value	Any 28 bits value

STROBE_CTRL1

Address: section "ACQ" base address + 0x048

31	30	29	28	27	26	25	24
STROBE_E	Reserved		STROBE_POL	STROBE_START(27:24)			
23	22	21	20	19	18	17	16
STROBE_START(23:16)							
15	14	13	12	11	10	9	8
STROBE_START(15:8)							
7	6	5	4	3	2	1	0
STROBE_START(7:0)							

STROBE_E	STROBE Enable	
RW	This register enables the strobe logic. For Nexis 3 systems, to enable STROBE_A signal, STROBE_E and STROBE_A_EN must be enabled. For Nexis 3 systems, to enable STROBE_B signal, STROBE_E and STROBE_B_EN must be enabled. For Nexis 3 systems, STROBE_A and STROBE B can be activated at the same time, in this case the two strobes will be the same as they share the same programmation. This register is double buffered	
Value at Reset:	0x0	
Possible Values:	0x0	Strobe disabled
	0x1	Strobe enabled

STROBE_POL	STROBE POLarity	
RW	This is the strobe polarity at the pin of the FPGA only for GTR systems. For NEXIS3 systems use register ANPUT\IO\IO_OUT_POL\OUTx_POL This register is not double buffered.	
Value at Reset:	0x0	
Possible Values:	0x0	Active high strobe
	0x1	Active low strobe

STROBE_START (27:0)	STROBE START	
RW	This is the strobe start location. This location depends on the Strobe Mode used. In Strobe Mode='0', the start of the strobe is situated during the exposure time. In Strobe Mode='1', the start of the strobe is situated during the trigger delay. This register is double buffered	
Value at Reset:	0x0	
Possible Values:	Any Value	Any 28 bits value

STROBE_CTRL2

Address: section "ACQ" base address + 0x050

31	30	29	28	27	26	25	24
STROBE_MODE	Reserved	STROBE_B_EN	STROBE_A_EN	STROBE_END(27:24)			
23	22	21	20	19	18	17	16
STROBE_END(23:16)							
15	14	13	12	11	10	9	8
STROBE_END(15:8)							
7	6	5	4	3	2	1	0
STROBE_END(7:0)							

STROBE_MODE	STROBE MODE	
RW	This register selects the location of the Strobe Start. When this register is set to 0, the STROBE_START register is located during the exposure timer. When this register is set to 1, the STROBE_START register is located during the trigger delay timer. In HW level mode the strobe mode must be set to STROBE MODE=0 since the trigger cannot be delayed. This register is double buffered	
Value at Reset:	0x0	
Possible Values:	0x0	Strobe start during exposure
	0x1	Strobe start during trigger delay

STROBE_B_EN	STROBE phase B ENable	
RW	This field enables the generation of STROBE_B signal, for a NEXIS 3 system. This register is double buffered to support back2back mode in nexis systems.	
Value at Reset:	0x0	
Possible Values:	0x0	Enable Strobe B
	0x1	Disable Strobe B

STROBE_A_EN	STROBE phase A ENable	
RW	This field enables the generation of STROBE_A signal(Default strobe), for a NEXIS 3 system. This register is double buffered to support back2back mode in nexis systems.	
Value at Reset:	0x1	
Possible Values:	0x0	Enable Strobe A (default strobe)
	0x1	Disable Strobe A

STROBE_END (27:0)	STROBE END	
RW	This is the strobe end location. This location does not depend on the Strobe Mode used. This register is double buffered	
Value at Reset:	0xfffffff	
Possible Values:	Any Value	Any 28 bits value

Address: section "ACQ" base address + 0x058

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							SER_RWn
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved						SER_CMD(1:0)	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			SER_RF_SS	Reserved			SER_WF_SS

SER_RWn	SERial Read/Writen	
RW	This register configures the type of the serial access to the CMOS sensor	
Value at Reset:	0x1	
Possible Values:	0x0	Write access
	0x1	Read access

SER_CMD (1:0)	SERial CoMmand	
RW	This is the type of command sent to the serial fifo. To access the Sensor, write SER_WF_SS=1 with SER_CMD=0x0, with the parametters: SER_WRn, SER_ADD(8:0) and SER_DAT(15:0). To insert a timer between fifo commands, write SER_WF_SS=1 with SER_CMD=0x1, with the parameter: SER_DAT(15:0). The value of the timer inserted is calculated with the following formula: Timer= SER_DAT(15:0)*1024*SYS_PERIOD, SYS_PERIOD is 1/62.5mhz. The granularity of the timer is 16.384us To insert a Stop separator command, write SER_WF_SS=1 with SER_CMD=0x3. When the read logic encounter this command, it will stop read from the fifo until a new SER_RF_SS is received.	
Value at Reset:	0x0	
Possible Values:	0x0	CMOS sensor access COMMAND
	0x1	Insert timer COMMAND
	0x2	STOP separator COMMAND
	0x3	RESERVED

SER_RF_SS	SERial Read Fifo SnapShot	
WO/AutoClr	This is the read fifo snapshot. When the read fifo logic receives this snapshot, it will read all the fifo comands until a STOP separator command is read or Empty fifo is detected.	
Possible Values:	0x0	Idle
	0x1	Start Read FIFO

SER_WF_SS	SERial Write Fifo SnapShot	
WO/AutoClr	When the system toggle this bit, the address, data and command are wrote to the command fifo. This fifo can contain the entire dcf, so the driver will not need to pool the status bit. This is a auto reset bit register, so after the driver write one, the bit will be auto reset to 0. To start the FIFO read logic write '1' to regsiter SER_RF_SS.	
Possible Values:	0x0	Idle
	0x1	Write a command to the FIFO

ACQ_SER_ADDATA — Serial Interface Data

Address: section "ACQ" base address + 0x060

31	30	29	28	27	26	25	24
SER_DAT(15:8)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SER_DAT(7:0)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved	SER_ADD(14:8)						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SER_ADD(7:0)							

SER_DAT (15:0)	SERial interface DATa	
RW	This is the write data to be send to the CMOS sensor by the serial interface, or the config data to a TIMER command or to a POWER sequence command. See register SER_CMD.	
Value at Reset:	0x0	
Possible Values:	Any Value	Any 16 bits value

SER_ADD (14:0)	SERial interface ADDress	
RW	This is the read/write address of the register in the CMOS sensor.	
Value at Reset:	0x0	
Possible Values:	Any Value	Any 9 bits value

Address: section "ACQ" base address + 0x068

31	30	29	28	27	26	25	24
Reserved							SER_FIFO_EMPTY
23	22	21	20	19	18	17	16
Reserved							SER_BUSY
15	14	13	12	11	10	9	8
SER_DAT_R(15:8)							
7	6	5	4	3	2	1	0
SER_DAT_R(7:0)							

SER_FIFO_EMPTY	SERial FIFO EMPTY
RO	This is the EMPTY flag of the xilinx fifo, when '1' there are no pending operations in the fifo.

SER_BUSY	SERial BUSY	
RO	This is the BUSY status of the FIFO read logic. The flag will be set to '1' when the SER_RF_SS is set to '1'. It will be reseted to '0' when the read logic will decode a STOP separator command or when the FIFO will be empty.	
Possible Values:	0x0	FIFO read logic is idle
	0x1	FIFO read logic is runnning

SER_DAT_R (15:0)	SERial interface DATa Read	
RO	This is the data read from CMOS sensor.	
Possible Values:	Any Value	Any 16 bits value

Address: section "ACQ" base address + 0x090

31	30	29	28	27	26	25	24
Reserved							SENSOR_REFRESH_TEMP
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							SENSOR_POWERDOWN
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							SENSOR_COLOR
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			SENSOR_REG_UPDATE	Reserved		SENSOR_RESETN	SENSOR_POWERUP

SENSOR_REFRESH_TEMP	SENSOR REFRESH TEMPerature	
WO/AutoClr	This register starts a sensor temperature read on the serial interface of the Python sensor. The temperature value readed will be available on field SENSOR_TEMP when field SENSOR_TEMP_VALID is set to '1'. [Pas utilise pour le moment dans IRIS4]	
Possible Values:	0x0	Idle
	0x1	Starts a Temperature read on Python SPI interface

SENSOR_POWERDOWN	
WO/AutoClr	After a PowerUp sequence(SESOR_POWERUP_DONE=1), successfull or not, this register can reset the clock oscillator and enable the reset to the sensor. This power down don't do power sequencing.

SENSOR_COLOR	SENSOR COLOR	
RW	This register informs the datapath logic that a color sensor is used. This information is needed for the remapper logic.	
Value at Reset:	0x0	
Possible Values:	0x0	Monochrone sensor
	0x1	Color sensor

SENSOR_REG_UPDATE	SENSOR REGister UPDATE	
RW	By setting this bit to 1, the SENSOR CONTROLLER WILL UPDATE the programed CMOS sensor registers at the beginning of each grab.	
Value at Reset:	0x1	
Possible Values:	0x0	Do not update registers
	0x1	Update registers

SENSOR_RESETN	SENSOR RESET Not	
RW	After a successfull PowerUP sequence, writing this field to '0' reset the Python CMOS sensor.	
Value at Reset:	0x1	
Possible Values:	0x0	Reset the sensor after a successfull powerUP
	0x1	Nothing

SENSOR_POWERUP		
WO/AutoClr	This register Enables the clk oscillator and removes the reset from the sensor.	
Possible Values:	0x0	idle
	0x1	Start the power sequence

Address: section "ACQ" base address + 0x098

31	30	29	28	27	26	25	24
SENSOR_TEMP(7:0)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SENSOR_TEMP_VALID	Reserved						SENSOR_POWERDOWN
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved		SENSOR_RESETN	SENSOR_OSC_EN	Reserved			SENSOR_VCC_PG
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved						SENSOR_POWERUP_STAT	SENSOR_POWERUP_DONE

SENSOR_TEMP (7:0)		
RO	This register gives the Temperature of the Python sensor after a SENSOR_REFRESH_TEMP snapshot. The field SENSOR_TEMP_VALID indicates when the SENSOR_TEMP value is valid. [Pas utilise pour le moment dans IRIS4]	
Possible Values:	Any Value	

SENSOR_TEMP_VALID	SENSOR TEMPerature VALID	
RO	This field indicates that the field SENSOR_TEMP have valid temperature after a SENSOR_REFRESH_TEMP snapshot. [Pas utilise pour le moment dans IRIS4]	
Possible Values:	0x0	SENSOR_TEMPERATURE register is not valid
	0x1	SENSOR_TEMPERATURE register is valid

SENSOR_POWERDOWN		
RO	This field indicates that the sensor is in powerdown state.	
Possible Values:	0x0	Not in powerdown state
	0x1	Powerdown

SENSOR_RESETN	SENSOR RESET N	
RO	This is the sensor RESETN status.	
Possible Values:	0x0	In reset state
	0x1	Not in reset

SENSOR_OSC_EN	SENSOR OSCILLATOR ENable	
RO	This is the sensor oscillator enable status.	
Possible Values:	0x0	Disable
	0x1	Enable

SENSOR_VCC_PG	SENSOR supply VCC Power Good	
RO	This is the VCC Power Good status (generated by external HW). [TO BE DELETED, waiting for ON SEMI INFORMATION]	
Possible Values:	0x0	Disable
	0x1	Enable

SENSOR_POWERUP_STAT		
RO	When a powerup sequence is finish, this register indicates the result of the POWERUP sequence.	
Possible Values:	0x0	PowerUp sequence fail
	0x1	PowerUp sequence success

SENSOR_POWERUP_DONE		
RO	This register indicates that the POWERUP sequence is finish. Read register SENSOR_POWERUP_STAT to see the result.	
Possible Values:	0x0	PowerUp sequence not started
	0x1	PowerUp sequence finish

SENSOR_SUBSAMPLING

Address: section "ACQ" base address + 0x09C

Description:
SENSOR ADDRESS

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
reserved1(11:4)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
reserved1(3:0)				ACTIVE_SUBSAMPLING_Y	reserved0	M_SUBSAMPLING_Y	SUBSAMPLING_X

reserved1 (11:0)		
STATIC		
Value at Reset:	0x0	

ACTIVE_SUBSAMPLING_Y		
RW	Subsampling (Row) for ROI Configurations	
Value at Reset:	0x0	
Possible Values:	0x0	
	0x1	

reserved0		
STATIC		
Value at Reset:	0x0	
Possible Values:	0x0	Idle
	0x1	Enable

M_SUBSAMPLING_Y		
RW	Subsampling (Row) for M Region	
Value at Reset:	0x0	
Possible Values:	0x0	
	0x1	

SUBSAMPLING_X		
RW	Readout in Column Subsampling Mode. We don't use SUB_X in sensor, no fps advantages , and noise is increased! instead using DMA subsampling.	
Value at Reset:	0x0	
Possible Values:	0x0	
	0x1	

SENSOR_GAIN_ANA

Address: section "ACQ" base address + 0x0A4

Description:

SENSOR ADDRESS 204 DEC

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
reserved1(4:0)					ANALOG_GAIN(2:0)		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
reserved0(7:0)							

reserved1 (4:0) *STATIC*	
Value at Reset:	0x0

ANALOG_GAIN (2:0) *RW*		
Value at Reset:	0x1	
Possible Values:	0x1	1x
	0x3	2x
	0x7	4x

reserved0 (7:0) *STATIC*	
Value at Reset:	0x0

SENSOR_ROI_Y_START

Address: section "ACQ" base address + 0x0A8

Description:

SENSOR ADDRESS

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
reserved(5:0)						Y_START(9:8)	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Y_START(7:0)							

reserved (5:0)	
STATIC	
Value at Reset:	0x0

Y_START (9:0)	Y START
RW	Y Start in Kernel size (Kernel is 4 lines)
Value at Reset:	0x0

SENSOR_ROI_Y_SIZE

Address: section "ACQ" base address + 0x0AC

Description:
SENSOR ADDRESS

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
reserved(5:0)						Y_SIZE(9:8)	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Y_SIZE(7:0)							

reserved (5:0)	
STATIC	
Value at Reset:	0x0

Y_SIZE (9:0)	Y SIZE
RW	Y SIZE in Kernel size (Kernel is 4 lines)
Value at Reset:	0x302

SENSOR_M_LINES

Address: section "ACQ" base address + 0x0B8

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
M_LINES_DISPLAY	M_SUPPRESSED(4:0)					M_LINES_SENSOR(9:8)	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
M_LINES_SENSOR(7:0)							

M_LINES_DISPLAY	
RW	When setting to 1, the Y_SIZE will have the Black lines included and the first_lines_mask_cnt will be set to 1, to remove only the embedded data
Value at Reset:	0x0

M_SUPPRESSED (4:0)	
RW	Suppress the Readout of Initial Lines in the M Region
Value at Reset:	0x0

M_LINES_SENSOR (9:0)	
RW	Number of Lines to Readout from M Region in Context 0 Unit is #lines Total number of Black lines = M_LINES Total number of Black lines transfered as valid Black lines= M_LINES-M_SUPRESSED
Value at Reset:	0x8

SENSOR_DP_GR

Address: section "ACQ" base address + 0x0BC

Description:

Sensor Analog data pedestal for Gr pixels (Black offset)

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
reserved(3:0)				DP_OFFSET_GR(11:8)			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DP_OFFSET_GR(7:0)							

reserved (3:0)	
STATIC	
Value at Reset:	0x0

DP_OFFSET_GR (11:0)	
RW	Sensor Analog data pedestal for Gr pixels (Black offset)
Value at Reset:	0x100

SENSOR_DP_GB

Address: section "ACQ" base address + 0x0C0

Description:

Sensor Analog data pedestal for Gb pixels (Black offset)

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
reserved(3:0)				DP_OFFSET_GB(11:8)			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DP_OFFSET_GB(7:0)							

reserved (3:0)	
STATIC	
Value at Reset:	0x0

DP_OFFSET_GB (11:0)	
RW	Sensor Analog data pedestal for Gb pixels (Black offset)
Value at Reset:	0x100

SENSOR_DP_R

Address: section "ACQ" base address + 0x0C4

Description:

Sensor Analog data pedestal for R pixels (Black offset)

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
reserved(3:0)				DP_OFFSET_R(11:8)			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DP_OFFSET_R(7:0)							

reserved (3:0)	
STATIC	
Value at Reset:	0x0

DP_OFFSET_R (11:0)	
RW	Sensor Analog data pedestal for R pixels (Black offset)
Value at Reset:	0x100

SENSOR_DP_B

Address: section "ACQ" base address + 0x0C8

Description:

Sensor Analog data pedestal for B pixels (Black offset)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
reserved(3:0)				DP_OFFSET_B(11:8)			
7	6	5	4	3	2	1	0
DP_OFFSET_B(7:0)							

reserved (3:0)	
STATIC	
Value at Reset:	0x0

DP_OFFSET_B (11:0)	
RW	Sensor Analog data pedestal for B pixels (Black offset)
Value at Reset:	0x100

SENSOR_GAIN_DIG_G

Address: section "ACQ" base address + 0x0CC

Description:

XGS Context0 : R0x3846

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
reserved1	DG_FACTOR_GR(6:0)						
7	6	5	4	3	2	1	0
reserved0	DG_FACTOR_GB(6:0)						

reserved1		
STATIC		
Value at Reset:	0x0	

DG_FACTOR_GR (6:0)		
RW	Digital Gain Factor for GREEN-R Pixels The digital gain can be configured to separate levels for each color channel (GR, GB, R and B). The digital gain factor ranges from 1/32 to 2 in steps of 1/32 (64 steps) and its configuration can berepresented by the equation below: Digital gain = Dg_factor/32 Dg_factor=0x20 is unitary gain 1.000 Dg_factor=0x40 is gain x2.00000 Dg_factor=0x01 is gain x0.03125 Dg_factor=0x7f is gain x3.96875	
Value at Reset:	0x20	
Possible Values:	0x1 - 0x7F	Any value in range

reserved0		
STATIC		
Value at Reset:	0x0	

DG_FACTOR_GB (6:0)		
RW	Digital Gain Factor for GREEN-B Pixels The digital gain can be configured to separate levels for each color channel (GR, GB, R and B). The digital gain factor ranges from 1/32 to 2 in steps of 1/32 (64 steps) and its configuration can berepresented by the equation below: Digital gain = Dg_factor/32 Dg_factor=0x20 is unitary gain 1.000 Dg_factor=0x40 is gain x2.00000 Dg_factor=0x01 is gain x0.03125 Dg_factor=0x7f is gain x3.96875	
Value at Reset:	0x20	
Possible Values:	0x1 - 0x7F	Any value in range

SENSOR_GAIN_DIG_RB

Address: section "ACQ" base address + 0x0D0

Description:

XGS Context0 : R0x3848

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
reserved1	DG_FACTOR_R(6:0)						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
reserved0	DG_FACTOR_B(6:0)						

reserved1 *STATIC*	
Value at Reset:	0x0

DG_FACTOR_R (6:0) *RW*	Digital Gain Factor for RED Pixels The digital gain can be configured to separate levels for each color channel (GR, GB, R and B). The digital gain factor ranges from 1/32 to 2 in steps of 1/32 (64 steps) and its configuration can berepresented by the equation below: Digital gain = Dg_factor/32 Dg_factor=0x20 is unitary gain 1.000 Dg_factor=0x40 is gain x2.00000 Dg_factor=0x01 is gain x0.03125 Dg_factor=0x7f is gain x3.96875	
Value at Reset:	0x20	
Possible Values:	0x1 - 0x7F	Any value in range

reserved0 *STATIC*	
Value at Reset:	0x0

DG_FACTOR_B (6:0) *RW*	Digital Gain Factor for BLUE Pixels The digital gain can be configured to separate levels for each color channel (GR, GB, R and B). The digital gain factor ranges from 1/32 to 2 in steps of 1/32 (64 steps) and its configuration can berepresented by the equation below: Digital gain = Dg_factor/32 Dg_factor=0x20 is unitary gain 1.000 Dg_factor=0x40 is gain x2.00000 Dg_factor=0x01 is gain x0.03125 Dg_factor=0x7f is gain x3.96875	
Value at Reset:	0x20	
Possible Values:	0x1 - 0x7F	Any value in range

DEBUG_PINS

Address: section "ACQ" base address + 0x0E0

31	30	29	28	27	26	25	24
Reserved			Debug3_sel(4:0)				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved			Debug2_sel(4:0)				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved			Debug1_sel(4:0)				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			Debug0_sel(4:0)				

Debug3_sel (4:0)	

RW	debug_vector(0x0) <= python_monitor0;
	debug_vector(0x1) <= python_monitor1;
	debug_vector(0x2) <= grab_mngr_trig_rdy;
	debug_vector(0x3) <= curr_trig0;
	debug_vector(0x4) <= strobe;
	debug_vector(0x5) <= python_exposure;
	debug_vector(0x6) <= FOT;
	debug_vector(0x7) <= readout;
	debug_vector(0x8) <= readout_stateD;
	debug_vector(0x9) <= ext_trig;
	debug_vector(0xa) <= REGFILE.ACQ.GRAB_CTRL.GRAB_CMD;
	debug_vector(0xb) <= REGFILE.ACQ.GRAB_CTRL.GRAB_SS;
	debug_vector(0xc)<= grab_mngr_trig;
	debug_vector(0xd) <= grab_mngr_trig_rdy;
	debug_vector(0xe) <= grab_pending;
	debug_vector(0xf) <= grab_active;
	debug_vector(0x10) <= DEC_DATA_EN;
	debug_vector(0x11) <= DEC_SOL;
	debug_vector(0x12) <= DEC_SOF;
	debug_vector(0x13) <= DEC_EOL;
	debug_vector(0x14) <= DEC_EOF;
	debug_vector(0x15) <= DEC_CRC;
	debug_vector(0x16) <= DEC_TRAIN;
	debug_vector(0x17) <= fpnprnu_corr_sof;
	debug_vector(0x18) <= fpnprnu_corr_sol;
	debug_vector(0x19) <= fpnprnu_corr_data_val;
	debug_vector(0x1a) <= fpnprnu_corr_eol;
	debug_vector(0x1b) <= fpnprnu_corr_eof;
	debug_vector(0x1c) <= python_ssn_int;
	debug_vector(0x1d) <= debug_lvds(0);
	debug_vector(0x1e) <= debug_lvds(1);
	debug_vector(0x1f) <= 'Z';

Value at Reset:	0x1f

Debug2_sel (4:0)	

RW	debug_vector(0x0) <= python_monitor0;
	debug_vector(0x1) <= python_monitor1;
	debug_vector(0x2) <= grab_mngr_trig_rdy;
	debug_vector(0x3) <= curr_trig0;
	debug_vector(0x4) <= strobe;
	debug_vector(0x5) <= python_exposure;
	debug_vector(0x6) <= FOT;
	debug_vector(0x7) <= readout;
	debug_vector(0x8) <= readout_stateD;
	debug_vector(0x9) <= ext_trig;
	debug_vector(0xa) <= REGFILE.ACQ.GRAB_CTRL.GRAB_CMD;
	debug_vector(0xb) <= REGFILE.ACQ.GRAB_CTRL.GRAB_SS;
	debug_vector(0xc)<= grab_mngr_trig;
	debug_vector(0xd) <= grab_mngr_trig_rdy;
	debug_vector(0xe) <= grab_pending;
	debug_vector(0xf) <= grab_active;
	debug_vector(0x10) <= DEC_DATA_EN;
	debug_vector(0x11) <= DEC_SOL;
	debug_vector(0x12) <= DEC_SOF;
	debug_vector(0x13) <= DEC_EOL;
	debug_vector(0x14) <= DEC_EOF;
	debug_vector(0x15) <= DEC_CRC;
	debug_vector(0x16) <= DEC_TRAIN;
	debug_vector(0x17) <= fpnprnu_corr_sof;
	debug_vector(0x18) <= fpnprnu_corr_sol;
	debug_vector(0x19) <= fpnprnu_corr_data_val;
	debug_vector(0x1a) <= fpnprnu_corr_eol;
	debug_vector(0x1b) <= fpnprnu_corr_eof;
	debug_vector(0x1c) <= python_ssn_int;
	debug_vector(0x1d) <= debug_lvds(0);
	debug_vector(0x1e) <= debug_lvds(1);
	debug_vector(0x1f) <= 'Z';

Value at Reset:	0x1f

Debug1_sel (4:0)	

RW	debug_vector(0x0) <= python_monitor0;
	debug_vector(0x1) <= python_monitor1;
	debug_vector(0x2) <= grab_mngr_trig_rdy;
	debug_vector(0x3) <= curr_trig0;
	debug_vector(0x4) <= strobe;
	debug_vector(0x5) <= python_exposure;
	debug_vector(0x6) <= FOT;
	debug_vector(0x7) <= readout;
	debug_vector(0x8) <= readout_stateD;
	debug_vector(0x9) <= ext_trig;
	debug_vector(0xa) <= REGFILE.ACQ.GRAB_CTRL.GRAB_CMD;
	debug_vector(0xb) <= REGFILE.ACQ.GRAB_CTRL.GRAB_SS;
	debug_vector(0xc)<= grab_mngr_trig;
	debug_vector(0xd) <= grab_mngr_trig_rdy;
	debug_vector(0xe) <= grab_pending;
	debug_vector(0xf) <= grab_active;
	debug_vector(0x10) <= DEC_DATA_EN;
	debug_vector(0x11) <= DEC_SOL;
	debug_vector(0x12) <= DEC_SOF;
	debug_vector(0x13) <= DEC_EOL;
	debug_vector(0x14) <= DEC_EOF;
	debug_vector(0x15) <= DEC_CRC;
	debug_vector(0x16) <= DEC_TRAIN;
	debug_vector(0x17) <= fpnprnu_corr_sof;
	debug_vector(0x18) <= fpnprnu_corr_sol;
	debug_vector(0x19) <= fpnprnu_corr_data_val;
	debug_vector(0x1a) <= fpnprnu_corr_eol;
	debug_vector(0x1b) <= fpnprnu_corr_eof;
	debug_vector(0x1c) <= python_ssn_int;
	debug_vector(0x1d) <= debug_lvds(0);
	debug_vector(0x1e) <= debug_lvds(1);
	debug_vector(0x1f) <= 'Z';

Value at Reset:	0x1f

Debug0_sel (4:0)	

RW	debug_vector(0x0) <= python_monitor0;
	debug_vector(0x1) <= python_monitor1;
	debug_vector(0x2) <= grab_mngr_trig_rdy;
	debug_vector(0x3) <= curr_trig0;
	debug_vector(0x4) <= strobe;
	debug_vector(0x5) <= python_exposure;
	debug_vector(0x6) <= FOT;
	debug_vector(0x7) <= readout;
	debug_vector(0x8) <= readout_stateD;
	debug_vector(0x9) <= ext_trig;
	debug_vector(0xa) <= REGFILE.ACQ.GRAB_CTRL.GRAB_CMD;
	debug_vector(0xb) <= REGFILE.ACQ.GRAB_CTRL.GRAB_SS;
	debug_vector(0xc)<= grab_mngr_trig;
	debug_vector(0xd) <= grab_mngr_trig_rdy;
	debug_vector(0xe) <= grab_pending;
	debug_vector(0xf) <= grab_active;
	debug_vector(0x10) <= DEC_DATA_EN;
	debug_vector(0x11) <= DEC_SOL;
	debug_vector(0x12) <= DEC_SOF;
	debug_vector(0x13) <= DEC_EOL;
	debug_vector(0x14) <= DEC_EOF;
	debug_vector(0x15) <= DEC_CRC;
	debug_vector(0x16) <= DEC_TRAIN;
	debug_vector(0x17) <= fpnprnu_corr_sof;
	debug_vector(0x18) <= fpnprnu_corr_sol;
	debug_vector(0x19) <= fpnprnu_corr_data_val;
	debug_vector(0x1a) <= fpnprnu_corr_eol;
	debug_vector(0x1b) <= fpnprnu_corr_eof;
	debug_vector(0x1c) <= python_ssn_int;
	debug_vector(0x1d) <= debug_lvds(0);
	debug_vector(0x1e) <= debug_lvds(1);
	debug_vector(0x1f) <= 'Z';

Value at Reset:	0x1f

TRIGGER_MISSED

Address: section "ACQ" base address + 0x0E8

31	30	29	28	27	26	25	24
Reserved			TRIGGER_MISSED_RST	Reserved			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TRIGGER_MISSED_CNTR(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRIGGER_MISSED_CNTR(7:0)							

TRIGGER_MISSED_RST	TRIGGER MISSED ReSeT	
WO/AutoClr	This is the trigger missed reset.	
Possible Values:	0x1	Reset the Trigger counter reset

TRIGGER_MISSED_CNTR (15:0)	TRIGGER MISSED CouNTeR	
RO	This is the number of trigger missed detected.	
Possible Values:	Any Value	

SENSOR_FPS

Address: section "ACQ" base address + 0x0F0

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
SENSOR_FPS(15:8)							
7	6	5	4	3	2	1	0
SENSOR_FPS(7:0)							

SENSOR_FPS (15:0)	SENSOR Frame Per Second
RO	This is the number of frames received in 1 second interval. This register can count up to 64k frame/s. This counter counts on SO_FOT event.

SENSOR_FPS2

Address: section "ACQ" base address + 0x0F4

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved				SENSOR_FPS(19:16)			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SENSOR_FPS(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SENSOR_FPS(7:0)							

SENSOR_FPS (19:0)	SENSOR Frame Per Second
RO	This is the number of frames received in 10 second interval. This register can count up to 1.049 million frames. This counter counts on SO_FOT event.

DEBUG

Address: section "ACQ" base address + 0x1A0

31	30	29	28	27	26	25	24
Reserved			DEBUG_RST_CNTR	Reserved			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					LED_TEST_COLOR(1:0)		LED_TEST

DEBUG_RST_CNTR		
RW	This register clears the debug cntrs	
Value at Reset:	0x1	
Possible Values:	0x0	
	0x1	Reset counters

LED_TEST_COLOR (1:0)		
RW		
Value at Reset:	0x0	
Possible Values:	0x0	The LED is OFF
	0x1	The LED is GREEN
	0x2	The LED is RED
	0x3	The LED is ORANGE

LED_TEST		
RW	This register will put the LED status in test mode. The test mode is controlled by LED_TEST_COLOR	
Value at Reset:	0x0	
Possible Values:	0x0	The LED is in user mode.
	0x1	The LED is in test mode.

DEBUG_CNTR1

Address: section "ACQ" base address + 0x1A8

31	30	29	28	27	26	25	24
Reserved				SENSOR_FRAME_DURATION(27:24)			
23	22	21	20	19	18	17	16
SENSOR_FRAME_DURATION(23:16)							
15	14	13	12	11	10	9	8
SENSOR_FRAME_DURATION(15:8)							
7	6	5	4	3	2	1	0
SENSOR_FRAME_DURATION(7:0)							

SENSOR_FRAME_DURATION (27:0)		
RO	This is the time between the last 2 EOF received(in sys clock domain). This register can count up to 4.29 seconds. It can be used to predict sensor framerate or to verify sync between 3D profiler heads. This feature is enabled by setting register regfile.ACQ.DEBUG.DEBUG_RST_CNTR to 0.	
Possible Values:	Any Value	Any 28 bits value

DEBUG_CNTR2

Address: section "ACQ" base address + 0x1B0

31	30	29	28	27	26	25	24
EOF_CNTR(31:24)							
23	22	21	20	19	18	17	16
EOF_CNTR(23:16)							
15	14	13	12	11	10	9	8
EOF_CNTR(15:8)							
7	6	5	4	3	2	1	0
EOF_CNTR(7:0)							

EOF_CNTR (31:0)	
RO	This is the EOF CNTR. This feature is enabled by setting register regfile.ACQ.DEBUG.DEBUG_RST_CNTR to 0.

DEBUG_CNTR3

Address: section "ACQ" base address + 0x1B4

31	30	29	28	27	26	25	24
TRIG_INT_CNTR(31:24)							
23	22	21	20	19	18	17	16
TRIG_INT_CNTR(23:16)							
15	14	13	12	11	10	9	8
TRIG_INT_CNTR(15:8)							
7	6	5	4	3	2	1	0
TRIG_INT_CNTR(7:0)							

TRIG_INT_CNTR (31:0)	
RO	This is the TRIG_INT CNTR. This feature is enabled by setting register regfile.ACQ.DEBUG.DEBUG_RST_CNTR to 0.

EXP_FOT

Address: section "ACQ" base address + 0x1B8

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							EXP_FOT
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXP_FOT_TIME(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EXP_FOT_TIME(7:0)							

EXP_FOT	EXPosure during FOT	
RW	When set to '1' this register, the output exposure and strobe signals will take into account the exposure in the FOT of the frame. This timing must be programmed in register EXP_FOT_TIME. This timing must be calculated from the OnSemi setting files .	
Value at Reset:	0x1	
Possible Values:	0x0	Disable exposure during FOT in output exposure signal and Strobe
	0x1	Enable exposure during FOT in output exposure signal and Strobe

EXP_FOT_TIME (15:0)	EXPosure during FOT TIME
RW	This is the time of the exposure during the FOT. This timing must be calculated from the OnSemi setting files .
Value at Reset:	0x9ee

ACQ_SFNC

Address: section "ACQ" base address + 0x1C0

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							RELOAD_GRAB_PARAMS

RELOAD_GRAB_PARAMS *RW*	This register is not used for the moment. It may be used in the future to reload the exposure time	
Value at Reset:	0x1	
Possible Values:	0x0	
	0x1	

TIMER_CTRL

Address: section "ACQ" base address + 0x1D0

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							ADAPTATIVE
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			TIMERSTOP	Reserved			TIMERSTART

ADAPTATIVE		
RW	When this field is set to 1, the timer will adapt the trigger to the trigger_rdy of the controller to not generate trigger missed. When the timer is programmed too fast and the ADAPTATIVE field is set to 0, trigger missed will be generated.	
Value at Reset:	0x1	
Possible Values:	0x0	Non adaptative
	0x1	Adaptative to trigger_rdy

TIMERSTOP	
WO/AutoClr	This field stops the internal programmable Timer Trigger

TIMERSTART	
WO/AutoClr	This field starts the internal programmable Timer Trigger.

TIMER_DELAY

Address: section "ACQ" base address + 0x1D4

31	30	29	28	27	26	25	24
VALUE(31:24)							
23	22	21	20	19	18	17	16
VALUE(23:16)							
15	14	13	12	11	10	9	8
VALUE(15:8)							
7	6	5	4	3	2	1	0
VALUE(7:0)							

VALUE (31:0) *RW*	This register sets the delay for the first trigger generated when the timer is used. This register is double buffered with TimerStart register.
Value at Reset:	0x0

TIMER_DURATION

Address: section "ACQ" base address + 0x1D8

31	30	29	28	27	26	25	24
VALUE(31:24)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VALUE(23:16)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VALUE(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VALUE(7:0)							

VALUE (31:0) *RW*	This register sets the timer duration. When the counter reaches the value programmed in this register the counter will be reseted to 0. The trigger will be generated when the counter reaches value 0x1. This register is double buffered with TIMERSTART register.
Value at Reset:	0x0

Address Range: [0x400 - 0x454]

CTRL

Address: section "HISPI" base address + 0x000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			SW_CLR_IDELAYCTRL	SW_CLR_HISPI	SW_CALIB_SERDES	ENABLE_DATA_PATH	ENABLE_HISPI

SW_CLR_IDELAYCTRL *RW*	Reset the Xilinx macro IDELAYCTRL	
Value at Reset:	0x1	
Possible Values:	0x0	No effect
	0x1	Reset IDELAYCTRL

SW_CLR_HISPI *RW*	
Value at Reset:	0x0

SW_CALIB_SERDES *WO/AutoClr*	Initiate the SERDES TAP calibrartion	
Possible Values:	0x0	No effect
	0x1	Initiate the calibration

ENABLE_DATA_PATH *RW*	When setting this field to 1, the HISPI module will send the images received to the fpga data pipeline. This field is used to mask images. This field can be changed when no acquisition is in IDLE state.
Value at Reset:	0x0

ENABLE_HISPI *RW*	
Value at Reset:	0x0

Address: section "HISPI" base address + 0x004

31	30	29	28	27	26	25	24
FSM(3:0)				Reserved			
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			CRC_ERROR	PHY_BIT_LOCKED_ERROR	FIFO_ERROR	CALIBRATION_ERROR	CALIBRATION_DONE

FSM (3:0) *RO*	HISPI finite state machine status	
Possible Values:	0x0	S_DISABLED
	0x1	S_IDLE
	0x2	S_RESET_PHY
	0x3	S_INIT
	0x4	S_START_CALIBRATION
	0x5	S_CALIBRATE
	0x6	S_PACK
	0x7	S_FLUSH_PACKER
	0x8	S_SOF
	0x9	S_EOF
	0xA	S_SOL
	0xB	S_EOL
	0xC	Reserved
	0xD	Reserved
	0xE	FSM error (Unknown state)
	0xF	S_DONE

CRC_ERROR *RO*	Lane CRC error	
Possible Values:	0x0	No lane CRC error occured
	0x1	Lane CRC error occured

PHY_BIT_LOCKED_ERROR *RO*	

FIFO_ERROR *RO*	Calibration active	
Possible Values:	0x0	No FiFo error occured
	0x1	FiFo error occured

CALIBRATION_ERROR *RO*	Calibration error	
Possible Values:	0x0	No calibration error
	0x1	A calibration error occured

CALIBRATION_DONE *RO*	Calibration sequence completed	
Possible Values:	0x0	Calibration sequence not completed
	0x1	Last calibration sequence completed successfully

IDELAYCTRL_STATUS

Address: section "HISPI" base address + 0x008

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							PLL_LOCKED

PLL_LOCKED	IDELAYCTRL PLL locked	
RO		
Possible Values:	0x0	IDELAYCTRL PLL unlocked
	0x1	IDELAYCTRL PLL locked

IDLE_CHARACTER

Address: section "HISPI" base address + 0x00C

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved				VALUE(11:8)			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VALUE(7:0)							

VALUE (11:0)		
RW		
Value at Reset:	0x3A6	
Possible Values:	Any Value	

PHY

Address: section "HISPI" base address + 0x010

31	30	29	28	27	26	25	24
Reserved						PIXEL_PER_LANE(9:8)	
23	22	21	20	19	18	17	16
PIXEL_PER_LANE(7:0)							
15	14	13	12	11	10	9	8
Reserved					MUX_RATIO(2:0)		
7	6	5	4	3	2	1	0
Reserved					NB_LANES(2:0)		

PIXEL_PER_LANE (9:0)	Number of pixels per lanes	
RW		
Value at Reset:	0xAE	
Possible Values:	Any Value	

MUX_RATIO (2:0)	
STATIC	This is the configuration MUX ratio of the XGS sensor used. For GTX camera the mux ratio is fixed and set to 4.
Value at Reset:	0x4

NB_LANES (2:0)	Number of physical lane enabled	
RW	This is the physical number of HiSPI lanes available for the XGS sensor used. In GTX camera configuration : - Must be set to 4 in XGS5000, XGS3000,XGS2000 and XGS1300. - Must be set to 6 in XGS16M, XGS12M, XGS9.4M and XGS8M XGS1300.	
Value at Reset:	0x0	
Possible Values:	0x0	All lanes are disabled
	0x4	4 lanes enabled
	0x6	6 lanes enabled
	Others	Reserved (All lanes are disabled)

FRAME_CFG

Address: section "HISPI" base address + 0x014

31	30	29	28	27	26	25	24
Reserved				LINES_PER_FRAME(11:8)			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LINES_PER_FRAME(7:0)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved			PIXELS_PER_LINE(12:8)				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PIXELS_PER_LINE(7:0)							

LINES_PER_FRAME (11:0)	
RW	This is the total number of lines in a frame including dummy, BL, Interpolation and valid pixels. Reset value is 3102 (XGS12M). The value may change depending on the Black Lines(BL) programmed in the M-LINES section of the frame. Reset value is 3102 (0xc1e, XGS12M)
Value at Reset:	0xc1e

PIXELS_PER_LINE (12:0)	
RW	This is the total number of pixel in a line, including dummy, BL, Interpolation and valid pixels. Reset value is 4176 (0x1050, XGS12M)
Value at Reset:	0x1050

FRAME_CFG_X_VALID

Address: section "HISPI" base address + 0x018

31	30	29	28	27	26	25	24
Reserved			X_END(12:8)				
23	22	21	20	19	18	17	16
X_END(7:0)							
15	14	13	12	11	10	9	8
Reserved			X_START(12:8)				
7	6	5	4	3	2	1	0
X_START(7:0)							

X_END (12:0)	
RW	This register defines the position of the last horizontal valid pixel (including initials dummy pixels, black reference pixels and interpolation pixels). The location of the last X valid pixel differs between XGS family members and configurations. The dcf will load the location of the X end. It is defined as 1-based number For XGS12000, in a monochrome sensor the x end is 4132 (0x1024). For XGS12000, in a color sensor the x end is 4136 (0x1028). (For BAYER correction)
Value at Reset:	0x1023

X_START (12:0)	
RW	This register defines the position of the first horizontal valid pixel (including dummy pixels, black reference pixels and interpolation pixels). The location of the first X valid pixel differs between XGS family members and configurations. The dcf will load the location of the X start. It is defined as 1-based number For XGS12000, in a monochrome sensor the x start is 36 (0x24). For XGS12000, in a color sensor the x start is 32 (0x22). (For BAYER correction)
Value at Reset:	0x24

LANE_DECODER_STATUS (5:0)

Address: section "HISPI" base address + 0x024 + (index * 0x4)

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_ERROR	PHY_SYNC_ERROR	PHY_BIT_LOCKED_ERROR	PHY_BIT_LOCKED	Reserved			CALIBRATION_TAP_VALUE(4)
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALIBRATION_TAP_VALUE(3:0)				CALIBRATION_ERROR	CALIBRATION_DONE	FIFO_UNDERRUN	FIFO_OVERRUN

CRC_ERROR	CRC Error	
RW2C		
Value at Reset:	0x0	
Possible Values:	0x0	CRC no error occured
	0x1	CRC error occured

PHY_SYNC_ERROR		
RW2C		
Value at Reset:	0x0	
Possible Values:	0x0	Pixel bit boundaries unlocked
	0x1	Pixel bit boundaries locked

PHY_BIT_LOCKED_ERROR		
RW2C		
Value at Reset:	0x0	
Possible Values:	0x0	Pixel bit boundaries unlocked
	0x1	Pixel bit boundaries locked

PHY_BIT_LOCKED		
RO		
Possible Values:	0x0	Pixel bit boundaries unlocked
	0x1	Pixel bit boundaries locked

CALIBRATION_TAP_VALUE (4:0)	
RO	

CALIBRATION_ERROR	
RW2C	
Value at Reset:	0x0

CALIBRATION_DONE	
RO	

FIFO_UNDERRUN	
RW2C	
Value at Reset:	0x0

FIFO_OVERRUN	
RW2C	
Value at Reset:	0x0

TAP_HISTOGRAM (5:0)

Address: section "HISPI" base address + 0x03C + (index * 0x4)

31	30	29	28	27	26	25	24
VALUE(31:24)							
23	22	21	20	19	18	17	16
VALUE(23:16)							
15	14	13	12	11	10	9	8
VALUE(15:8)							
7	6	5	4	3	2	1	0
VALUE(7:0)							

VALUE (31:0) *RO*	

DEBUG

Address: section "HISPI" base address + 0x054

31	30	29	28	27	26	25	24
MANUAL_CALIB_EN	LOAD_TAPS	TAP_LANE_5(4:0)					TAP_LANE_4(4)
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TAP_LANE_4(3:0)				TAP_LANE_3(4:1)			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TAP_LANE_3(0)	TAP_LANE_2(4:0)					TAP_LANE_1(4:3)	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TAP_LANE_1(2:0)			TAP_LANE_0(4:0)				

MANUAL_CALIB_EN	
RW	
Value at Reset:	0x0

LOAD_TAPS	
WO/AutoClr	

TAP_LANE_5 (4:0)	
RW	
Value at Reset:	0x0

TAP_LANE_4 (4:0)	
RW	
Value at Reset:	0x0

TAP_LANE_3 (4:0)	
RW	
Value at Reset:	0x0

TAP_LANE_2 (4:0)	
RW	
Value at Reset:	0x0

TAP_LANE_1 (4:0)	
RW	
Value at Reset:	0x0

TAP_LANE_0 (4:0) *RW*	
Value at Reset:	0x0

Section: DPC

Address Range: [0x480 - 0x498]

DPC_CAPABILITIES

Address: section "DPC" base address + 0x000

31	30	29	28	27	26	25	24
Reserved				DPC_LIST_LENGTH(11:8)			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DPC_LIST_LENGTH(7:0)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				DPC_VER(3:0)			

DPC_LIST_LENGTH (11:0)	
RO	This register defines the maximum number of pixels that can be corrected by the DPC module. (ONE-based). This register is calculated with formula : (2^DPC_CORR_PIXELS_DEPTH)-1 , where DPC_CORR_PIXELS_DEPTH is a generic to the DPC module. For GTX value is 511

DPC_VER (3:0)		
RO	Implemented version of the DPC module	
Possible Values:	0x0	Initial monochrone correction only, 2 lines buffered.

DPC_LIST_CTRL

Address: section "DPC" base address + 0x004

31	30	29	28	27	26	25	24
dpc_highlight_all	Reserved	dpc_fifo_reset	dpc_firstlast_line_rem	dpc_list_count(11:8)			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
dpc_list_count(7:0)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
dpc_pattern0_cfg	dpc_enable	dpc_list_WRn	dpc_list_ss	dpc_list_add(11:8)			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
dpc_list_add(7:0)							

dpc_highlight_all	
RW	When set this bit to 1, all dead pixels in the list will be set to white.
Value at Reset:	0x0

dpc_fifo_reset		
RW	Write '1' then '0' to field dpcL_FIFO_RST to reset overrun/underrun flags of the line buffers and reset the Fifo logic. The DPC dual port ram is not SW reset . The fifo in each processing DPC unit is HW reset at each SOF.	
Value at Reset:	0x0	
Possible Values:	0x0	Fifo in normal operation
	0x1	Fifo in reset State

dpc_firstlast_line_rem		
RW	When this register is set to 1, the DPC macro will remove the first and last line of the image corrected. This can be usefull if we want to correct the 4 pixels in the corners of the image. The SW can program two more lines in the frame so the DPC macro can have enough pixels to correct the 4 pixel coners.	
Value at Reset:	0x0	
Possible Values:	0x0	Do not remove any lines of the image received
	0x1	Remove first and last line of the image received

dpc_list_count (11:0)		
RW	This is the number of entries in the DPC list. The driver need to set the dcp_list_count in order to correct the image. The value 0 is allowed and when set to 0 no pixel will be corrected. Up to (2^DPC_CORR_PIXELS_DEPTH)-1 pixels can be corrected. In GTX DPC_CORR_PIXELS_DEPTH is set to 9, up to 511 pixels may be corrected.	
Value at Reset:	0x0	
Possible Values:	Any Value	0 to 2^DPC_CORR_PIXELS_DEPTH

dpc_pattern0_cfg		
RW	This field configures the behabieur of the correction pattern 0x0. If this field is set to 0x0 then the current pixel will not be corrected. If this field is set to 0x1 then the current pixel will be replaced by the value 0x3ff (white pixel)	
Value at Reset:	0x0	
Possible Values:	0x0	Do not correct current pixel
	0x1	Replace current pixel by a white pixel (0x3ff)

dpc_enable		
RW	Dead Pixel Correction core Enable, when this field is set to 1, the DPC logic will correct all the dead pixels that are listed in the DPC list. The grab must be idle when changing this register.	
Value at Reset:	0x0	
Possible Values:	0x0	DPC logic is bypassed
	0x1	DPC logic is enabled

dpc_list_WRn		
RW	This is the Write/ReadN flag. To write to the DPC list set this bit to 1 and start the transaction with the dpc_list_ss field. To read from the DPC list set this bit to 0 and start the transaction with the dpc_list_ss field.	
Value at Reset:	0x0	
Possible Values:	0x0	Read list operation
	0x1	Write list operation

dpc_list_ss		
WO/AutoClr	This is the DPC snapshot. In order to start a write or read transaction the snapsot needs to be writen to '1'. This bit is a auto clear regsiter.	
Possible Values:	0x0	Do nothing
	0x1	Start the READ/WRITE transaction

dpc_list_add (11:0)		
RW	This is the address of the DPC list to be access by the read/write operation. Pixel 0 to correct is located at address 0x000. In GTX DPC_CORR_PIXELS_DEPTH is set to 9, up to 511 pixels may be corrected. Since the dpc_list_count field is also 9 bit wide, address 0 to 0x1fe of the list can be used. Adress 0x1ff cannot be used. This DPC location will not be corrected.	
Value at Reset:	0x0	
Possible Values:		Valid DPC adress

DPC_LIST_STAT

Address: section "DPC" base address + 0x008

31	30	29	28	27	26	25	24
dpc_fifo_underrun	dpc_fifo_overrun	Reserved					
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

dpc_fifo_underrun		
RO	This is the fifo underrun status of the 2 linebuffers in the dpc macro. Write '1' then '0' to field dpc_FIFO_RST to reset this flag and reset the Fifo logic.	
Possible Values:	0x0	Underrun not detected
	0x1	Underrun detected

dpc_fifo_overrun		
RO	This is the fifo overrun status of the 2 linebuffers in the dpc macro. Write '1' then '0' to field dpc_FIFO_RST to reset this flag and reset the Fifo logic.	
Possible Values:	0x0	Overrun not detected
	0x1	Overrun detected

DPC_LIST_DATA1

Address: section "DPC" base address + 0x00C

31	30	29	28	27	26	25	24
Reserved				dpc_list_corr_y(11:8)			
23	22	21	20	19	18	17	16
dpc_list_corr_y(7:0)							
15	14	13	12	11	10	9	8
Reserved			dpc_list_corr_x(12:8)				
7	6	5	4	3	2	1	0
dpc_list_corr_x(7:0)							

dpc_list_corr_y (11:0)	
RW	This is Y location of the pixel to be corrected when executing a write to the DPC list.
Value at Reset:	0x0

dpc_list_corr_x (12:0)	
RW	This is X location of the pixel to be corrected when executing a write to the DPC list.
Value at Reset:	0x0

DPC_LIST_DATA2

Address: section "DPC" base address + 0x010

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
dpc_list_corr_pattern(7:0)							

dpc_list_corr_pattern (7:0) *RW*	This is pattern of the pixel to be corrected when executing a write to the DPC list. 2 bit correction : 34, 17, 136, 68 4 bit correction : 170, 153, 51, 204, 85, 102 6 bit correcttion: 187,238 (mapped to 170), 119,221 (mapped to 85) 8 bit correction : 255 Set pixel to 255 (white), debug : 0
Value at Reset:	0x0

DPC_LIST_DATA1_RD

Address: section "DPC" base address + 0x014

31	30	29	28	27	26	25	24
Reserved				dpc_list_corr_y(11:8)			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
dpc_list_corr_y(7:0)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved			dpc_list_corr_x(12:8)				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
dpc_list_corr_x(7:0)							

dpc_list_corr_y (11:0)	
RO	This is Y location of the pixel to be corrected when executing a write to the DPC list.

dpc_list_corr_x (12:0)	
RO	This is X location of the pixel to be corrected when executing a write to the DPC list.

DPC_LIST_DATA2_RD

Address: section "DPC" base address + 0x018

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
dpc_list_corr_pattern(7:0)							

dpc_list_corr_pattern (7:0)	
RO	This is pattern of the pixel to be corrected when executing a write to the DPC list. 2 bit correction : 34, 17, 136, 68 4 bit correction : 170, 153, 51, 204, 85, 102 6 bit correcttion: 187,238 (mapped to 170), 119,221 (mapped to 85) 8 bit correction : 255 Set pixel to 255 (white), debug : 0

Section: LUT

Address Range: [0x4B0 - 0x4B8]

LUT_CAPABILITIES

Address: section "LUT" base address + 0x000

31	30	29	28	27	26	25	24
Reserved				LUT_SIZE_CONFIG(11:8)			
23	22	21	20	19	18	17	16
LUT_SIZE_CONFIG(7:0)							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				LUT_VER(3:0)			

LUT_SIZE_CONFIG (11:0)		
RO		
Possible Values:	0x0	Reserved
	0x1	10 to 8 bits LUT (Mono Only)
	0x2	8 to 8 bits RGB LUT (Color Only)

LUT_VER (3:0)		
RO	Implemented version of the LUT module	
Possible Values:	0x0	Initial monochrone LUT
	0x1	Initial color LUT

LUT_CTRL

Address: section "LUT" base address + 0x004

31	30	29	28	27	26	25	24
Reserved		LUT_BYPASS_COLOR	LUT_BYPASS	Reserved		LUT_DATA_W(9:8)	
23	22	21	20	19	18	17	16
LUT_DATA_W(7:0)							
15	14	13	12	11	10	9	8
LUT_SEL(3:0)				LUT_WRN	LUT_SS	LUT_ADD(9:8)	
7	6	5	4	3	2	1	0
LUT_ADD(7:0)							

LUT_BYPASS_COLOR	LUT BYPASS COLOR
RW	When set this register to '1', the RGB LUT logic will not be used, and the 8 bits of the input data will send to the DMA. Bypassing the LUT, decrease power comsunption of the fpga. This register applies to : 1) Color sensors 10 to 8 per component LUT (between CCM and DMA/YUV conversion)
Value at Reset:	0x1

LUT_BYPASS	LUT BYPASS
RW	When set this register to '1', the LUT will not be used This register applies to : 1) Mono sensors 10 to 8 LUT 2) Color sensors 10 to 10 LUT (between DPC and WB) If a 10 to 8 LUT is used, the 8MSB bits of the input data will send to the DMA. Bypassing the LUT, decrease power comsumption of the fpga.
Value at Reset:	0x1

LUT_DATA_W (9:0)	LUT DATA to Write
RW	Data to write in the LUT. When using 10 to 8 bits LUT (Mono camera), program bits LUT_DATA_W(7 :0) When using 8 to 8 bits LUT (Color camera, RGB LUT), program bits LUT_DATA_W(7 :0) When using 10 to 10 bits LUT(Color camera RAW LUT), program bits LUT_DATA_W(9 :0)
Value at Reset:	0x0

LUT_SEL (3:0)	LUT SELection	
RW	LUT programmation selector.	
Value at Reset:	0x0	
Possible Values:	0x1	Write Blue LUT(Color only)
	0x2	Write Green LUT(Color only)
	0x4	Write Red LUT(Color only)
	0x7	Write all component RGB LUT (Color only)
	0x8	Write LUT 10 to 8(Mono) or LUT 10 to 10(color) with same data

LUT_WRN	LUT Write ReadNot	
RW	LUT Write mode	
Value at Reset:	0x0	
Possible Values:	0x0	Read operation
	0x1	Write operation

LUT_SS	LUT SnapShot
WO/AutoClr	Start the LUT READ or WRITE OPERATION

LUT_ADD (9:0)	
RW	When writing to RGB LUT(after the bayer demosaic, 8 to 8 LUT), only the LSB bits of the address are used.
Value at Reset:	0x0

LUT_RB

Address: section "LUT" base address + 0x008

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LUT_RB(7:0)							

LUT_RB (7:0)	
STATIC	Not Implemented to save FPGA ressources
Value at Reset:	0x0

Section: BAYER

Address Range: [0x4C0 - 0x4F0]

BAYER_CAPABILITIES

Address: section "BAYER" base address + 0x000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved						BAYER_VER(1:0)	

BAYER_VER (1:0) *RO*	Implemented version of the BAYER module	
Possible Values:	0x0	Bayer not implemented
	0x1	Initial Bayer 2x2 version

WB_MUL1

Address: section "BAYER" base address + 0x004

31	30	29	28	27	26	25	24
WB_MULT_G(15:8)							
23	22	21	20	19	18	17	16
WB_MULT_G(7:0)							
15	14	13	12	11	10	9	8
WB_MULT_B(15:8)							
7	6	5	4	3	2	1	0
WB_MULT_B(7:0)							

WB_MULT_G (15:0)	
RW	White Balance factor [4].[12]
Value at Reset:	0x1000

WB_MULT_B (15:0)	
RW	White Balance factor [4].[12]
Value at Reset:	0x1000

WB_MUL2

Address: section "BAYER" base address + 0x008

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
WB_MULT_R(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WB_MULT_R(7:0)							

WB_MULT_R (15:0) *RW*	White Balance factor [4].[12]
Value at Reset:	0x1000

WB_B_ACC

Address: section "BAYER" base address + 0x00C

31	30	29	28	27	26	25	24
Reserved	B_ACC(30:24)						
23	22	21	20	19	18	17	16
B_ACC(23:16)							
15	14	13	12	11	10	9	8
B_ACC(15:8)							
7	6	5	4	3	2	1	0
B_ACC(7:0)							

B_ACC (30:0)	
RO	ACQuisition Blue ACCumulator

WB_G_ACC

Address: section "BAYER" base address + 0x010

31	30	29	28	27	26	25	24
G_ACC(31:24)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
G_ACC(23:16)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
G_ACC(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G_ACC(7:0)							

G_ACC (31:0) *RO*	ACQuisition Green ACCumulator

WB_R_ACC

Address: section "BAYER" base address + 0x014

31	30	29	28	27	26	25	24
Reserved	R_ACC(30:24)						
23	22	21	20	19	18	17	16
R_ACC(23:16)							
15	14	13	12	11	10	9	8
R_ACC(15:8)							
7	6	5	4	3	2	1	0
R_ACC(7:0)							

R_ACC (30:0)	
RO	ACQuisition Red ACCumulator

CCM_CTRL

Address: section "BAYER" base address + 0x018

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							CCM_EN

CCM_EN	
RW	
Value at Reset:	0x0

CCM_KR1

Address: section "BAYER" base address + 0x01C

31	30	29	28	27	26	25	24
Reserved				Kg(11:8)			
23	22	21	20	19	18	17	16
Kg(7:0)							
15	14	13	12	11	10	9	8
Reserved				Kr(11:8)			
7	6	5	4	3	2	1	0
Kr(7:0)							

Kg (11:0) *RW*	Signed 12 bits value, complement a 2 : s3.8
Value at Reset:	0x000

Kr (11:0) *RW*	Signed 12 bits value, complement a 2 : s3.8
Value at Reset:	0x100

CCM_KR2

Address: section "BAYER" base address + 0x020

31	30	29	28	27	26	25	24
Reserved							KOff(8)
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KOff(7:0)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved				Kb(11:8)			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Kb(7:0)							

KOff (8:0)	
RW	Signed 9 bits value, complement a 2 : s8
Value at Reset:	0x00

Kb (11:0)	
RW	Signed 12 bits value, complement a 2 : s3.8
Value at Reset:	0x000

CCM_KG1

Address: section "BAYER" base address + 0x024

31	30	29	28	27	26	25	24
Reserved				Kg(11:8)			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Kg(7:0)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved				Kr(11:8)			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Kr(7:0)							

Kg (11:0) *RW*	Signed 12 bits value, complement a 2 : s3.8
Value at Reset:	0x100

Kr (11:0) *RW*	Signed 12 bits value, complement a 2 : s3.8
Value at Reset:	0x000

CCM_KG2

Address: section "BAYER" base address + 0x028

31	30	29	28	27	26	25	24
Reserved							KOff(8)
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KOff(7:0)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved				Kb(11:8)			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Kb(7:0)							

KOff (8:0)	
RW	Signed 9 bits value, complement a 2 : s8
Value at Reset:	0x00

Kb (11:0)	
RW	Signed 12 bits value, complement a 2 : s3.8
Value at Reset:	0x000

CCM_KB1

Address: section "BAYER" base address + 0x02C

31	30	29	28	27	26	25	24
Reserved				Kg(11:8)			
23	22	21	20	19	18	17	16
Kg(7:0)							
15	14	13	12	11	10	9	8
Reserved				Kr(11:8)			
7	6	5	4	3	2	1	0
Kr(7:0)							

Kg (11:0)	
RW	Signed 12 bits value, complement a 2 : s3.8
Value at Reset:	0x00

Kr (11:0)	
RW	Signed 12 bits value, complement a 2 : s3.8
Value at Reset:	0x00

CCM_KB2

Address: section "BAYER" base address + 0x030

31	30	29	28	27	26	25	24
Reserved							KOff(8)
23	22	21	20	19	18	17	16
KOff(7:0)							
15	14	13	12	11	10	9	8
Reserved				Kb(11:8)			
7	6	5	4	3	2	1	0
Kb(7:0)							

KOff (8:0)	
RW	Signed 9 bits value, complement a 2 : s8
Value at Reset:	0x00

Kb (11:0)	
RW	Signed 12 bits value, complement a 2 : s3.8
Value at Reset:	0x100

Address Range: [0x700 - 0x7FC]

Description:
Access Xilinx embedded system monitoring module.
See Xilinx UG480

TEMP

Address: external "SYSMONXIL" base address + 0x000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
SMTEMP(11:4)							
7	6	5	4	3	2	1	0
SMTEMP(3:0)				Reserved			

SMTEMP (11:0)	System Monitor TEMPerature	
RO	This field reports the temperature of the die. Maximum-measurement error is ±4 degC. The temperature in Celcius = (SMTEMP*503.975/4096) – 273.15.	
Possible Values:	Any Value	

Address: external "SYSMONXIL" base address + 0x004

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SMVINT(11:4)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SMVINT(3:0)				Reserved			

SMVINT (11:0)	System Monitor VCCINT	
RO	This field reports voltage for VCCINT supply: VCCINT = (SMVINT/4096)x3V. VCCINT is the core voltage nominally set to 1.0V	
Possible Values:	Any Value	

Address: external "SYSMONXIL" base address + 0x008

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SMVAUX(11:4)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SMVAUX(3:0)				Reserved			

SMVAUX (11:0)	System Monitor VCCAUX	
RO	This field reports voltage for VCCAUX supply: VCCAUX = (SMVAUX/4096)x3V. VCCAUX is the auxiliary voltage nominally set to 1.8V.	
Possible Values:	Any Value	

Address: external "SYSMONXIL" base address + 0x018

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SMVBRAM(11:4)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SMVBRAM(3:0)				Reserved			

SMVBRAM (11:0)	System Monitor VCCBRAM	
RO	This field reports voltage for VCCBRAM supply: VCCBRAM = (SMVBRAM/4096)x3V. VCCBRAM is the block RAM supply nominally set to 1.0V.	
Possible Values:	Any Value	

Address: external "SYSMONXIL" base address + 0x080

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SMTMAX(11:4)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SMTMAX(3:0)				Reserved			

SMTMAX (11:0)	System Monitor Temperature MAXimum	
RO	This field reports the maximum temperature that has been measured by on-chip sensor. The maximum temperature (in Celcius) = (SMTMAX*503.975/4096) – 273.15.	
Possible Values:	Any Value	

Address: external "SYSMONXIL" base address + 0x090

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SMTMIN(11:4)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SMTMIN(3:0)				Reserved			

SMTMIN (11:0)	System Monitor Temperature MINimum	
RO	This field reports the maximum temperature that has been measured by on-chip sensor. The maximum temperature (in Celcius) = (SMTMIN*503.975/4096) – 273.15.	
Possible Values:	Any Value	