4.2.3.2. Timing Parameters

Table 4-6 provides the timing parameters for 3.3V and 5V signaling environments.

Table 4-6: 3.3V and 5V Timing Parameters

Symbol	Parameter	Min	Max	Units	Notes
T_{val}	CLK to Signal Valid Delay - bused signals	2	11	ns	1, 2, 3
$T_{val}(ptp)$	CLK to Signal Valid Delay - point to point	2	12	ns	1, 2, 3
T_{on}	Float to Active Delay	2		ns	1, 7
T_{off}	Active to Float Delay		28	ns	1, 7
T_{su}	Input Setup Time to CLK - bused signals	7		ns	3, 4, 8
$T_{su}(ptp)$	Input Setup Time to CLK - point to point	10, 12		ns	3, 4
T_{h}	Input Hold Time from CLK	0		ns	4
T_{rst}	Reset active time after power stable	1		ms	5
$T_{rst-clk}$	Reset active time after CLK STABLE	100		µs	5
$T_{rst-off}$	Reset Active to Output Float delay		40	ns	5, 6,7
T_{rrsu}	REQ64# to RST# Setup time	$10*T_{cyc}$		ns	
T_{rrh}	RST# to REQ64# Hold time	0	50	ns	
T_{rhfa}	RST# High to First configuration Access	2^{25}		clocks	
T_{rhff}	RST# High to First FRAME# assertion	5		clocks	
T_{pvrh}	Power valid to RST# high	100		ms	

Notes:
1. See the timing measurement conditions in Figure 4-7.
2. For parts compliant to the 3.3V signaling environment:
   Minimum times are evaluated with the same load used for slew rate measurement (as shown in Table 4-4, note 3); maximum times are evaluated with the following load circuits, for high-going and low-going edges respectively.

   For parts compliant to the 5V signaling environment:
   Minimum times are evaluated with 0 pF equivalent load; maximum times are evaluated with 50 pF equivalent load. Actual test capacitance may vary, but results must be correlated to these specifications. Note that faster buffers may exhibit some ring back when attached to a 50 pF lump load which should be of no consequence as long as the output buffers are in full compliance with slew rate and V/I curve specifications.