AND9713/D

XGS 12000, XGS 9400, XGS 8000 and XGS 5000 Register Reference

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APPLICATION NOTE

Introduction

This register reference is provided for engineers who are designing cameras that use the XGS 12000, XGS 9400, XGS 8000 and XGS 5000.

Conventions and Notations

This document follows the conventions and notations described below.

- Hexadecimal numbers have a 0x prefix
- Binary numbers have 0b prefix
  Example: 0b1010 = 0xA

Register Address Space

The image sensor provides a 16-bit register address space accessed through a serial interface.

The address space is divided into the five major regions shown in Table 1.

Table 1. ADDRESS SPACE REGIONS

Address Range	Description
0x0000−0x0FFF	Reserved
0x1000−0x2FFF	Reserved (Undefined)
0x3000−0x3FFF	Manufacturer-specific Registers (Read-only and Read-write Dynamic Registers)
0x4000−0xFFFF	Reserved

Register Notation

In this document, registers are described either by address or by name. When registers are described by address, the size of the registers is explicit. For example, R0x3024 is an 16-bit register at address 0x3024. When registers are described by name, the size of the register is implicit. It is necessary to refer to the register table to determine that model_id is a 16-bit register.

Register Aliases

A consequence of the internal architecture of the image sensor is that some registers are decoded at multiple addresses. Some registers in “configuration space” are also decoded in “manufacturer-specific space.” To provide unique names for all registers, the name of the register within manufacturer-specific register space has a trailing underscore. For example, R0x0000 is model_id, and R0x3000 is model_id_. The effect of reading or writing a register through any of its aliases is identical.

Bit Fields

Some registers provide control of several different pieces of related functionality, and this makes it necessary to refer to bit fields within registers. As an example of the notation used for this, the least significant 4 bits of the model_id register are referred to as model_id[3:0] or R0x3000−1[3:0].

Bit Field Aliases

In addition to the register aliases described above, some register fields are aliased in multiple places. For example, R0x301C (mode_select) only has one operational bit, R0x301C[0]. This bit is aliased to R0x301A−B[2]. The effect of reading or writing a bit field through any of its aliases is identical.

Address Alignment

All register addresses are aligned naturally. Registers that occupy two bytes of address space are aligned to even 16-bit addresses, and registers that occupy four bytes of address space are aligned to 16−bit addresses that are an integer multiple of 4.

Data Format

Most registers represent an unsigned binary value or set of bit fields. For all other register formats, the format is stated explicitly at the start of the register description. The notation for these formats is shown in Table 2.

Table 2. DATA FORMATS

Name	Description
FIX16	Signed fixed-point, 16-bit number: two's complement number, 8 fractional bits. Examples: 0x0100 = 1.0, 0x8000 = −128, 0xFFFF = −0.0039065
UFIX16	Unsigned fixed−point, 16-bit number: 8.8 format. Examples: 0x0100 = 1.0, 0x280 = 2.5
FLP32	Signed floating-point, 32-bit number: IEEE 754 format. Example: 0x4280_0000 = 64.0

Register Behavior

Registers vary from "read-only," "read/write," and "read, write−1−to−clear."

Table 3. MANUFACTURER SPECIFIC

(1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic)

Register Hex	Name	Data Format (Binary)	Default Value Dec(Hex)
R0x0000	CHIP_VERSION_REG	dddd dddd dddd dddd	88 (0x0058)
R0x0002	REVISION_NUMBER_REG	dddd dddd dddd dddd	1 (0x0001)
R0x3012	FUSE_ID9	dddd dddd dddd dddd	0 (0x0000)
R0x3500	PLL_COMPONENT0_REG	dddd dddd 00dd dddd	12291 (0x3003)
R0x3602	MONITOR_CTRL_REG	d000 000d dddd dddd	429 (0x01AD)
R0x3700	RESET_REGISTER_REG	d000 0000 dddd dd0d	128 (0x0080)
R0x3800	GENERAL_CONFIG0_REG	dddd dddd dddd dddd	2 (0x0002)
R0x3802	GENERAL_CONFIG1_REG	dddd dddd 00dd 0ddd	768 (0x0300)
R0x3804	CONTEXTS_REG	dddd dddd dddd dddd	4369 (0x1111)
R0x3806	MONITOR_REG	0ddd dddd dddd dddd	0 (0x0000)
R0x3808	MONITOR_INTEGRATION_LEAD_REG	dddd dddd dddd dddd	0 (0x0000)
R0x380A	SYNC_CONFIG_REG	0000 000d 0000 dddd	15 (0x000F)
R0x380E	ACTIVE_CONFIG_REG	0000 0000 0000 00dd	0 (0x0000)
R0x3810	LINE_TIME_REG	dddd dddd dddd dddd	366 (0x016E)
R0x3812	INTEGRATION_OFFSET_COARSE_REG	0000 dddd dddd dddd	0 (0x0000)
R0x381A	ROI0_START_REG	0000 00dd dddd dddd	0 (0x0000)
R0x381C	ROI0_SIZE_REG	0000 00dd dddd dddd	770 (0x0302)
R0x381E	ROI1_START_REG	0000 00dd dddd dddd	0 (0x0000)
R0x3820	ROI1_SIZE_REG	0000 00dd dddd dddd	770 (0x0302)
R0x3822	ROI2_START_REG	0000 00dd dddd dddd	0 (0x0000)
R0x3824	ROI2_SIZE_REG	0000 00dd dddd dddd	770 (0x0302)
R0x3826	ROI3_START_REG	0000 00dd dddd dddd	0 (0x0000)
R0x3828	ROI3_SIZE_REG	0000 00dd dddd dddd	770 (0x0302)
R0x382A	ROI4_START_REG	0000 00dd dddd dddd	0 (0x0000)
R0x382C	ROI4_SIZE_REG	0000 00dd dddd dddd	770 (0x0302)

Table 3. MANUFACTURER SPECIFIC (continued)
(1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic)

Register Hex	Name	Data Format (Binary)	Default Value Dec(Hex)
R0x382E	ROI5_START_REG	0000 00dd dddd dddd	0 (0x0000)
R0x3830	ROI5_SIZE_REG	0000 00dd dddd dddd	770 (0x0302)
R0x3832	ROI6_START_REG	0000 00dd dddd dddd	0 (0x0000)
R0x3834	ROI6_SIZE_REG	0000 00dd dddd dddd	770 (0x0302)
R0x3836	ROI7_START_REG	0000 00dd dddd dddd	0 (0x0000)
R0x3838	ROI7_SIZE_REG	0000 00dd dddd dddd	770 (0x0302)
R0x383A	FRAME_LENGTH_CTXT0_REG	dddd dddd dddd dddd	3160 (0x0C58)
R0x383C	SUBSAMPLING_CTXT0_REG	0000 0000 0000 dddd	0 (0x0000)
R0x383E	ROI_ACTIVE_CTXT0_REG	0000 0000 dddd dddd	1 (0x0001)
R0x3840	INTEGRATION_COARSE_CTXT0_REG	dddd dddd dddd dddd	3000 (0x0BB8)
R0x3842	INTEGRATION_FINE_CTXT0_REG	dddd dddd dddd dddd	0 (0x0000)
R0x3844	ANALOG_GAIN_CODE_CTXT0_REG	000d dddd 0000 0000	0 (0x0000)
R0x3846	DIGITAL_GAIN_CODE_G_CTXT0_REG	0ddd dddd 0ddd dddd	8224 (0x2020)
R0x3848	DIGITAL_GAIN_CODE_RB_CTXT0_REG	0ddd dddd 0ddd dddd	8224 (0x2020)
R0x384A	DP_OFFSET_GR_CTXT0_REG	0000 dddd dddd dddd	256 (0x0100)
R0x384C	DP_OFFSET_GB_CTXT0_REG	0000 dddd dddd dddd	256 (0x0100)
R0x384E	DP_OFFSET_R_CTXT0_REG	0000 dddd dddd dddd	256 (0x0100)
R0x3850	DP_OFFSET_B_CTXT0_REG	0000 dddd dddd dddd	256 (0x0100)
R0x385A	FRAME_LENGTH_CTXT1_REG	dddd dddd dddd dddd	3160 (0x0C58)
R0x385C	SUBSAMPLING_CTXT1_REG	0000 0000 0000 dddd	0 (0x0000)
R0x385E	ROI_ACTIVE_CTXT1_REG	0000 0000 dddd dddd	1 (0x0001)
R0x3860	INTEGRATION_COARSE_CTXT1_REG	dddd dddd dddd dddd	3000 (0x0BB8)
R0x3862	INTEGRATION_FINE_CTXT1_REG	dddd dddd dddd dddd	0 (0x0000)
R0x3864	ANALOG_GAIN_CODE_CTXT1_REG	000d dddd 0000 0000	0 (0x0000)
R0x3866	DIGITAL_GAIN_CODE_G_CTXT1_REG	0ddd dddd 0ddd dddd	8224 (0x2020)

Table 3. MANUFACTURER SPECIFIC (continued)
(1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic)

Register Hex	Name	Data Format (Binary)	Default Value Dec(Hex)
R0x3868	DIGITAL_GAIN_CODE_RB_CTXT1_REG	0ddd dddd 0ddd dddd	8224 (0x2020)
R0x386A	DP_OFFSET_GR_CTXT1_REG	0000 dddd dddd dddd	256 (0x0100)
R0x386C	DP_OFFSET_GB_CTXT1_REG	0000 dddd dddd dddd	256 (0x0100)
R0x386E	DP_OFFSET_R_CTXT1_REG	0000 dddd dddd dddd	256 (0x0100)
R0x3870	DP_OFFSET_B_CTXT1_REG	0000 dddd dddd dddd	256 (0x0100)
R0x387A	FRAME_LENGTH_CTXT2_REG	dddd dddd dddd dddd	3160 (0x0C58)
R0x387C	SUBSAMPLING_CTXT2_REG	0000 0000 0000 dddd	0 (0x0000)
R0x387E	ROI_ACTIVE_CTXT2_REG	0000 0000 dddd dddd	1 (0x0001)
R0x3880	INTEGRATION_COARSE_CTXT2_REG	dddd dddd dddd dddd	3000 (0x0BB8)
R0x3882	INTEGRATION_FINE_CTXT2_REG	dddd dddd dddd dddd	0 (0x0000)
R0x3884	ANALOG_GAIN_CODE_CTXT2_REG	000d dddd 0000 0000	0 (0x0000)
R0x3886	DIGITAL_GAIN_CODE_G_CTXT2_REG	0ddd dddd 0ddd dddd	8224 (0x2020)
R0x3888	DIGITAL_GAIN_CODE_RB_CTXT2_REG	0ddd dddd 0ddd dddd	8224 (0x2020)
R0x388A	DP_OFFSET_GR_CTXT2_REG	0000 dddd dddd dddd	256 (0x0100)
R0x388C	DP_OFFSET_GB_CTXT2_REG	0000 dddd dddd dddd	256 (0x0100)
R0x388E	DP_OFFSET_R_CTXT2_REG	0000 dddd dddd dddd	256 (0x0100)
R0x3890	DP_OFFSET_B_CTXT2_REG	0000 dddd dddd dddd	256 (0x0100)
R0x389A	M_LINES_CTXT0_REG	0ddd dddd dddd dddd	0 (0x0000)
R0x389C	F_LINES_CTXT0_REG	0ddd dddd dddd dddd	0 (0x0000)
R0x38A0	M_LINES_CTXT1_REG	0ddd dddd dddd dddd	0 (0x0000)
R0x38A2	F_LINES_CTXT1_REG	0ddd dddd dddd dddd	0 (0x0000)
R0x38A6	M_LINES_CTXT2_REG	0ddd dddd dddd dddd	0 (0x0000)
R0x38A8	F_LINES_CTXT2_REG	0ddd dddd dddd dddd	0 (0x0000)
R0x3972	ACTIVE_CONTEXTS_STATUS_REG	???? ???? 00?? ????	8 (0x0008)
R0x3974	FRAME_LENGTH_STATUS_REG	???? ???? ???? ????	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)
(1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic)

Register Hex	Name	Data Format (Binary)	Default Value Dec(Hex)
R0x3976	INTEGRATION_COARSE_STATUS_REG	???? ???? ???? ????	0 (0x0000)
R0x3978	INTEGRATION_FINE_STATUS_REG	???? ???? ???? ????	0 (0x0000)
R0x3982	ANALOG_GAIN_CODE_REG_STATUS_REG	000? ???? 0000 0000	0 (0x0000)
R0x3984	DG_FACTOR_G_REG_STATUS_REG	0??? ???? 0??? ????	0 (0x0000)
R0x3986	DG_FACTOR_RB_REG_STATUS_REG	0??? ???? 0??? ????	0 (0x0000)
R0x3988	DP_OFFSET_GR_STATUS_REG	0000 ???? ???? ????	0 (0x0000)
R0x398A	DP_OFFSET_GB_STATUS_REG	0000 ???? ???? ????	0 (0x0000)
R0x398C	DP_OFFSET_R_STATUS_REG	0000 ???? ???? ????	0 (0x0000)
R0x398E	DP_OFFSET_B_STATUS_REG	0000 ???? ???? ????	0 (0x0000)
R0x3E0E	TEST_PATTERN_MODE_REG	0000 0000 0000 dddd	0 (0x0000)
R0x3E10	TEST_DATA_RED_REG	000d dddd dddd dddd	0 (0x0000)
R0x3E12	TEST_DATA_GREENR_REG	000d dddd dddd dddd	0 (0x0000)
R0x3E14	TEST_DATA_BLUE_REG	000d dddd dddd dddd	0 (0x0000)
R0x3E16	TEST_DATA_GREENB_REG	000d dddd dddd dddd	0 (0x0000)
R0x3E28	HISPI_CONTROL_COMMON_REG	0ddd dddd 0ddd dddd	9519 (0x252F)
R0x3E2E	PIX_COMP_CTRL_REG	0000 0000 0000 000d	0 (0x0000)
R0x3E32	HISPI_BLANKING_DATA_REG	dddd dddd dddd dddd	934 (0x03A6)
R0x3E40	MDH_MONITOR_REG	0ddd dddd dddd dddd	0 (0x0000)
R0x3E42	HISPI_STATUS_REG	0000 0000 ???? 0???	244 (0x00F4)
R0x3E80	CLK_DOMAIN_CTRL_REG	d000 0000 0000 dddd	9 (0x0009)

REGISTER DESCRIPTIONS

Manufacturer Specific Register Descriptions

Attributes Columns; Usage and Values, left to right

Column 1; Buffering	Column 2; Bad Frame	Column 3; Embedded	Column 4; Locked
<blank> = Unbuffered S = Single Frame Synced D = Double Frame Synced	<blank> = No bad frame Y = Causes a bad frame YM = Maskable bad frame	<blank> = Not embedded E = embedded	<blank> = Not locked L = locked

Table 4. MANUFACTURER SPECIFIC
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x0002	**15:0**	**0x0001**	**REVISION_NUMBER_REG (R/W)**				
	15:8	0x0000	REVISION_NUMBER_MINOR Minor Silicon Revision Number.				
	7:0	0x0001	REVISION_NUMBER_MAJOR Major Silicon Revision Number.				
R0x3012	**15:0**	**0x0000**	**Chip Configuration**				
	15:0	0x0000	Bits [1:0] - RGB/Mono : 0b01 = color /0b10 = mono / 0b11 = Reserved Bits [4:2] - Resolution : 0b000 = 12MP / 0b011 = 8MP Bits [6:5] - Speed grade : 0b00 = 24 ports / 0b01 = 12 ports /0b 11 = 6 ports Bits [8:7] - Lens shift : 0b00 = 0 degree /0b01 = 7.3 degree				

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3602	**15:0**	**0x01AD**	**MONITOR_CTRL_REG (R/W)**				
	15	0x0000	Reserved				
	14:9	X	Reserved				
	8:6	0x0006	MONITOR2_CTRL Monitor2 Source 0x0; static 0 0x1; static 1 0x2: monitor2 from sequencer 0x3: monitor2 from bottom datapath 0x4: monitor2 from top datapath 0x5: monitor2 from sensor config 0x6: monitor2 from clock and reset others: static 0				
	5:3	0x0005	MONITOR1_CTRL Monitor1 Source 0x0; static 0 0x1; static 1 0x2: monitor1 from sequencer 0x3: monitor1 from bottom datapath 0x4: monitor1 from top datapath 0x5: monitor1 from sensor config 0x6: monitor1 from clock and reset others: static 0				
	2:0	0x0005	MONITOR0_CTRL Monitor0 source 0x0; static 0 0x1; static 1 0x2: monitor0 from sequencer 0x3: monitor0 from bottom datapath 0x4: monitor0 from top datapath 0x5: monitor0 from sensor config 0x6: monitor0 from clock and reset others: static 0				

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3700	**15:0**	**0x0080**	**RESET_REGISTER_REG (R/W)**				
	15	0x0000	Reserved				
	14:8	X	Reserved				
	7	0x0001	Reserved				
	6	0x0000	Reserved				
	5	0x0000	Reserved				
	4	0x0000	STANDBY_PWR_AHM Enter Standby State after Powering up the Analog Blocks		**Y**		
	3	0x0000	STANDBY_PWR_PLL Enter Standby State after Enabling the PLL		**Y**		
	2	0x0000	STREAM_STANDBYN Control the Sensor Operation. ‘0’: Standby Request, ‘1’: Streaming Request		**Y**		
	1	X	Reserved				
	0	0x0000	Reserved				

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3800	**15:0**	**0x0002**	**GENERAL_CONFIG0_REG (R/W)**				
	15:8	0x0000	FRAMES Number of frames to readout. '0' = continuous in non-triggered mode '0' = no frame readout in triggered mode	**S**			
	7	0x0000	Reserved				
	6	0x0000	Reserved				
	5	0x0000	SLAVE_MODE Integration Trigger Mode (only valid when triggered_mode = '1') '0': MASTER - Integration Control handled by Sequencer '1': SLAVE - Integration Control handled by TRIG_INT pin		**Y**		
	4	0x0000	TRIGGERED_MODE Integration Trigger Configuration '0': Non-Triggered '1': Triggered		**Y**		
	3	0x0000	LINE_TRIGGER_EN Line Trigger Readout Configuration '0': Sequencer Master Readout '1': Line Triggered Readout Note: frame_trigger_en has priority over this configuration.		**Y**		
	2	0x0000	FRAME_TRIGGER_EN Frame Trigger Readout Configuration '0': Sequencer Master Readout '1' Frame Triggered Readout		**Y**		
	1	0x0001	COLOR Color/Monochrome Configuration '0': Monochrome '1': Color				
	0	0x0000	ENABLE Enable sequencer '0': Idle '1': Enabled				

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3802	**15:0**	**0x0300**	**GENERAL_CONFIG1_REG (R/W)**				
	15	0x0000	Reserved				
	14	0x0000	Reserved				
	13	0x0000	EXT_EMB_DATA_EN Extended Embedded Data				
	12	0x0000	SEL_MONO_ODD Select Even/Odd Columns in Mono Subsampling ‘0’: Even Columns ‘1’: Odd Columns		**Y**		
	11	0x0000	SWAP_TOP_BTM_ASC Swap top/bottom ‘0’: Green on top ‘1’: Green on bottom		**Y**		
	10	0x0000	INT_PRIORITY Integration Priority ‘0’: Frame Readout has Priority over Integration ‘1’: Integration End has Priority over Frame Readout				
	9	0x0001	OFFSET_LAT_COMP Offset Latency Compensation ‘0’: No Compensation ‘1’: 1 Frame Compensation (Synchronized to Integration Updates)				
	8	0x0001	GAIN_LAT_COMP Gain Latency Compensation ‘0’: No Compensation ‘1’: 1 Frame Compensation (Synchronized to Integration Updates)				
	7:6	X	Reserved				
	5	0x0000	Reserved				
	4	0x0000	FRAME_TRIGGER_MODE Frame Trigger Mode ‘0’: Start Frame Readout upon Rising Edge ‘1’: Trigger = Asynchronous Sequencer Enable For frame_trigger_mode = ‘1’: - Readout of *frames* number of *frames* when frames > 0 - Continue frame readout as long as TRIG_RD is asserted (*frames* = 0)		**Y**		
	3	X	Reserved				
	2:0	0x0000	TRIGGER_POLARITY Active Trigger Polarity trigger_polarity[0]: TRIG_INT Polarity trigger_polarity[2]: TRIG_RD Polarity				

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3804	**15:0**	**0x1111**	**CONTEXTS_REG (R/W)**				
	15:12	0x0001	FRAMES_CTXT2 Frames in Context 2	S			
	11:8	0x0001	FRAMES_CTXT1 Frames in Context 1	S			
	7:4	0x0001	FRAMES_CTXT0 Frames in Context 0	S			
	3	0x0000	FRAME_LENGTH_CTXT_MODE Frame Length Context Mode ‘0’: Frame Length is Context Switched Together with Integration ‘1’: Frame Length is Context Switched together with ROI Context Switches	S			
	2:0	0x0001	ACTIVE_CONTEXTS Bitmap Indicating which Contexts are Valid active_contexts[0]: Context 0 Selection active_contexts[1]: Context 1 Selection active_contexts[2]: Context 2 Selection	S			

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3806	**15:0**	**0x0000**	**MONITOR_REG (R/W)**				
	15	X	Reserved				
	14:10	0x0000	MONITOR2_SELECT Sequencer Monitor_2 Selection Refer to monitor0_select for further descriptions				
	9:5	0x0000	MONITOR1_SELECT Sequencer Monitor_1 Selection Refer to monitor0_select for further descriptions				
	4:0	0x0000	MONITOR0_SELECT Sequencer Monitor_0 Selection 0x00: '0' 0x01: new_line 0x02: integrate 0x03: integrate_lead 0x04: Reserved 0x05: Reserved 0x06: fsm_monitor (real integration) 0x07: lsm_monitor 0x08: TRIG_INT Rising Edge Acceptance 0x09: TRIG_INT Falling Edge Acceptance 0x0A: Reserved 0x0B: Reserved 0x0C: TRIG_RD Rising Edge Acceptance 0x0D: TRIG_RD Falling Edge Acceptance 0x0E: Global Sequence Active (FOT Overhead) 0x0F: SFOT Indication 0x10: EFOT Indication 0x11: End of Global (Frame Overhead) Sequence 0x12: End of Row Overhead Sequence 0x13: M-Line Active 0x14: Reserved 0x15: Effective (ROI) Line Active 0x16: Overrun Indication 0x17: Reserved 0x18: Reserved 0x19: Integration Request 0x1A: Reserved 0x1B: Reserved 0x1C: Integration End Request 0x1D: Reserved 0x1E: Reserved 0x1F: Reserved				
R0x3808	**15:0**	**0x0000**	**MONITOR_INTEGRATION_LEAD_REG (R/W)**				
	15:0	0x0000	MONITOR_INTEGRATION_LEAD Integration Lead for Monitoring. Expressed in lines				

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x380A	**15:0**	**0x000F**	**SYNC_CONFIG_REG (R/W)**				
	15:9	X	Reserved				
	8	0x0000	INTEGRATION_SYNC_MODE '0': exposure configurations are sync'ed at the start of a new frame (EFOT). '1': exposure configurations sync is disabled (continuously syncing). This mode is only relevant for Triggered-master mode, where the exposure configurations are sync'ed at the start of exposure rather than the start of EFOT. For all other modes it should be set to 0 Note: Sync is still postponed if sync_exposure='0'				
	7:4	X	Reserved				
	3	0x0001	SYNC_ROI ROI Configuration Synch'ing '0': ROI Configurations are frozen and will not be synch'ed at the next frame boundaries. Reconfiguration will not have any impact on image grabbing '1': ROI Configurations are Synch'ed at the next frame boundary				
	2	0x0001	SYNC_OFFSET Offset Configuration Synch'ing '0': Offset Configurations are frozen and will not be synch'ed at the next frame boundaries. Reconfiguration will not have any impact on image grabbing '1': Offset Configurations are Synch'ed at the next frame boundary				
	1	0x0001	SYNC_GAIN Gain (Analog and Digital) Configuration Synch'ing '0': Gain Configurations are frozen and will not be synch'ed at the next frame boundaries. Reconfiguration will not have any impact on image grabbing '1': Gain Configurations are Synch'ed at the next frame boundary				
	0	0x0001	SYNC_INTEGRATION Integration Configuration Synch'ing '0': Integration Configurations are frozen and will not be synch'ed at the next frame boundaries. Reconfiguration will not have any impact on image grabbing '1': Integration Configurations are Synch'ed at the next frame boundary				

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x380E	**15:0**	**0x0000**	**ACTIVE_CONFIG_REG (R/W)**				
	15:2	X	Reserved				
	1	0x0000	ACTIVE_REVERSED ROI Readout Direction '0': Bottom to Top '1': Top to Bottom	S			
	0	0x0000	Reserved				
R0x3810	**15:0**	**0x016E**	**LINE_TIME_REG (R/W)**				
	15:0	0x016E	LINE_TIME Line Time Unit is Sequencer Clock Cycles		Y		
R0x3812	**15:0**	**0x0000**	**INTEGRATION_OFFSET_COARSE_REG (R/W)**	S			
	15:12	X	Reserved				
	11:8	0x0000	Reserved				
	7:4	0x0000	Reserved				
	3:0	0x0000	INTEGRATION_OFFSET_COARSE Coarse Integration Offset Unit is #lines	S			
R0x381A	**15:0**	**0x0000**	**ROI0_START_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0000	Y_START_0 ROI0 Y Start Address Unit is One Kernel (4 Lines)	S			
R0x381C	**15:0**	**0x0302**	**ROI0_SIZE_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0302	Y_SIZE_0 ROI0 Y Size Unit is One Kernel (4 Lines)	S			
R0x381E	**15:0**	**0x0000**	**ROI1_START_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0000	Y_START_1 ROI1 Y Start Address Unit is One Kernel (4 Lines)	S			
R0x3820	**15:0**	**0x0302**	**ROI1_SIZE_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0302	Y_SIZE_1 ROI1 Y Size Unit is One Kernel (4 Lines)	S			

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3822	**15:0**	**0x0000**	**ROI2_START_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0000	Y_START_2 ROI2 Y Start Address Unit is One Kernel (4 Lines)	S			
R0x3824	**15:0**	**0x0302**	**ROI2_SIZE_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0302	Y_SIZE_2 ROI2 Y Size Unit is One Kernel (4 Lines)	S			
R0x3826	**15:0**	**0x0000**	**ROI3_START_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0000	Y_START_3 ROI3 Y Start Address Unit is One Kernel (4 Lines)	S			
R0x3828	**15:0**	**0x0302**	**ROI3_SIZE_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0302	Y_SIZE_3 ROI3 Y Size Unit is One Kernel (4 Lines)	S			
R0x382A	**15:0**	**0x0000**	**ROI4_START_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0000	Y_START_4 ROI4 Y Start Address Unit is One Kernel (4 Lines)	S			
R0x382C	**15:0**	**0x0302**	**ROI4_SIZE_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0302	Y_SIZE_4 ROI4 Y Size Unit is One Kernel (4 Lines)	S			
R0x382E	**15:0**	**0x0000**	**ROI5_START_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0000	Y_START_5 ROI5 Y Start Address Unit is One Kernel (4 Lines)	S			
R0x3830	**15:0**	**0x0302**	**ROI5_SIZE_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0302	Y_SIZE_5 ROI5 Y Size Unit is One Kernel (4 Lines)	S			

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3832	**15:0**	**0x0000**	**ROI6_START_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0000	Y_START_6 ROI6 Y Start Address Unit is One Kernel (4 Lines)	S			
R0x3834	**15:0**	**0x0302**	**ROI6_SIZE_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0302	Y_SIZE_6 ROI6 Y Size Unit is One Kernel (4 Lines)	S			
R0x3836	**15:0**	**0x0000**	**ROI7_START_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0000	Y_START_7 ROI7 Y Start Address Unit is One Kernel (4 Lines)	S			
R0x3838	**15:0**	**0x0302**	**ROI7_SIZE_REG (R/W)**	S			
	15:10	X	Reserved				
	9:0	0x0302	Y_SIZE_7 ROI7 Y Size Unit is One Kernel (4 Lines)	S			
R0x383A	**15:0**	**0x0C58**	**FRAME_LENGTH_CTXT0_REG (R/W)**	S			
	15:0	0x0C58	FRAME_LENGTH_CTXT0 Frame Length Unit is #Lines. Granularity defined by mult_timer	S			
R0x383C	**15:0**	**0x0000**	**SUBSAMPLING_CTXT0_REG (R/W)**	S			
	15:4	X	Reserved				
	3	0x0000	ACTIVE_SUBSAMPLING_Y_CTXT0 Subsampling (Row) for ROI Configurations	S			
	2	0x0000	Reserved	S			
	1	0x0000	M_SUBSAMPLING_Y_CTXT0 Subsampling (Row) for M Region	S			
	0	0x0000	SUBSAMPLING_X_CTXT0 Readout in Column Subsampling Mode	S			
R0x383E	**15:0**	**0x0001**	**ROI_ACTIVE_CTXT0_REG (R/W)**	S			
	15:8	X	Reserved				
	7:0	0x0001	ROI_ACTIVE_CTXT0 Active ROI Selection. Each Bit Corresponds to One ROI	S			

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3840	**15:0**	**0x0BB8**	**INTEGRATION_COARSE_CTXT0_REG (R/W)**	S			
	15:0	0x0BB8	INTEGRATION_COARSE_CTXT0 Coarse Integration Time Unit is number of Lines.	S			
R0x3842	**15:0**	**0x0000**	**INTEGRATION_FINE_CTXT0_REG (R/W)**	S			
	15:0	0x0000	INTEGRATION_FINE_CTXT0 Fine Integration Time (Fractional) Unit is Sequencer Clock Cycles	S			
R0x3844	**15:0**	**0x0000**	**ANALOG_GAIN_CODE_CTXT0_REG (R/W)**	**S**			
	15:13	X	Reserved				
	12:11	0x0000	Reserved				
	10:8	0x0000	Analog _Gain_CTXT0 0x1: 1x 0x3: 2x 0x7: 4x	**S**			
	7:0	X	Reserved				
R0x3846	**15:0**	**0x2020**	**DIGITAL_GAIN_CODE_G_CTXT0_REG (R/W)**	**S**			
	15	X	Reserved				
	14:8	0x0020	DG_FACTOR_GR_CTXT0 Digital Gain Factor for GR Pixels x1/32~x2, 1/32 step	**S**			
	7	X	Reserved				
	6:0	0x0020	DG_FACTOR_GB_CTXT0 Digital Gain Factor for GB Pixels x1/32~x2, 1/32 step	**S**			
R0x3848	**15:0**	**0x2020**	**DIGITAL_GAIN_CODE_RB_CTXT0_REG (R/W)**	**S**			
	15	X	Reserved				
	14:8	0x0020	DG_FACTOR_R_CTXT0 Digital Gain Factor for R Pixels x1/32~x2, 1/32 step	**S**			
	7	X	Reserved				
	6:0	0x0020	DG_FACTOR_B_CTXT0 Digital Gain Factor for B Pixels x1/32~x2, 1/32 step	**S**			

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x384A	**15:0**	**0x0100**	**DP_OFFSET_GR_CTXT0_REG (R/W)**	S			
	15:12	X	Reserved				
	11:0	0x0100	DP_OFFSET_GR_CTXT0 Data Pedestal for GR Pixels	S			
R0x384C	**15:0**	**0x0100**	**DP_OFFSET_GB_CTXT0_REG (R/W)**	S			
	15:12	X	Reserved				
	11:0	0x0100	DP_OFFSET_GB_CTXT0 Data Pedestal for GB Pixels	S			
R0x384E	**15:0**	**0x0100**	**DP_OFFSET_R_CTXT0_REG (R/W)**	S			
	15:12	X	Reserved				
	11:0	0x0100	DP_OFFSET_R_CTXT0 Data Pedestal for R Pixels	S			
R0x3850	**15:0**	**0x0100**	**DP_OFFSET_B_CTXT0_REG (R/W)**	S			
	15:12	X	Reserved				
	11:0	0x0100	DP_OFFSET_B_CTXT0 Data Pedestal for B Pixels	S			
R0x385A	**15:0**	**0x0C58**	**FRAME_LENGTH_CTXT1_REG (R/W)**	S			
	15:0	0x0C58	FRAME_LENGTH_CTXT1 Frame Length Unit is number of Lines.	S			
R0x385C	**15:0**	**0x0000**	**SUBSAMPLING_CTXT1_REG (R/W)**	S			
	15:4	X	Reserved				
	3	0x0000	ACTIVE_SUBSAMPLING_Y_CTXT1 Subsampling (Row) for ROI Configurations	S			
	2	0x0000	Reserved	S			
	1	0x0000	M_SUBSAMPLING_Y_CTXT1 Subsampling (Row) for M Region	S			
	0	0x0000	SUBSAMPLING_X_CTXT1 Readout in Column Subsampling Mode	S			
R0x385E	**15:0**	**0x0001**	**ROI_ACTIVE_CTXT1_REG (R/W)**	S			
	15:8	X	Reserved				
	7:0	0x0001	ROI_ACTIVE_CTXT1 Active ROI Selection. Each Bit Corresponds to One ROI	S			
R0x3860	**15:0**	**0x0BB8**	**INTEGRATION_COARSE_CTXT1_REG (R/W)**	S			
	15:0	0x0BB8	INTEGRATION_COARSE_CTXT1 Coarse Integration Time Unit is number of Lines.	S			
R0x3862	**15:0**	**0x0000**	**INTEGRATION_FINE_CTXT1_REG (R/W)**	S			
	15:0	0x0000	INTEGRATION_FINE_CTXT1 Fine Integration Time (Fractional) Unit is Sequencer Clock Cycles	S			

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3864	**15:0**	**0x0000**	**ANALOG_GAIN_CODE_CTXT1_REG (R/W)**	**S**			
	15:13	X	Reserved				
	12:11	0x0000	Reserved				
	10:8	0x0000	Analog _Gain_CTXT1 0x1: 1x 0x3: 2x 0x7: 4x	**S**			
	7:0	X	Reserved				
R0x3866	**15:0**	**0x2020**	**DIGITAL_GAIN_CODE_G_CTXT1_REG (R/W)**	**S**			
	15	X	Reserved				
	14:8	0x0020	DG_FACTOR_GR_CTXT1 Digital Gain Factor for GR Pixels x1/32~x2, 1/32 step	**S**			
	7	X	Reserved				
	6:0	0x0020	DG_FACTOR_GB_CTXT1 Digital Gain Factor for GB Pixels x1/32~x2, 1/32 step	**S**			
R0x3868	**15:0**	**0x2020**	**DIGITAL_GAIN_CODE_RB_CTXT1_REG (R/W)**	**S**			
	15	X	Reserved				
	14:8	0x0020	DG_FACTOR_R_CTXT1 Digital Gain Factor for R Pixels x1/32~x2, 1/32 step	**S**			
	7	X	Reserved				
	6:0	0x0020	DG_FACTOR_B_CTXT1 Digital Gain Factor for B Pixels x1/32~x2, 1/32 step	**S**			
R0x386A	**15:0**	**0x0100**	**DP_OFFSET_GR_CTXT1_REG (R/W)**	S			
	15:12	X	Reserved				
	11:0	0x0100	DP_OFFSET_GR_CTXT1 Data Pedestal for GR Pixels	S			
R0x386C	**15:0**	**0x0100**	**DP_OFFSET_GB_CTXT1_REG (R/W)**	S			
	15:12	X	Reserved				
	11:0	0x0100	DP_OFFSET_GB_CTXT1 Data Pedestal for GB Pixels	S			

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x386E	**15:0**	**0x0100**	**DP_OFFSET_R_CTXT1_REG (R/W)**	S			
	15:12	X	Reserved				
	11:0	0x0100	DP_OFFSET_R_CTXT1 Data Pedestal for R Pixels	S			
R0x3870	**15:0**	**0x0100**	**DP_OFFSET_B_CTXT1_REG (R/W)**	S			
	15:12	X	Reserved				
	11:0	0x0100	DP_OFFSET_B_CTXT1 Data Pedestal for B Pixels	S			
R0x387A	**15:0**	**0x0C58**	**FRAME_LENGTH_CTXT2_REG (R/W)**	S			
	15:0	0x0C58	FRAME_LENGTH_CTXT2 Frame Length Unit is number of lines.	S			
R0x387C	**15:0**	**0x0000**	**SUBSAMPLING_CTXT2_REG (R/W)**	S			
	15:4	X	Reserved				
	3	0x0000	ACTIVE_SUBSAMPLING_Y_CTXT2 Subsampling (Row) for ROI Configurations	S			
	2	0x0000	Reserve	S			
	1	0x0000	M_SUBSAMPLING_Y_CTXT2 Subsampling (Row) for M Region	S			
	0	0x0000	SUBSAMPLING_X_CTXT2 Readout in Column Subsampling Mode	S			
R0x387E	**15:0**	**0x0001**	**ROI_ACTIVE_CTXT2_REG (R/W)**	S			
	15:8	X	Reserved				
	7:0	0x0001	ROI_ACTIVE_CTXT2 Active ROI Selection. Each Bit Corresponds to One ROI	S			
R0x3880	**15:0**	**0x0BB8**	**INTEGRATION_COARSE_CTXT2_REG (R/W)**	S			
	15:0	0x0BB8	INTEGRATION_COARSE_CTXT2 Coarse Integration Time Unit is number of lines.				
R0x3882	**15:0**	**0x0000**	**INTEGRATION_FINE_CTXT2_REG (R/W)**	S			
	15:0	0x0000	INTEGRATION_FINE_CTXT2 Fine Integration Time (Fractional) Unit is Sequencer Clock Cycles	S			

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3884	**15:0**	**0x0000**	**ANALOG_GAIN_CODE_CTXT2_REG (R/W)**	**S**			
	15:13	X	Reserved				
	12:11	0x0000	Reserved				
	10:8	0x0000	Analog _Gain_CTXT2 0x1: 1x 0x3: 2x 0x7: 4x	**S**			
	7:0	X	Reserved				
R0x3886	**15:0**	**0x2020**	**DIGITAL_GAIN_CODE_G_CTXT2_REG (R/W)**	**S**			
	15	X	Reserved				
	14:8	0x0020	DG_FACTOR_GR_CTXT2 Digital Gain Factor for GR Pixels x1/32~x2, 1/32 step	**S**			
	7	X	Reserved				
	6:0	0x0020	DG_FACTOR_GB_CTXT2 Digital Gain Factor for GB Pixels x1/32~x2, 1/32 step	**S**			
R0x3888	**15:0**	**0x2020**	**DIGITAL_GAIN_CODE_RB_CTXT2_REG (R/W)**	**S**			
	15	X	Reserved				
	14:8	0x0020	DG_FACTOR_R_CTXT2 Digital Gain Factor for R Pixels x1/32~x2, 1/32 step	**S**			
	7	X	Reserved				
	6:0	0x0020	DG_FACTOR_B_CTXT2 Digital Gain Factor for B Pixels x1/32~x2, 1/32 step	**S**			
R0x388A	**15:0**	**0x0100**	**DP_OFFSET_GR_CTXT2_REG (R/W)**	S			
	15:12	X	Reserved				
	11:0	0x0100	DP_OFFSET_GR_CTXT2 Data Pedestal for GR Pixels	S			
R0x388C	**15:0**	**0x0100**	**DP_OFFSET_GB_CTXT2_REG (R/W)**	S			
	15:12	X	Reserved				
	11:0	0x0100	DP_OFFSET_GB_CTXT2 Data Pedestal for GB Pixels	S			

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x388E	**15:0**	**0x0100**	**DP_OFFSET_R_CTXT2_REG (R/W)**	S			
	15:12	X	Reserved				
	11:0	0x0100	DP_OFFSET_R_CTXT2 Data Pedestal for R Pixels	S			
R0x3890	**15:0**	**0x0100**	**DP_OFFSET_B_CTXT2_REG (R/W)**	S			
	15:12	X	Reserved				
	11:0	0x0100	DP_OFFSET_B_CTXT2 Data Pedestal for B Pixels	S			
R0x389A	**15:0**	**0x0000**	**M_LINES_CTXT0_REG (R/W)**	S			
	15	X	Reserved				
	14:10	0x0000	M_SUPPRESSED_CTXT0 Suppress the Readout of Initial Lines in the M Region in Context 0 Unit is #lines	S			
	9:0	0x0000	M_LINES_CTXT0 Number of Lines to Read from M Region in Context 0 Unit is #lines	S			
R0x38A0	**15:0**	**0x0000**	**M_LINES_CTXT1_REG (R/W)**	S			
	15	X	Reserved				
	14:10	0x0000	M_SUPPRESSED_CTXT1 Suppress the Readout of Initial Lines in the M Region in Context 1 Unit is #lines	S			
	9:0	0x0000	M_LINES_CTXT1 Number of Lines to Read from M Region in Context 1 Unit is #lines	S			
	15	X	Reserved				
	14:10	0x0000	Reserved				
	9:0	0x0000	Reserved				
R0x38A6	**15:0**	**0x0000**	**M_LINES_CTXT2_REG (R/W)**	S			
	15	X	Reserved				
	14:10	0x0000	M_SUPPRESSED_CTXT2 Suppress the Readout of Initial Lines in the M Region in Context 2 Unit is number of lines	S			
	9:0	0x0000	M_LINES_CTXT2 Number of Lines to Read from M Region in Context 2 Unit is number of lines	S			

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3972	**15:0**	**0x0008**	**ACTIVE_CONTEXTS_STATUS_REG (RO)**				
	15:8	RO	FRAME_COUNT Frame Count Number Incremented at the start of every new frame. When 255 is reached, the counter rolls over to 0 and starts incrementing again.				
	7:6	X	Reserved				
	5	X	Reserved				
	4	X	Reserved				
	3	RO	HALT Flag set When SCU is Halted				
	2:0	RO	ACTIVE_CONTEXT Currently Active Context 0x1: Context 0 Enabled 0x2: Context 1 Enabled 0x4:Context 2 Enabled				
R0x3974	**15:0**	**0x0000**	**FRAME_LENGTH_STATUS_REG (RO)**				
	15:0	RO	FRAME_LENGTH Current Frame Length (not in Slave mode)				
R0x3976	**15:0**	**0x0000**	**INTEGRATION_COARSE_STATUS_REG (RO)**				
	15:0	RO	INTEGRATION_COARSE Current Coarse Exposure Time (not in Slave mode)				
R0x3978	**15:0**	**0x0000**	**INTEGRATION_FINE_STATUS_REG (RO)**				
	15:0	RO	INTEGRATION_FINE Current Fine Exposure Time (not in Slave mode)				
R0x3982	**15:0**	**0x0000**	**ANALOG_GAIN_CODE_REG_STATUS_REG (RO)**				
	15:13	X	Reserved				
	12	RO	Reserved				
	11:8	RO	CIN_CTRL Current Analog Gain				
	7:0	X	Reserved				
R0x3984	**15:0**	**0x0000**	**DG_FACTOR_G_REG_STATUS_REG (RO)**				
	15	X	Reserved				
	14:8	RO	DG_FACTOR_GR Current Digital Gain GR Pixels				
	7	X	Reserved				
	6:0	RO	DG_FACTOR_GB Current Digital Gain GB Pixels				

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3986	**15:0**	**0x0000**	**DG_FACTOR_RB_REG_STATUS_REG (RO)**				
	15	X	Reserved				
	14:8	RO	DG_FACTOR_R Current Digital Gain R Pixels				
	7	X	Reserved				
	6:0	RO	DG_FACTOR_B Current Digital Gain B Pixels				
R0x3988	**15:0**	**0x0000**	**DP_OFFSET_GR_STATUS_REG (RO)**				
	15:12	X	Reserved				
	11:0	RO	DP_OFFSET_GR Current Data Pedestal for GR Pixels				
R0x398A	**15:0**	**0x0000**	**DP_OFFSET_GB_STATUS_REG (RO)**				
	15:12	X	Reserved				
	11:0	RO	DP_OFFSET_GB Current Data Pedestal for GB Pixels				
R0x398C	**15:0**	**0x0000**	**DP_OFFSET_R_STATUS_REG (RO)**				
	15:12	X	Reserved				
	11:0	RO	DP_OFFSET_R Current Data Pedestal for R Pixels				
R0x398E	**15:0**	**0x0000**	**DP_OFFSET_B_STATUS_REG (RO)**				
	15:12	X	Reserved				
	11:0	RO	DP_OFFSET_B Current Data Pedestal for B Pixels				

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
	15:0	**0x0000**	**TEST_PATTERN_MODE_REG (R/W)**	**S**			
	15:4	X	Reserved				
	3	0x0000	Reserved	**S**			
R0x3E0E	2:0	0x0000	TEST_PATTERN_MODE Test Pattern Selection 0x0: Normal Operation 0x1: Solid Color 0x2: Color Bar 0x3: Fade-to-Gray 0x4:Diagonal-Gray 1x 0x5: Diagonal-Gray 3x 0x6: White/Black Bar (Coarse) 0x7: White/Black Bar (Fine) If 0x3 (fade-to-gray) is selected, test_data* should be all-0 or all-1. Other values are not supported in this mode. If 0x7 (white/black bar fine) is selected, test_data_red/greenr should be configured with the same value.	**S**			
	15:0	**0x0000**	**TEST_DATA_RED_REG (R/W)**	**S**			
	15:13	X	Reserved				
R0x3E10	12:0	0x0000	TEST_DATA_RED Data Inserted into the Data Path for Solid Color Mode. This register is used for white/ black bar fine width for the bottom channels.	**S**			
	15:0	**0x0000**	**TEST_DATA_GREENR_REG (R/W)**	**S**			
	15:13	X	Reserved				
R0x3E12	12:0	0x0000	TEST_DATA_GREENR Data Inserted into the Data Path for Solid Color Mode. This register is used for white/ black bar fine width for the top channels.	**S**			
	15:0	**0x0000**	**TEST_DATA_BLUE_REG (R/W)**	**S**			
	15:13	X	Reserved				
R0x3E14	12:0	0x0000	TEST_DATA_BLUE Data Inserted into the Data Path for Solid Color Mode.	**S**			
	15:0	**0x0000**	**TEST_DATA_GREENB_REG (R/W)**	**S**			
	15:13	X	Reserved				
R0x3E16	12:0	0x0000	TEST_DATA_GREENB Data Inserted into the Data Path for Solid Color Mode.	**S**			

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
	15:0	**0x252F**	**HISPI_CONTROL_COMMON_REG (R/W)**				
	15	X	Reserved				
	14	0x0000	Reserved				
	13	0x0001	Reserved				
	12	0x0000	Reserved				
	11	0x0000	Reserved				
	10:8	0x0005	HISPI_PIXEL_DEPTH Serial Link Data Width 0x4: 10 bit (Companding) 0x5:: 12 bit others: Not Supported		Y		
	7	X	Reserved				
	6	0x0000	Reserved				
R0x3E28	5:4	0x0002	HISPI_MUX_SEL Multiplexing Scheme 0x0: 4:4 Multiplex 0x1: 4:3 Multiplex 0x2: 4:2 Multiplex 0x3: 4:1 Multiplex		Y		
	3	0x0001	Reserved				
	2	0x0001	Reserved				
	1	0x0001	OUTPUT_MSB_FIRST Serializer Output Order ‘0’: LSB first ‘1’: MSB first				
	0	0x0001	HISPI_IF_EN HiSpi I/F Enable ‘0’: Disabled ‘1’: Enabled				
R03E2E	**15:0**	**0x0000**	**PIX_COMP_CTRL_REG(R/W)**	S			
	15:1	X	Reserved				
	0	0x0000	COMP_EN_12_TO_10 Companding ‘0’: No data compression ‘1’: 12 bit to 10 bit pixel compression				
	15:0	**0x03A6**	**HISPI_BLANKING_DATA_REG (R/W)**				
R0x3E32	15:0	0x03A6	BLANKING_DATA Blanking Data Data word sent out during blanking period in HiSpi packetized protocol				

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3E40	**15:0**	**0x0000**	**MDH_MONITOR_REG (R/W)**				
	15	X	Reserved				
	14:10	0x0000	MDH_MONITOR2_SEL Selection of monitor2 Refer to mdh_monitor0_sel for further descriptions				
	9:5	0x0000	MDH_MONITOR1_SEL Selection of monitor1 Refer to mdh_monitor0_sel for further descriptions				
	4:0	0x0000	MDH_MONITOR0_SEL Selection of Monitor 0 Indication 0x00: frame_valid_0_3 0x01: line_valid_0_3 0x02: pixel_valid_0_3 0x03: frame_valid_4_7 0x04: line_valid_4_7 0x05: pixel_valid_4_7 0x06: frame_valid_8_11 0x07: line_valid_8_11 0x08: pixel_valid_8_11 0x09 – 0x18: Reserved				
R0x3E42	**15:0**	**0x00F4**	**HISPI_STATUS_REG (RO)**				
	15:8	X	Reserved				
	7:6	RO	HISPI_MUX_SEL_PROT Maximum Multiplexing Factor 0x0: 4:4 Multiplex 0x1: 4:3 Multiplex 0x2: 4:2 Multiplex 0x3: 4:1 Multiplex				
	5:4	RO	HISPI_MUX_SEL_APPLIED Effectively Applied Multiplexing Scheme 0x0: 4:4 Multiplex 0x1: 4:3 Multiplex 0x2: 4:2 Multiplex 0x3: 4:1 Multiplex				
	3	X	Reserved				
	2	RO	Reserved				
	1	RO	Reserved				
	0	RO	Reserved				

Table 4. MANUFACTURER SPECIFIC (continued)
(R/W (Read or Write) bit; RO (Read Only) Bit)

Register Hex	Bits	Default	Name	Attributes			
R0x3E80	**15:0**	**0x0009**	**CLK_DOMAIN_CTRL_REG (R/W)**				
	15	0x0000	Reserved				
	14:4	X	Reserved				
	3:2	0x0002	CLK_ISP_GATE_SEL Select the Clock Gating Scheme for clk_isp 0x0: 4:4 Multiplex 0x1: 4:3 Multiplex 0x2: 4:2 Multiplex 0x3: 4:1 Multiplex		Y		
	1:0	0x0001	Reserved				

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