REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7480-91-0100	JPG			

IRIS3 ON Semi Python IS Board

Python 300/500/1300 (LCC48)

Python 2000/5000 (LCC84)

Revision 2.20 (Official Release)

August 11, 2016

Revision History

Y7480-00 Rev.A:

R1.00: First Release
R1.10: Updated REF DES (to match PCB)
R1.11:
- All 1uF caps now 16V rated (single 1uF cap usage)

R1.20:
- Changed VCCINT & +1.8V VREG Cfb to 100pF
- Removed delay cap on MGTAVTT VREG STBY pin

R1.21:
- Corrected offpage direction for PEn signals (ZIF right-side)

R1.30:
- Enabled remote JTAG access (CPUB SoC)
- Improved VDDPIX LDO stability (image ripple fix)
  - Reduced total bulk capacitance on VDDPIX
  - Changed LDO ADJ resistor divider value
  - Reduced LDO output capacitance
  - Added LDO feedforward capacitor (PMB 7480-90-000a)

Y7480-01 Rev.A: 7480-91-0100

R2.00:
- Added VDDPIX LDO feedforward capacitor
  - In replacement for PMB 7480-90-000
- Connected PRNST1# and PRSNT2# directly to ground
- Removed support for DXP/N thermal diode sensing
  - Default uses XADC
  - Makes room for PE REFCLK AC caps
- +4x 10uF caps on 5-12V input rail (reduce Vripple)
- +6x 47uF caps on PYT VDDPIX rail (reduce Vripple,default=NI)

R2.10:
- Removed 100MHz OSC (not used anymore)

R2.20:
- Increased FPGA-SPI damping resistor value

Digitally signed by Jean-Philippe Gagnon
Date: 2016.08.11 12:53:44 -04'00'

DRAWN: J-P Gagnon	MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT: IRIS3		
GROUP: Imaging	THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED: Jean-Philippe Gagnon		
ING# 127861	TITLE: IRIS3 Python IS Board	
SIZE: B / DATE: 2016-08-11	DRAWING NO: 7480-04-01 / REV: A / SHEET: 1 OF 13	

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7480-91-0100	JPG			

Locate LED on opposite side of Python

DS100 DL7017RM0

R136 RSK100M01M0

R135 RSK100M01M0

QMN2400M0 Q2-A

QMN2400M0 Q2-B

+3.3V

+1.8V

When VCCBAT is not used, connect to ground or VCCAUX

R130 RS4K75M01M0

FPGA_INIT#

FPGA_DONE

iPU-10k

Rev.1: Remove DXP/N support

SUB=FPGA35T

IF00735C01B2_7478

A6-A

BANK 0

C13	VCCADC_0		CCLK_0	C11	FW_CCLK_R
C9	VCCBATT_0		M0_0	V12	
B12	VREFP_0		M1_0	W11	
A13	VREFN_0		M2_0	U10	
U11	INIT_B_0		PROGRAM_B_0	V10	FPGA_PROG#
A12	VP_0		TDI_0	W10	iPU
B13	VN_0		TDO_0	W8	iPU
			TCK_0	C8	iPU
U12	DONE_0		TMS_0	W9	iPU
A11	DXP_0		CFGBVS_0	V11	
B11	DXN_0		GNDADC_0	C12	

R48 RS49R9M01M0 FW_CCLK

Master SPI: M[2:0] = 001

R131 RS4K75M01M0

CFGBVS: Set low for 1.8V/1.5V IO operation (Banks 0,14)

JTAG inputs are not 3.3V tolerant

FPGA_TCK R124 RSR000M00M0

FPGA_TMS R127 RSR000M00M0

TDI R120 RSR000M00M0

R121 NI RSR000M00M0

NI when Platform Cable USB II used

Install when Platform Cable USB II and only Athena FPGA (remote) in JTAG chain.

TDO	9
FPGA_TDO	9
TCK	9
TMS	9

J101 PHDR014MTSM1 NI

VREF TMS TCK TDO TDI NC HALT

NC GND GND GND GND GND PGND

Platform Cable USB II

Artix-7 decoupling guide (ug483 table 2-1)

+1.8V VCCADC C64 CCU47WMM3 C56 CCU10XKM5

VCCINT C55 CC47UWMM2 6.3V cc0805_0; C67 CC47UWMM2; C120 CC4U7WMM2 6.3V cc0603_2; C130 CC4U7WMM2; C127 CCU47WMM3 16V cc0402_0; C123 CCU47WMM3; C125 CCU47WMM3

VCCINT VCCBRAM C62 CC47UWMM2 6.3V cc0805_0; C132 CCU47WMM3

+1.8V VCCAUX C73 CC47UWMM2; C136 CC4U7WMM2; C119 CCU47WMM3; C138 CCU47WMM3

VCCINT

G10	VCCINT_1		VCCO_0_1	V9	
H10	VCCINT_2		VCCO_0_2	G12	
J10	VCCINT_3		VCCO_14_1	F17	
L10	VCCINT_4		VCCO_14_2	K12	
M10	VCCINT_5		VCCO_14_3	K13	
N10	VCCINT_6		VCCO_14_4	L12	
			VCCO_14_5	L13	
			VCCO_14_6	M12	
			VCCO_14_7	M17	
			VCCO_14_8	R17	
			VCCO_14_9	U13	
		POWER	VCCO_16_1	B19	
			VCCO_16_2	C14	
			VCCO_16_3	C18	
			VCCO_16_4	G13	
M11	VCCBRAM_1		VCCO_34_1	M8	
N11	VCCBRAM_2		VCCO_34_2	N7	
			VCCO_34_3	N8	
			VCCO_34_4	R1	
H13	VCCAUX_1		VCCO_34_5	V1	
J13	VCCAUX_2		VCCO_34_6	V6	
			VCCO_35_1	H3	
			VCCO_35_2	J7	
			VCCO_35_3	K1	
			VCCO_35_4	K7	
			VCCO_35_5	L7	
			VCCO_35_6	M7	

IF00735C01B2_7478

+1.8V +3.3V

VCCO_14 C76 CC47UWMM2; C121 CC4U7WMM2; C131 CC4U7WMM2; C124 CCU47WMM3; C133 CCU47WMM3; C137 CCU47WMM3; C75 CCU47WMM3

Power sequencing: VCCINT (1.0V), VCCBRAM (1.0V), VCCAUX (1.8V) and VCCO (3.3V)
Power sequencing GTP: VCCINT, MGTAVCC, MGTAVTT or MGTAVCC, VCCINT, MGTAVTT

VCCO_16 C72 CC47UWMM2; C68 CC4U7WMM2; C63 CC4U7WMM2; C126 CCU47WMM3; C128 CCU47WMM3; C134 CCU47WMM3; C139 CCU47WMM3

VCCO_34 C51 CC47UWMM2; C106 CC4U7WMM2; C107 CC4U7WMM2; C116 CCU47WMM3; C115 CCU47WMM3; C35 CCU47WMM3; C117 CCU47WMM3

VCCO_35 C22 CC47UWMM2; C113 CC4U7WMM2; C114 CC4U7WMM2; C37 CCU47WMM3; C36 CCU47WMM3; C34 CCU47WMM3; C118 CCU47WMM3

FW_SI_IO0

FW_CCLK

FW_CS#

FW_SO_IO1

R140 RS2K40M05M0

R43 RS4K75M01M0

C74 CCU10XKM5

R42 RS4K75M01M0

R46 NI RSK200M01M0

R41 RS49R9M01M0

A102

1	CS#	VCC	8
2	SO_IO1	HOLD#_IO3	7
3	W#_ACC_IO2	SCK	6
4	GND	SI_IO0	5

MB064M01CXXM2
Vih(min)=1.26V, Vil(max)=0.54V

R53 RS49R9M01M0

R47 NI RSK200M01M0

A6-G

GROUND

A1	1	27	H7
A3			H8
A5			H11
A7			H12
A9			H18
A19			J8
B3			J9
B5			J11
B7			J12
B9			K8
B14			L8
C2			L9
C3			L11
C4			L19
C6			M9
C10			M13
C19			N9
D3			N12
E3			N13
E17			P2
F1			T19
F2			U6
F19			U9
G1			V18
G8			W1
G11	26	52	W12

IF00735C01B2_7478

+1.8V VCCO_0 C66 CC47UWMM2; C135 CCU47WMM3 (opt.)

SUB=FPGACOM

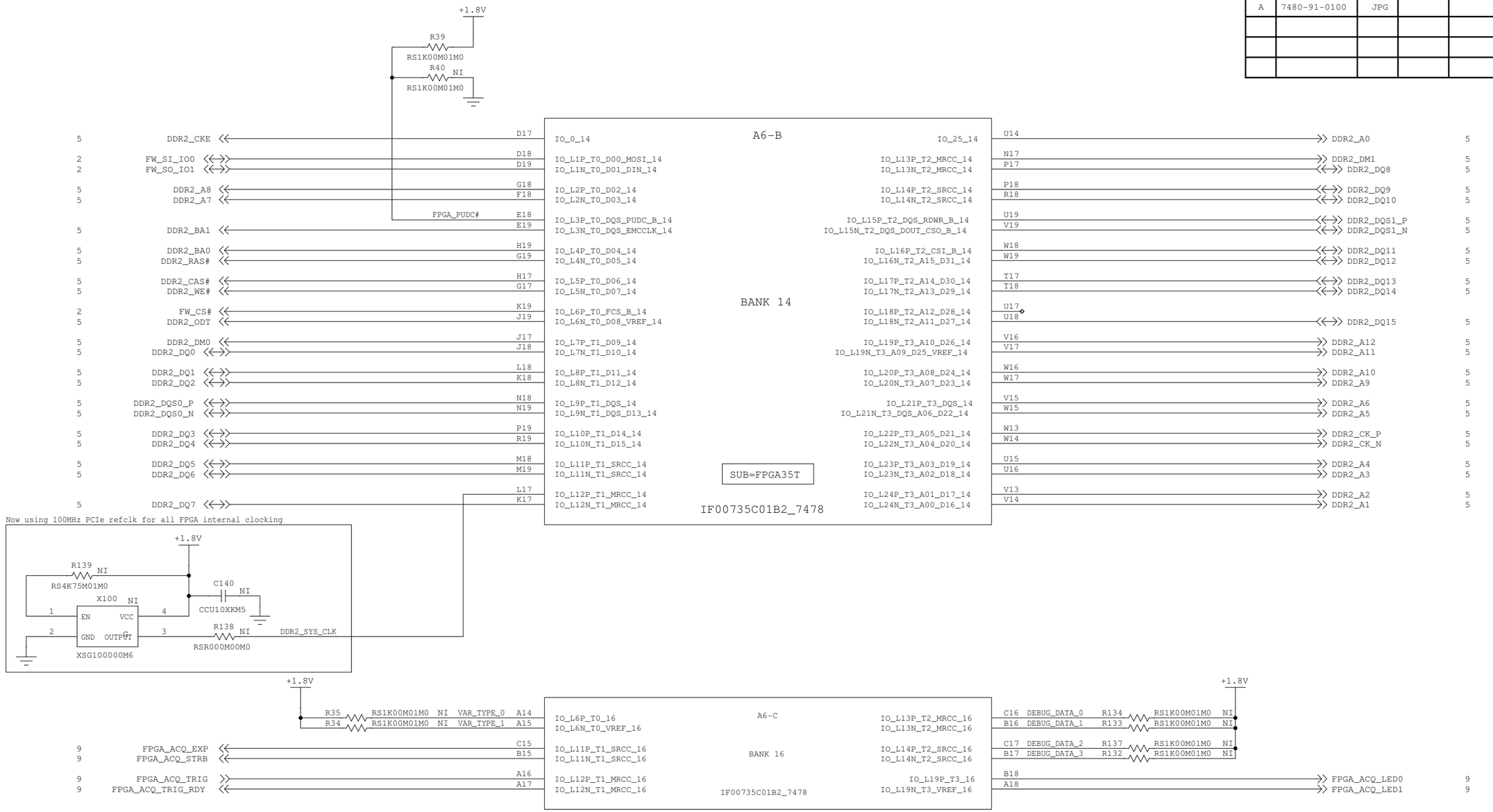
DRAWN	J-P Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-08-11

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: Athena Grab FPGA 1 of 3

DRAWING NO	REV	SHEET
7480-04-01	A	2 OF 13

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7480-91-0100	JPG			



DRAWN	J-P Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-08-11

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: Athena Grab FPGA 2 of 3

DRAWING NO	REV	SHEET
7480-04-01	A	3 OF 13

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7480-91-0100	JPG			

SUB=PYTCOM

6 PYT_RESET#
6 PYT_CLK_PLL_EN
11 PYT_VDD18_EN
11 PYT_VDD18_PG
11 PYT_VDD33_EN
11 PYT_VDD33_PG
11 PYT_VDDPIX_EN
11 PYT_VDDPIX_PG
6 PYT_DOUT0_P
6 PYT_DOUT0_N
8 TEMP_ALERT#

R125 RSK100M01M0

+3.3V

R122 RS4K75M01M0
R25 RS4K75M01M0

9 PE_RST#
7:8:9 I2C_SCL
7:8:9 I2C_SDA

R24 RSK100M01M0 FPGA_I2C_SCL
R123 RSK100M01M0 FPGA_I2C_SDA

6 PYT_SPI_MOSI
6 PYT_SPI_MISO

A6-D

R2	IO_L1P_T0_34	IO_L12P_T1_MRCC_34	W5
T2	IO_L1N_T0_34	IO_L12N_T1_MRCC_34	W4
R3	IO_L2P_T0_34	IO_L13P_T2_MRCC_34	W7
T3	IO_L2N_T0_34	IO_L13N_T2_MRCC_34	W6
T1	IO_L3P_T0_DQS_34	IO_L14P_T2_SRCC_34	U8
U1	IO_L3N_T0_DQS_34	IO_L14N_T2_SRCC_34	V8
V2	IO_L5P_T0_34		
W2	IO_L5N_T0_34		
V3	IO_L6P_T0_34	IO_L16P_T2_34	U5
W3	IO_L6N_T0_VREF_34	IO_L16N_T2_34	V5
U3	IO_L9P_T1_DQS_34	IO_L19P_T3_34	U7
U2	IO_L9N_T1_DQS_34	IO_L19N_T3_VREF_34	V7
U4	IO_L11P_T1_SRCC_34		
V4	IO_L11N_T1_SRCC_34		

BANK 34

SUB=FPGA35T

IF00735C01B2_7478

R23 RSK100M01M0
R26 RSK100M01M0
R129 RSK100M01M0
R128 RSK100M01M0
R27 RSK100M01M0

PYT_CLKOUT_P 6
PYT_CLKOUT_N 6
PYT_SYNC_P 6
PYT_SYNC_N 6
PYT_DOUT3_P 6
PYT_DOUT3_N 6
PYT_DOUT2_P 6
PYT_DOUT2_N 6
PYT_DOUT1_P 6
PYT_DOUT1_N 6

A6-E

G3	IO_L1P_T0_AD4P_35	IO_L9P_T1_DQS_AD7P_35	M2
G2	IO_L1N_T0_AD4N_35	IO_L9N_T1_DQS_AD7N_35	M1
H2	IO_L2P_T0_AD12P_35	IO_L10P_T1_AD15P_35	N2
J2	IO_L2N_T0_AD12N_35	IO_L10N_T1_AD15N_35	N1
H1	IO_L3P_T0_DQS_AD5P_35	IO_L12P_T1_MRCC_35	N3
J1	IO_L3N_T0_DQS_AD5N_35	IO_L12N_T1_MRCC_35	P3
K2	IO_L5P_T0_AD13P_35	IO_L8P_T1_AD14P_35	L3
L2	IO_L5N_T0_AD13N_35	IO_L8N_T1_AD14N_35	M3
L1	IO_L6N_T0_VREF_35	IO_L19N_T3_VREF_35	P1
J3	IO_L7P_T1_AD6P_35		
K3	IO_L7N_T1_AD6N_35		

BANK 35

Route P2.GND through P1

IF00735C01B2_7478

PYT_SPI_SS# 6
PYT_SPI_SCLK 6
PYT_MON_0 6
PYT_MON_1 6
PYT_TRIG_0 6
PYT_TRIG_1 6
PYT_TRIG_2 6

Artix-7 GTP decoupling guide (ug482 table 5-7)

MGTAVCC
C38 CC4U7WMM2 6.3V cc0603_2
C39 CCU10XKM5
C129 CCU10XKM5

MGTAVTT
C48 CC4U7WMM2
C40 CCU10XKM5
C112 CCU10XKM5

R126 RSK100M01M0 MGTRREF

A6-F

C7	MGTRREF_216	MGTPRXP0_216	B4
		MGTPRXN0_216	A4
		MGTPRXP1_216	B6
		MGTPRXN1_216	A6
C1	MGTAVCC_1		
E1	MGTAVCC_2		
F3	MGTAVCC_3		
G9	MGTAVCC_4		
H9	MGTAVCC_5		
		MGTPTXP0_216	D2 PE_FPGA_TX0_P_C
		MGTPTXN0_216	D1 PE_FPGA_TX0_N_C
		MGTPTXP1_216	B2 PE_FPGA_TX1_P_C
		MGTPTXN1_216	A2 PE_FPGA_TX1_N_C
B1	MGTAVTT_1		
C5	MGTAVTT_2		
E2	MGTAVTT_3		
G7	MGTAVTT_4		
		MGTREFCLK0P_216	B8 PE_REFCLK_P_C
		MGTREFCLK0N_216	A8 PE_REFCLK_N_C
		MGTREFCLK1P_216	B10
		MGTREFCLK1N_216	A10

BANK 216

IF00735C01B2_7478

C108 CCU10XKM5
C109 CCU10XKM5
C110 CCU10XKM5
C111 CCU10XKM5
C47 CCU10XKM5
C52 CCU10XKM5

MGTREFCLK1P/N: Leave unconnected if not used

PE_FPGA_RX0_P 9
PE_FPGA_RX0_N 9
PE_FPGA_RX1_P 9
PE_FPGA_RX1_N 9
PE_FPGA_TX0_P 9
PE_FPGA_TX0_N 9
PE_FPGA_TX1_P 9
PE_FPGA_TX1_N 9
PE_REFCLK_P 9
PE_REFCLK_N 9

SUB=FPGACOM

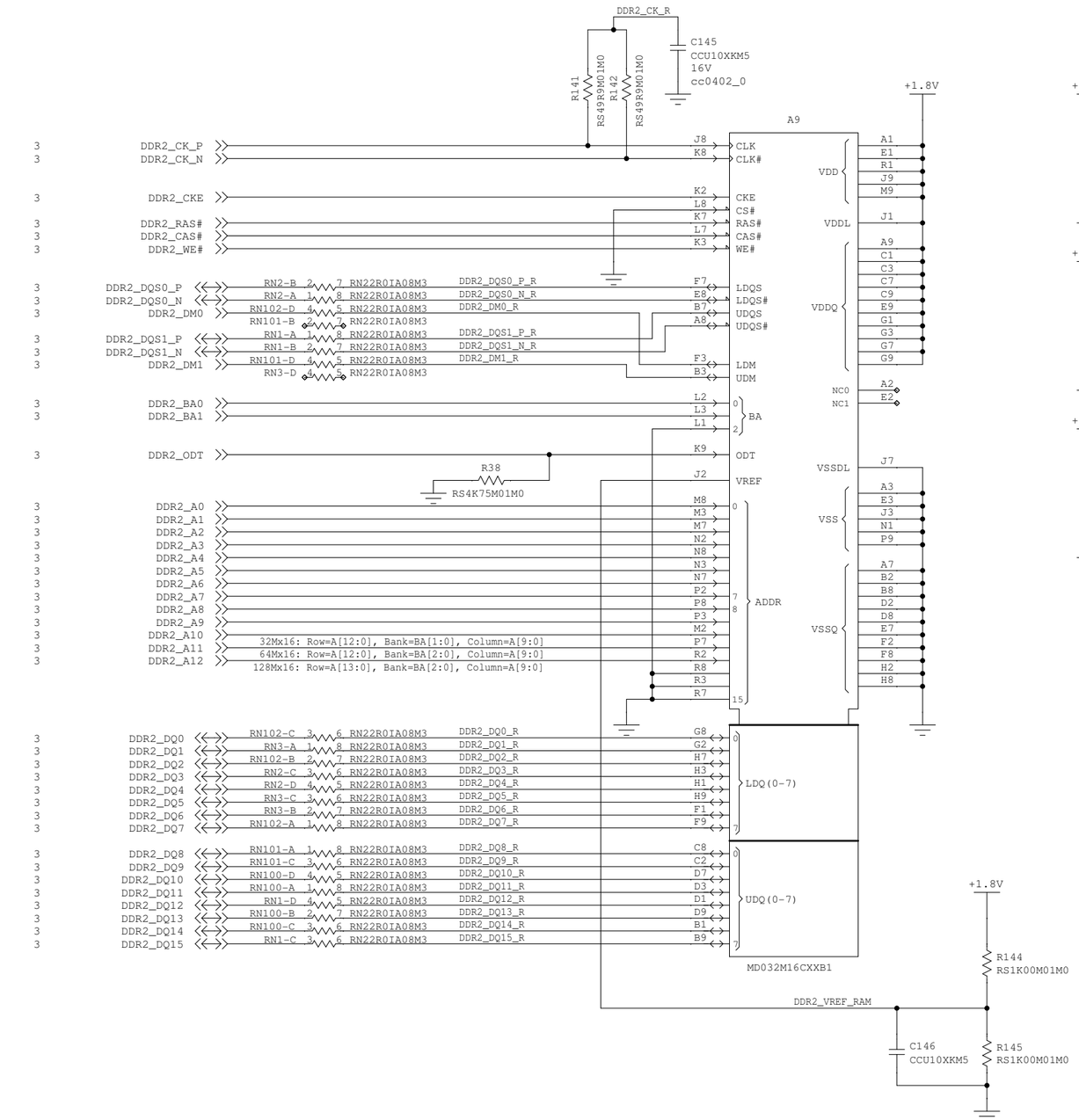
DRAWN	J-P Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-08-11

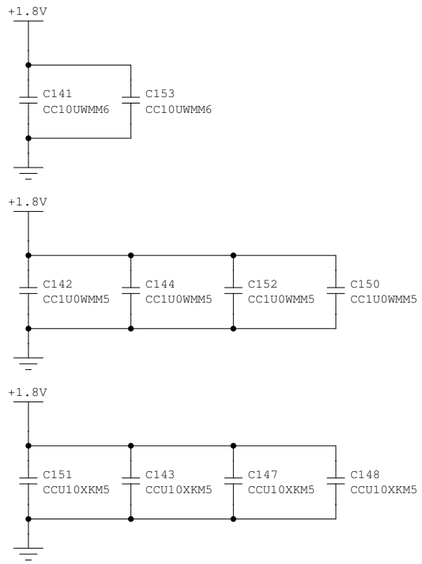
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE
Athena Grab FPGA
3 of 3

DRAWING NO	REV	SHEET
7480-04-01	A	4 OF 13

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7480-91-0100	JPG			





SUB=DDR2

DRAWN	J-P Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-08-11

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: FPGA DDR2

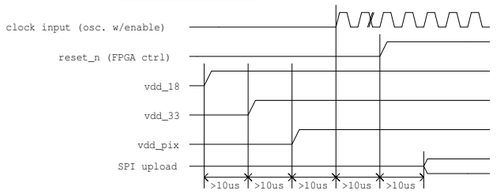
DRAWING NO	REV	SHEET
7480-04-01	A	5 OF 13

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7480-91-0100	JPG			

Overlap geometries (align image plane centers, not package centers)

IO voltage is 3.3V CMOS
LVDS output voltage is 1.8V

Power sequencing:



FPGA will control sensor sequencing
FPGA also requires 1.8V and 3.3V rails
3.3V will come for cpu board interconnect or PCIe interface (standalone)

clock input: clock oscillator enabled by FPGA
reset_n: controlled by FPGA
vdd_18: load switch enabled by FPGA
vdd_33: load switch enabled by FPGA
vdd_pix: LDO enabled by FPGA

Drive low or Z prior to enabling PYT_VDD33
(internal clamp diode or pull-up)

4 PYT_SPI_MOSI
4 PYT_SPI_MISO
4 PYT_SPI_SS#
4 PYT_SPI_SCLK
4 PYT_TRIG_0
4 PYT_TRIG_1
4 PYT_TRIG_2
4 PYT_RESET#
4 PYT_CLK_PLL_EN

PYT_VDD18 PYT_VDD33 PYT_VDDPIX

A2
IL01300CXXL0_7480
SUB=PYT1300

VDD_18 VDD_33 VDD_PIX
SPI_MOSI SPI_MISO SPI_SS_N SPI_SCLK
TRIGGER_0 TRIGGER_1 TRIGGER_2
CLKIN_P CLKIN_N CLK_PLL RESET_N IBIAS_MASTER
DOUT0_P DOUT0_N DOUT1_P DOUT1_N DOUT2_P DOUT2_N DOUT3_P DOUT3_N
SYNC_P SYNC_N CLKOUT_P CLKOUT_N MONITOR_0 MONITOR_1
GND_18 GND_33 GND_COLPC

PYT_DOUT0_P 4
PYT_DOUT0_N 4
PYT_DOUT1_P 4
PYT_DOUT1_N 4
PYT_DOUT2_P 4
PYT_DOUT2_N 4
PYT_DOUT3_P 4
PYT_DOUT3_N 4
PYT_SYNC_P 4
PYT_SYNC_N 4
PYT_CLKOUT_P 4
PYT_CLKOUT_N 4
PYT_MON_0 4
PYT_MON_1 4

A1
IL05000CXXL0_7480
SUB=PYT5000

VDD_18 VDD_33 VDD_PIX
SPI_MOSI SPI_MISO SPI_SS_N SPI_SCLK
TRIGGER_0 TRIGGER_1 TRIGGER_2
CLKIN_P CLKIN_N CLK_PLL RESET_N IBIAS_MASTER
DOUT0_P DOUT0_N DOUT1_P DOUT1_N DOUT2_P DOUT2_N DOUT3_P DOUT3_N DOUT4_P DOUT4_N DOUT5_P DOUT5_N DOUT6_P DOUT6_N DOUT7_P DOUT7_N
SYNC_P SYNC_N CLKOUT_P CLKOUT_N MONITOR_0 MONITOR_1
NC
GND_18 GND_33 GND_COLPC

Connect DOUT0,2,4,6 to operate in 4-ch mode

PYT_VDDPIX
Rev.1: Added bulk capacitance
Locate on solder side (default=NI)
C86 CC47UWMM2 NI
C87 CC47UWMM2 NI
C89 CC47UWMM2 NI
C88 CC47UWMM2 NI
C90 CC47UWMM2 NI
C91 CC47UWMM2 NI

PYT_VDD33
C33 CCU10XKM5
R22 RS4K75M01M0
X1 XS72M0000M1 (EN, VCC, GND, OUTPUT)
R16 RSR000M00M0
PYT_CLK_PLL
Pin1 SiT1602: Enable (Tsu=5ms, Ten=130ns), OUT=Z when OE=0
Pin1 DSC1001: Standby# (Tsu=1.3ms, Ten=1.3ms), OUT=Z when STDBY#=0
PYT_IBIAS_MASTER

PYT_VDD33
C43 CC47UWMM2 6.3V cc0805_0
C9 CC47UWMM2
C8 CC10UWMM6 6.3V cc0603_2
C30 CC10UWMM6
C50 CC10UWMM6
C46 CC1U0WMM5 16V cc0402_0
C61 CC1U0WMM5
C18 CC1U0WMM5
C31 CC1U0WMM5
C19 CC1U0WMM5

R17 RS4K75M01M0
R15 RS4K75M01M0
R10 RS47K0M01M0

PYT_VDD18
C32 CC47UWMM2 6.3V cc0805_0
C59 CC10UWMM6 6.3V cc0603_2
C20 CC10UWMM6
C49 CC10UWMM6
C60 CCU10XKM5 16V cc0402_0
C44 CCU10XKM5
C45 CCU10XKM5
C25 CCU10XKM5

PYT_VDDPIX
Image ripple fix
C12 RS3K57I01M0 LDO fix load
C6 CC47UWMM2 NI
C7 CC10UWMM6 6.3V NI
C10 CC10UWMM6 NI
C13 CC10UWMM6 6.3V NI
C11 CC10UWMM6 NI
C17 CC1U0WMM5 16V cc0402_0
C16 CC1U0WMM5
C14 CC1U0WMM5
C15 CC1U0WMM5

SUB=PYTCOM

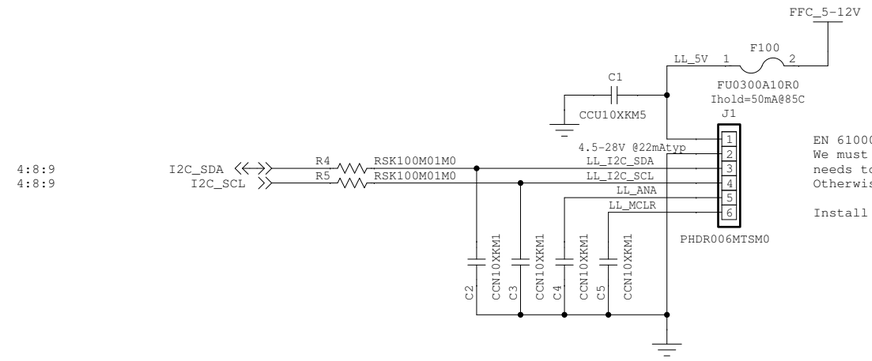
DRAWN	J-P Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-08-11

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE
Python ISP8
CMOS Sensor

DRAWING NO	REV	SHEET
7480-04-01	A	6 OF 13

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7480-91-0100	JPG			



EN 61000-4-2 (ESD):
We must add note in the manual stating that the IP CAP
needs to be installed when connecting device to this connector.
Otherwise, we may need to add protection to withstand discharges done to the cable.

Install PHDR006FTXX0 (cable-side connector housing) to isolate PCB-mount header pin from outside

Caspian C-39N0-16 I2C address: 18h (0011 000xb)

SUB=LLCON

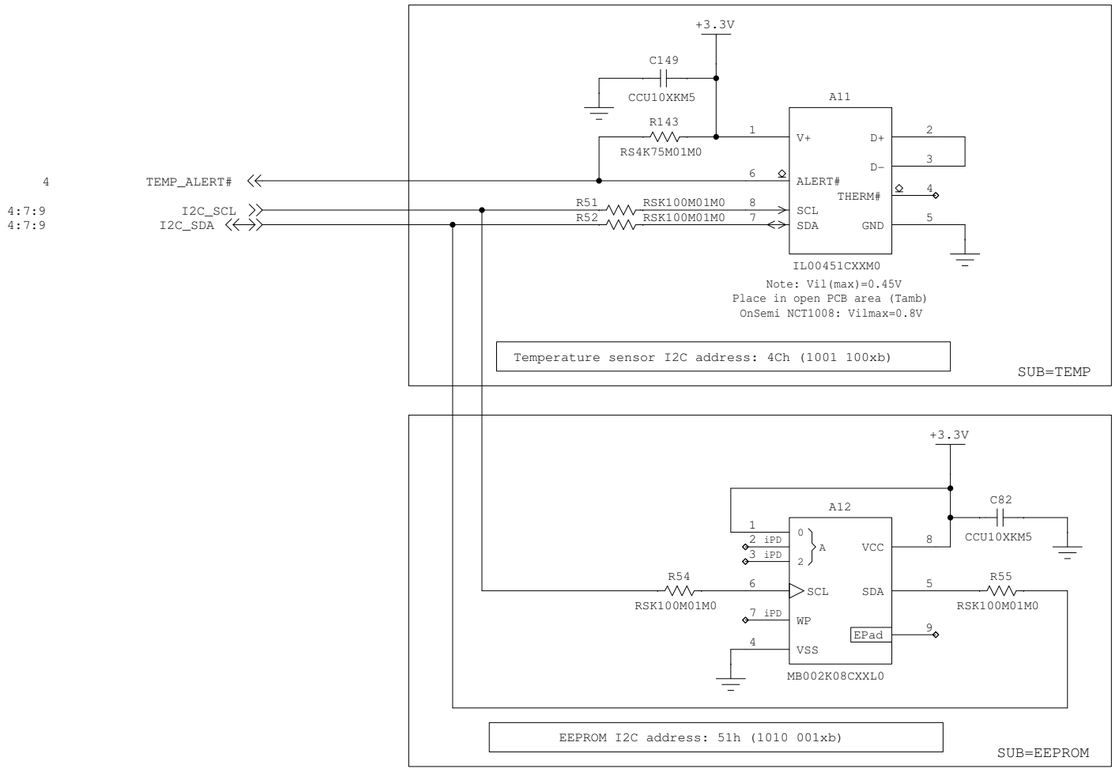
DRAWN: J-P Gagnon
PROJECT: IRIS3
GROUP: Imaging
CHECKED: Jean-Philippe Gagnon
ING# 127861
SIZE: B
DATE: 2016-08-11

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: Caspian C-39N0-16 IF Connector

DRAWING NO: 7480-04-01
REV: A
SHEET: 7 OF 13

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7480-91-0100	JPG			



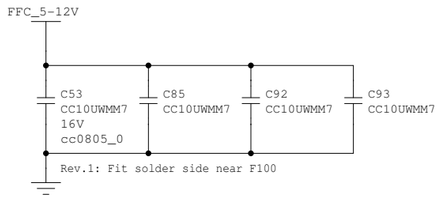
DRAWN	J-P Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-08-11

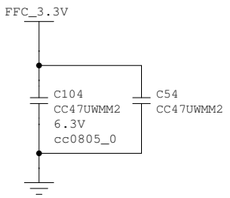
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

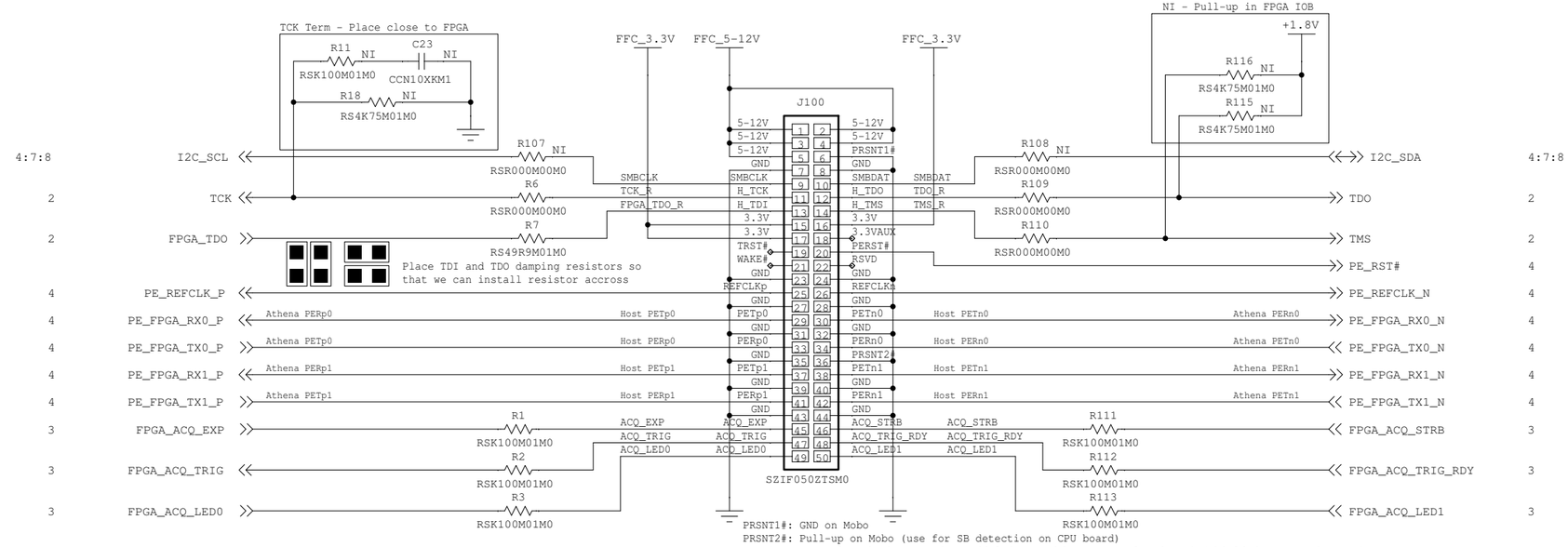
TITLE
Temp. Sensor
Local and Remote

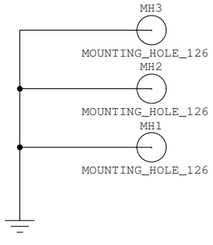
DRAWING NO	REV	SHEET
7480-04-01	A	8 OF 13

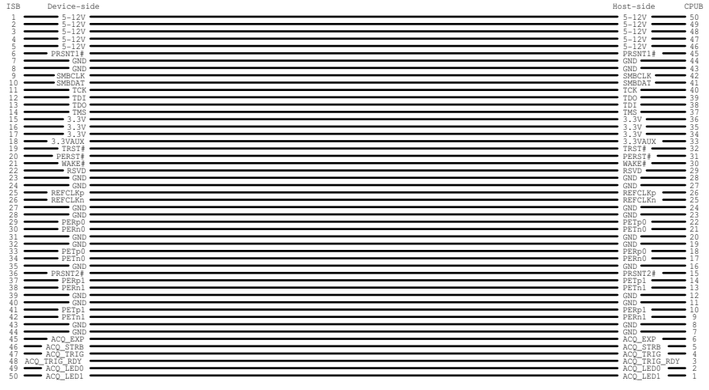
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7480-91-0100	JPG			











SUB=ZIF50CON

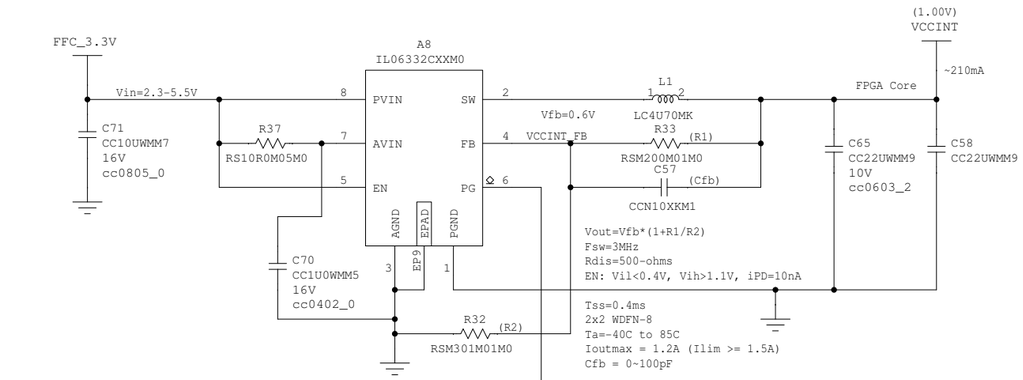
DRAWN	J-P Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-08-11

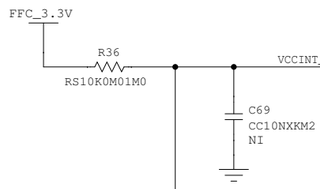
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

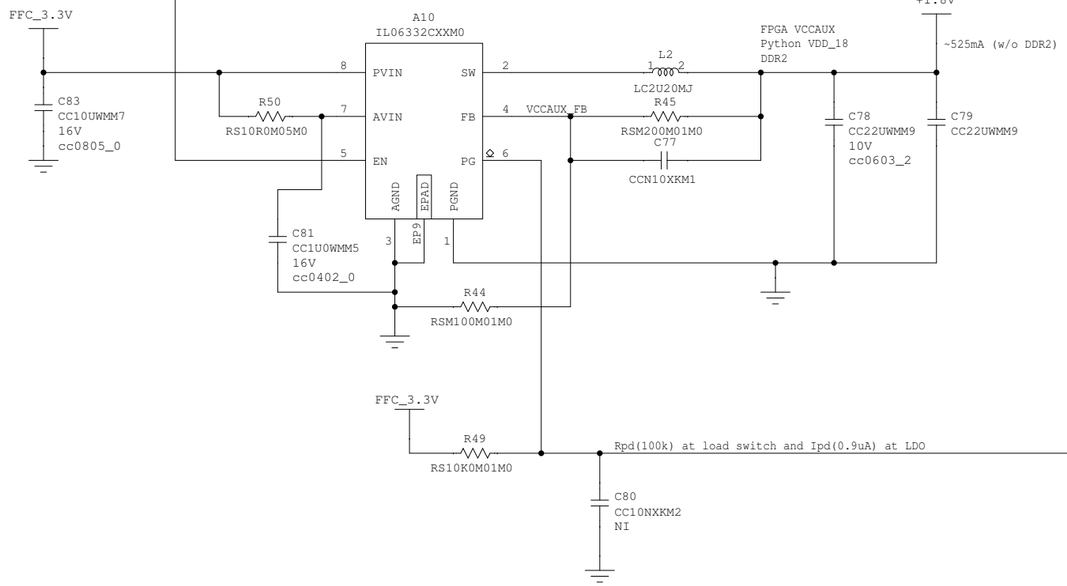
TITLE: Sensor Board Connector

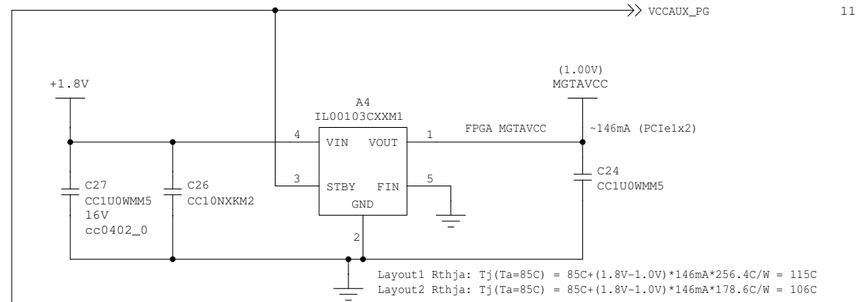
DRAWING NO	REV	SHEET
7480-04-01	A	9 OF 13

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7480-91-0100	JPG			

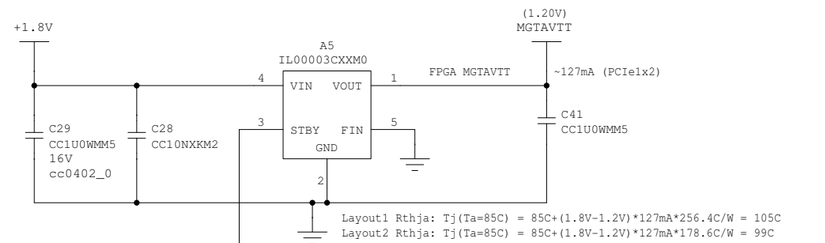


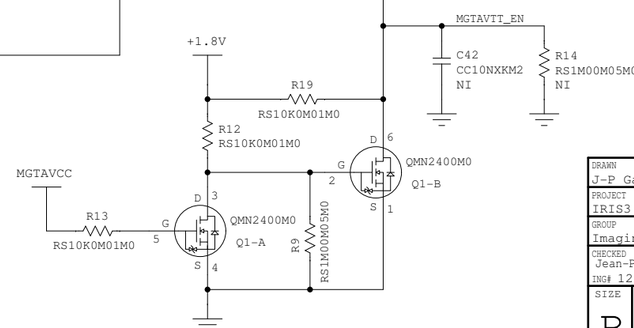






STBY#: Connect to VCCAUX_PG to discharge output before ramp-up





DRAWN	J-P Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-08-11

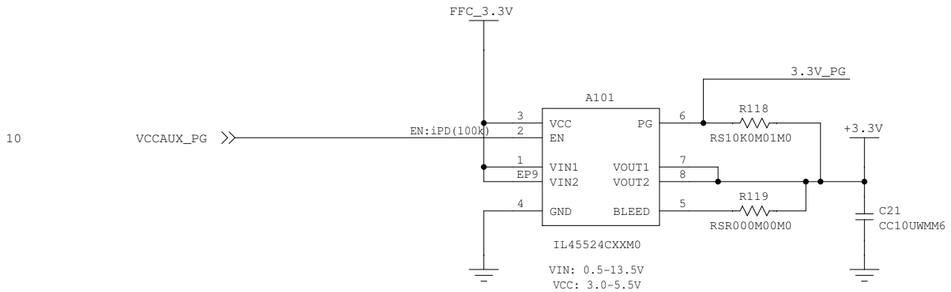
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

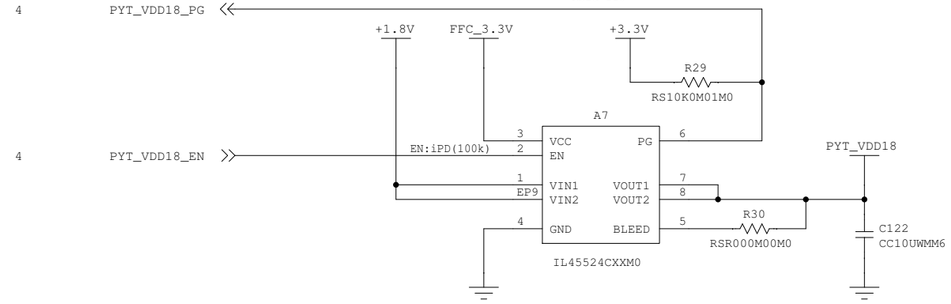
TITLE: POWER 1

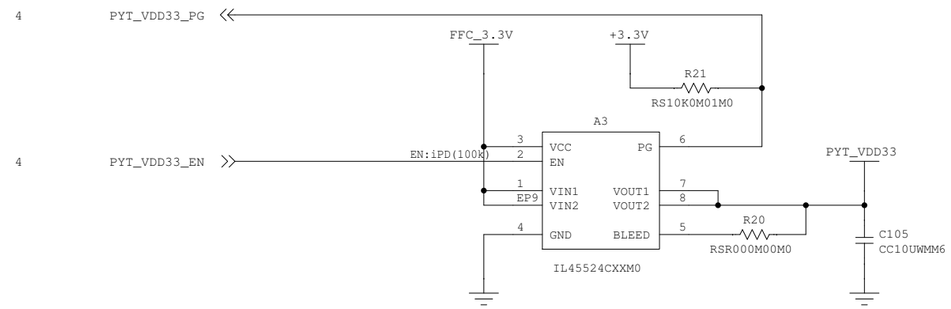
DRAWING NO	REV	SHEET
7480-04-01	A	10 OF 13

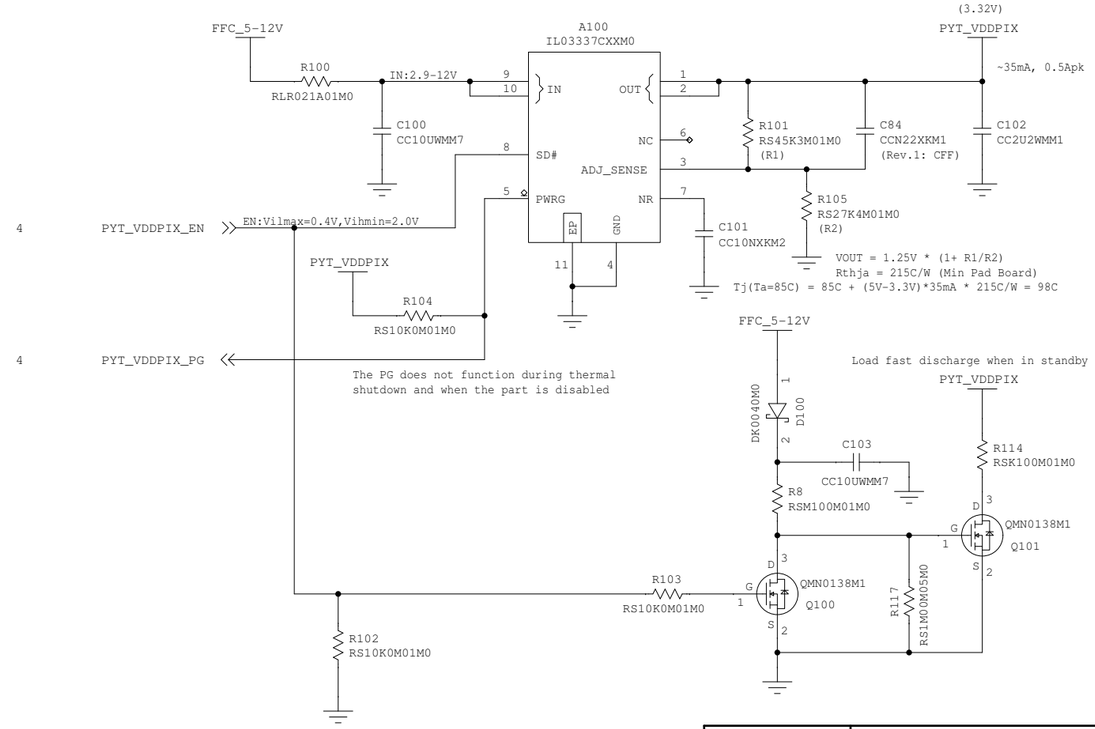
SUB=POWER

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7480-91-0100	JPG			









SUB=POWER

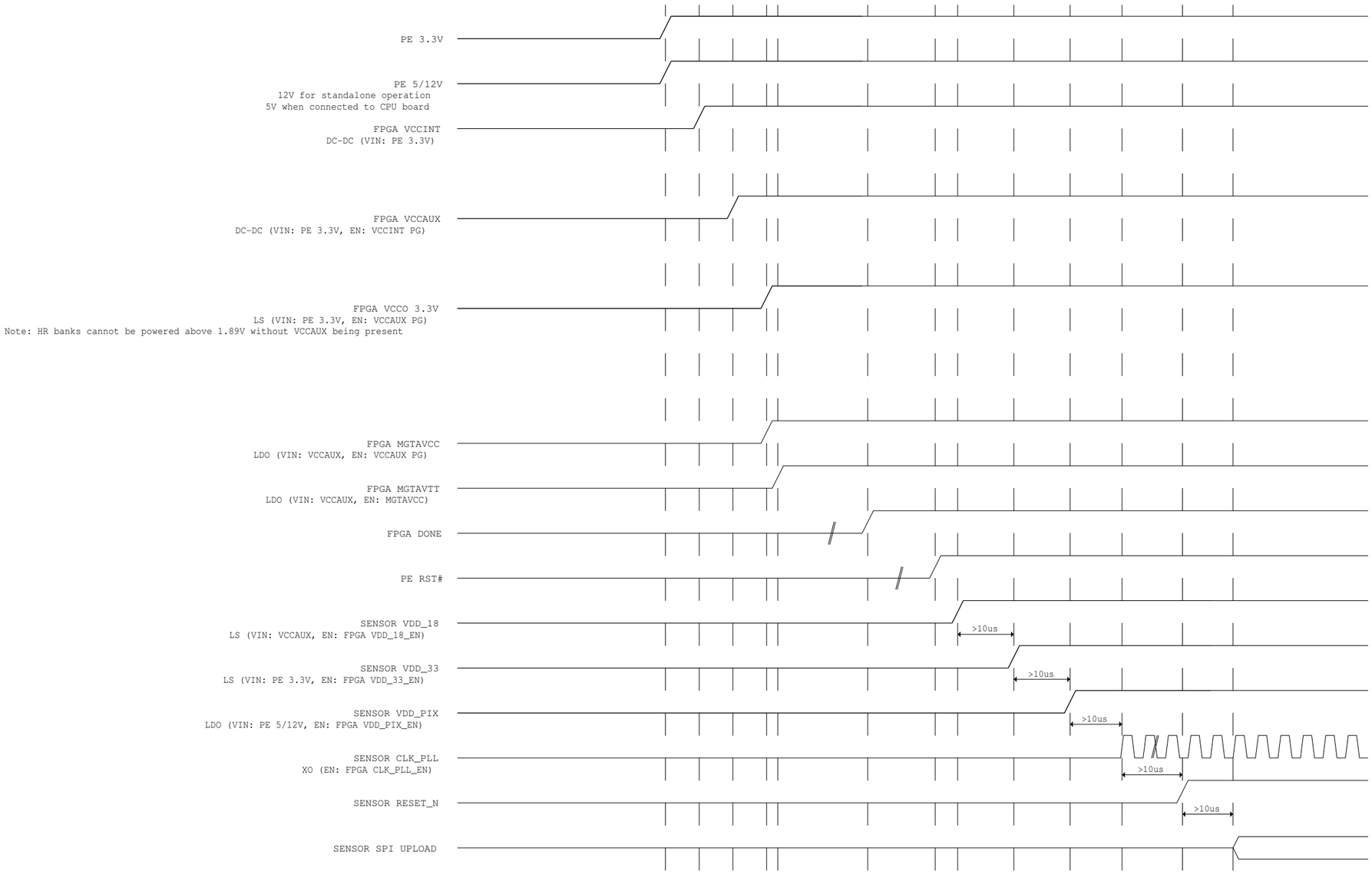
DRAWN	J-P Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-08-11

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: POWER 2

DRAWING NO	REV	SHEET
7480-04-01	A	11 OF 13

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7480-91-0100	JPG			



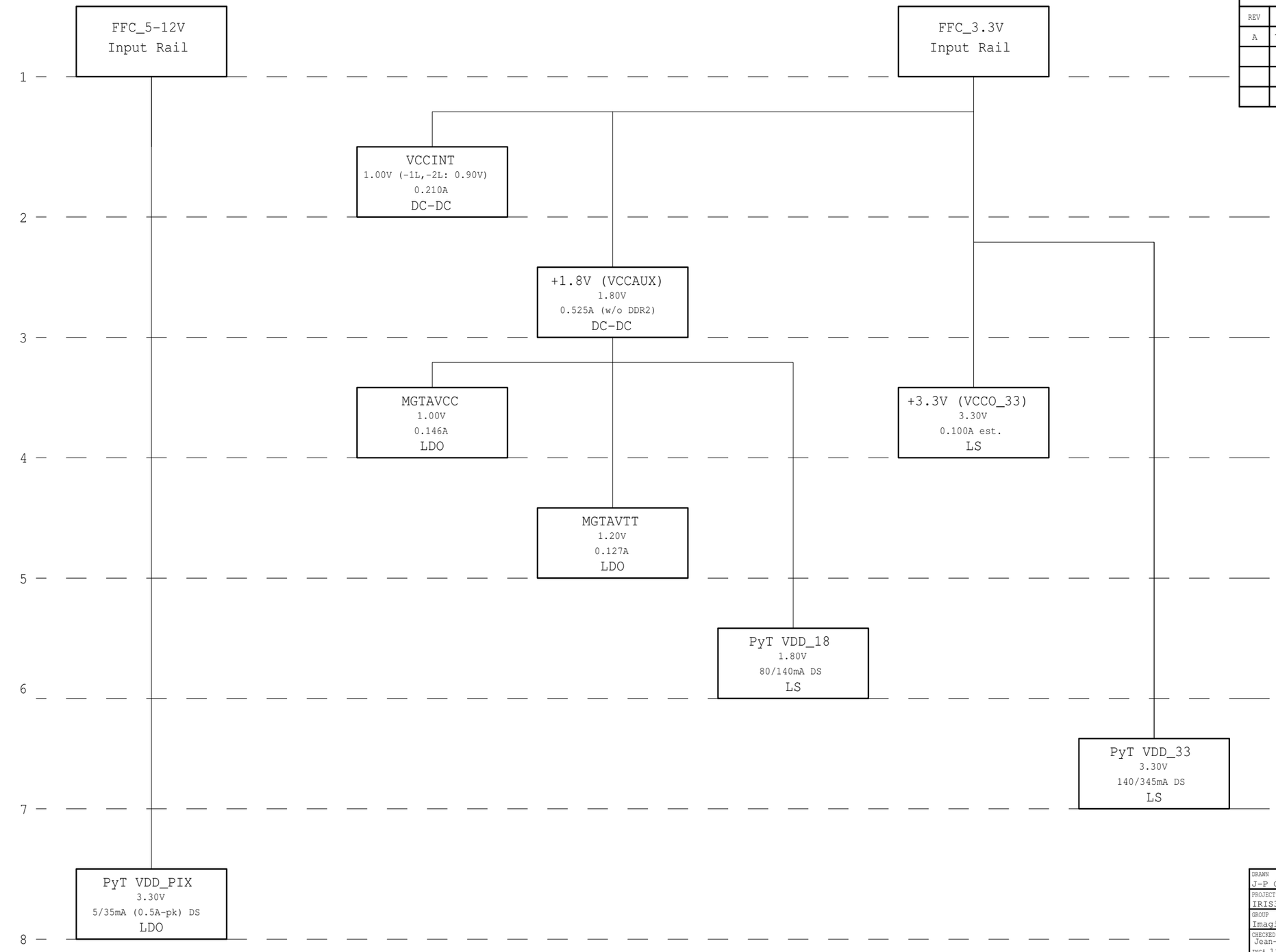
DRAWN	J-P Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-08-11

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: Power Sequencing Diagram

DRAWING NO	REV	SHEET
7480-04-01	A	12 OF 13

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED
A	7480-91-0100	JPG			



DRAWN	J-P Gagnon
PROJECT	IRIS3
GROUP	Imaging
CHECKED	Jean-Philippe Gagnon
ING#	127861
SIZE	B
DATE	2016-08-11

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: POWER TREE

DRAWING NO	REV	SHEET
7480-04-01	A	13 OF 13