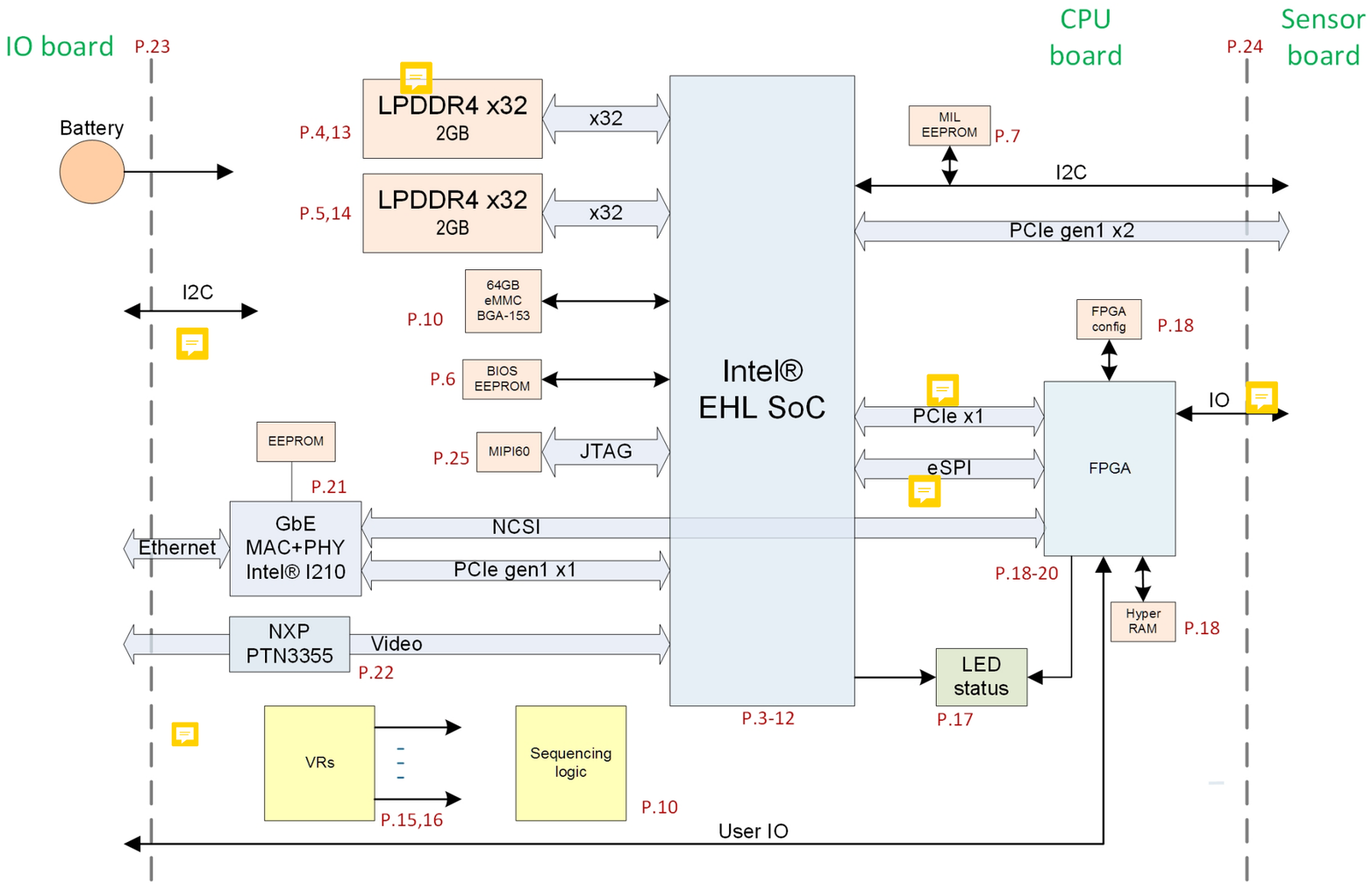
IRIS4 CPU Board

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

MATROX CONFIDENTIAL

INDEX

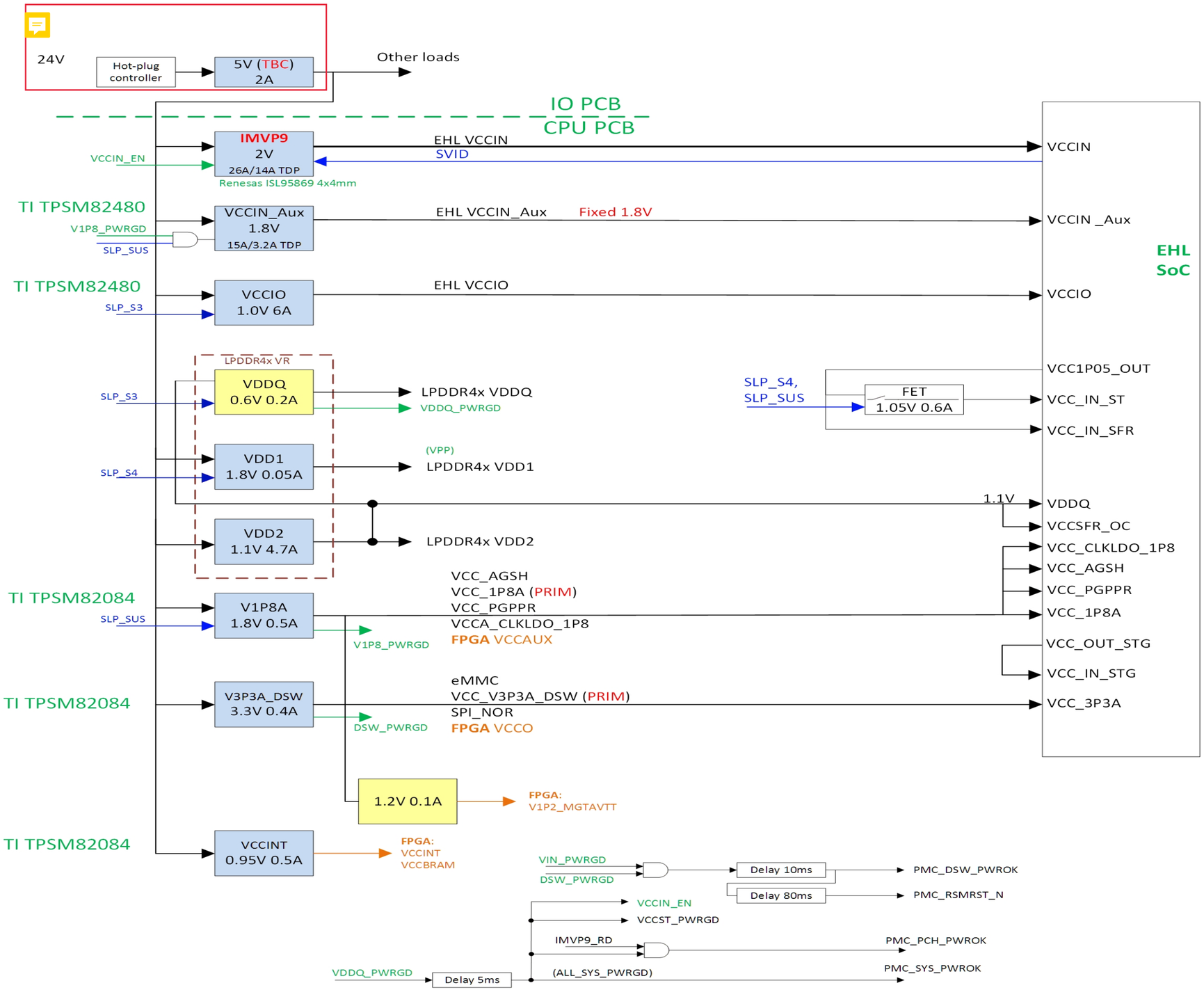


DRAWN	Dmitri Golovanov
PROJECT	IRIS4
GROUP	Imaging
CHECKED BY	
ING#	
SIZE	B
DATE	21/01/2020:07:53

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE	IRIS4 CPU board Block_Diagram		
DRAWING NO	7571 -04- 00	REV A	SHEET 1 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



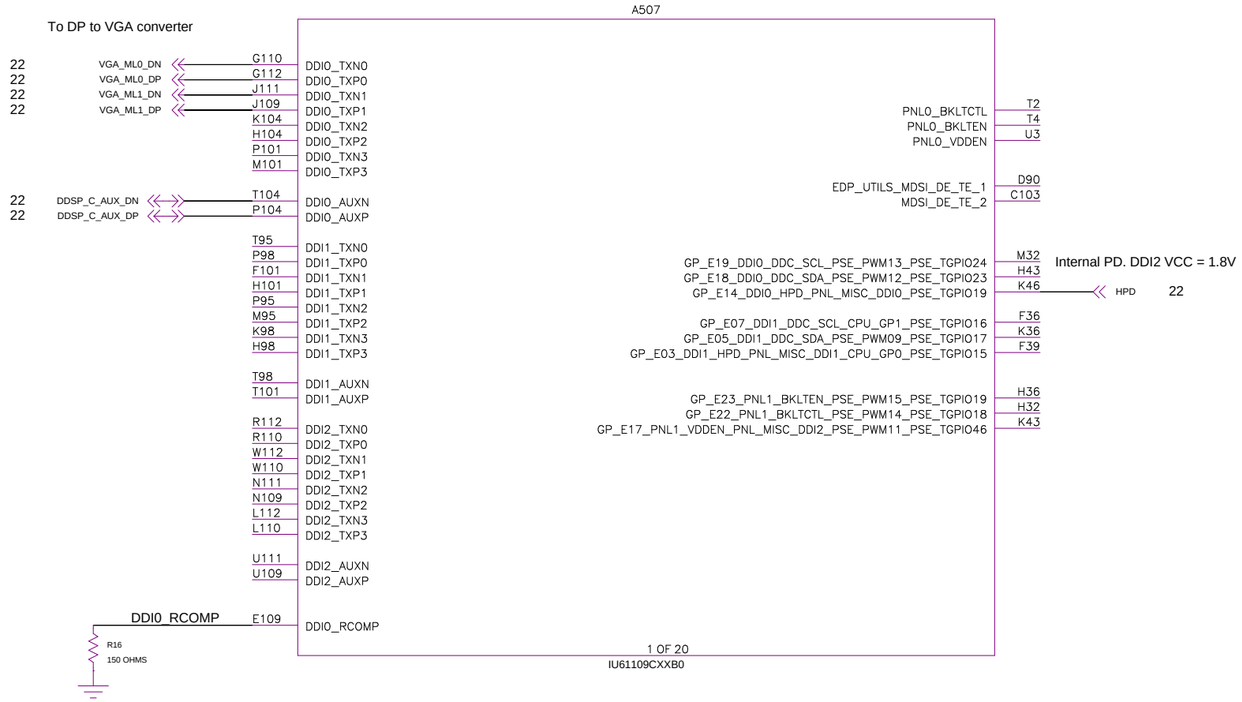
DRAWN	Dmitri Golovanov
PROJECT	IRIS4
GROUP	Imaging
CHECKED BY	
ING#	
SIZE	B
DATE	17/01/2020:15:45

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: IRIS4 CPU board
Power Distribution

DRAWING NO	REV	SHEET
7571 -04- 00	A	2 OF 27

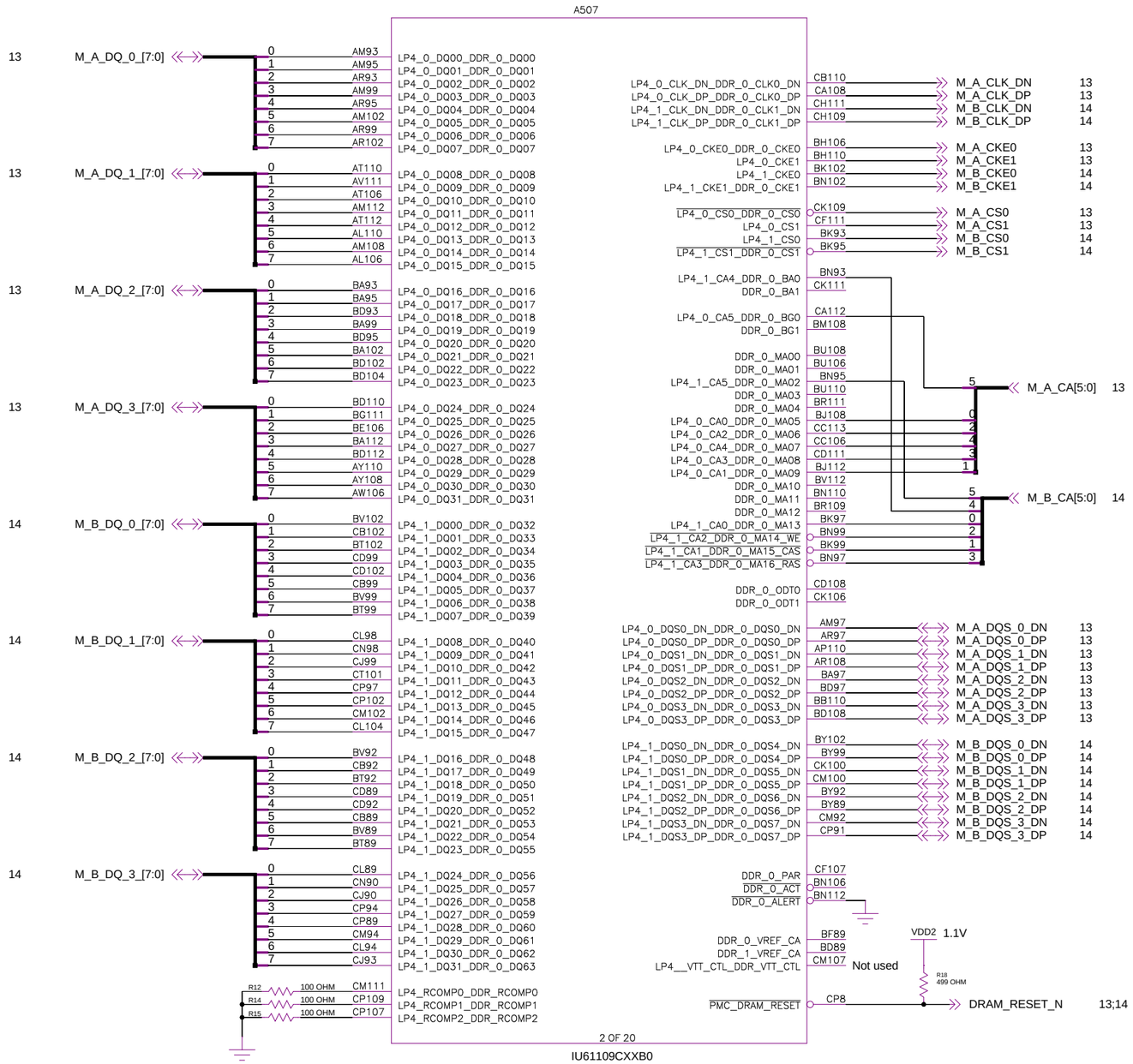
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



DRAWN Dmitri Golovanov	MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4		
PROJECT IRIS4			
GROUP Imaging	THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.		
CHECKED BY			
ING#	TITLE IRIS4 CPU board EHL display port		
SIZE B	DATE 12/02/2020:13:39		
DRAWING NO 7571 -04- 00	REV A	SHEET 3 OF 27	

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

DDR sub-channels 0 and 1



DRAWN	Dmitri Golovanov
PROJECT	IRIS4
GROUP	Imaging
CHECKED BY	
ING#	
SIZE	B
DATE	12/02/2020:13:39

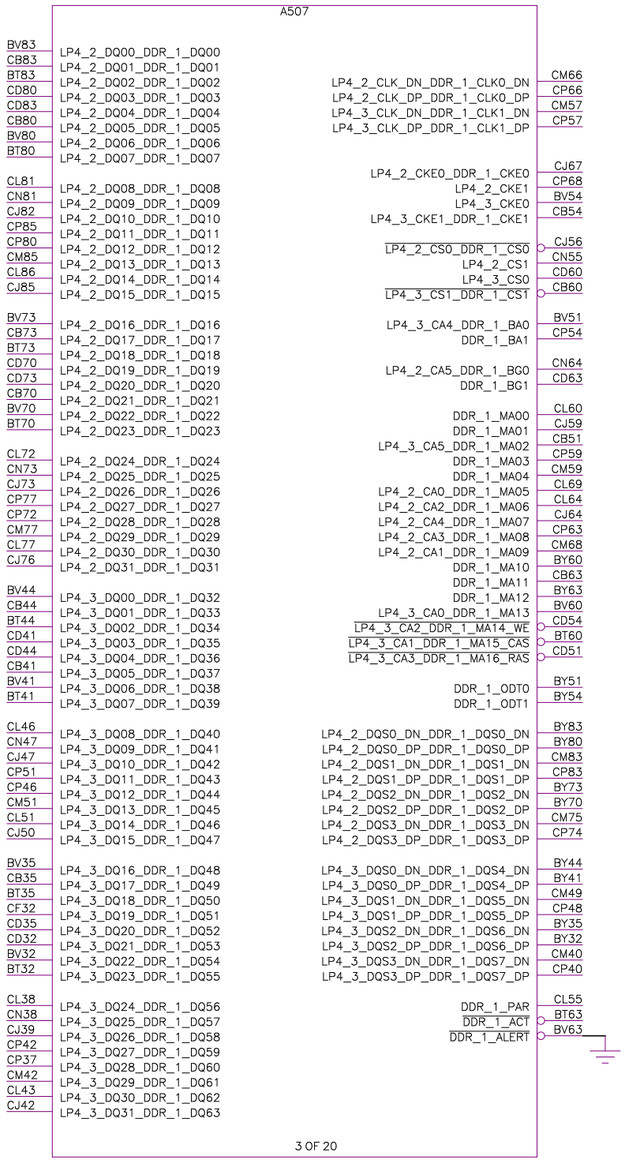
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: IRIS4 CPU board
EHL DDR0

DRAWING NO	REV	SHEET
7571 -04- 00	A	4 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

DDR sub-channels 2 and 3 are not used



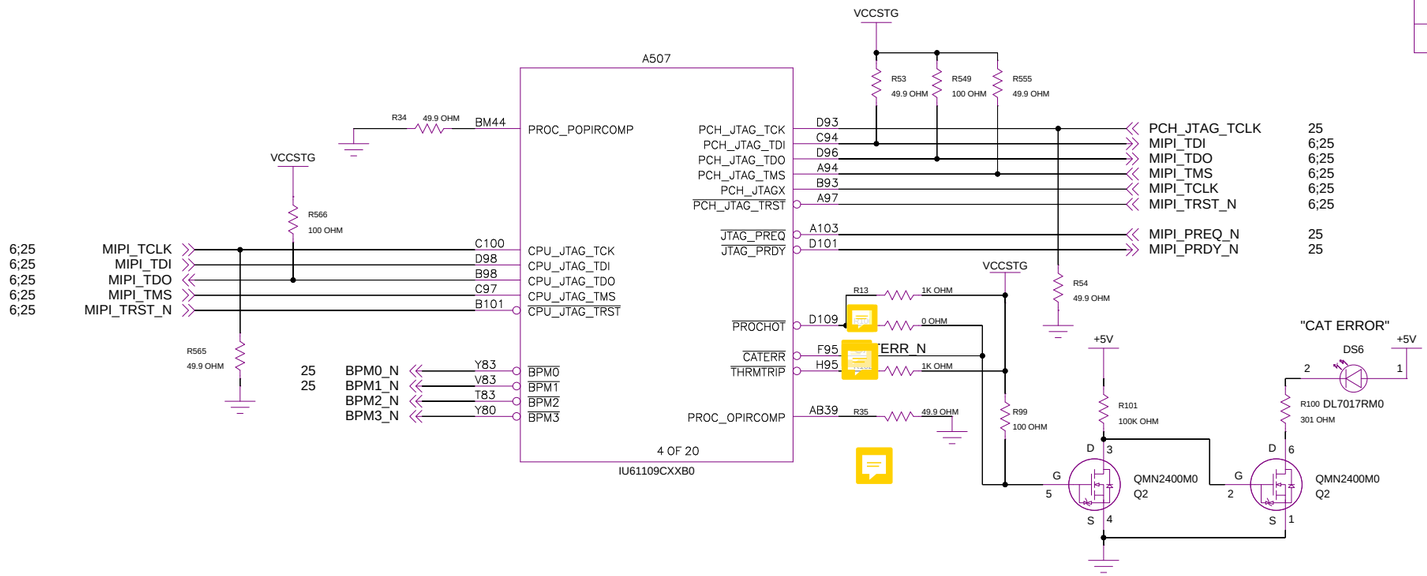
IU61109CXXB0

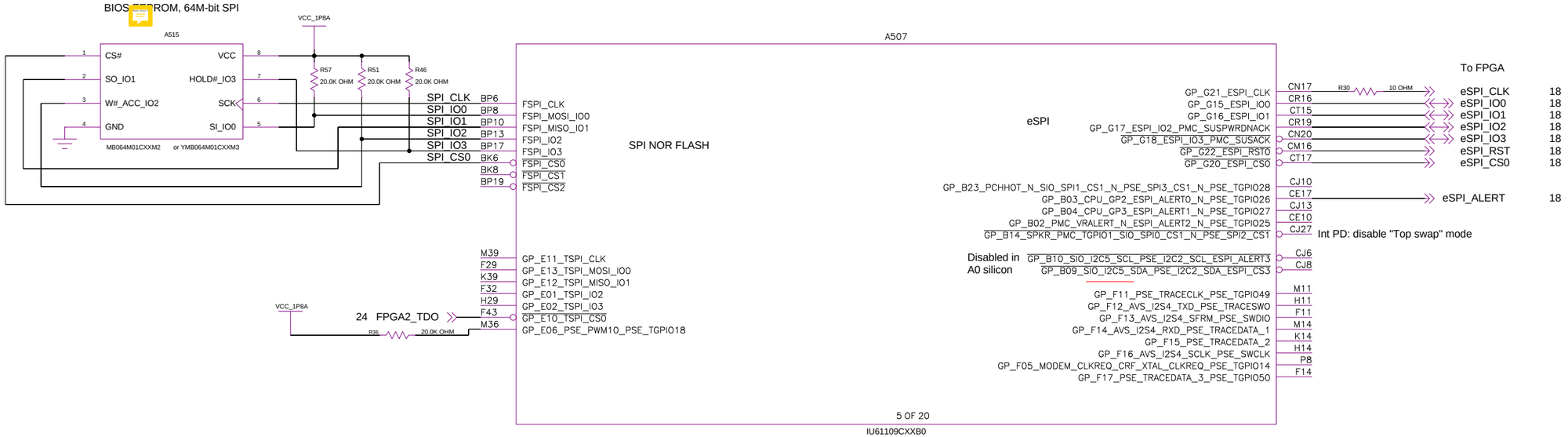
DRAWN	Dmitri Golovanov
PROJECT	IRIS4
GROUP	Imaging
CHECKED BY	
ING#	
SIZE	B
DATE	22/01/2020:08:23

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE	IRIS4 CPU board EHL DDR1
DRAWING NO	7571 -04- 00
REV	A
SHEET	5 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED





DRAWN Dmitri Golovanov	MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4		
PROJECT IRIS4			
GROUP Imaging	THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.		
CHECKED BY	TITLE IRIS4 CPU board EHL SPI and debug		
ING#			
SIZE B	DATE 18/02/2020:08:31		
DRAWING NO 7571 -04- 00	REV A	SHEET 6 OF 27	

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

A507

GP_B18 strap: not used
Int PD: disable "No Reboot" mode

18 FPGA_CLK_50MHz — R45 49.9 OHM NI

Board ID strapping
The pull-downs of GPIO pins must be enabled

VCC_3P3A_DSW

Board Revision
0000 = 00
To increase board revision, add a wire to board ID pin

BOARD SUBLEVEL
ECR number
00

OPTIONAL ID
assembly variant
00

R61 NI 2.21K OHMS
R64 NI 2.21K OHMS
R65 NI 2.21K OHMS
R63 NI 2.21K OHMS

BOARD_ID3
BOARD_ID1
BOARD_ID2
BOARD_ID0
BOARD_ID5
BOARD_ID7
BOARD_ID6
BOARD_ID4

18 FPGA1_TMS — R105 49.9 OHM — 24 FPGA2_TMS

18,24 FPGA1_TDO

CE8	GP_B16_SIO_SPI0_CLK_PSE_SPI2_CLK
CJ24	GP_B18_SIO_SPI0_MOSI_PSE_SPI2_MOSI
CJ21	GP_B17_SIO_SPI0_MISO_PSE_SPI2_MISO
CJ17	GP_B15_SIO_SPI0_CS0_N_PSE_SPI2_CS0_N_ESPI_CS1
CE27	GP_B20_SIO_SPI1_CLK_PSE_SPI3_CLK
CE21	GP_B22_SIO_SPI1_MOSI_PSE_SPI3_MOSI
CJ19	GP_B21_SIO_SPI1_MISO_PSE_SPI3_MISO
CG27	GP_B19_SIO_SPI1_CS0_N_PSE_SPI3_CS0_N_ESPI_CS2
AJ13	GP_D10_PSE_SPI0_CLK_SIO_SPI2_CLK_PSE_TGPIO11
AJ9	GP_D12_PSE_SPI0_MOSI_SIO_SPI2_MOSI_PSE_TGPIO13
AJ11	GP_D11_PSE_SPI0_MISO_SIO_SPI2_MISO_PSE_TGPIO12
AJ15	GP_D09_PSE_SPI0_CS0_N_SIO_SPI2_CS0_N_PSE_TGPIO10
AR2	GP_D15_PSE_PWM03_SIO_SPI2_CS1_N_PSE_SPI0_CS1_N_PSE_TGPIO39
AN7	GP_D01_PSE_QEPB0_PSE_SPI1_CLK_PSE_TGPIO33
AJ24	GP_D03_PSE_PWM06_PSE_SPI1_MOSI_PSE_TGPIO35
AJ21	GP_D02_PSE_QEPI0_PSE_SPI1_MISO_PSE_TGPIO34
AJ26	GP_D00_PSE_QEPA0_PSE_SPI1_CS0_N_PSE_TGPIO32
AJ19	GP_D04_PSE_PWM02_PSE_SPI1_CS1_N_PSE_TGPIO36
V2	GP_U05_ISI_SPIM_SCLK_PSE_SPI1_CLK
AE1	GP_U06_ISI_SPIM_MISO_PSE_SPI1_MISO
Y1	GP_U04_ISI_SPIM_CS_PSE_SPI1_CS0
AD13	GP_U09_ISI_SPIS_SCLK_ISI_I2CS_SCL_PSE_TGPIO11
AE3	GP_U10_ISI_SPIS_MISO_ISI_I2CS_SDA_PSE_TGPIO12
AD19	GP_U08_ISI_SPIS_CS_PSE_TGPIO10
V4	GP_U13_ISI_CHX_OKNOK_1
AD11	GP_U15_ISI_CHX_PMIC_EN_PSE_TGPIO13
AD9	GP_U14_ISI_CHX_RLY_SWTCH
AA4	GP_U12_ISI_CHX_OKNOK_0
AD26	GP_U17_ISI_OKNOK_1
AD24	GP_U18_ISI_ALERT
AD7	GP_U16_ISI_OKNOK_0

H25	GP_C00_SMB_CLK_PSE_I2C3_SCL_PSE_TGPIO18
Y22	GP_C01_SMB_DATA_PSE_I2C3_SDA_PSE_TGPIO19
F25	GP_C02_PSE_PWM00_SMB_ALERT_N_PSE_TGPIO29
CN12	GP_B05_PSE_I2C0_SCL_PSE_TGPIO06
CR13	GP_B06_PSE_I2C0_SDA_PSE_TGPIO07
CT12	GP_B07_PSE_I2C1_SCL_PSE_TGPIO08
CK31	GP_B08_PSE_I2C1_SDA_PSE_TGPIO09
BA13	GP_H04_SIO_I2C2_SDA_PSE_PWM08_PSE_TGPIO10
BA11	GP_H05_SIO_I2C2_SCL_PSE_PWM09_PSE_TGPIO11
BA9	GP_H07_SIO_I2C3_SCL_PSE_I2C5_SCL_PSE_PWM11
BA7	GP_H06_SIO_I2C3_SDA_PSE_I2C5_SDA_PSE_PWM10
AU24	GP_H08_SIO_I2C4_SDA_CNV_MFUART2_RXD_PSE_PWM12
AU21	GP_H09_SIO_I2C4_SCL_CNV_MFUART2_TXD_PSE_PWM13
CC27	GP_T00_PSE_QEPA2_SIO_I2C6_SDA_PSE_TGPIO08
CA17	GP_T01_PSE_QEPB2_SIO_I2C6_SCL_PSE_TGPIO09
H18	GP_C19_PSE_I2C4_SCL_SML_CLK0_SIO_I2C1_SCL
F18	GP_C18_PSE_I2C4_SDA_SML_DATA0_SIO_I2C1_SDA
CM13	GP_B11_PMC_ALERT_N_PSE_TGPIO06
AG2	GP_D14_PSE_QEPB1_PSE_TGPIO38
AK2	GP_D13_PSE_QEPA1_PSE_TGPIO37
CC24	GP_T03_SIO_I2C7_SCL_PSE_TGPIO06
CA27	GP_T02_PSE_QEPI2_SIO_I2C7_SDA_PSE_TGPIO07
U1	GP_U07_PSE_QEPA3_PSE_SPI1_MOSI_PSE_TGPIO10
AD15	GP_U11_PSE_QEPB3_PSE_TGPIO11
AD28	GP_U19_PSE_QEPI3_PSE_TGPIO12
AL1	GP_D16_PSE_QEPI1_PSE_TGPIO40
CE6	GPIO_RCOMP — R56 200 OHM

EEPROM_DIS
BOARD_ID3

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IU61109CXXB0

To IO board
I2C1_SCL 23
I2C1_SDA 23

VCC_3P3A_DSW

R545 2.21K OHMS
R546 2.21K OHMS
R71 10 OHM

I2C0_SCL 24
I2C0_SDA 24
To sensor board

VCC_3P3A_DSW
R550 0 OHM NI
QMP2307M0 Q501
A511

MB002K08CXXL0
2k-bit EEPROM
EEPROM I2C address: 50h (1010 000xb)
Board info, MIL license

DRAWN	Dmitri Golovanov
PROJECT	IRIS4
GROUP	Imaging
CHECKED BY	
ING#	
SIZE	B
DATE	21/02/2020:08:26

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: IRIS4 CPU board
EHL IO I2C

DRAWING NO	REV	SHEET
7571 -04- 00	A	7 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

A507

CA21 GP_T05_PSE_GBE0_RGMO_RST
BN27 GP_T04_PSE_GBE0_RGMO_INT

V22 GP_C03_PSE_GBE0_RGMO_MDC_PSE_HSUART3_EN
T22 GP_C04_PSE_GBE0_RGMO_MDIO_PSE_UART3_RTS_N_PSE_HSUART3_DE

17 STATUS2_RLED — BR24 GP_T07_PSE_GBE0_RGMO_PPS_PSE_TGPIO59
17 STATUS2_GLED — BU24 GP_T06_PSE_GBE0_RGMO_AUXTS_USB2_OCT

Y53 GP_A04_PSE_GBE0_RGMO_TXCLK
AB50 GP_A05_PSE_GBE0_RGMO_TXCTL
V53 GP_A03_PSE_GBE0_RGMO_TXD0
AB53 GP_A02_PSE_GBE0_RGMO_TXD1
Y58 GP_A01_PSE_GBE0_RGMO_TXD2
AB58 GP_A00_PSE_GBE0_RGMO_TXD3

SGMII 0

AB46 GP_A06_PSE_GBE0_RGMO_RXCLK
V46 GP_A23_PSE_GBE0_RGMO_RXCTL
T46 GP_A10_PSE_GBE0_RGMO_RXD0
Y46 GP_A09_PSE_GBE0_RGMO_RXD1
V50 GP_A08_PSE_GBE0_RGMO_RXD2
Y50 GP_A07_PSE_GBE0_RGMO_RXD3

VCC_1P8A
Boot from SPI, eSPI disabled — R42 4K99 OHMS
Boot option bit [1] = 0
Boot option bit [2] = 0
BA21 GP_H01_PSE_GBE1_RGM1_RST_N_PSE_UART5_TXD
BA24 GP_H00_PSE_GBE1_RGM1_INT_PSE_UART5_RXD

T18 GP_C06_PSE_GBE1_RGM1_MDC
V18 GP_C07_PSE_GBE1_RGM1_MDIO_PSE_HSUART3_RE

Boot option bit [0] = 0
BA17 GP_H03_PSE_GBE1_RGM1_PPS_PSE_UART5_CTS_N_PSE_TGPIO21
BA19 GP_H02_PSE_GBE1_RGM1_AUXTS_PSE_UART5_RTS

Y43 GP_A15_PSE_GBE1_RGM1_TXCLK
Y39 GP_A16_PSE_GBE1_RGM1_TXCTL
V39 GP_A14_PSE_GBE1_RGM1_TXD0
T39 GP_A13_PSE_GBE1_RGM1_TXD1
V43 GP_A12_PSE_GBE1_RGM1_TXD2
T43 GP_A11_PSE_GBE1_RGM1_TXD3

Y36 GP_A17_PSE_GBE1_RGM1_RXCLK
Y32 GP_A18_PSE_GBE1_RGM1_RXCTL
V32 GP_A22_PSE_GBE1_RGM1_RXD0_AVS_I2S5_RXD
T32 GP_A21_PSE_GBE1_RGM1_RXD1_AVS_I2S5_TXD
V36 GP_A20_PSE_GBE1_RGM1_RXD2_AVS_I2S5_SFRM
T36 GP_A19_PSE_GBE1_RGM1_RXD3_AVS_I2S5_SCLK

AD21 GP_U01_GBE_RGM2_RST_N_PSE_I2C6_SDA
AD4 GP_U00_GBE_RGM2_INT_PSE_I2C6_SCL

M18 GP_C17_GBE_RGM2_MDC_PSE_UART3_TXD_SIO_I2C0_SCL
K18 GP_C16_GBE_RGM2_MDIO_PSE_UART3_RXD_SIO_I2C0_SDA
Disabled in A0 silicon

AA2 GP_U02_GBE_RGM2_PPS_PSE_I2C7_SCL
AC3 GP_U03_GBE_RGM2_AUXTS_PSE_I2C7_SDA

Boot option bit [3] = 0
M22 GP_C05_PSE_PWM01_PSE_UART3_CTS_N_SML_ALERT0_N_PSE_TGPIO30

R26 200 OHM
V58 PSE_GBE0_RGM0_RCOMP

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IU61109CXXB0

GP_C13_PSE_UART0_TXD_SIO_UART1_TXD F22
GP_C12_PSE_UART0_RXD_SIO_UART1_RXD H22
GP_C15_PSE_UART0_CTS_N_SIO_UART1_CTS T25
GP_C14_PSE_UART0_RTS_N_PSE_HSUART0_DE_SIO_UART1_RTS Y25

GP_C11_PSE_HSUART0_RE K25
GP_C09_PSE_HSUART0_EN Y18

GP_H12_PSE_UART1_RXD_M2_SKT2_CFG0_PSE_TGPIO51 AU13
GP_H13_PSE_UART1_TXD_M2_SKT2_CFG1_PSE_TGPIO52 AU17
GP_H15_PSE_UART1_CTS_N_M2_SKT2_CFG3_PSE_TGPIO54 AN13
GP_H21_PSE_HSUART1_DE_PSE_UART1_RTS_N_PSE_TGPIO56 AU7
GP_H22_PSE_HSUART1_RE_PSE_TGPIO57 AN19
GP_H23_PSE_HSUART1_EN_PSE_TGPIO58 AN26

GP_T13_PSE_UART2_TXD_SIO_UART0_TXD CA6
GP_T12_PSE_UART2_RXD_SIO_UART0_RXD CA10
GP_T15_PSE_UART2_CTS_N_SIO_UART0_CTS BU27
GP_T14_PSE_UART2_RTS_N_SIO_UART0_RTS_N_PSE_HSUART2_DE CA24
GP_T10_PSE_HSUART2_RE CA8
GP_T09_PSE_HSUART2_EN CA13

GP_C21_PSE_UART4_TXD_CNV_MFUART0_TXD_SIO_UART2_TXD AB18
GP_C20_PSE_UART4_RXD_CNV_MFUART0_RXD_SIO_UART2_RXD K22
GP_C23_PSE_UART4_CTS_N_ISI_SPIS_MOSI_CNV_MFUART0_CTS_N_SIO_UART2_CTS V25
GP_C22_PSE_UART4_RTS_N_ISI_SPIM_MOSI_CNV_MFUART0_RTS_N_SIO_UART2_RTS Y29

GP_H20_PSE_PWM07_DDI2_HPD_PSE_TGPIO55 AN21
GP_H19_DDI2_DDC_SDA_PMC_TGPIO0_PSE_TGPIO20 AN11

GP_D17_PSE_PWM04_ISI_SPIM_MOSI_PSE_TGPIO41 AH3
GP_D18_PSE_PWM05_ISI_SPIS_MOSI_PSE_TGPIO42 AJ7

PSE_ADC0 B90
PSE_ADC1 C89
PSE_ADC2 A89
PSE_ADC3 D87
PSE_ADC4 C86
PSE_ADC5 A86
PSE_ADC6 D85
PSE_ADC7 B85

GP_C10_PSE_TGPIO05 M25

FPGA_S[illegible]N 18
SB_PRESENT_N 24
IRQ_FPGA 18
PWRRST 19;23
THERM2_N 23
FPGA_UART_RXD 18
FPGA_UART_TXD 18
UART2_RXD 25
UART2_TXD 25
UART2 for debug purposes
TP17
TP16
TP15
TP14

A507

25 MIPI60_CFG_0 — T80 CFG_00
25 MIPI60_CFG_1 — P90 CFG_01
25 MIPI60_CFG_2 — T90 CFG_02
25 MIPI60_CFG_3 — V80 CFG_03
25 MIPI60_CFG_4 — V87 CFG_04
25 MIPI60_CFG_5 — P87 CFG_05
25 MIPI60_CFG_6 — M87 CFG_06
25 MIPI60_CFG_7 — T87 CFG_07
25 MIPI60_CFG_8 — K83 CFG_08
25 MIPI60_CFG_9 — F80 CFG_09
25 MIPI60_CFG_10 — H83 CFG_10
25 MIPI60_CFG_11 — H87 CFG_11
25 MIPI60_CFG_12 — M83 CFG_12
25 MIPI60_CFG_13 — F90 CFG_13
25 MIPI60_CFG_14 — F87 CFG_14
25 MIPI60_CFG_15 — F83 CFG_15
25 MIPI60_CFG_16 — K80 CFG_16
25 MIPI60_CFG_17 — M80 CFG_17
25 MIPI60_CFG_18 — H90 CFG_18
25 MIPI60_CFG_19 — K90 CFG_19

R23 49.9 OHM — F75 CFG_RCOMP
D6 RSVD_58
A6 RSVD_5
AN61 RSVD_NCTF_1
AR61 RSVD_NCTF_2
25 DBG_PMODE — Internal PU — P1 DBG_PMODE
CM6 RSVD_50
E111 RSVD_60
B111 RSVD_24
A112 RSVD_2
G2 RSVD_62
E2 RSVD_61
A110 RSVD_1
B109 RSVD_23
CT2 RSVD_54
CM1 RSVD_48
CP2 RSVD_51
BM2 RSVD_41
C92 RSVD_47
CT112 RSVD_53
CR113 RSVD_52
BM38 RSVD_44
BM35 RSVD_43

RSVD_3 A12
RSVD_45 C12
RSVD_57 D113
RSVD_25 B113
RSVD_6 AB76
RSVD_33 BF26
RSVD_32 BF24
RSVD_7 AC63
RSVD_37 BH59
RSVD_36 BF59
RSVD_8 AD61
RSVD_30 BB81
RSVD_21 AY81
RSVD_9 AE72
RSVD_63 H1
RSVD_64 H3
RSVD_10 AE75
RSVD_12 AG61
RSVD_27 B6
RSVD_28 B8
RSVD_13 AG69
RSVD_65 K2
RSVD_66 K4
RSVD_14 AJ61
RSVD_4 A4
RSVD_26 B2
RSVD_17 AM75
RSVD_15 AL43
RSVD_11 AF40
RSVD_18 AV61
RSVD_55 D1
RSVD_59 E1
RSVD_20 AY61
RSVD_22 AY89
RSVD_29 BB72
RSVD_16 AL61
RSVD_31 BD73
RSVD_19 AV74
RSVD_46 C83
RSVD_34 BF40
RSVD_35 BF43
RSVD_38 BK32
RSVD_56 D10
RSVD_39 BK35
RSVD_40 BK38
RSVD_42 BM32
RSVD_49 CM105

20 OF 20
IU61109CXXB0

A507

VCC_1P8A
J4 NI — 1 2 — R21 1K OHM
TSTR.430S021
Flash security:
no jumper = enabled

BP21 GP_R00_HDA_BCLK_AVS_I2S0_SCLK_PSE_I2S0_SCLK
BV8 GP_R02_HDA_SDO_AVS_I2S0_TXD_PSE_I2S0_TXD_DMIC_CLK_B0
BV6 GP_R03_HDA_SDI0_AVS_I2S0_RXD_PSE_I2S0_RXD_DMIC_CLK_B1
BV10 GP_R05_HDA_SDI1_AVS_I2S1_RXD_DMIC_DATA1
BV21 GP_R01_HDA_SYNC_AVS_I2S0_SFRM_PSE_I2S0_SFRM
BV17 GP_R04_HDA_RST_N_DMIC_CLK_A1

CM24 GP_G19_AVS_I2S1_SCLK
BV13 GP_R06_AVS_I2S1_TXD_DMIC_CLK_A0
BV19 GP_R07_AVS_I2S1_SFRM_DMIC_DATA0

24 FPGA2_TCK — R104 10 OHM
18 FPGA1_TCK

AM4 GP_D19_AVS_I2S_MCLK1_PSE_TGPIO43
G5 GP_F08_AVS_I2S_MCLK2_PSE_TRACEDATA_0_PSE_TGPIO48

Internal PD
N6 GP_F07_PSE_I2S1_SCLK_AVS_I2S4_SCLK_PSE_TGPIO14
V11 GP_F18_PSE_I2S1_TXD_AVS_I2S4_TXD_PSE_TGPIO16
Internal PD
T11 GP_F19_PSE_I2S1_RXD_AVS_I2S4_RXD_PSE_TGPIO17
K11 GP_F10_PSE_I2S1_SFRM_AVS_I2S4_SFRM_PSE_TGPIO15

8 OF 20
IU61109CXXB0

GP_G06_SD_SDIO_CLK CT29
GP_G00_SD_SDIO_CMD CN29
GP_G01_SD_SDIO_D0 CM30
GP_G02_SD_SDIO_D1 CT34
GP_G03_SD_SDIO_D2 CM33
GP_G04_SD_SDIO_D3 CR33 — FPGA_RECONFIG 18
GP_G05_SD_SDIO_CD CT31
GP_G23_SD_SDIO_WP CR30
GP_H17_SD_SDIO_PWR_EN AN24

GP_G13_AVS_I2S3_TXD_DMIC_CLK_B0_PSE_TGPIO08 CR22
GP_G12_AVS_I2S3_SFRM_SATA_1_GP_SATAXPCIE_1_DMIC_DATA1_PSE_TGPIO31 CR24
GP_G11_AVS_I2S3_SCLK_DMIC_DATA0_PSE_TGPIO07 CT23
GP_G14_AVS_I2S3_RXD_DMIC_CLK_B1_PSE_TGPIO09 CM22

GP_E15_PSE_I2S0_RXD_PSE_CAN0_TX_PSE_TGPIO17 F46
GP_E16_PSE_I2S0_TXD_PSE_CAN0_RX_PSE_TGPIO16 M43

GP_E20_PSE_I2S0_SCLK_PSE_CAN1_TX_PSE_TGPIO14 M29
GP_E21_PSE_I2S0_SFRM_PSE_CAN1_RX_PSE_TGPIO15 K32

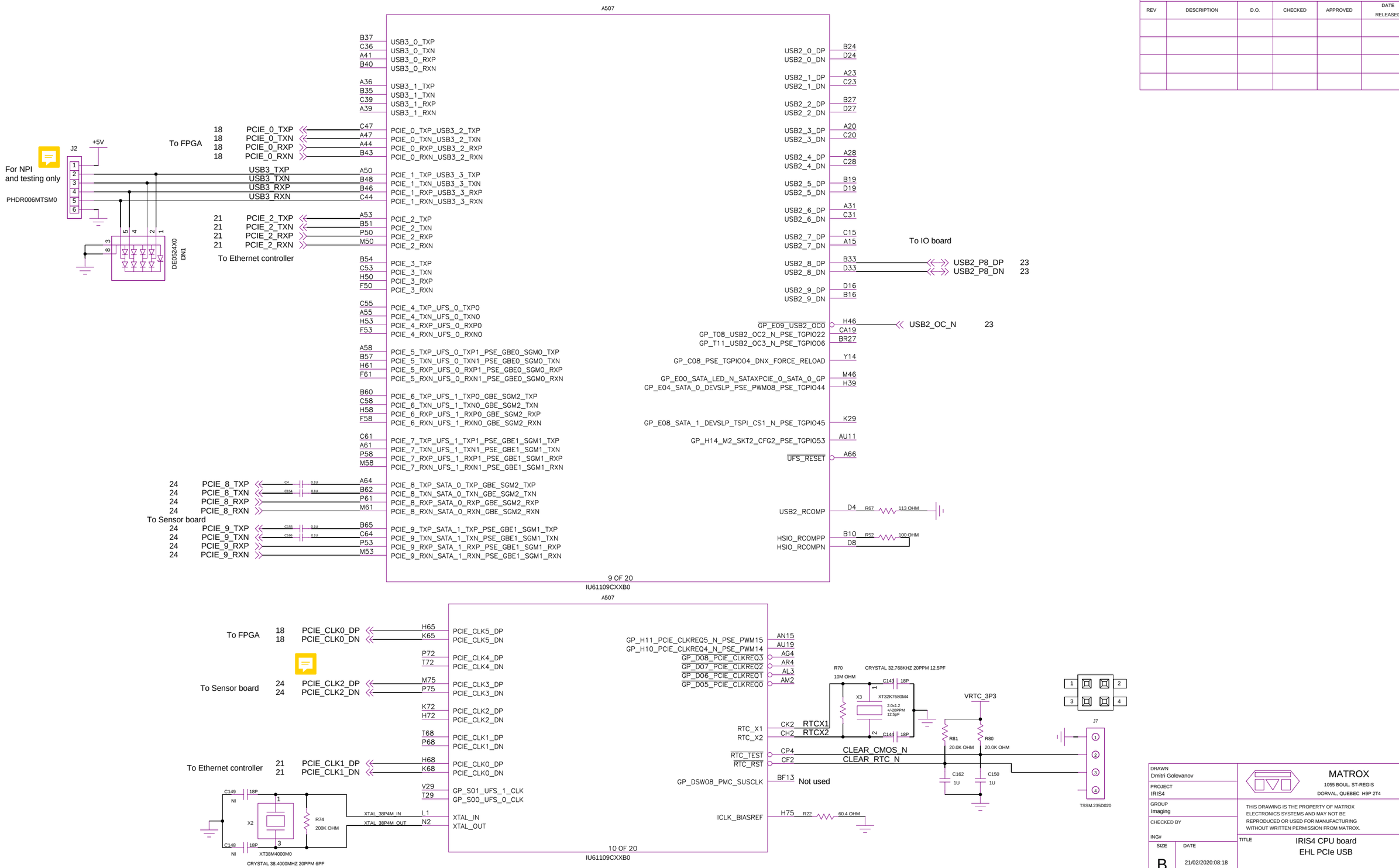
DRAWN	Dmitri Golovanov
PROJECT	IRIS4
GROUP	Imaging
CHECKED BY	
ING#	
SIZE	B
DATE	21/02/2020:08:51

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: IRIS4 CPU board
EHL GPIO

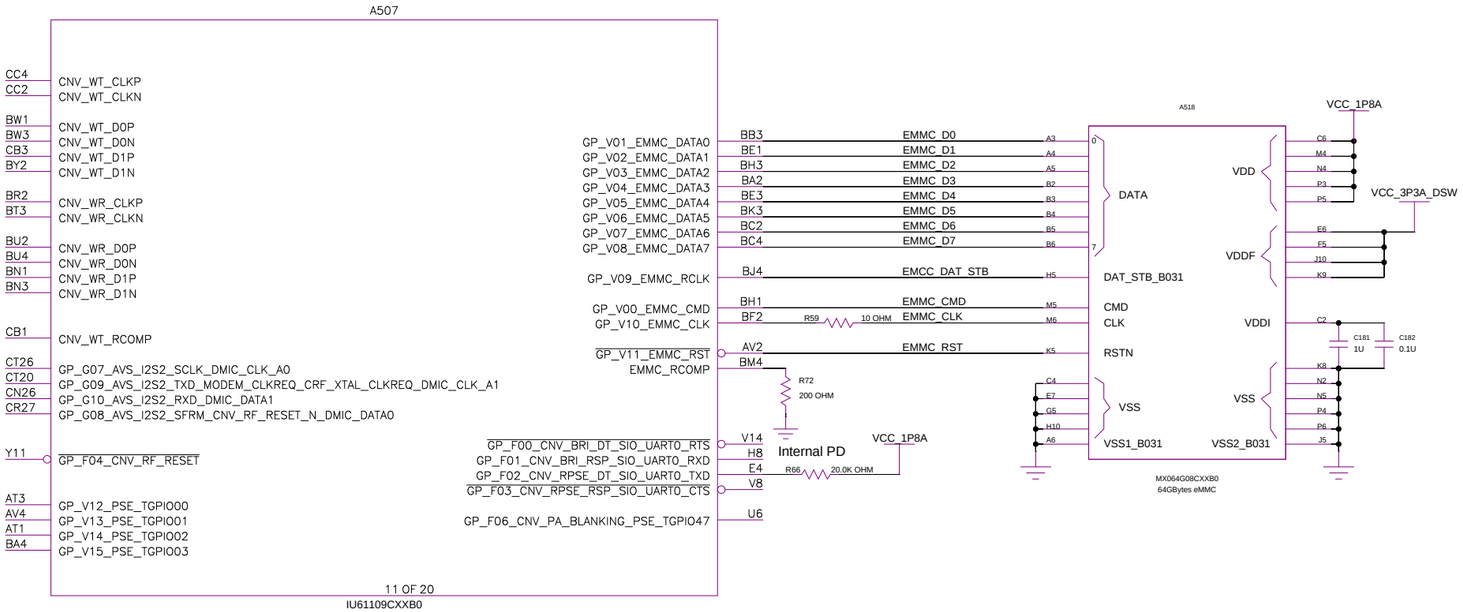
DRAWING NO	REV	SHEET
7571 -04- 00	A	8 OF 27

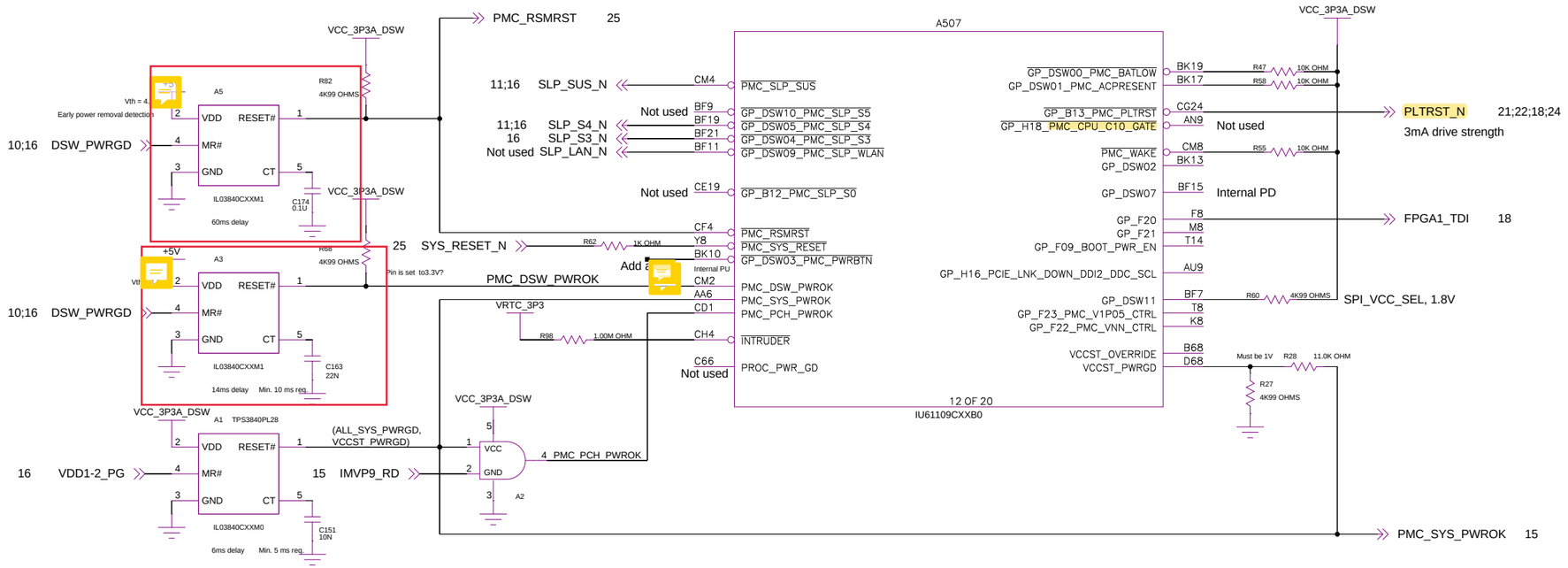
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



DRAWN	Dmitri Golovanov	MATROX	
PROJECT	IRIS4	1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
GROUP	Imaging	THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY			
ING#			
SIZE	DATE	TITLE	IRIS4 CPU board EHL PCIe USB
B	21/02/2020:08:18		
DRAWING NO	7571 -04- 00	REV	A
		SHEET	9 OF 27

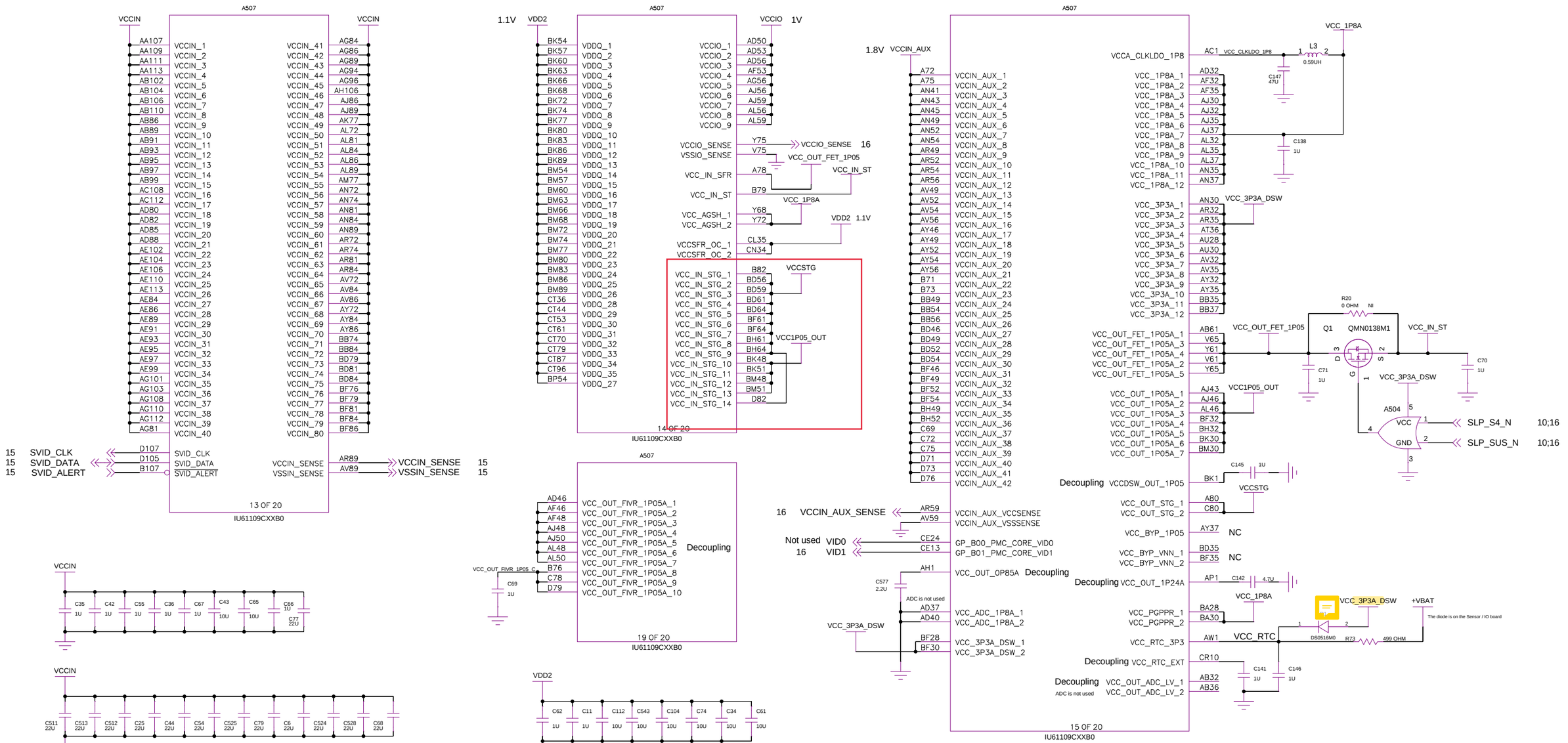
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED





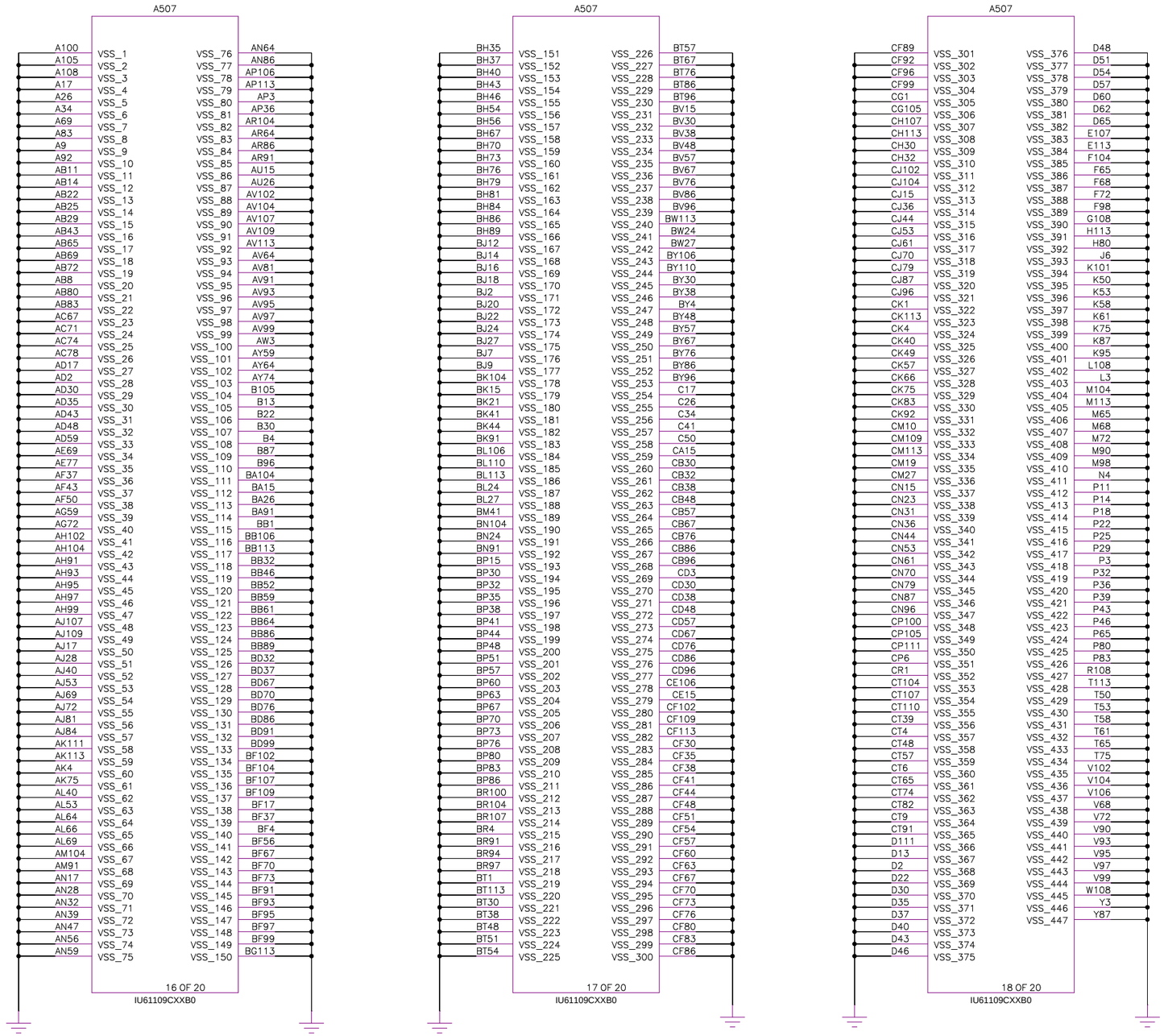
DRAWN	Dmitri Golovanov	MATROX	
PROJECT	IRIS4	1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
GROUP	Imaging	THIS DRAWING IS THE PROPERTY OF MATROX GRAPHICS INC. AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY			
ING#			
SIZE	DATE	TITLE	IRIS4 CPU board EHL eMMC PMC
B	21/02/2020:08:32	DRAWING NO	7571 -04- 00
		REV	A
		SHEET	10 OF 27

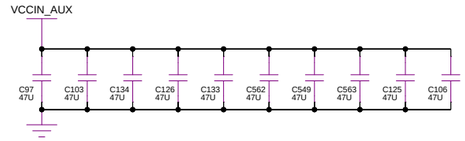
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

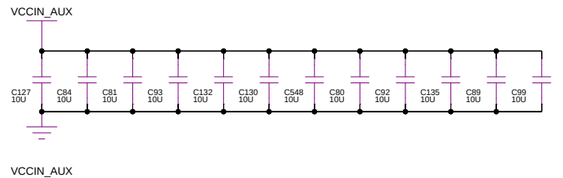


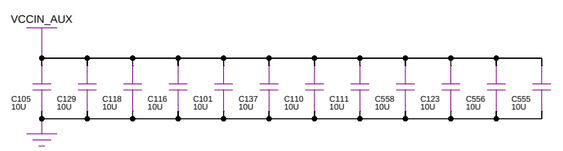
DRAWN	Dmitri Golovanov	MATROX	
PROJECT	IRIS4	1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
GROUP	Imaging	THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY			
ING#			
SIZE	DATE	TITLE	IRIS4 CPU board EHL Power
B	21/02/2020:09:15	DRAWING NO	7571 -04- 00
		REV	A
		SHEET	11 OF 27

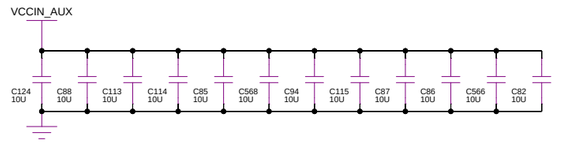
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

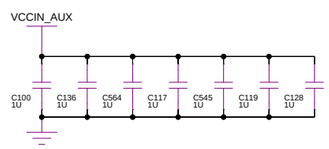






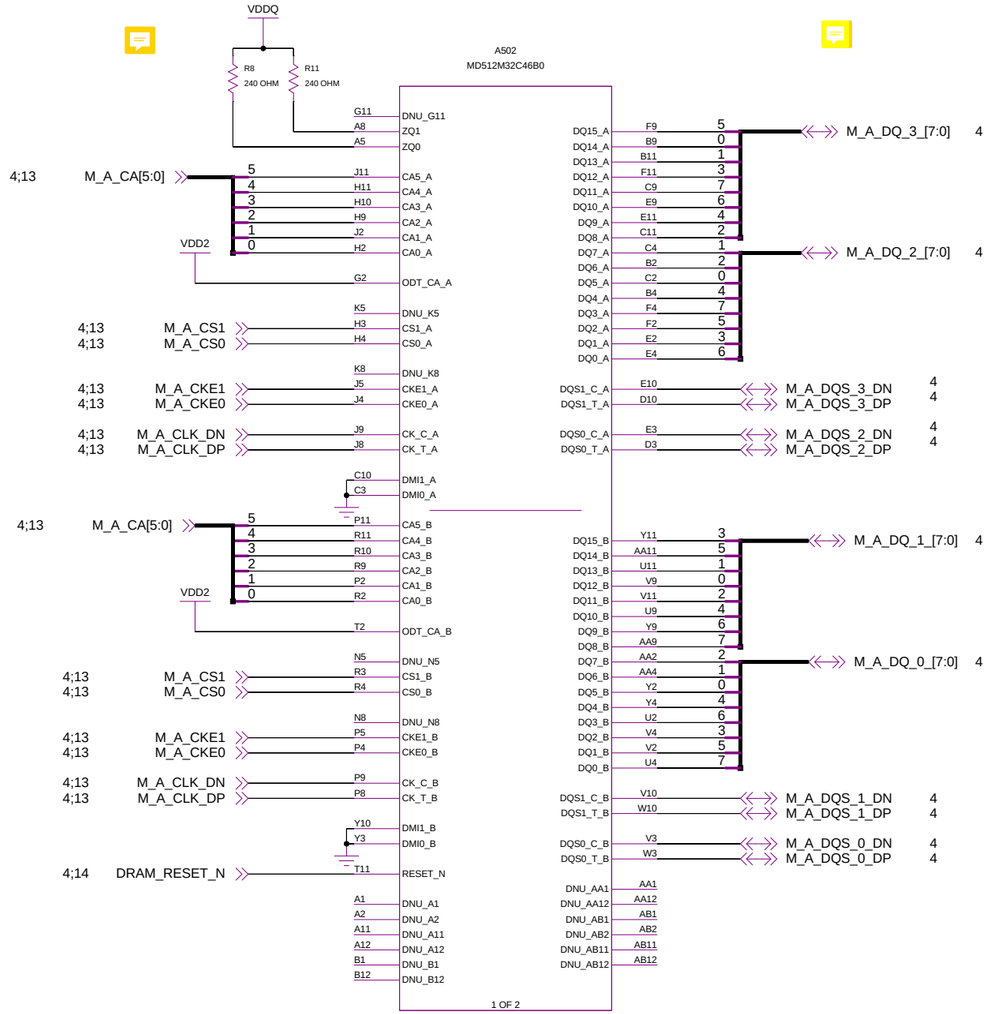






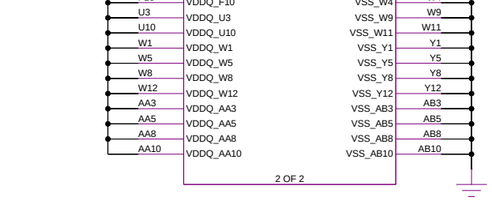
DRAWN: Dmitri Golovanov	MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4		
PROJECT: IRIS4			
GROUP: Imaging	THIS DRAWING IS THE PROPERTY OF MATROX GRAPHICS INC. AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.		
CHECKED BY			
ING#	TITLE: IRIS4 CPU board EHL GND pins		
SIZE: B	DATE: 2019/11/08 24/01/2020 08:28	DRAWING NO: 7571 -04- 00	REV: A / SHEET: 12 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

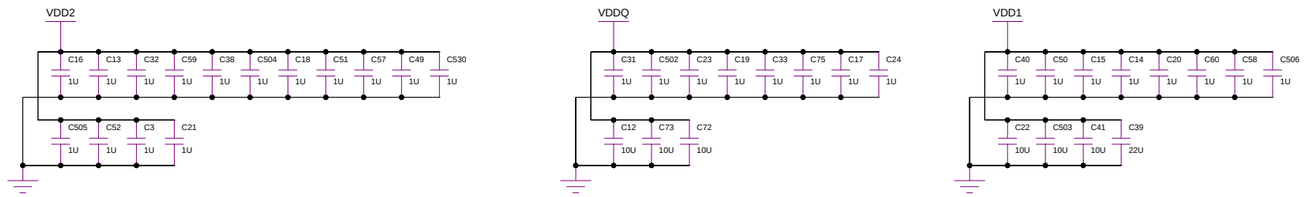


LPDDR4X MEMORY 512MX32 DRAM

10 x 14.5 x 0.7mm



LPDDR4x decoupling for 2 devices



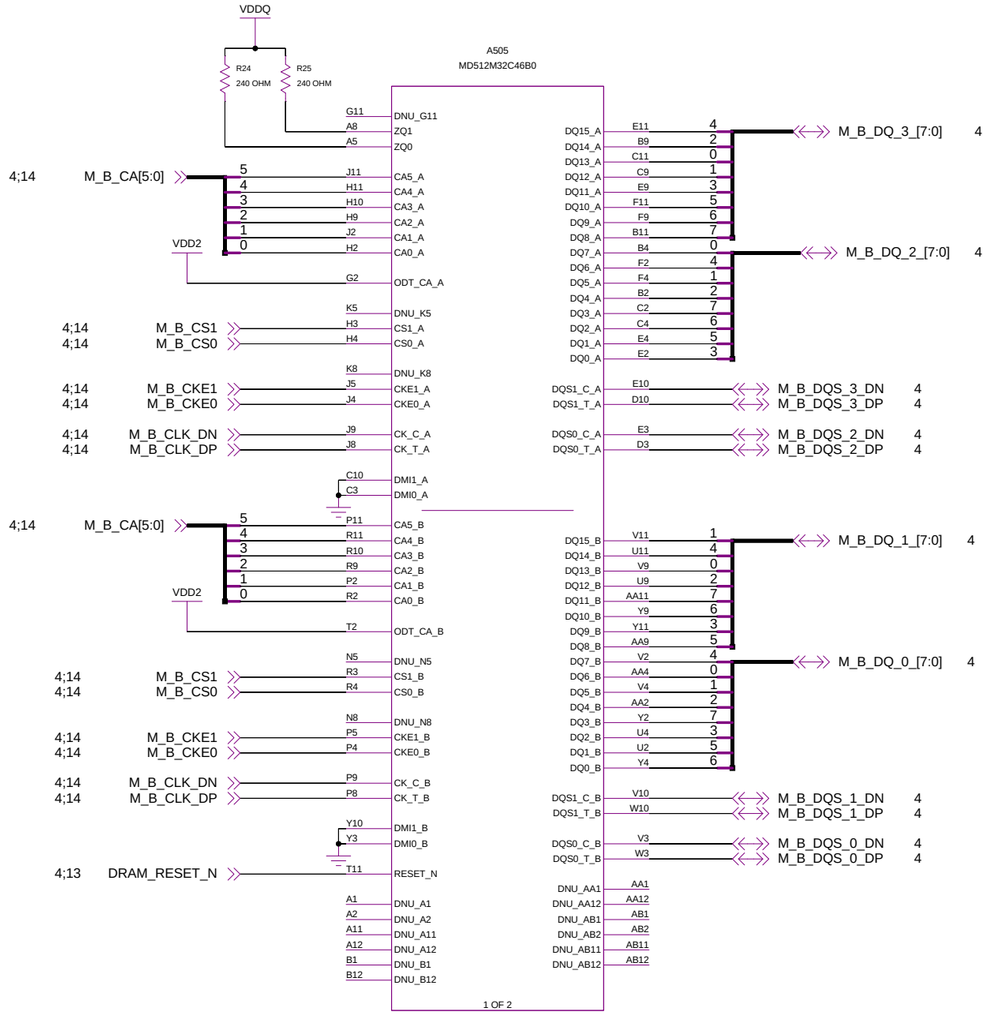
DRAWN	Dmitri Golovanov
PROJECT	IRIS4
GROUP	Imaging
CHECKED BY	
ING#	
SIZE	B
DATE	21/02/2020:07:58

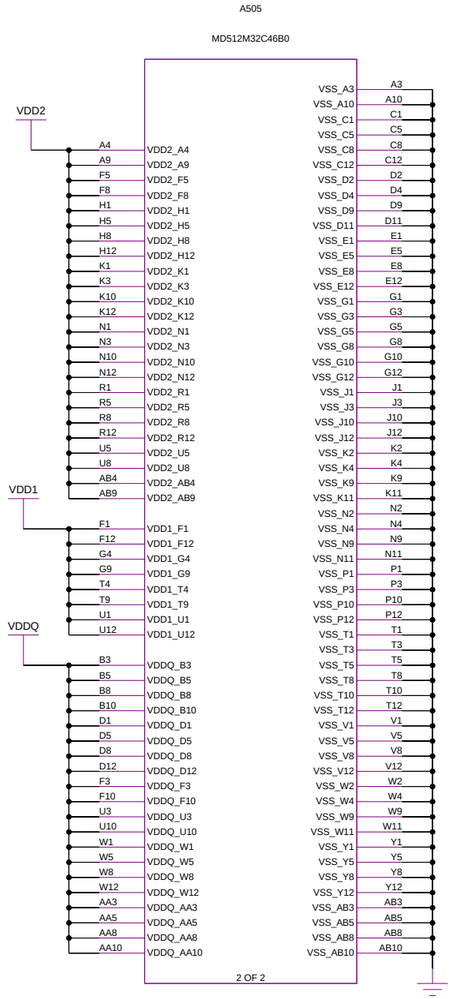
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: IRIS4 CPU board
LPDDR4x sub-channel 0

DRAWING NO	REV	SHEET
7571 -04- 00	A	13 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED





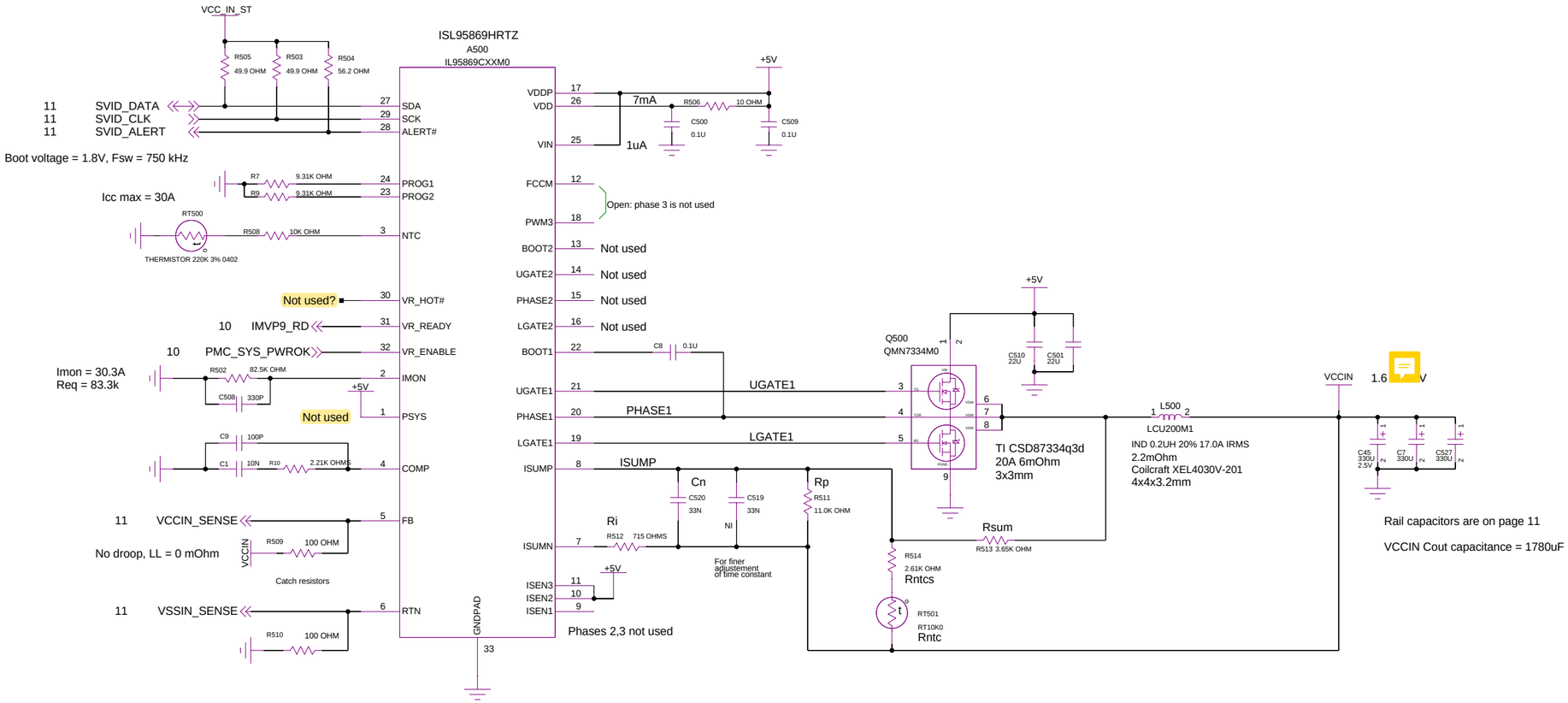
DRAWN	Dmitri Golovanov
PROJECT	IRIS4
GROUP	Imaging
CHECKED BY	
ING#	
SIZE	B
DATE	12/02/2020:13:39

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: IRIS4 CPU board
LPDDR4x sub-channel 1

DRAWING NO	REV	SHEET
7571 -04- 00	A	14 OF 27

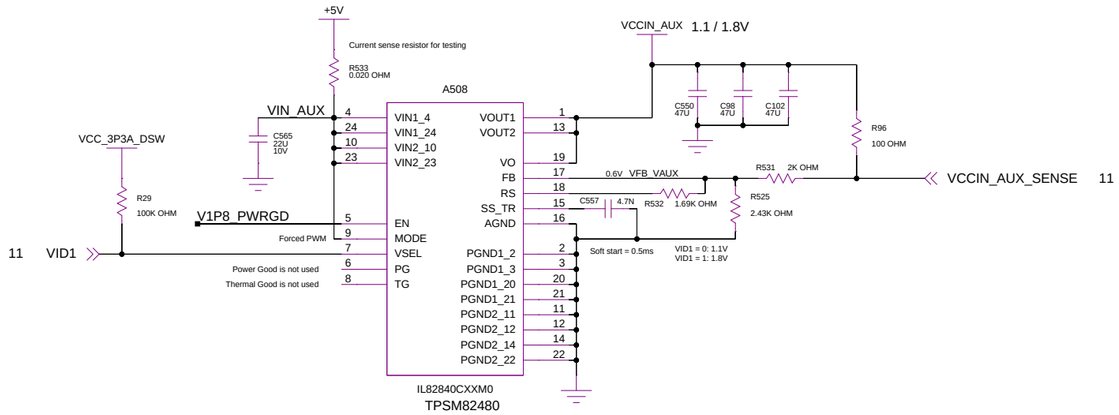
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

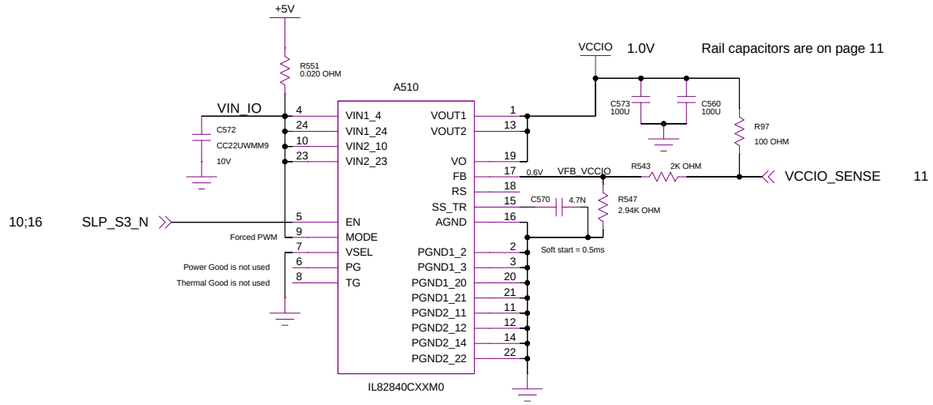


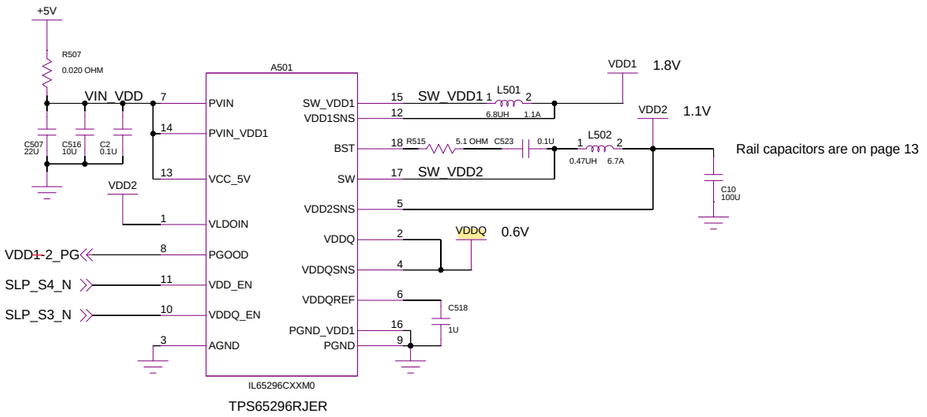
DRAWN	Dmitri Golovanov	MATROX	
PROJECT	IRIS4	1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
GROUP	Imaging	THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY			
ING#		TITLE	IRIS4 CPU board VR VCCIN IMVP9
SIZE	DATE		
B	12/02/2020:13:39	DRAWING NO 7571 -04- 00	REV A / SHEET 15 OF 27

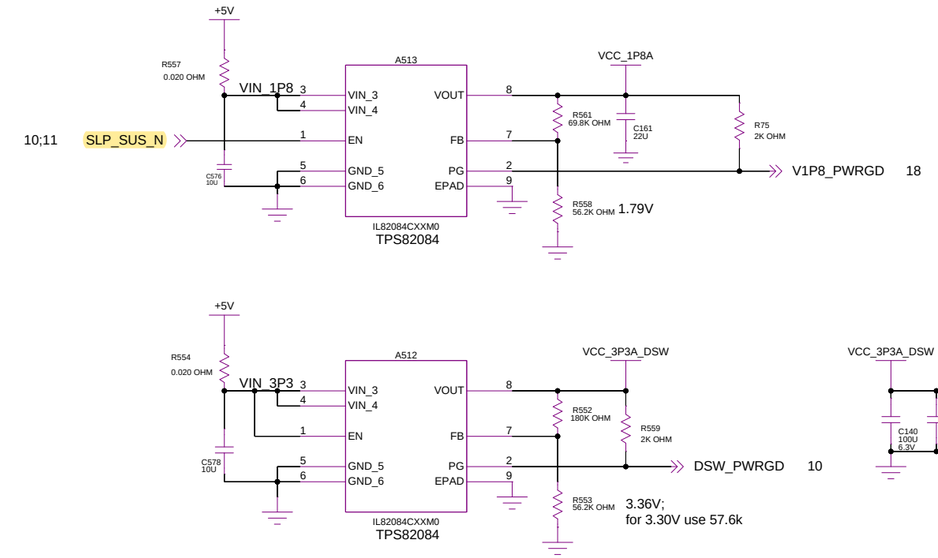
Rail capacitors are on page 12

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED









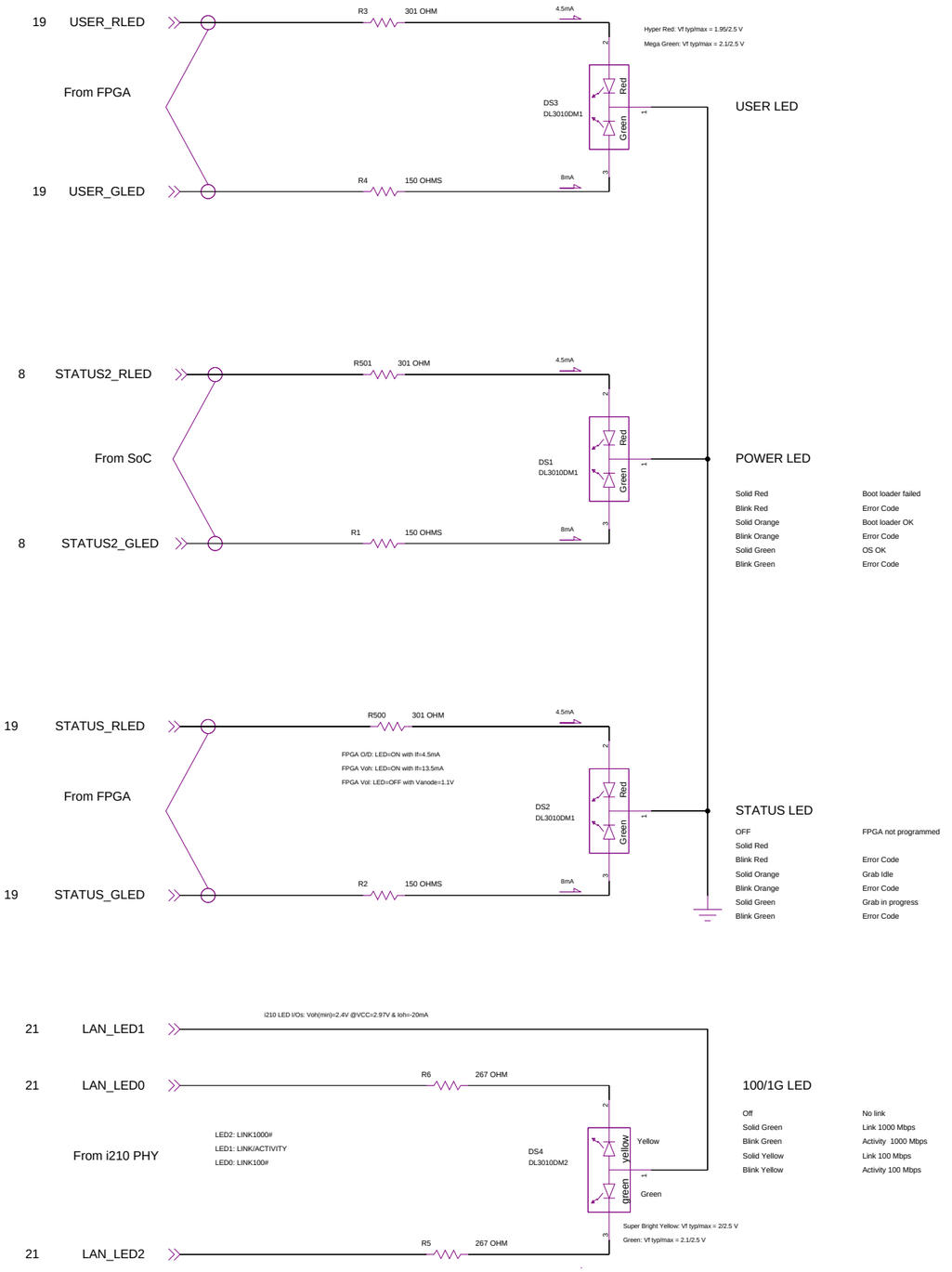
DRAWN	Dmitri Golovanov
PROJECT	IRIS4
GROUP	Imaging
CHECKED BY	
ING#	
SIZE	B
DATE	21/02/2020:07:44

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: IRIS4 CPU board
VRs

DRAWING NO	REV	SHEET
7571 -04- 00	A	16 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



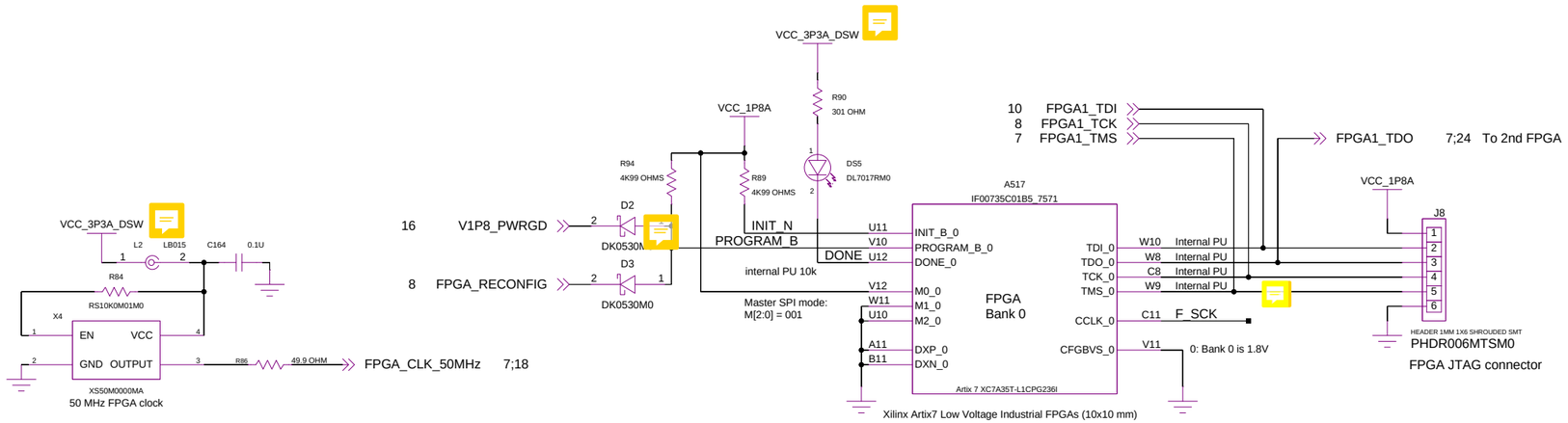
DRAWN	Dmitri Golovanov
PROJECT	IRIS4
GROUP	Imaging
CHECKED BY	
ING#	
SIZE	B
DATE	12/02/2020:13:39

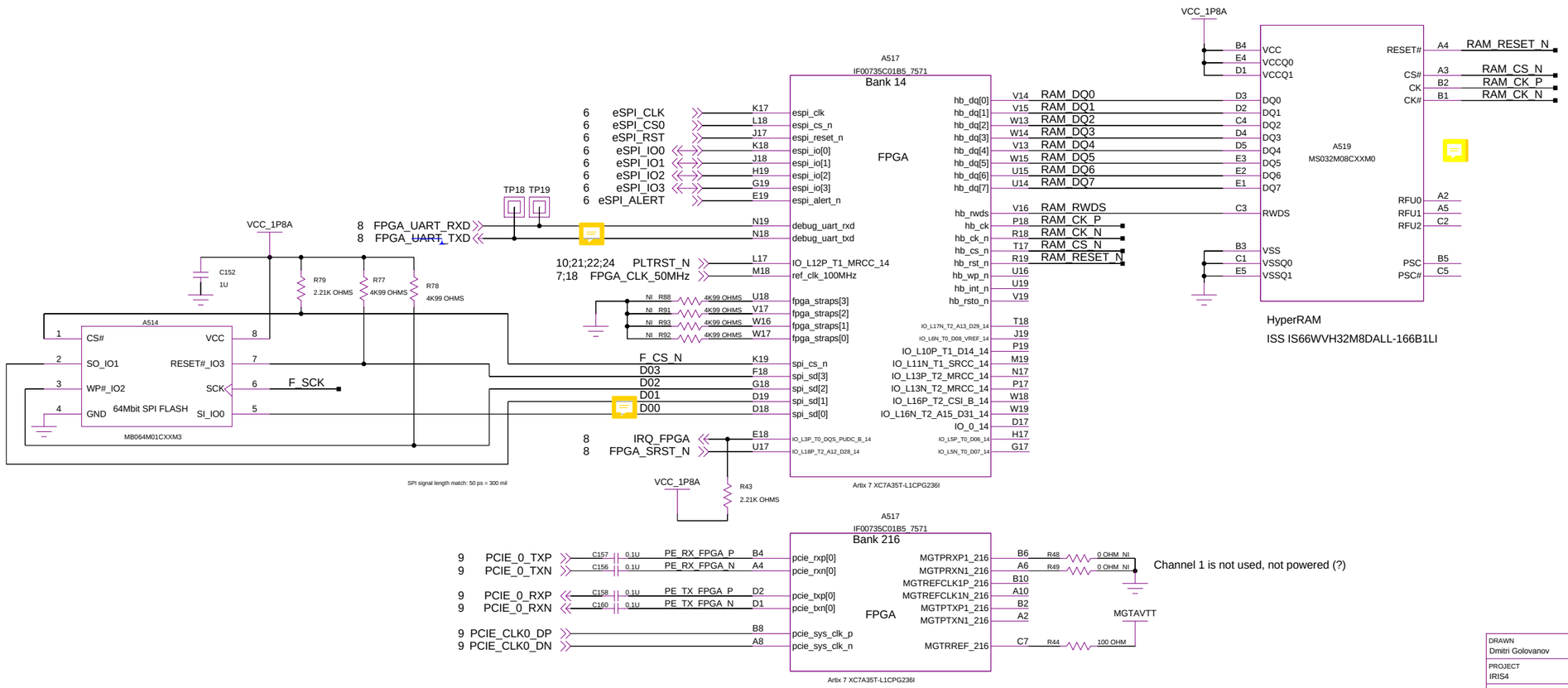
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: IRIS4 CPU board LEDs

DRAWING NO	REV	SHEET
7571 -04- 00	A	17 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED





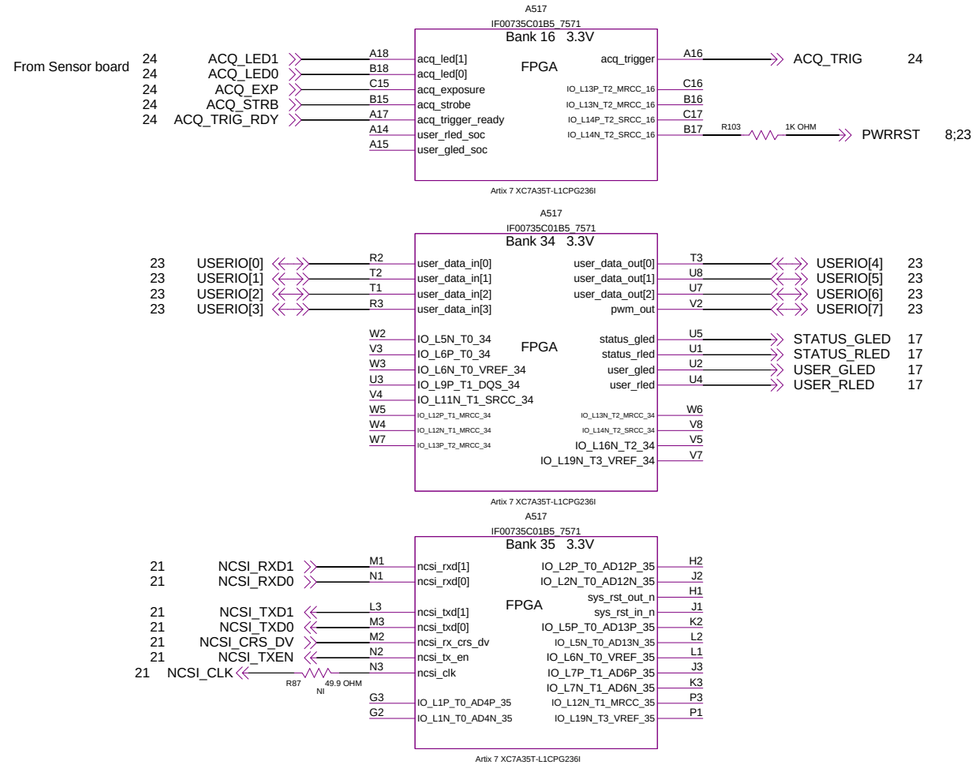
DRAWN	Dmitri Golovanov
PROJECT	IRIS4
GROUP	Imaging
CHECKED BY	
ING#	
SIZE	B
DATE	14/02/2020:11:41

MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE
IRIS4 CPU board
FPGA config and PCIe

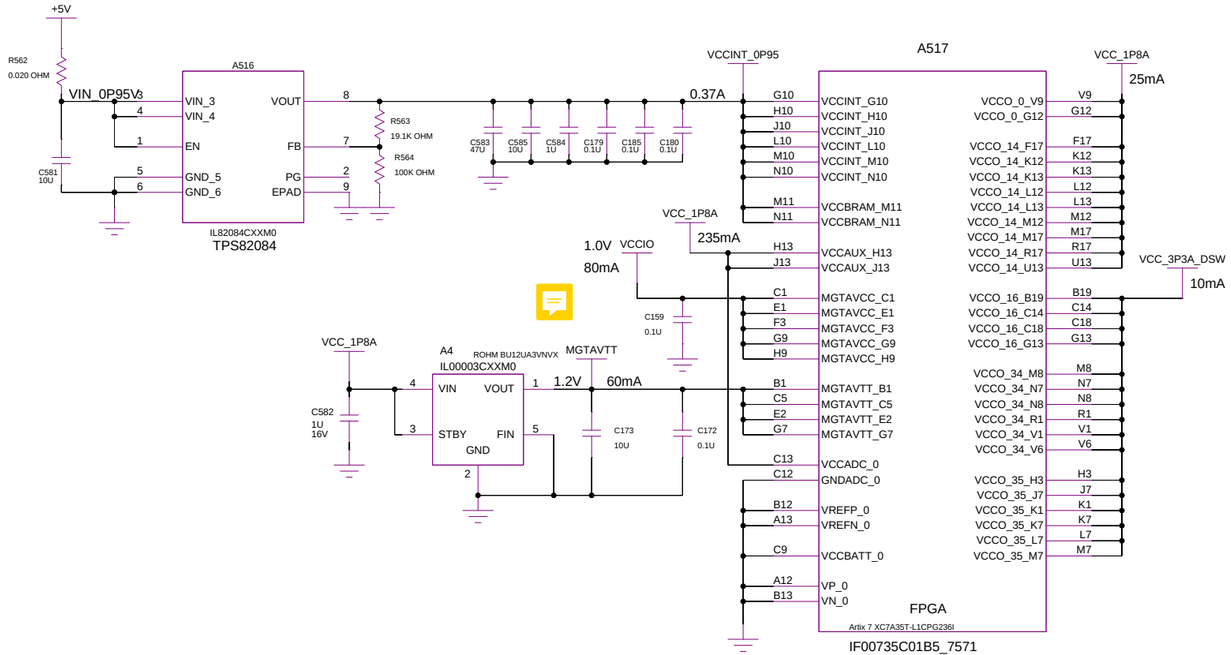
DRAWING NO	REV	SHEET
7571 -04- 00	A	18 OF 27

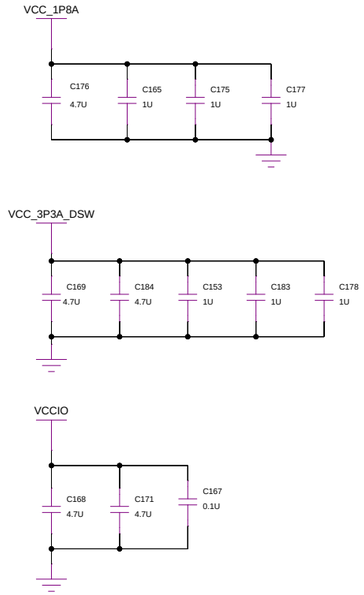
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

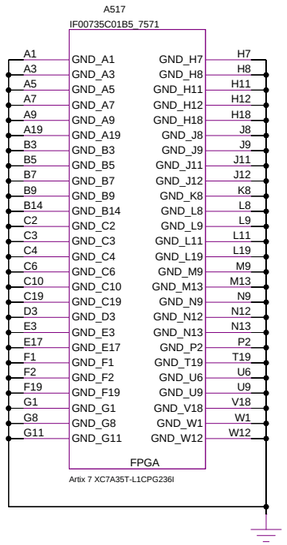


DRAWN	Dmitri Golovanov	MATROX	
PROJECT	IRIS4	1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
GROUP	Imaging	THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY			
ING#		TITLE	IRIS4 CPU board FPGA IO
SIZE	DATE		
B	12/02/2020:13:39	DRAWING NO 7571 -04- 00	REV A / SHEET 19 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

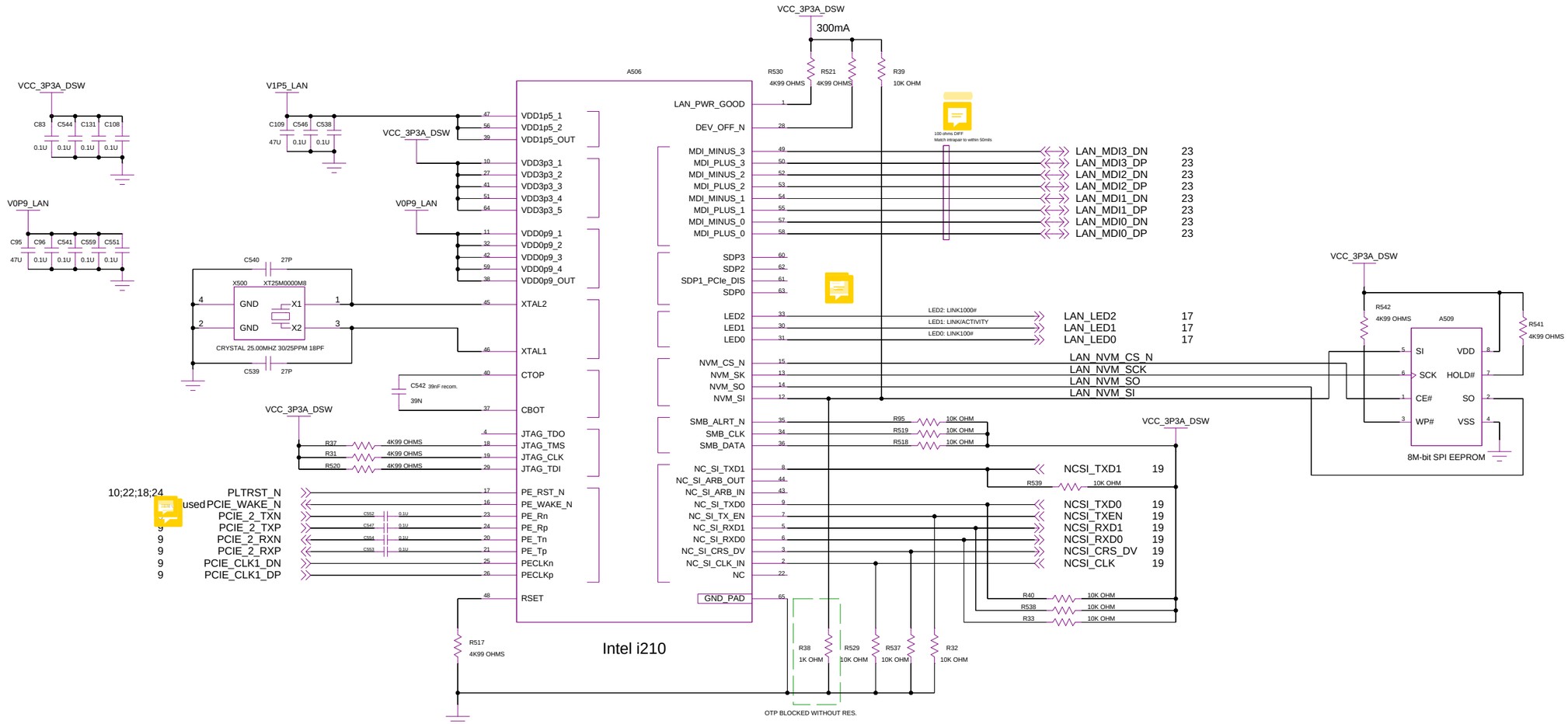






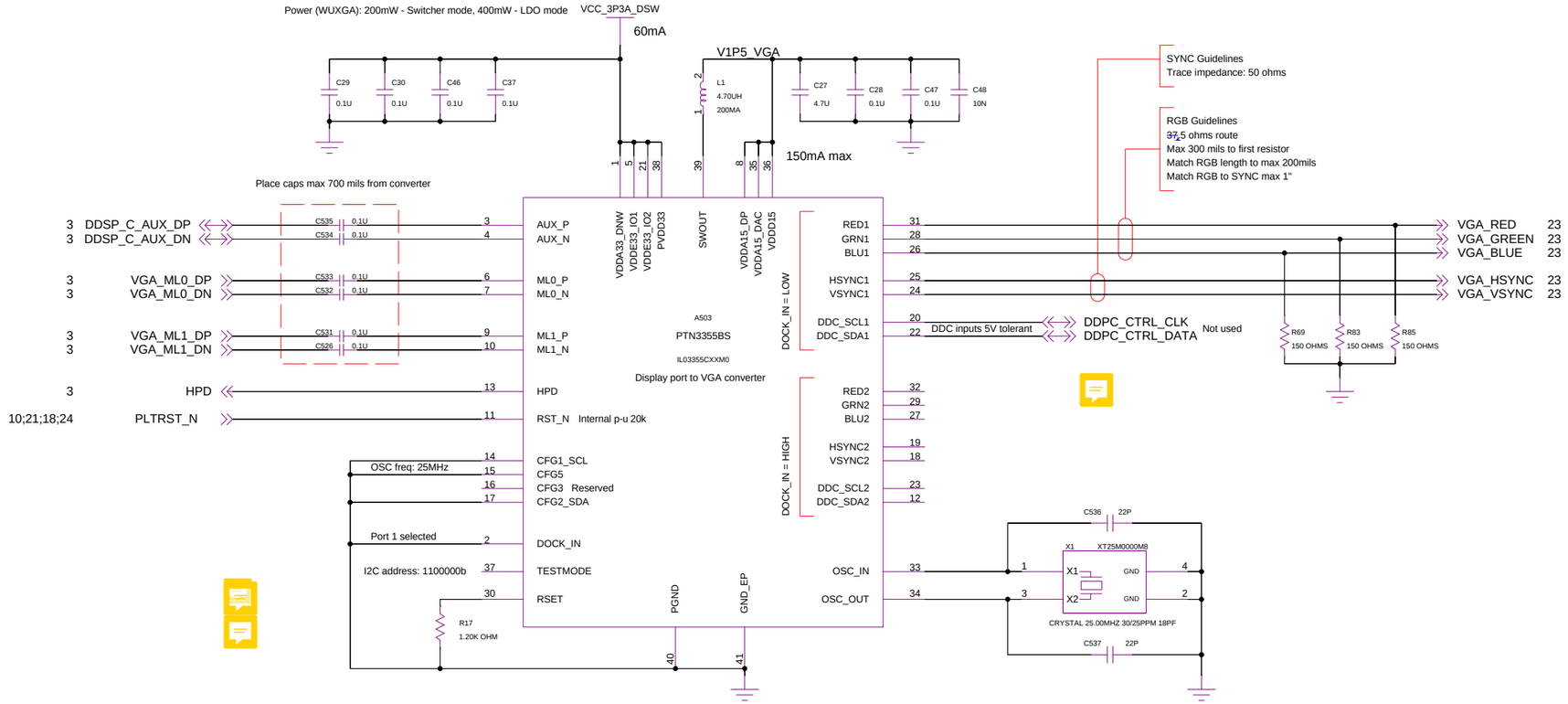
DRAWN	Dmitri Golovanov	MATROX	
PROJECT	IRIS4	1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
GROUP	Imaging	THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY			
ING#		TITLE	IRIS4 CPU board FPGA power
SIZE	B	DATE	18/02/2020:07:23
DRAWING NO	7571 -04- 00	REV	A
SHEET	20 OF 27		

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



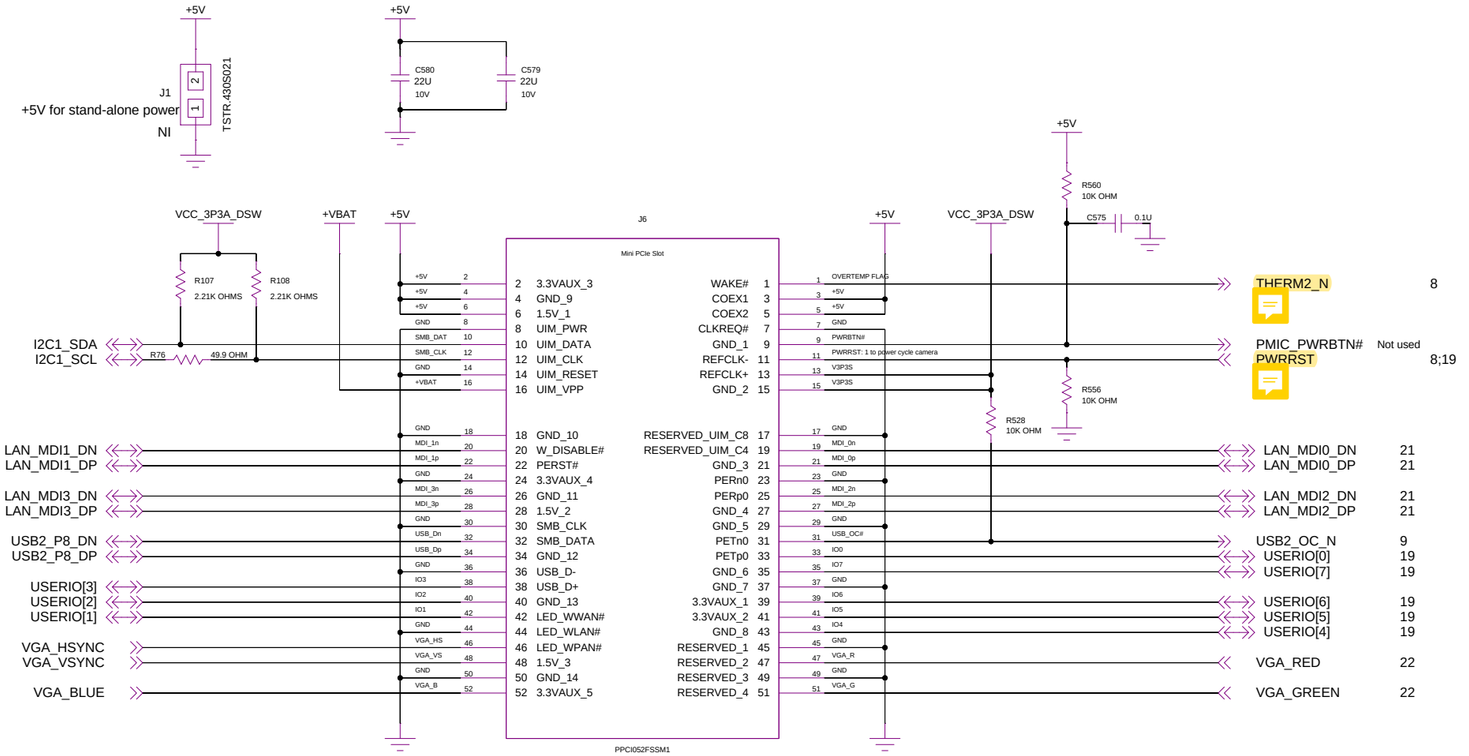
DRAWN	Dmitri Golovanov	MATROX	
PROJECT	IRIS4	1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
GROUP	Imaging	THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY			
ING#		TITLE	IRIS4 CPU board Ethernet controller
SIZE	B	DATE	21/02/2020:09:17
DRAWING NO	7571 -04- 00	REV	A
SHEET	21 OF 27		

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



DRAWN Dmitri Golovanov	MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4		
PROJECT IRIS4			
GROUP Imaging	THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.		
CHECKED BY			
ING#	TITLE IRIS4 CPU board VGA converter		
SIZE B	DATE 13/02/2020:13:49		
DRAWING NO 7571 -04- 00	REV A	SHEET 22 OF 27	

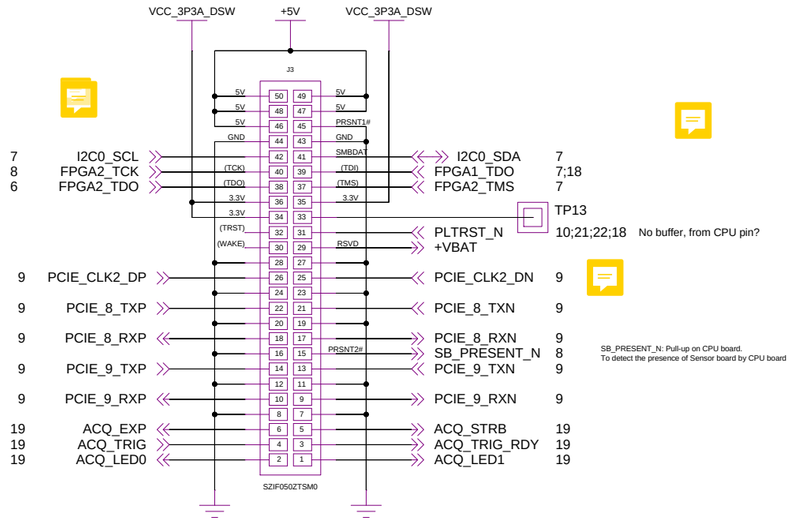
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



DRAWN	Dmitri Golovanov	MATROX	
PROJECT	IRIS4	1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
GROUP	Imaging	THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY		TITLE	IRIS4 CPU board IO board connector
ING#			
SIZE	DATE		
B	21/02/2020:08:27	DRAWING NO	7571 -04- 00
		REV	A
		SHEET	23 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

CPU Board ZIF pinout is inverted
Sensor board pos 1 aligned with CPU board pos 50
Connectors are head-to-head with latch on same side



Sensor board connector

CPU board connector

DRAWN	Dmitri Golovanov
PROJECT	IRIS4
GROUP	Imaging
CHECKED BY	
ING#	
SIZE	B
DATE	20/02/2020:15:21

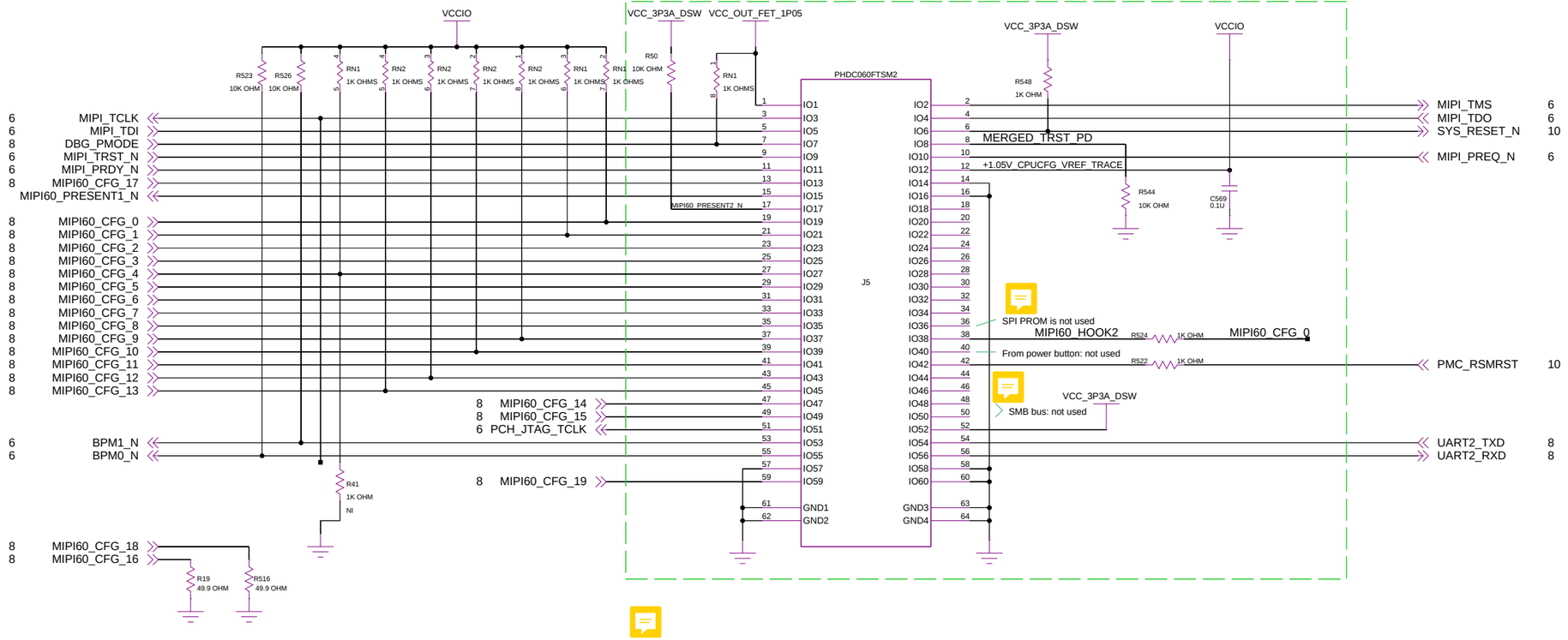
MATROX
1055 BOUL. ST-REGIS
DORVAL, QUEBEC H9P 2T4

TITLE: IRIS4 CPU board
Sensor Board Connector

DRAWING NO	REV	SHEET
7571 -04- 00	A	24 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

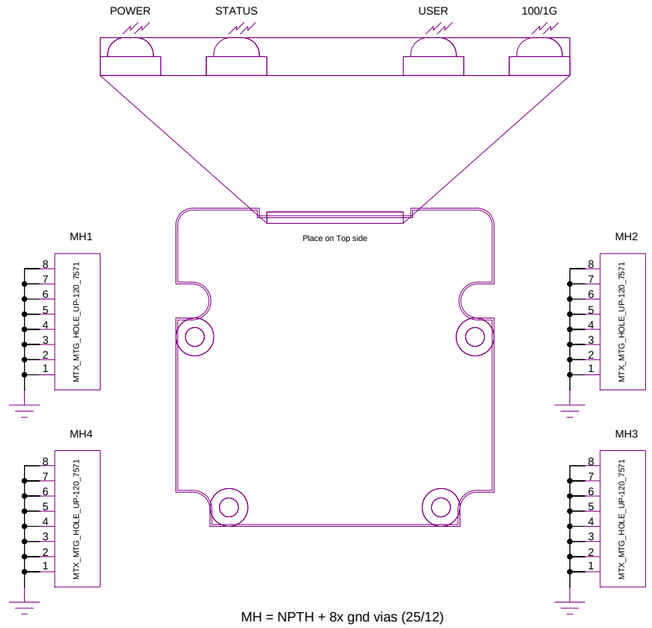
The MIPI 60 debug connector could be implemented on a break-away extension of the PCB, on prototype version only.
In this case. all components inside this outline will be disconected from EHL SoC pins on production revision



SUB=XDP

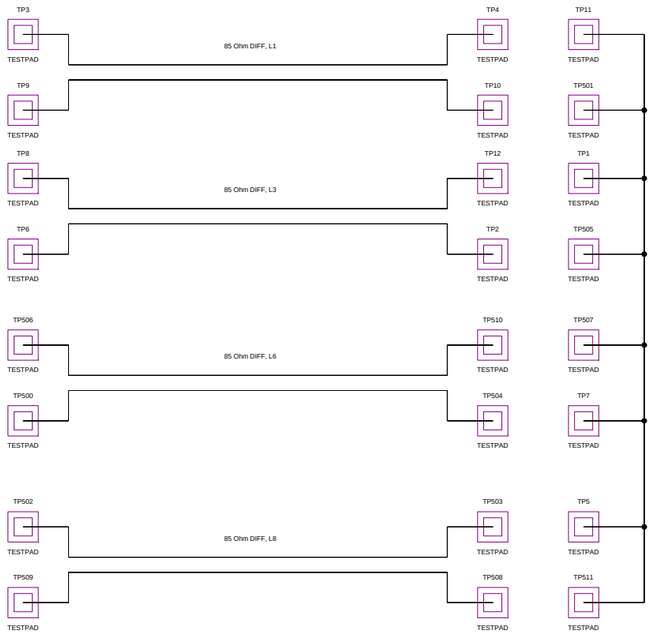
DRAWN: Dmitri Golovanov		MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT: IRIS4			
GROUP: Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY			
ING#		TITLE: IRIS4 CPU board CPU debug port	
SIZE: B	DATE: 12/02/2020:13:39	DRAWING NO: 7571 -04- 00	REV: A / SHEET: 25 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



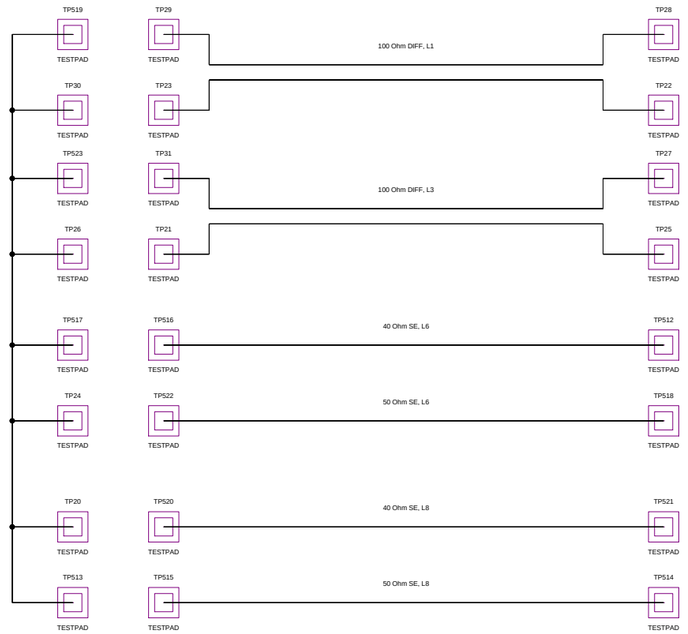
Test coupons on panel upper cracker section

Route straight on full cracker length



Test coupons on panel lower cracker section

Route straight on full cracker length



DRAWN Dmitri Golovanov	MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4		
GROUP Imaging		
CHECKED BY		
ING#	TITLE IRIS4 CPU board Mounting holes and test coupons	
SIZE B / DATE 31/01/2020:09:29		
DRAWING NO 7571 -04- 00	REV A	SHEET 26 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

Revision History

Y7571-00 Rev.A:

R1.00: First Release

R1.10: Bring-up changes

DRAWN Dmitri Golovanov	MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4		
GROUP Imaging		
CHECKED BY		
ING#	TITLE: IRIS4 CPU board Revision history	
SIZE: B / DATE: 17/01/2020:15:45	DRAWING NO: 7571 -04- 00	REV: A / SHEET: 27 OF 27