Register file structure: xadc_wizard.pdf
Created by amarchan on 2019/05/13 13:39:06

1. Main Parameters

Register file endianness: little endian
Address bus width: 11 bits
Data bus width: 32 bits

2. Memory Map

Section name	Address(es) / Address Ranges	Register name
local_register	0x000	ssr
	0x004	sr
	0x008	aosr
	0x00C	convstr
	0x010	xadc_reset
interrupt_controller	0x05C	global_interrupt
	0x060	interrupt_status
	0x068	interrupt_enable
xadc_hard_macro	0x200	temperature
	0x204	vcc_int
	0x208	vcc_aux
	0x20C	vp_vn
	0x210	vref_p
	0x214	vref_n
	0x218	vcc_bram
	0x220	supply_a_offset
	0x224	adc_a_offset
	0x228	adc_a_gain
	0x234	vcc_pint
	0x238	vcc_paux
	0x23C	vcco_ddr
	0x240, 0x244, ... ,0x27C	vaux_p_n (15:0)
	0x280	max_temperature
	0x284	max_vcc_int
	0x288	max_vcc_aux
	0x28C	max_vcc_bram
	0x290	min_temperature
	0x294	min_vcc_int
	0x298	min_vcc_aux
	0x29C	min_vcc_bram
	0x2A0	max_vcc_pint
	0x2A4	max_vcc_paux
	0x2A8	max_vcco_ddr

Section name	Address(es) / Address Ranges	Register name
	0x2B0	min_vcc_pint
	0x2B4	min_vcc_paux
	0x2B8	main_vcco_ddr
	0x2C0	supply_b_offset
	0x2C4	adc_b_offset
	0x2C8	adc_b_gain
	0x2D4	flag
control	0x300	config_0
	0x304	config_1
	0x308	config_2
alarm_tresholds	0x340	temperature_upper
	0x344	vccint_upper
	0x348	vccaux_upper
	0x34C	ot_alarm_limit
	0x350	temperature_lower
	0x354	vccint_lower
	0x358	vccaux_lower
	0x35C	ot_alarm_reset
	0x360	vccbram_upper
	0x364	vccpint_upper
	0x368	vccpaux_upper
	0x36C	vcco_ddr_upper
	0x370	vccbram_lower
	0x374	vccpint_lower
	0x378	vccpaux_lower
	0x37C	vcco_ddr_lower

Section: local_register — XADC Wizard Local Register Grouping

Address Range: [0x000 - 0x010]

Description:
It is expected that the XADC Wizard IP core registers are accessed in their preferred-access mode only. If the write attempt is made to read-only registers, then there is not any effect on register contents. If the write-only registers are read, the result is undefined data. All the internal registers of the core have to be accessed in 32-bit format. If any other kind of access (like halfword or byte access) is done for the XADC Wizard IP core local 32-bit registers, the transaction is completed but with errors for the corresponding transaction.

ssr — Software Reset Register (SSR)

Address: section "local_register" base address + 0x000

Description:
The Software Reset register permits you to reset the XADC Wizard IP core including the XADC hard macro output ports (except JTAG related outputs), independently of other IP cores in the systems. To activate software reset, the value 0x0000_000A must be written to the register. Any other access, read or write, has undefined results. The bit assignment in the Software Reset register is shown in Figure 2-1 and described in Table 2-4.

31	30	29	28	27	26	25	24
value(31:24)							
23	22	21	20	19	18	17	16
value(23:16)							
15	14	13	12	11	10	9	8
value(15:8)							
7	6	5	4	3	2	1	0
value(7:0)							

value (31:0)	
RW	
Value at Reset:	N/A (Non-resettable flip-flops used)

Address: section "local_register" base address + 0x004

Description:

The Status register contains the XADC Wizard IP core channel status, End of Conversion (EOC), End of Sequence (EOS), and Joint Test Action Group (JTAG) access signals. This register is read only. Any attempt to write to the bits of the register would not change the bits. The Status register bit definitions are shown in Figure 2-2 and explained in Table 2-5.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved					jtag_busy	jtag_modified	jtag_locked
7	6	5	4	3	2	1	0
busy	eos	eoc	channel(4:0)				

jtag_busy	JTAG busy
RO	Used to indicate that a JTAG DRP transaction is in progress.

jtag_modified	JTAG modified
RO	Used to indicate that a write to DRP through JTAG interface has occurred. This bit is cleared when a successful DRP read/write operation through the FPGA logic is performed. The DRP read/write through the FPGA logic fails, if JTAGLOCKED = 1.

jtag_locked	JTAG locked
RO	Used to indicate that a DRP port lock request has been made by the Joint Test Action Group (JTAG) interface.

busy	ADC busy signal
RO	This signal transitions High during an ADC conversion.

eos	End of Sequence
RO	This signal transitions to an active-High when the measurement data from the last channel in the auto sequence is written to the Status registers. This bit is cleared when a read operation is performed on Status register.

eoc	End of Conversion signal
RO	This signal transitions to an active-High at the end of an ADC conversion when the measurement is written to the XADC hard macro Status register. This bit is cleared when a read operation is performed on Status register.

channel (4:0)	Channel selection outputs
RO	The ADC input MUX channel selection for the current ADC conversion is placed on these outputs at the end of an ADC conversion.

Address: section "local_register" base address + 0x008

Description:

The Alarm Output Status register contains all the alarm outputs for the XADC Wizard IP core. This register is read-only. Any attempt to write to the bits of the register would not change the bits. The Alarm Output Status register bit definitions are shown in Figure 2-3 and explained in Table 2-6.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							alarm_7
7	6	5	4	3	2	1	0
alarm_6	alarm_5	alarm_4	alarm_3	alarm_2	alarm_1	alarm_0	over_temperature

alarm_7	Logical ORing of ALARM bits 0 to 7
RO	This is direct output from the XADC macro.

alarm_6	XADC VCCDDRO-Sensor Status
RO	The XADC VCCDDRO-sensor alarm output interrupt occurs when VCCDDRO exceeds the user-defined threshold. This bit is only valid for Zynq-7000 devices.

alarm_5	XADC VCCPAUX-Sensor Status
RO	The XADC VCCPAUX-sensor alarm output interrupt occurs when VCCPAUX exceeds the user-defined threshold. This bit is only valid for Zynq-7000 devices.

alarm_4	XADC VCCPINT-Sensor Status
RO	The XADC VCCPINT-sensor alarm output interrupt occurs when VCCPINT exceeds the user-defined threshold. This bit is only valid for Zynq-7000 devices.

alarm_3	XADC VBRAM-Sensor Status
RO	XADC VBRAM-sensor alarm output interrupt occurs when VBRAM exceeds user-defined threshold.

alarm_2	XADC VCCAUX-Sensor Status
RO	XADC VCCAUX-sensor alarm output interrupt occurs when VCCAUX exceeds user-defined threshold.

alarm_1	XADC VCCINT-Sensor Status
RO	XADC VCCINT-sensor alarm output interrupt occurs when VCCINT exceeds user-defined threshold.

alarm_0	XADC Temperature-Sensor Status
RO	XADC temperature-sensor alarm output interrupt occurs when device temperature exceeds user-defined threshold.

over_temperature	XADC Over-Temperature Alarm Status
RO	Over-Temperature alarm output interrupt occurs when the die temperature exceeds a factory set limit of 125°C.

Address: section "local_register" base address + 0x00C

Description:
The CONVST register is used for initiating a new conversion in the event-driven sampling mode. The output of this register is logically ORed with the external CONVST input signal. This register also defines enable for the Temperature Bus update logic and the wait cycle count. The attempt to read this register results in undefined data. The CONVST register bit definitions are shown in Figure 2-4 and explained in Table 2-7.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						temp_rd_wait_cycle(15:14)	
15	14	13	12	11	10	9	8
temp_rd_wait_cycle(13:6)							
7	6	5	4	3	2	1	0
temp_rd_wait_cycle(5:0)						temp_bus_update	convst

temp_rd_wait_cycle (15:0)	Wait cycle for temperature update
RW	Temperature update logic waits for this count of the S_AXI_ACLK before reading the Temperature register. This value should be such that the period is more than the ADC conversion rate.
Value at Reset:	N/A (Non-resettable flip-flops used)

temp_bus_update	Temperature bus update
RW	Enable temperature update logic enables the temperature read from XADC and updates of TEMP_OUT port.
Value at Reset:	0x0

convst	Conversion Start
RW	A rising edge on the CONVST input initiates start of ADC conversion in event-driven sampling mode. For the selected channel the CONVST bit in the register needs to be set to 1 and again reset to 0 to start a new conversion cycle. The conversion cycle ends with EOC bit going High.
Value at Reset:	0x0

xadc_reset XADC Hard Macro Reset Register

Address: section "local_register" base address + 0x010

Description:
The XADC Reset register is used to reset only the XADC hard macro. As soon as the reset is released the ADC begins with a new conversion. If sequencing is enabled this conversion is the first in the sequence. This register resets the OT and ALM[n] output from the XADC hard macro. This register does not reset the interrupt registers if they are included in the design. Also any reset from the FPGA logic does not affect the RFI (Register File Interface) contents of XADC hard macro. The attempt to read this register results in undefined data. The XADC Reset register bit definitions are shown in Figure 2-5 and explained in Table 2-8.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							reset

reset		
RW	Writing a 1 to this bit position resets the XADC hard macro. The reset is released only after 0 is written to this register.	
Value at Reset:	0x0	
Possible Values:	0x0	Release the reset (Normal operation)
	0x1	Reset the XADC

Section: interrupt_controller XADC Wizard Interrupt Controller

Address Range: [0x05C - 0x068]

Description:
The Interrupt Controller Module is included in the XADC Wizard IP core design when C_INCLUDE_INTR = 1. The XADC Wizard has several distinct interrupts that are sent to the Interrupt Controller Module, which is one of the submodules of the XADC Wizard IP core.
The Interrupt Controller Module allows each interrupt to be enabled independently (by the IP Interrupt Enable register (IPIER)). All the interrupt signals are rising-edge sensitive. Interrupt registers are strictly 32-bit accessible. If byte/halfword or without byte enables access is made, the core behavior is not guaranteed. The interrupt registers are in the Interrupt Controller Module. The XADC Wizard permits multiple conditions for an interrupt or an interrupt strobe which occurs only after the completion of a transfer.

global_interrupt Global Interrupt Enable Register (GIER)

Address: section "interrupt_controller" base address + 0x000

Description:
The Global Interrupt Enable register is used to globally enable the final interrupt output from the Interrupt Controller as shown in Figure 2-6 and described in Table 2-9. This bit is a read/write bit and is cleared upon reset.

31	30	29	28	27	26	25	24
enable	Reserved						
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

enable *RW*	Global Interrupt Enable It enables all individually enabled interrupts to be passed to the interrupt controller.	
Value at Reset:	0x0	
Possible Values:	0x0	All interrupts are disabled
	0x1	All interrupts are enabled

interrupt_status IP Interrupt Status Register (IPISR)

Address: section "interrupt_controller" base address + 0x004

Description:
The six unique interrupt conditions in the XADC Wizard IP core include:

1) OT
2) ALM[6:0]
3) OT DEACTIVE,
4) ALM[0] DEACTIVE,
5) JTAG LOCKED/MODIFIED
6) EOC/EOS

The Interrupt Controller has a register that can enable each interrupt independently. Bit assignment in the Interrupt register for a 32-bit data bus is shown in Figure 2-7 and described in Table 2-10. The interrupt register is a read/toggle on write register and by writing a 1 to a bit position within the register causes the corresponding bit position in the register to toggle. All register bits are cleared upon reset.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		alarm_6	alarm_5	alarm_4	alarm_2	alarm_0_deactive	over_temperature_deactive
7	6	5	4	3	2	1	0
jtag_modified	jtag_locked	eoc	eos	alarm_3	alarm_1	alarm_0	over_temperature

alarm_6	XADC VCCDDRO-Sensor Interrupt
RW2C	The XADC VCCDDRO-sensor alarm output interrupt occurs when VCCDDRO exceeds the user-defined threshold. This bit is only valid for Zynq-7000 devices.
Value at Reset:	0x0

alarm_5	XADC VCCPAUX-Sensor Interrupt
RW2C	The XADC VCCPAUX-sensor alarm output interrupt occurs when VCCPAUX exceeds the user-defined threshold. This bit is only valid for Zynq-7000 devices.
Value at Reset:	0x0

alarm_4	XADC VCCPINT-Sensor Interrupt
RW2C	The XADC VCCPINT-sensor alarm output interrupt occurs when VCCPINT exceeds the user-defined threshold. This bit is only valid for Zynq-7000 devices
Value at Reset:	0x0

alarm_2	XADC VCCAUX-Sensor Interrupt
RW2C	XADC VCCAUX-sensor alarm output interrupt occurs when VCCAUX exceeds the user-defined threshold.
Value at Reset:	0x0

alarm_0_deactive	ALM[0] Deactive Interrupt.
RW2C	This signal indicates that the falling edge of the Over Temperature signal is detected. It is cleared by writing a 1 to this bit position. The ALM[0] signal is generated locally from the core. This signal indicates that the XADC macro has deactivated the Over Temperature signal output.
Value at Reset:	0x0

over_temperature_deactive	Over-Temperature Deactive Interrupt.
RW2C	This signal indicates that falling edge of the Over Temperature signal is detected. It is cleared by writing a 1 to this bit position. The OT Deactive signal is generated locally from the core. This signal indicates that the XADC macro has deactivated the Over-Temperature signal output.
Value at Reset:	0x0

jtag_modified	JTAGMODIFIED Interrupt
RW2C	This signal indicates that a write to DRP through the JTAG interface has occurred. It is cleared by writing a 1 to this bit position.
Value at Reset:	0x0

jtag_locked	JTAGLOCKED Interrupt
RW2C	This signal is used to indicate that a DRP port lock request has been made by the Joint Test Action Group (JTAG) interface.
Value at Reset:	0x0

eoc	End of Sequence Interrupt
RW2C	End of Conversion Signal Interrupt. This signal transitions to an active-High at the end of an ADC conversion when the measurement is written to the XADC hard macro Status register.
Value at Reset:	0x0

eos	End of Sequence Interrupt
RW2C	This signal transitions to an active-High when the measurement data from the last channel in the auto sequence is written to the Status registers.
Value at Reset:	0x0

alarm_3	XADC VBRAM-Sensor Interrupt
RW2C	XADC VBRAM-sensor alarm output interrupt occurs when VBRAM exceeds user-defined threshold.
Value at Reset:	0x0

alarm_1	XADC VCCINT-Sensor Interrupt
RW2C	XADC VCCINT-sensor alarm output interrupt occurs when VCCINT exceeds the user-defined threshold.
Value at Reset:	0x0

alarm_0	XADC Temperature-Sensor Interrupt
RW2C	XADC temperature-sensor alarm output interrupt occurs when device temperature exceeds the user-defined threshold.
Value at Reset:	0x0

over_temperature	Over-Temperature Alarm Interrupt
RW2C	Over-Temperature alarm output interrupt occurs when the die temperature exceeds a factory set limit of 125 °C.
Value at Reset:	0x0

interrupt_enable IP Interrupt Enable Register (IPIER)

Address: section "interrupt_controller" base address + 0x00C

Description:
The IPIER has an enable bit for each defined bit of the IPISR as shown in Figure 2-8 and described in Table 2-11. All bits are cleared upon reset.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		alarm_6	alarm_5	alarm_4	alarm_2	alarm_0_deactive	over_temperature_deactive
7	6	5	4	3	2	1	0
jtag_modified	jtag_locked	eoc	eos	alarm_3	alarm_1	alarm_0	over_temperature

alarm_6	XADC VCCDDRO-Sensor Interrupt	
RW		
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

alarm_5	XADC VCCPAUX-Sensor Interrupt	
RW		
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

alarm_4	XADC VCCPINT-Sensor Interrupt	
RW		
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

alarm_2	XADC VCCAUX-Sensor Interrupt	
RW		
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

alarm_0_deactive	ALM[0] Deactive Interrupt.	
RW		
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

over_temperature_deactive	Over-Temperature Deactive Interrupt.	
RW		
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

jtag_modified	JTAGMODIFIED Interrupt	
RW		
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

jtag_locked	JTAGLOCKED Interrupt	
RW		
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

eoc	End of Sequence Interrupt	
RW		
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

eos	End of Sequence Interrupt	
RW		
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

alarm_3	XADC VBRAM-Sensor Interrupt	
RW		
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

alarm_1 *RW*	XADC VCCINT-Sensor Interrupt	
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

alarm_0 *RW*	XADC Temperature-Sensor Interrupt	
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

over_temperature *RW*	Over-Temperature Alarm Interrupt	
Value at Reset:	0x0	
Possible Values:	0x0	Disabled
	0x1	Enabled

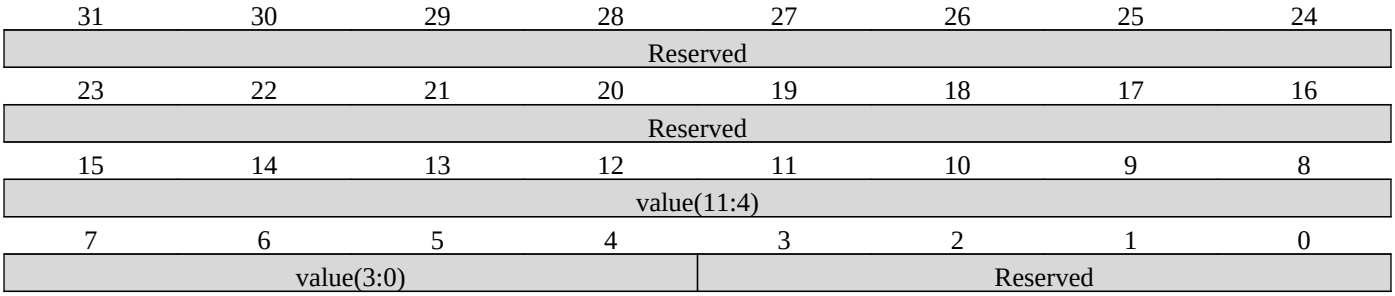
Address Range: [0x200 - 0x2D4]

Description:
The XADC hard macro register set consists of all the registers present in the XADC hard macro on 7 series FPGAs. The addresses of these registers are shown in Table 2-3. Because these registers are 16 bits wide but the processor data bus is 32 bits wide, the hard macro register data resides on the lower 16 bits of the 32-bit data bus. See Figure 2-9.

temperature

Address: section "xadc_hard_macro" base address + 0x000

Description:
The result of the on-chip temperature sensor measurement is stored in this location. The data is MSB justified in the 16-bit register. The 12 MSBs correspond to the temperature sensor transfer function shown in Figure 2-9, page 33.

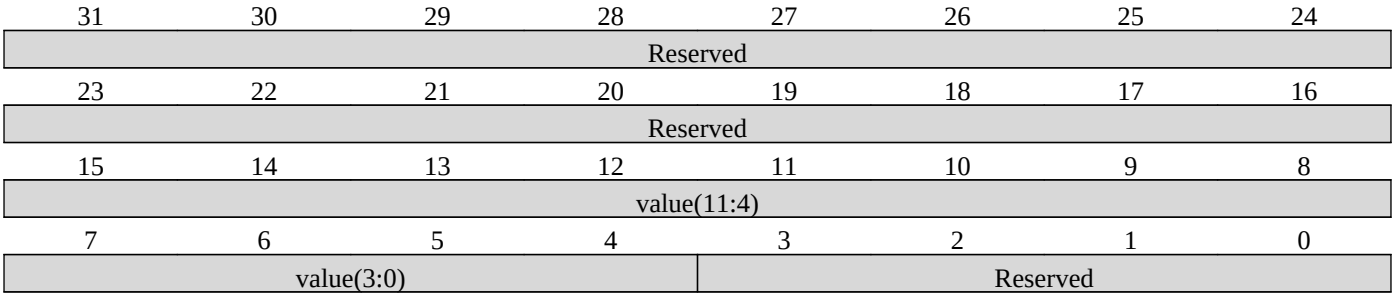


value (11:0) *RO*	Temperature value

vcc_int

Address: section "xadc_hard_macro" base address + 0x004

Description:
The result of the on-chip temperature sensor measurement is stored in this location. The data is MSB justified in the 16-bit register. The 12 MSBs correspond to the temperature sensor transfer function shown in Figure 2-9, page 33.

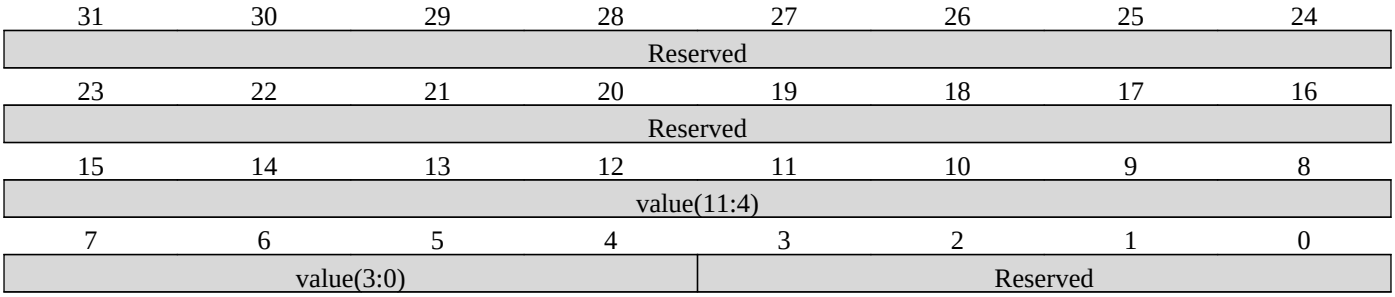


value (11:0)	Vccint value
RO	

vcc_aux

Address: section "xadc_hard_macro" base address + 0x008

Description:
The result of the on-chip VCCAUX data supply monitor measurement is stored at this location. The data is MSB justified in the 16 bit register. The 12 MSBs correspond to the supply sensor transfer function shown in Figure 2-10.



value (11:0)	Vccaux value
RO	

vp_vn

Address: section "xadc_hard_macro" base address + 0x00C

Description:
The result of a conversion on the dedicated analog input channel is stored in this register. The data is MSB justified in the 16-bit register. The 12 MSBs correspond to the transfer function shown in Figure 2-6, page 31 or Figure 2-7, page 32 depending on analog input mode settings.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Vp/Vn value
RO	

vref_p

Address: section "xadc_hard_macro" base address + 0x010

Description:
The result of a conversion on the reference input VREFP is stored in this register. The 12 MSBs correspond to the ADC transfer function shown in Figure 2-10. The data is MSB justified in the 16-bit register. The supply sensor is used when measuring VREFP.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Vrefp value
RO	

vref_n

Address: section "xadc_hard_macro" base address + 0x014

Description:
The result of a conversion on the reference input VREFN is stored in this register. This channel is measured in bipolar mode with a two's complement output coding as shown in Figure 2-3, page 27. By measuring in bipolar node, small positive and negative offset around 0V (VREFN) can be measured. The supply sensor is also used to measure VREFN, thus 1 LSB = 3V/4096. The data is MSB justified in the 16-bit register.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Vrefp value
RO	

vcc_bram

Address: section "xadc_hard_macro" base address + 0x018

Description:
The result of the on-chip VCCBRAM supply monitor measurement is stored at this location. The data is MSB justified in the 16-bit register. The 12 MSBs correspond to the supply sensor transfer function shown in Figure 2-10.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Vrefp value
RO	

supply_a_offset

Address: section "xadc_hard_macro" base address + 0x020

Description:
The calibration coefficient for the supply sensor offset using ADC A is stored at this location.

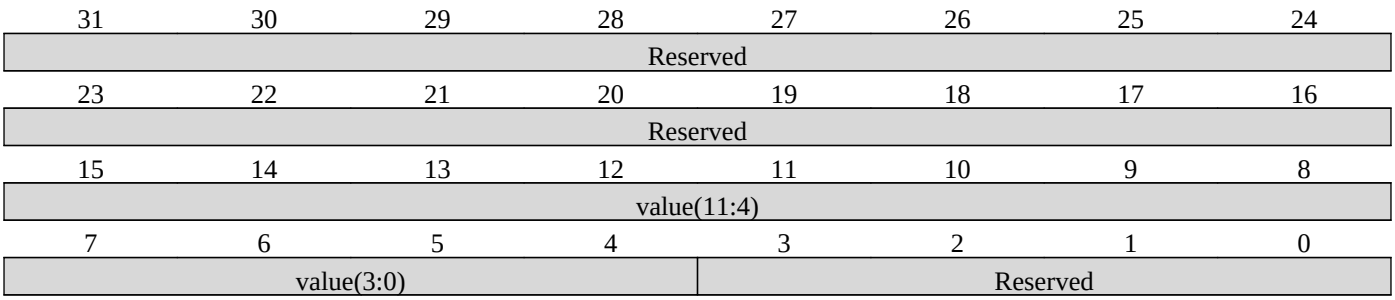
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Supply A offset value
RO	

adc_a_offset

Address: section "xadc_hard_macro" base address + 0x024

Description:
The calibration coefficient for the ADC A offset is stored at this location



value (11:0)	ADC A offset value
RO	

adc_a_gain

Address: section "xadc_hard_macro" base address + 0x028

Description:
The calibration coefficient for the ADC A gain error is stored at this location.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	sign	mag(5:0)					

sign *RO*	Gain sign	
Possible Values:	0x0	Negative gain
	0x1	Positive gain

mag (5:0) *RO*	Gain magnitude value

vcc_pint

Address: section "xadc_hard_macro" base address + 0x034

Description:
The result of a conversion on the PS supply, VCCPINT is stored in this register. The 12 MSBs correspond to the ADC transfer function shown in Figure 2-10, page 34. The data is MSB justified in the 16-bit register. The supply sensor is used when measuring VCCPINT.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Vcc Pint value
RO	

vcc_paux

Address: section "xadc_hard_macro" base address + 0x038

Description:
The result of a conversion on the PS supply, VCCPAUX is stored in this register. The 12 MSBs correspond to the ADC transfer function shown in Figure 2-10, page 34. The data is MSB justified in the 16-bit register. The supply sensor is used when measuring VCCPAUX.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Vcc Paux value
RO	

vcco_ddr

Address: section "xadc_hard_macro" base address + 0x03C

Description:
The result of a conversion on the PS supply, VCCO_DDR is stored in this register. The 12 MSBs correspond to the ADC transfer function shown in Figure 2-10, page 34. The data is MSB justified in the 16-bit register. The supply sensor is used when measuring VCCO_DDR.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Vcco DDR value
RO	

vaux_p_n (15:0)

Address: section "xadc_hard_macro" base address + 0x040 + (index * 0x4)

Description:
The results of the conversions on auxiliary analog input channels are stored in this register. The data is MSB justified in the 16-bit register. The 12 MSBs correspond to the transfer function shown in Figure 2-2, page 26 or Figure 2-3, page 27 depending on analog input mode settings.

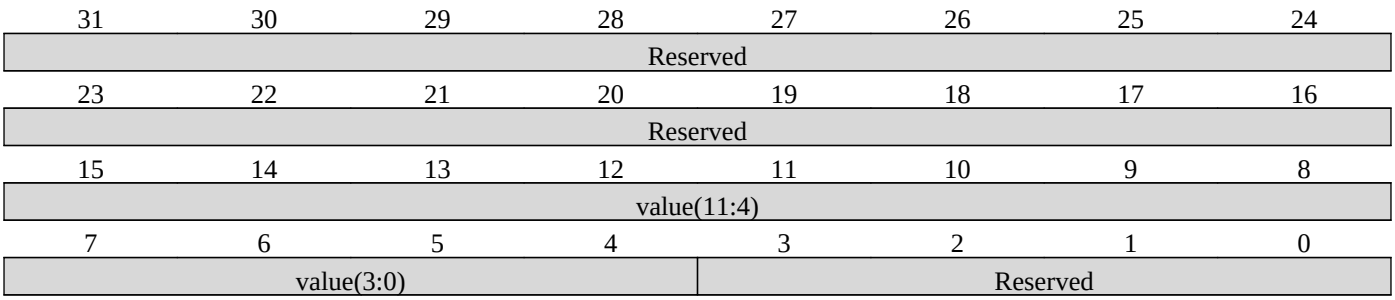
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Vaux_P/Vaux_N value
RO	

max_temperature

Address: section "xadc_hard_macro" base address + 0x080

Description:
Maximum temperature measurement recorded since power-up or the last XADC reset.



value (11:0)	Max temperature value
RO	

max_vcc_int

Address: section "xadc_hard_macro" base address + 0x084

Description:
Maximum VCCINT measurement recorded since power-up or the last XADC reset.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Max Vcc int value
RO	

max_vcc_aux

Address: section "xadc_hard_macro" base address + 0x088

Description:
Maximum VCCAUX measurement recorded since power-up or the last XADC reset

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Max Vcc int value
RO	

max_vcc_bram

Address: section "xadc_hard_macro" base address + 0x08C

Description:
Maximum VCCBRAM measurement recorded since power-up or the last XADC reset.

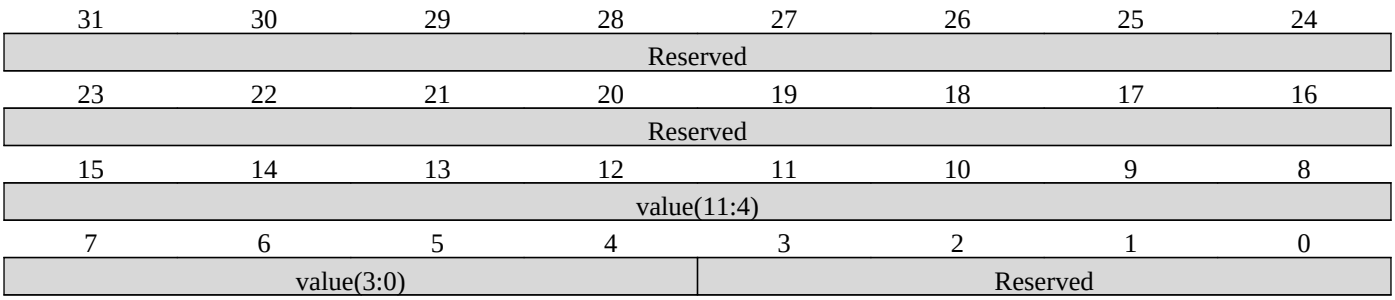
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Max Vcc int value
RO	

min_temperature

Address: section "xadc_hard_macro" base address + 0x090

Description:
Minimum temperature measurement recorded since power-up or the last XADC reset.



value (11:0)	Minimum temperature value
RO	

min_vcc_int

Address: section "xadc_hard_macro" base address + 0x094

Description:
Minimum VCCINT measurement recorded since power-up or the last XADC reset.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Minimum Vcc int value
RO	

min_vcc_aux

Address: section "xadc_hard_macro" base address + 0x098

Description:
Minimum VCCAUX measurement recorded since power-up or the last XADC reset.

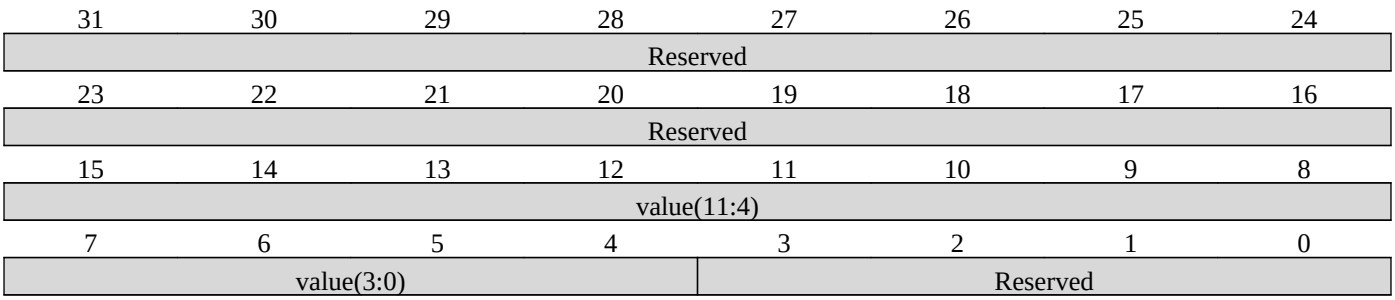
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Minimum Vcc int value
RO	

min_vcc_bram

Address: section "xadc_hard_macro" base address + 0x09C

Description:
Minimum VCCBRAM measurement recorded since power-up or the last XADC reset.



value (11:0)	Minimum Vcc int value
RO	

max_vcc_pint

Address: section "xadc_hard_macro" base address + 0x0A0

Description:
Maximum VCCPINT measurement recorded since power-up or the last XADC reset.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Max Vcc pint value
RO	

max_vcc_paux

Address: section "xadc_hard_macro" base address + 0x0A4

Description:
Maximum VCCPAUX measurement recorded since power-up or the last XADC reset.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Max_Vcc paux_value
RO	

max_vcco_ddr

Address: section "xadc_hard_macro" base address + 0x0A8

Description:
Maximum VCCO_DDR measurement recorded since power-up or the last XADC reset.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Max Vcco DDR value
RO	

min_vcc_pint

Address: section "xadc_hard_macro" base address + 0x0B0

Description:
Minimum VCCPINT measurement recorded since power-up or the last XADC reset.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Minimum Vcc pint value
RO	

min_vcc_paux

Address: section "xadc_hard_macro" base address + 0x0B4

Description:
Maximum VCCPAUX measurement recorded since power-up or the last XADC reset.

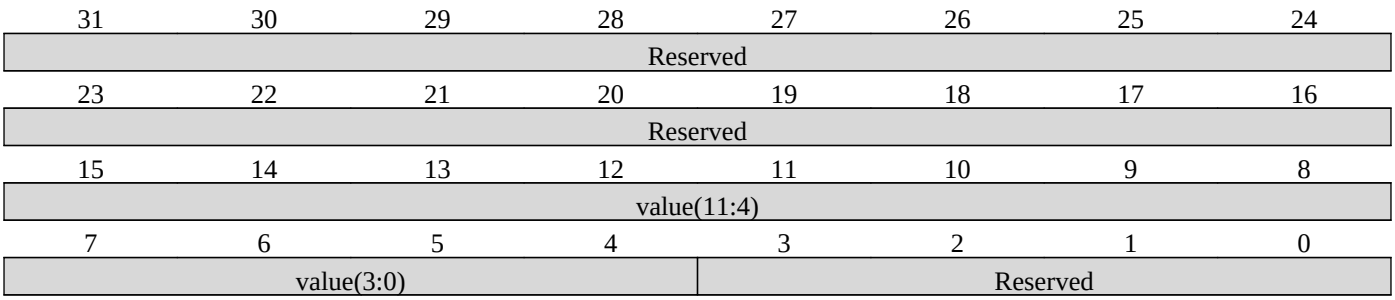
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Minimum Vcc paux value
RO	

main_vcco_ddr

Address: section "xadc_hard_macro" base address + 0x0B8

Description:
Maximum VCCO_DDR measurement recorded since power-up or the last XADC reset.



value (11:0)	Minimum Vcco DDR value
RO	

supply_b_offset

Address: section "xadc_hard_macro" base address + 0x0C0

Description:
The calibration coefficient for the supply sensor offset using ADC A is stored at this location.

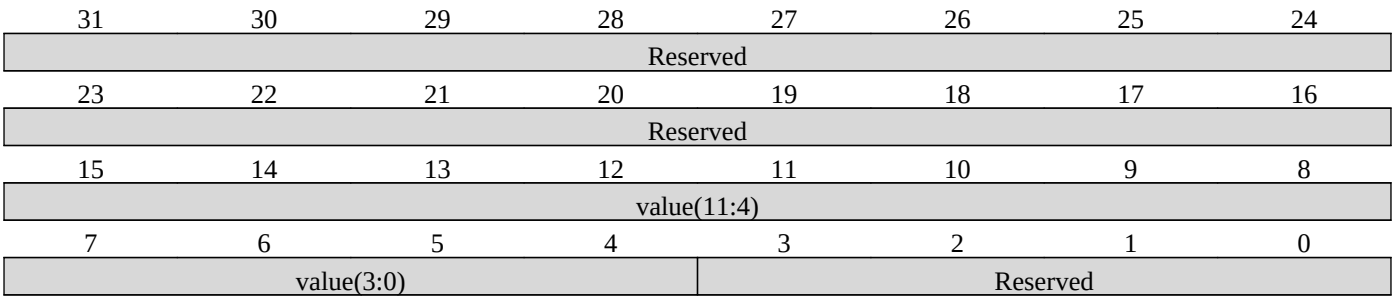
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	Supply A offset value
RO	

adc_b_offset

Address: section "xadc_hard_macro" base address + 0x0C4

Description:
The calibration coefficient for the ADC A offset is stored at this location



value (11:0)	ADC A offset value
RO	

adc_b_gain

Address: section "xadc_hard_macro" base address + 0x0C8

Description:
The calibration coefficient for the ADC A gain error is stored at this location.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	sign	mag(5:0)					

sign *RO*	Gain sign	
Possible Values:	0x0	Negative gain
	0x1	Positive gain

mag (5:0) *RO*	Gain magnitude value

flag

Address: section "xadc_hard_macro" base address + 0x0D4

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				jtgd	jtgr	ref	Reserved
7	6	5	4	3	2	1	0
alarm_6	alarm_5	alarm_4	alarm_3	over_temperature	alarm_2	alarm_1	alarm_0

jtgd	
RO	A logic 1 indicates that the JTAG_XADC bitstream option has been used to restrict JTAG access to read only. See DRP JTAG Interface for more information.

jtgr	
RO	A logic 1 indicates that the JTAG_XADC bitstream option has been used to disable all JTAG access. See DRP JTAG Interface for more information.

ref	ADC reference voltage	
RO	When this bit is a logic 1, the ADC is using the internal voltage reference. When this bit is a logic 0, the external reference is being used.	
Possible Values:	0x0	External reference voltage is used
	0x1	Internal reference voltage is used

alarm_6	Alarm 6 output
RO	These bits reflect the status of the alarm_6 output.

alarm_5	Alarm 5 output
RO	These bits reflect the status of the alarm_5 output.

alarm_4	Alarm 4 output output
RO	These bits reflect the status of the alarm_4 output.

alarm_3	Alarm 3 output
RO	These bits reflect the status of the alarm_3 output.

over_temperature	Over temperature output
RO	These bits reflect the status of the over temperature output.

alarm_2	Alarm 2 output
RO	These bits reflect the status of the alarm_2 output.

alarm_1	Alarm 1 output
RO	These bits reflect the status of the alarm_1 output.

alarm_0	Alarm 0 output
RO	These bits reflect the status of the alarm_0 output.

Address Range: [0x300 - 0x308]

Description:
The XADC has 32 control registers that are located at DRP addresses 40h to 5Fh (see Table 3-3). These registers are used to configure the XADC operation. All XADC functionality is controlled through these registers.
These control registers are initialized using the XADC attributes when the XADC is instantiated in a design. This means that the XADC can be configured to start in a predefined mode after FPGA configuration.

config_0

Address: section "control" base address + 0x000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
cavg	Reserved	avg(1:0)		mux	bu	ec	acq
7	6	5	4	3	2	1	0
Reserved			input_channel(4:0)				

cavg *RW*	Disable calculation averaging	
	This bit is used to disable averaging for the calculation of the calibration coefficients. Averaging is enabled by default (logic 0). To disable averaging, set this bit to logic 1. Averaging is fixed at 16 samples.	
Value at Reset:	0x0	
Possible Values:	0x0	Averaging enabled (default)
	0x1	Averaging disabled

avg (1:0) *RW*	Averaging	
	These bits are used to set the amount of sample averaging on selected channels in both single channel and sequence modes (see Table 3-8 and Chapter 4, XADC Operating Modes).	
Value at Reset:	0x0	
Possible Values:	0x0	No averaging
	0x1	Average 16 samples
	0x2	Average 64 samples
	0x3	Average 256 samples

mux *RW*	This bit should be set to a logic 1 to enable external multiplexer mode. See External Multiplexer Mode for more information.	
Value at Reset:	0x0	
Possible Values:	0x0	Internal Mux
	0x1	External mux

bu *RW*	This bit is used in single channel mode to select either unipolar or bipolar operating mode for the ADC analog inputs (see Analog Inputs, page 28). A logic 1 places the ADC in bipolar mode and a logic 0 places the ADC in unipolar mode.	
Value at Reset:	0x0	
Possible Values:	0x0	Unipolar mode
	0x1	Bipolar mode

ec *RW*	This bit is used to select either continuous or event-driven sampling mode for the ADC (see Chapter 5, XADC Timing). A logic 1 places the ADC in event-driven sampling mode and a logic 0 places the ADC in continuous sampling mode.	
Value at Reset:	0x0	
Possible Values:	0x0	Continuous sampling mode
	0x1	Event driven mode

acq *RW*	When using single channel mode, this bit is used to increase the settling time available on external analog inputs in continuous sampling mode by six ADCCLK cycles (see Chapter 2, Analog-to-Digital Converter and Chapter 5, XADC Timing). The acquisition time is increased by setting this bit to logic 1. (1)
Value at Reset:	0x0

input_channel (4:0) *RW*	ADC input channel When operating in single channel mode or external multiplexer mode, these bits are used to select the ADC input channel. See Table 3-7 for the channel assignments.	
Value at Reset:	0x0	
Possible Values:	0x0	On-chip temperature
	0x1	VCCINT
	0x2	VCCAUX
	0x3	VP , VN – Dedicated analog inputs
	0x4	VREFP (1.25V)
	0x5	VREFN (0V)
	0x6	VCCBRAM
	0x7	Invalid channel selection
	0x8	Carry out an XADC calibration
	0x9 - 0xC	Invalid channel selection
	0xD	VCCPINT
	0xE	VCCPAUX
	0xF	VCCO_DDR
	0x10	VAUXP[0], VAUXN[0] – Auxiliary
	0x11	VAUXP[1], VAUXN[1] – Auxiliary

config_1

Address: section "control" base address + 0x004

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
seq(3:0)				alarm_6_disable	alarm_5_disable	alarm_4_disable	alarm_3_disable
7	6	5	4	3	2	1	0
cal_enable_3	cal_enable_2	cal_enable_1	cal_enable_0	alarm_2_disable	alarm_1_disable	alarm_0_disable	ot_disable

seq (3:0)		
RW	These bits enable the channel-sequencer function. For the bit assignments, see Table 3-9. See Chapter 4, XADC Operating Modes, for more information.	
Value at Reset:	0x0	
Possible Values:	0x0	Default mode
	0x1	Single pass sequence
	0x2	Continuous sequence mode
	0x3	Single channel mode (seq uencer off)
	0x4	Simultaneous sampling mode
	0x5	Simultaneous sampling mode
	0x6	Simultaneous sampling mode
	0x7	Simultaneous sampling mode
	0x8	Independent ADC mode
	0x9	Independent ADC mode
	0xA	Independent ADC mode
	0xB	Independent ADC mode
	0xC	Independent ADC mode
	0xD	Default mode
	0xE	Default mode
	0xF	Default mode

alarm_6_disable	Alarm 6 disable	
RW	This is used to disable alarm 6 outputs. A logic 1 disables an alarm output.	
Value at Reset:	0x0	
Possible Values:	0x0	Alarm enabled
	0x1	Alarm disabled

alarm_5_disable	Alarm 5 disable	
RW	This is used to disable alarm 5 outputs. A logic 1 disables an alarm output.	
Value at Reset:	0x0	
Possible Values:	0x0	Alarm enabled
	0x1	Alarm disabled

alarm_4_disable	Alarm 4 disable	
RW	This is used to disable alarm 4 outputs. A logic 1 disables an alarm output.	
Value at Reset:	0x0	
Possible Values:	0x0	Alarm enabled
	0x1	Alarm disabled

alarm_3_disable	Alarm 3 disable	
RW	This is used to disable alarm 3 outputs. A logic 1 disables an alarm output.	
Value at Reset:	0x0	
Possible Values:	0x0	Alarm enabled
	0x1	Alarm disabled

cal_enable_3	Supply sensor offset and gain correction enable	
RW	This bit enable the application of the calibration coefficients to the ADC and on-chip supply sensor measurements. A logic 1 enables calibration and a logic 0 disables calibration. For bit assignments, see Table 3-10.	
Value at Reset:	0x0	
Possible Values:	0x0	Disable calibration
	0x1	Enable calibration

cal_enable_2	Supply sensor offset correction enable	
RW	This bit enable the application of the calibration coefficients to the ADC and on-chip supply sensor measurements. A logic 1 enables calibration and a logic 0 disables calibration. For bit assignments, see Table 3-10.	
Value at Reset:	0x0	
Possible Values:	0x0	Disable calibration
	0x1	Enable calibration

cal_enable_1	ADCs offset and gain correction enable	
RW	This bit enable the application of the calibration coefficients to the ADC and on-chip supply sensor measurements. A logic 1 enables calibration and a logic 0 disables calibration. For bit assignments, see Table 3-10.	
Value at Reset:	0x0	
Possible Values:	0x0	Disable calibration
	0x1	Enable calibration

cal_enable_0	ADCs offset correction enable	
RW	This bit enable the application of the calibration coefficients to the ADC and on-chip supply sensor measurements. A logic 1 enables calibration and a logic 0 disables calibration. For bit assignments, see Table 3-10.	
Value at Reset:	0x0	
Possible Values:	0x0	Disable calibration
	0x1	Enable calibration

alarm_2_disable	Alarm 2 disable	
RW	This is used to disable alarm 2 outputs. A logic 1 disables an alarm output.	
Value at Reset:	0x0	
Possible Values:	0x0	Alarm enabled
	0x1	Alarm disabled

alarm_1_disable	Alarm 0 disable	
RW	This is used to disable alarm 0 outputs. A logic 1 disables an alarm output.	
Value at Reset:	0x0	
Possible Values:	0x0	Alarm enabled
	0x1	Alarm disabled

alarm_0_disable	Alarm 0 disable	
RW	This is used to disable alarm 0 outputs. A logic 1 disables an alarm output.	
Value at Reset:	0x0	
Possible Values:	0x0	Alarm enabled
	0x1	Alarm disabled

ot_disable	Over temperature disable	
RW	This bit is used to disable the over-temperature signal. The alarm is disabled by setting this bit to logic 1.	
Value at Reset:	0x0	
Possible Values:	0x0	Over temperature signal enable
	0x1	Over temperature signal disable

config_2

Address: section "control" base address + 0x008

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
cd(7:0)							
7	6	5	4	3	2	1	0
Reserved		pd(1:0)		Reserved			

cd (7:0) *RW*	Clock division selection These bits select the division ratio between the DRP clock (DCLK) and the lower frequency ADC clock (ADCCLK) used for the ADC (see Chapter 5, XADC Timing). For bit assignments, see Table 3-12. Note : Minimum division ratio is 2, for example, ADCCLK = DCLK/2.	
Value at Reset:	0x1E	
Possible Values:	0x0 - 0x2	Divider value = 2
	0x3 - 0xFF	Divider value = field value

pd (1:0) *RW*	Power down selection Power-down bits for the XADC. The entire XADC block can be powered down permanently by setting PD1 = PD0 = 1. ADC B can also be powered down permanently by setting PD1 = 1 and PD0 = 0. See Table 3-11.	
Value at Reset:	0x0	
Possible Values:	0x0	Default. All XADC blocks powered up
	0x1	Not valid – do not select
	0x2	ADC B powered down
	0x3	XADC powered down

Section: alarm_tresholds

Address Range: [0x340 - 0x37C]

Description:
The XADC also generates an alarm signal on the logic outputs ALM[7:0] when an internal sensor measurement (Temperature, VCCINT, VCCAUX, VCCBRAM, VCCPINT, VCCPAUX, or VCCO_DDR) exceeds some user-defined thresholds. Only the values written to the status registers are used to generate alarms. If averaging has been enabled for a sensor channel, the averaged value is compared to the alarm threshold register contents. The alarm outputs are disabled by writing a 1 to bits ALM6 to ALM0 in configuration register 1. The alarm thresholds are stored in control registers 50h to 5Fh. Table 4-8 defines the alarm thresholds that are associated with specific control registers. The limits written to the threshold registers are MSB justified. Limits are derived from the temperature and power-supply sensor transfer functions (see Figure 2-9, page 33 and Figure 2-10, page 34).

temperature_upper — Temperature upper [alarm 0]

Address: section "alarm_tresholds" base address + 0x000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

vccint_upper VCCINT upper [alarm 1]

Address: section "alarm_tresholds" base address + 0x004

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

vccaux_upper VCCAUX upper [alarm 2]

Address: section "alarm_tresholds" base address + 0x008

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

ot_alarm_limit Over-temperature alarm limit

Address: section "alarm_tresholds" base address + 0x00C

Description:
OT alarm limit and OT alarm reset are described in Thermal Management section of Xiling UG480.

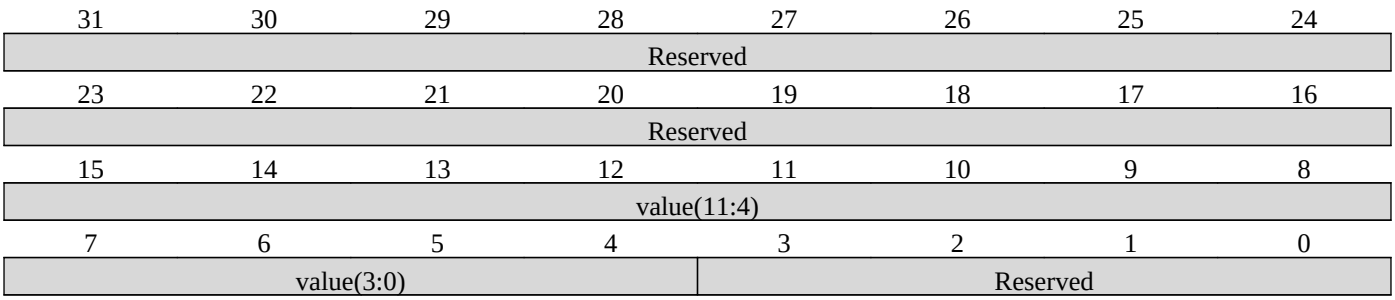
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

temperature_lower — OT alarm limit

Address: section "alarm_tresholds" base address + 0x010

Description:
OT alarm limit and OT alarm reset are described in Thermal Management section of Xiling UG480.



value (11:0)	
RW	
Value at Reset:	0x0

vccint_lower VCCINT lower [alarm 1]

Address: section "alarm_tresholds" base address + 0x014

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

vccaux_lower VCCAUX lower [alarm 2]

Address: section "alarm_tresholds" base address + 0x018

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

ot_alarm_reset Over-temperature alarm reset

Address: section "alarm_tresholds" base address + 0x01C

Description:
OT alarm limit and OT alarm reset are described in Thermal Management section of Xiling UG480.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

vccbram_upper VCCBRAM upper [alarm 3]

Address: section "alarm_tresholds" base address + 0x020

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

vccpint_upper VCCPINT upper [alarm 4]

Address: section "alarm_tresholds" base address + 0x024

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

vccpaux_upper VCCPAUX upper VCCBRAM lower [alarm 5]

Address: section "alarm_tresholds" base address + 0x028

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

vcco_ddr_upper VCCO DDR upper [alarm 6]

Address: section "alarm_tresholds" base address + 0x02C

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

vccbram_lower VCCBRAM lower [alarm 3]

Address: section "alarm_tresholds" base address + 0x030

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

vccpint_lower VCCPINT lower [alarm 4]

Address: section "alarm_tresholds" base address + 0x034

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

vccpaux_lower VCCPAUX lower [alarm 5]

Address: section "alarm_tresholds" base address + 0x038

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0

vcco_ddr_lower VCCO DDR lower [alarm 6]

Address: section "alarm_tresholds" base address + 0x03C

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(11:4)							
7	6	5	4	3	2	1	0
value(3:0)				Reserved			

value (11:0)	
RW	
Value at Reset:	0x0