ON Semiconductor

Create the XGS 12000 X-Celerator receiver block diagram in a Xilinx Vivado project

User Guide

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1 Disclaimer

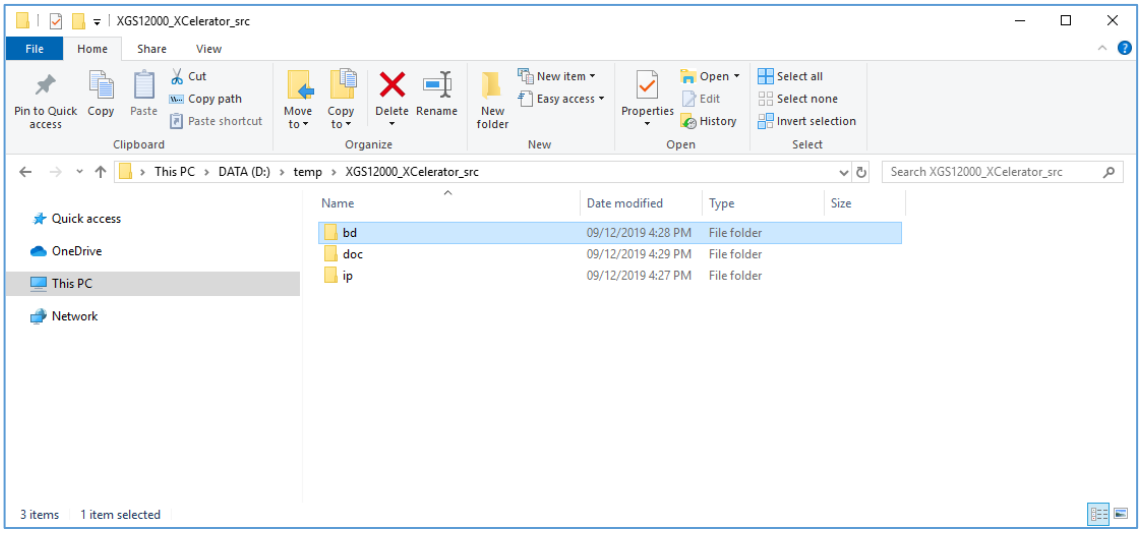
2 Description

This manual describes the steps to create a Xilinx Vivado project with the XGS12000 X-Celerator receiver block diagram. This project can be used by system developers as a starting point to integrate the different IP cores provided by On Semiconductor.

3 Project creation

3.1 Source files folder structure

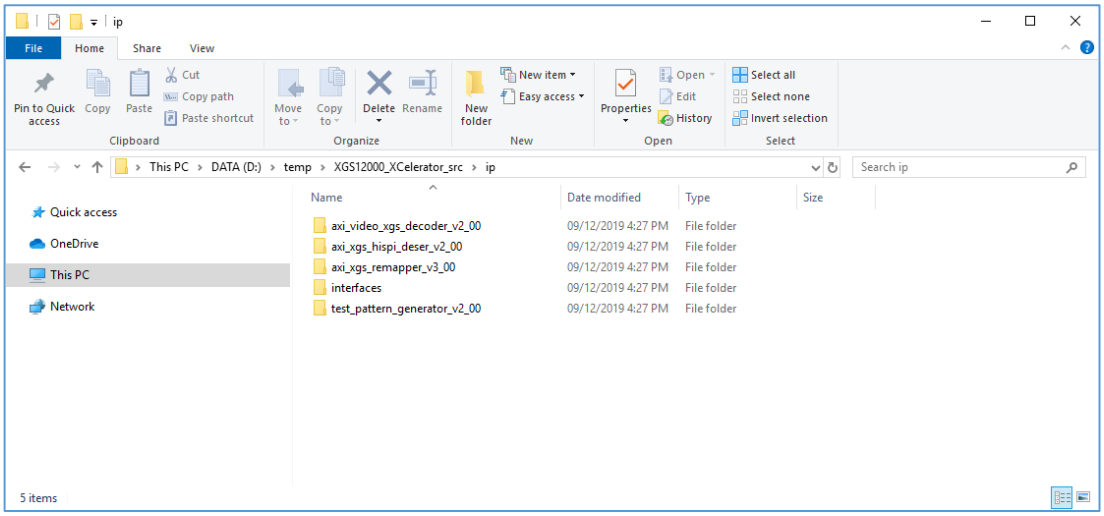
Extract the zip file, it will create a folder 'XGS12000_XCelerator_src', with some subfolders. This structure is mandatory to generate the project with the script.



The bd folder contains 2 files:

- BD_XGS12000_receiver.tcl : script to generate the block diagram
- create_XGS12000_XCelerator.tcl : script to generate the Vivado project, calling the BD script

The ip folder contains the IP cores and interfaces used in the block diagram.



3.2 Create Vivado project with block diagram

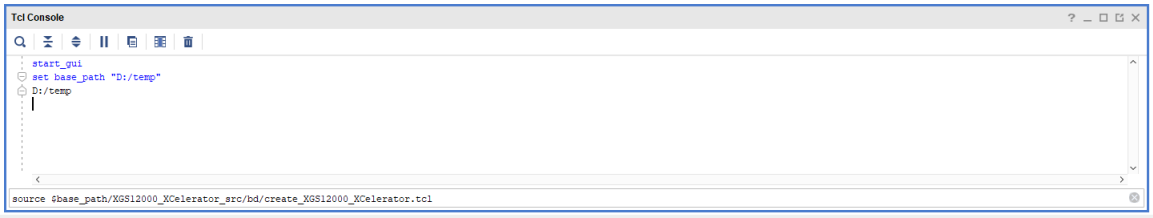
3.2.1 Start the Vivado software

Info: All development has been done with Vivado 2018.2

3.2.2 Execute the script

Enter this 2 lines in the Tcl Console:

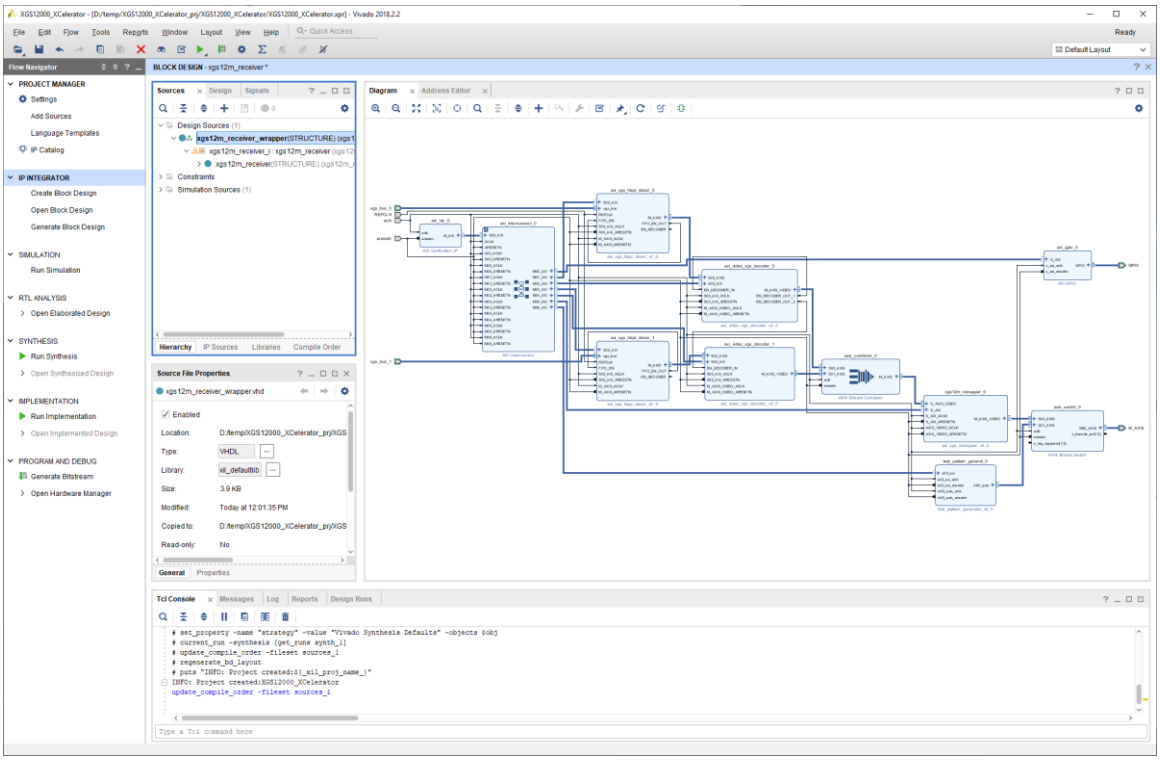
set base_path "D:/temp"
source $base_path/XGS12000_XCelerator_src/bd/create_XGS12000_XCelerator.tcl



Info: The base_path setting depends on the place where you stored the folder 'XGS12000_XCelerator_src' on your local drive.

Info: By default the Vivado project is generated in the folder "D:/temp/XGS12000_XCelerator_prj". In the project create script you can overrule this setting (line: set _xil_proj_dir_ "D:/temp/XGS12000_XCelerator_prj").

After execution of the script, a new project 'XGS12000_XCelerator' is created with the block diagram.



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