Register file structure : dma2tlp.pdf
Created by imaval on 2020/04/20 17:59:56
Register file CRC32 : 0xC8DD74C0

1. Main Parameters

Register file endianness: little endian
Address bus width: 8 bits
Data bus width: 32 bits

2. Memory Map

Section name	Address(es) / Address Ranges	Register name	Access Type
info	0x00	tag	R
	0x04	fid	R
	0x08	version	R
	0x0C	capability	R
	0x10	scratchpad	RW
dma	0x40	ctrl	RW
	0x44, 0x48	frame_start (1:0)	RW
	0x4C, 0x50	frame_start_g (1:0)	RW
	0x54, 0x58	frame_start_r (1:0)	RW
	0x5C	line_pitch	RW
	0x60	line_size	RW
	0x64	csc	RW
status	0xC0	active	R
	0xC4	debug	RW

Section: info

Address Range: [0x00 - 0x10]

tag

Address: section "info" base address + 0x00

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
value(23:16)							
15	14	13	12	11	10	9	8
value(15:8)							
7	6	5	4	3	2	1	0
value(7:0)							

value (23:0) *STATIC*	Tag identifier	
Value at Reset:	0x58544d	
Possible Values:	0x58544D	MTX ASCII string

fid — Matrox IP-Core Function ID

Address: section "info" base address + 0x04

31	30	29	28	27	26	25	24
value(31:24)							
23	22	21	20	19	18	17	16
value(23:16)							
15	14	13	12	11	10	9	8
value(15:8)							
7	6	5	4	3	2	1	0
value(7:0)							

value (31:0)	
STATIC	
Value at Reset:	0x0

version — Register file version

Address: section "info" base address + 0x08

Description:

Revisions

1.3.x : First functionnal revision with a single list of multiple Ethernet frames

1.4.x : Second revision. Implements multiple list of frames

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
major(7:0)							
15	14	13	12	11	10	9	8
minor(7:0)							
7	6	5	4	3	2	1	0
hw(7:0)							

major (7:0)	
STATIC	
Value at Reset:	0x1

minor (7:0)	
STATIC	
Value at Reset:	0x5

hw (7:0)	
RO	

capability Register file version

Address: section "info" base address + 0x0C

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
value(7:0)							

value (7:0)	
STATIC	
Value at Reset:	0x0

Address: section "info" base address + 0x10

31	30	29	28	27	26	25	24
value(31:24)							
23	22	21	20	19	18	17	16
value(23:16)							
15	14	13	12	11	10	9	8
value(15:8)							
7	6	5	4	3	2	1	0
value(7:0)							

value (31:0)	
RW	
Value at Reset:	0x0

Section: dma

Address Range: [0x40 - 0x70]

ctrl

Address: section "dma" base address + 0x00

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						grab_queue_enable	enable

grab_queue_enable		
RW		
Value at Reset:	0x0	
Possible Values:	0x0	Grab queue disabled
	0x1	Grab queue enabled

enable	
RW	
Value at Reset:	0x0

frame_start (1:0) Initial Grab Address Register

Address: section "dma" base address + 0x04 + (index * 0x4)

Description:
Initial Grab Address LOW 32 bits

31	30	29	28	27	26	25	24
value(31:24)							
23	22	21	20	19	18	17	16
value(23:16)							
15	14	13	12	11	10	9	8
value(15:8)							
7	6	5	4	3	2	1	0
value(7:0)							

value (31:0)	INitial GRAb ADDRess Register	
RW	This is the address in the host ram where the grab engine will start writing pixel data.	
Value at Reset:	N/A (Non-resettable flip-flops used)	
Possible Values:	Any Value	

frame_start_g (1:0) Green Grab Address Register

Address: section "dma" base address + 0x0C + (index * 0x4)

Description:
Grab Address LOW 32 bits for the Green plane. Only used when grabbing in Planar mode.

31	30	29	28	27	26	25	24
value(31:24)							
23	22	21	20	19	18	17	16
value(23:16)							
15	14	13	12	11	10	9	8
value(15:8)							
7	6	5	4	3	2	1	0
value(7:0)							

value (31:0)	GRAb ADDRess Register	
RW	This is the address in the host ram where the grab engine will start writing pixel data.	
Value at Reset:	N/A (Non-resettable flip-flops used)	
Possible Values:	Any Value	

frame_start_r (1:0) Red Grab Address Register

Address: section "dma" base address + 0x14 + (index * 0x4)

Description:
Grab Address LOW 32 bits for the Red plane. Only used when grabbing in Planar mode.

31	30	29	28	27	26	25	24
value(31:24)							
23	22	21	20	19	18	17	16
value(23:16)							
15	14	13	12	11	10	9	8
value(15:8)							
7	6	5	4	3	2	1	0
value(7:0)							

value (31:0)	GRAb ADDRess Register	
RW	This is the address in the host ram where the grab engine will start writing pixel data.	
Value at Reset:	N/A (Non-resettable flip-flops used)	
Possible Values:	Any Value	Any value

line_pitch — Grab Line Pitch Register

Address: section "dma" base address + 0x1C

Description:
Grab Line Pitch Register

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
value(15:8)							
7	6	5	4	3	2	1	0
value(7:0)							

value (15:0)	Grab LinePitch
RW	This is the line pitch when writing in ram. It is measured in bytes, not pixels.
Value at Reset:	N/A (Non-resettable flip-flops used)

line_size — Host Line Size Register

Address: section "dma" base address + 0x20

Description:

Host Line Size Register.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		value(13:8)					
7	6	5	4	3	2	1	0
value(7:0)							

value (13:0) *RW*	Host Line size This is the line size when writing in host ram. It is measured in bytes, not pixels. If this register is higher than the actual data provided by the sensor, stray data will be written into host memory. If this register is lower than the data provided by the sensor, image data will be cropped at the end of the line. For backward compatibility, the value of 0 indicates that the FPGA should auto-compute the line sized based on data provided by the sensor interface.	
Value at Reset:	0x0	
Possible Values:	0x1 - 0x3FFF	Written line size in host frame.
	0x0	Auto-compute line size from sensor data.

Address: section "dma" base address + 0x24

31	30	29	28	27	26	25	24
Reserved					COLOR_SPACE(2:0)		
23	22	21	20	19	18	17	16
DUP_LAST_ LINE	Reserved						MONO10
15	14	13	12	11	10	9	8
Reserved						reverse_y	GRAB_REVX
7	6	5	4	3	2	1	0
Reserved							

COLOR_SPACE (2:0)		
RW	Output color space used to transfer data to the DMA engine.	
Value at Reset:	0x0	
Possible Values:	0x0	Reserved for Mono sensor operation
	0x1	BGR32
	0x2	YUV 4:2:2 in full range
	0x3	Planar 8-bits
	0x4	Reserved for Y only with color sensor
	0x5	RAW color pixels (8bpp or 10bpp selected with MONO10 regsiter)

DUP_LAST_LINE		
RW	This field is used to enable the duplicate last line feature. When turned on, the datapath will regenerate the last line when it receives the end of frame marker from the acquisition section. The goal of this feature is to compensate for the lost line during the Bayer demosaic processing.	
Value at Reset:	0x0	
Possible Values:	0x0	normal processing
	0x1	last line is duplicated

MONO10		
RW	For monochrome sensors, this bit is used to select between 8-bit mode and 10-bit mode. This is a construction register since the 10-bit mode is not part of the product requirement. We want to qualify the noise reduction algorithm in 10 bits. This bit may move of its behavior may change.	
Value at Reset:	0x0	
Possible Values:	0x0	Mono is in 8 bits
	0x1	Mono is in 10 bits

reverse_y	REVERSE Y	
RW	Reverse readout	
Value at Reset:	0x0	
Possible Values:	0x0	Bottom to top readout
	0x1	Top to bottom readout

GRAB_REVX	
RW	
Value at Reset:	0x0

Section: status

Address Range: [0xC0 - 0xC4]

active

Address: section "status" base address + 0x00

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							busy

busy	
RO	

debug

Address: section "status" base address + 0x04

Description:
FOR DEBUG

31	30	29	28	27	26	25	24
GRAB_MAX_ADD(29:22)							
23	22	21	20	19	18	17	16
GRAB_MAX_ADD(21:14)							
15	14	13	12	11	10	9	8
GRAB_MAX_ADD(13:6)							
7	6	5	4	3	2	1	0
GRAB_MAX_ADD(5:0)						OUT_OF_MEMORY_CLEAR	OUT_OF_MEMORY_STAT

GRAB_MAX_ADD (29:0)	
RW	
Value at Reset:	0x3fffffff

OUT_OF_MEMORY_CLEAR	
WO/AutoClr	

OUT_OF_MEMORY_STAT	
RO	