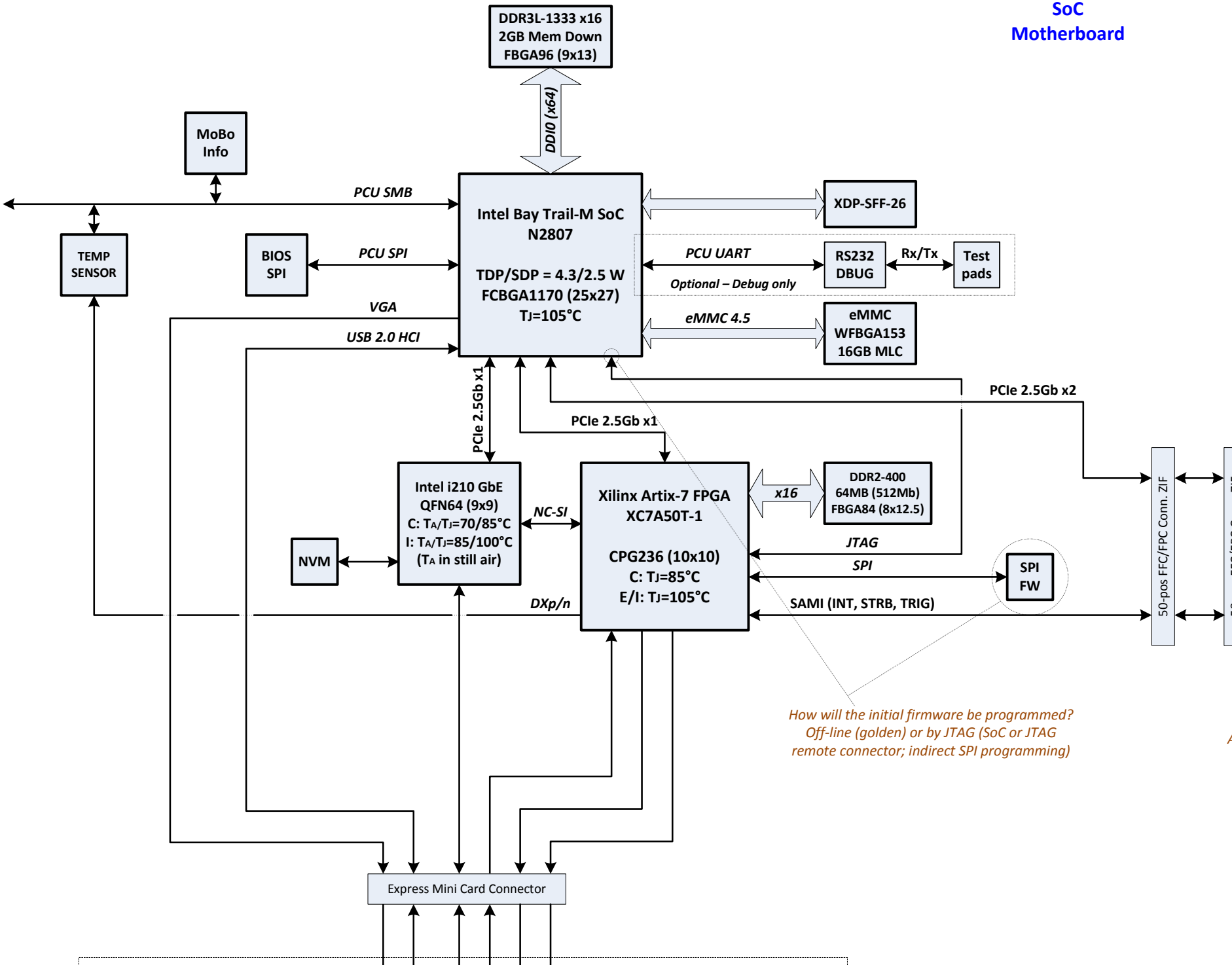
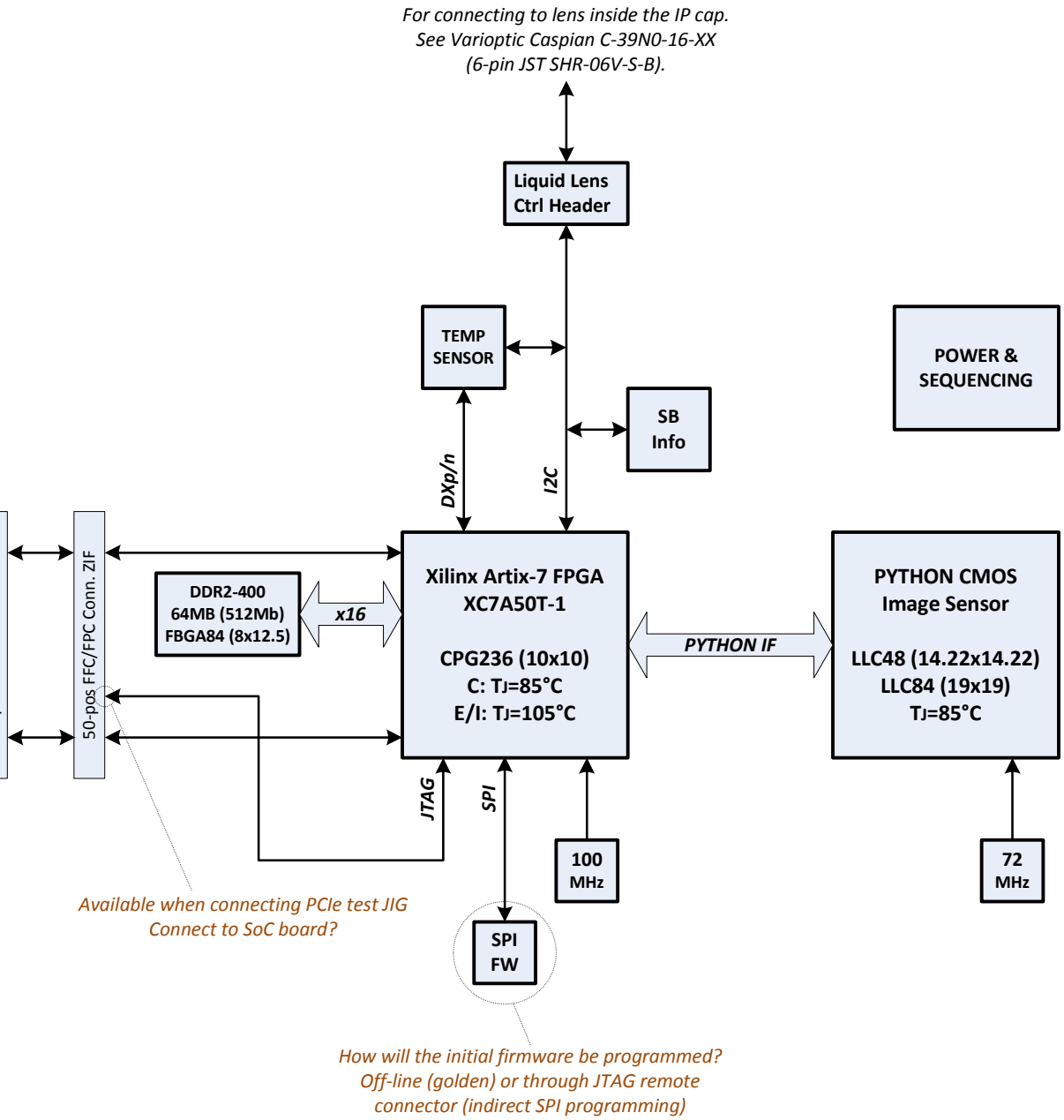
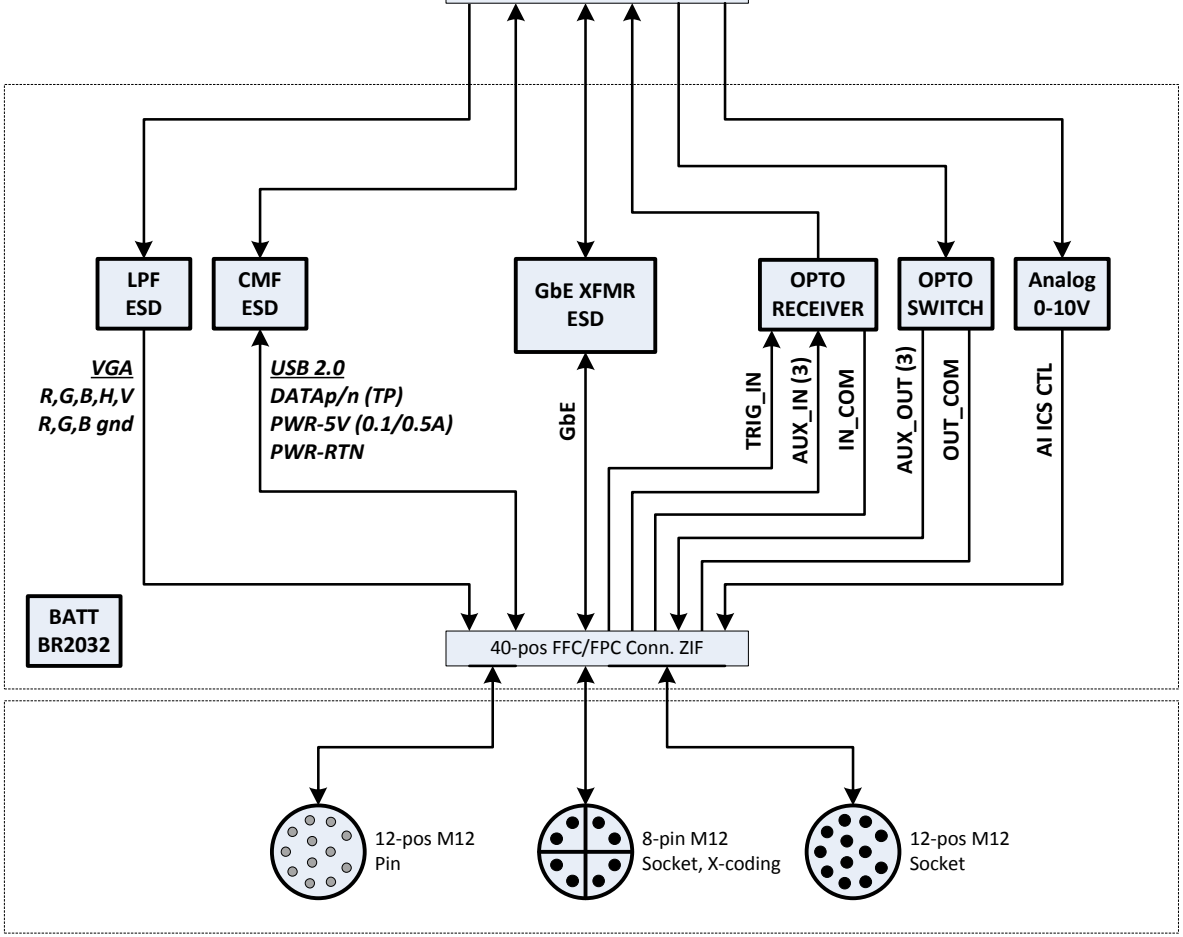

SoC
Motherboard
DDR3L-1333 x16
2GB Mem Down
FBGA96 (9x13)
DDI0 (x64)
MoBo
Info
PCU SMB
TEMP
SENSOR
BIOS
SPI
PCU SPI
Intel Bay Trail-M SoC
N2807
TDP/SDP = 4.3/2.5 W
FCBGA1170 (25x27)
TJ=105°C
XDP-SFF-26
PCU UART
Optional – Debug only
RS232
DBUG
Rx/Tx
Test
pads
VGA
USB 2.0 HCI
eMMC 4.5
eMMC
WFBGA153
16GB MLC
PCIe 2.5Gb x1
PCIe 2.5Gb x2
PCIe 2.5Gb x1
Intel i210 GbE
QFN64 (9x9)
C: TA/TJ=70/85°C
I: TA/TJ=85/100°C
(TA in still air)
NC-SI
Xilinx Artix-7 FPGA
XC7A50T-1
CPG236 (10x10)
C: TJ=85°C
E/I: TJ=105°C
x16
DDR2-400
64MB (512Mb)
FBGA84 (8x12.5)
JTAG
SPI
SPI
FW
NVM
DXp/n
SAMI (INT, STRB, TRIG)
50-pos FFC/FPC Conn. ZIF
How will the initial firmware be programmed?
Off-line (golden) or by JTAG (SoC or JTAG
remote connector; indirect SPI programming)
Express Mini Card Connector

Python Sensor Board



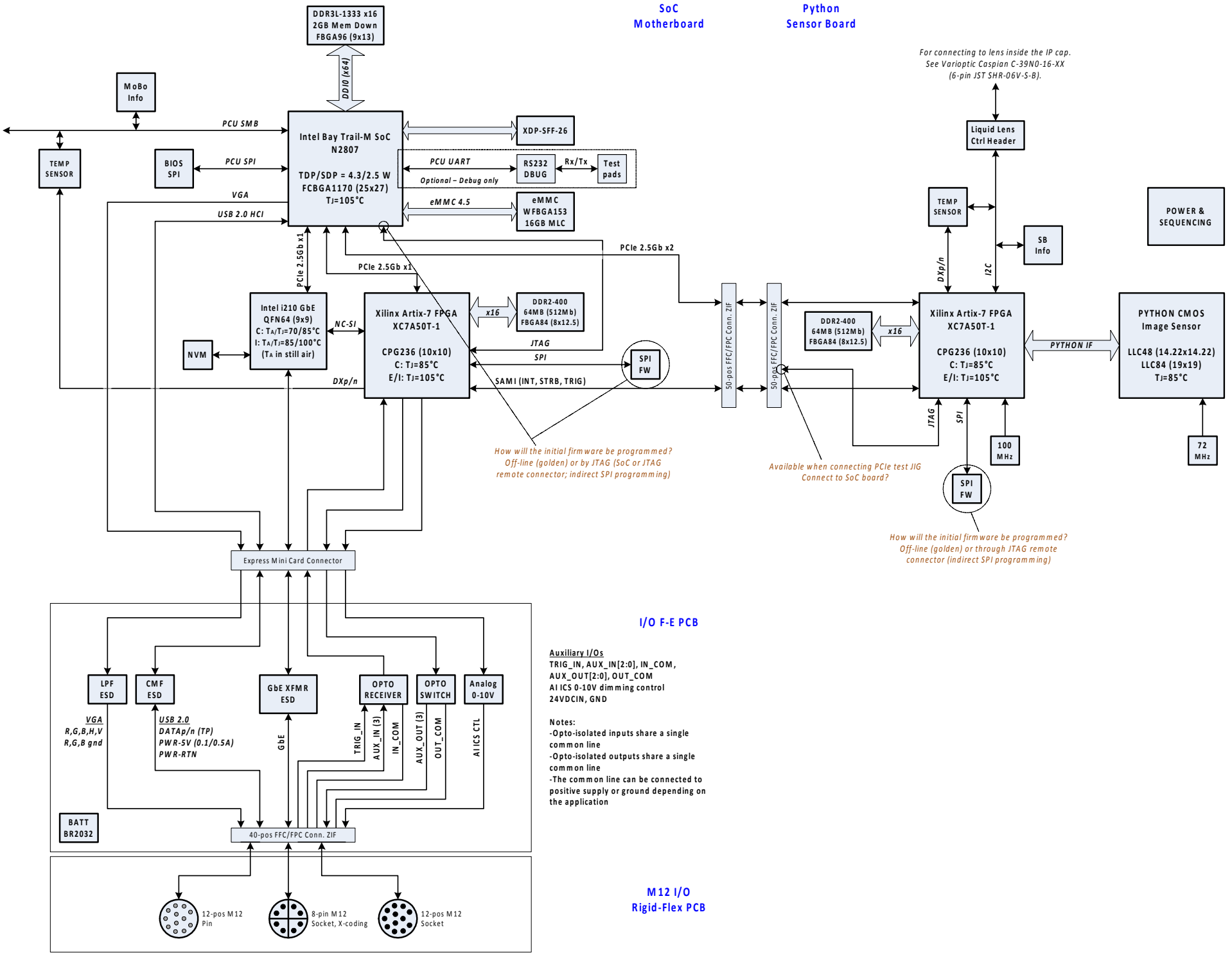


I/O F-E PCB

Auxiliary I/Os
TRIG_IN, AUX_IN[2:0], IN_COM, AUX_OUT[2:0], OUT_COM
AI ICS 0-10V dimming control
24VDCIN, GND

Notes:
-Opto-isolated inputs share a single common line
-Opto-isolated outputs share a single common line
-The common line can be connected to positive supply or ground depending on the application

M12 I/O Rigid-Flex PCB


SoC
Motherboard
Python
Sensor Board
DDR3L-1333 x16
2GB Mem Down
FBGA96 (9x13)
DDI0 (x64)
MoBo
Info
PCU SMB
TEMP
SENSOR
BIOS
SPI
PCU SPI
VGA
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Intel i210 GbE
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(TA in still air)
NC-SI
NVM
Xilinx Artix-7 FPGA
XC7A50T-1
CPG236 (10x10)
C: TJ=85°C
E/I: TJ=105°C
x16
DDR2-400
64MB (512Mb)
FBGA84 (8x12.5)
JTAG
SPI
SPI
FW
SAMI (INT, STRB, TRIG)
DXp/n
How will the initial firmware be programmed?
Off-line (golden) or by JTAG (SoC or JTAG
remote connector; indirect SPI programming)
50-pos FFC/FPC Conn. ZIF
50-pos FFC/FPC Conn. ZIF
For connecting to lens inside the IP cap.
See Varioptic Caspian C-39N0-16-XX
(6-pin JST SHR-06V-S-B).
Liquid Lens
Ctrl Header
TEMP
SENSOR
SB
Info
POWER &
SEQUENCING
DXp/n
I2C
DDR2-400
64MB (512Mb)
FBGA84 (8x12.5)
x16
Xilinx Artix-7 FPGA
XC7A50T-1
CPG236 (10x10)
C: TJ=85°C
E/I: TJ=105°C
PYTHON IF
PYTHON CMOS
Image Sensor
LLC48 (14.22x14.22)
LLC84 (19x19)
TJ=85°C
JTAG
SPI
100
MHz
72
MHz
Available when connecting PCIe test JIG
Connect to SoC board?
SPI
FW
How will the initial firmware be programmed?
Off-line (golden) or through JTAG remote
connector (indirect SPI programming)
Express Mini Card Connector
I/O F-E PCB
LPF
ESD
CMF
ESD
GbE XFMR
ESD
OPTO
RECEIVER
OPTO
SWITCH
Analog
0-10V
VGA
R,G,B,H,V
R,G,B gnd
USB 2.0
DATAp/n (TP)
PWR-5V (0.1/0.5A)
PWR-RTN
GbE
TRIG_IN
AUX_IN (3)
IN_COM
AUX_OUT (3)
OUT_COM
AI ICS CTL
BATT
BR2032
40-pos FFC/FPC Conn. ZIF
Auxiliary I/Os
TRIG_IN, AUX_IN[2:0], IN_COM,
AUX_OUT[2:0], OUT_COM
AI ICS 0-10V dimming control
24VDCIN, GND
Notes:
-Opto-isolated inputs share a single
common line
-Opto-isolated outputs share a single
common line
-The common line can be connected to
positive supply or ground depending on
the application
12-pos M12
Pin
8-pin M12
Socket, X-coding
12-pos M12
Socket
M12 I/O
Rigid-Flex PCB