AND9559/D

High-Speed Serial Pixel (HiSPi) Physical Layer 3.0

PHY Specification for CMOS Image Sensors

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APPLICATION NOTE

INTRODUCTION

Overview

With the advent of high performance CMOS image sensors and the increased demand for higher image quality and capturing speed, the large bandwidth requirements can no longer be met by the traditional low speed parallel CMOS interfaces.

To overcome this new reality Aptina developed an open access high speed serial interface – High Speed Serial Pixel Interface (HiSPi). HiSPi is a low power, source-synchronous DDR interface with a low pin count and reduced EMI emissions that supports the bandwidth requirements of the most stringent imaging applications.

A typical HiSPi physical layer link consists of a differential clock lane and between one and four unidirectional data lanes. Depending on the bandwidth requirements a product may use more than one HiSPi link.

Each lane comprises one line driver and serializing logic (TX), one line receiver and de-serializing logic (RX) and a transmission line interconnect system (TLIS) between the two. All previous elements are impedance matched for optimum signal integrity.

No external components are required in a HiSPi link as both the transmitter and receiver include all the necessary terminations on-chip.

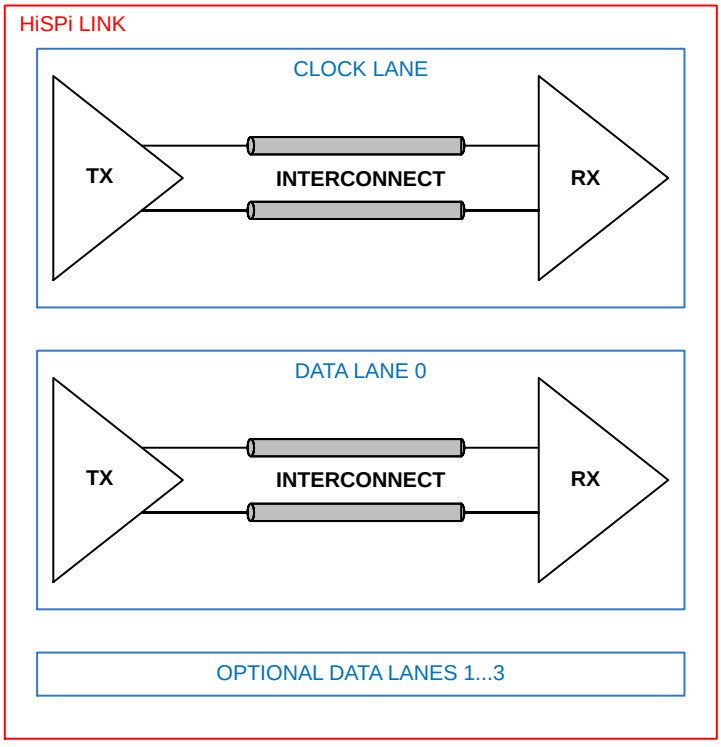

Figure 1. HiSPi Link Generic Configuration

Clock and Data streams are transmitted in quadrature to simplify data recovery on the receiving end. Usually direct sampling of the data with the received clock is possible but this does not preclude the use of additional de-skewing and retiming mechanisms to improve timing margins. If existent these mechanisms are application and/or product specific and their operation and characteristics are beyond the scope of this specification.

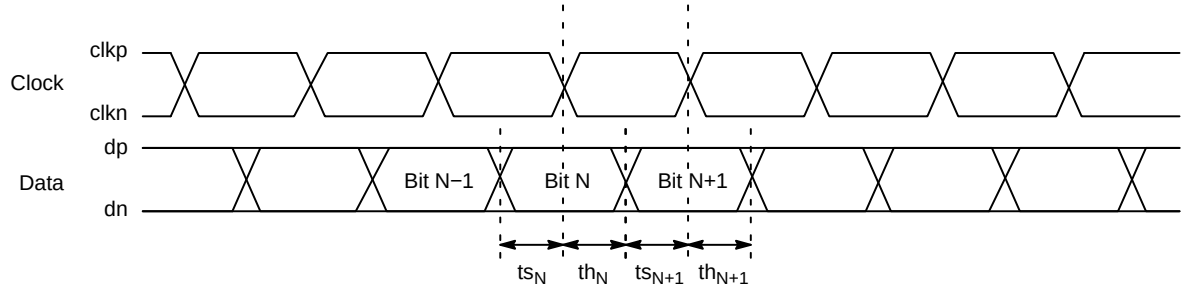

Figure 2. Quadrature Alignment between Clock and Data

Where multiple HiSPi instances are present, the phase relationship between any two PHYs should not be assumed fixed and may vary by up to $\pm t_{PHYSKEW}$ during normal operation.

There are two electrical interface standards outlined in this specification:

- Scalable Low Voltage Signalling (SLVS−200). This interface is a low amplitude, low common-mode voltage interface.
- SubLVDS. This interface is also a low amplitude but higher common mode voltage (typically 0.9 V) interface.

Any given HiSPi implementation must adopt at least one of these electrical standards.

ELECTRICAL SPECIFICATIONS

Table 1. LINK COMMON SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit
TIMING PARAMETERS					
DDR Clock High/Low Pulse	t_{HCLK}, t_{LCLK}		T/2		
DDR Clock Duty Cycle	DCYC	45	50	55	%
Bit Error Rate	BER	$1e^{-9}$			

Clock Signal

t_{HCLK} is defined as the high clock pulse, and t_{LCLK} is defined as the low clock pulse as shown in Figure 3. DCYC is defined as the clock duty cycle and represents the percentage of time the clock is high (t_{HCLK}) compared with the clock period T.

$$D_{CYC} = \frac{t_{HCLK}}{T} \quad \text{(eq. 1)}$$

$$t_{pw} \text{ or } 1 = \frac{T}{2} \quad \text{(eq. 2)}$$

$$\text{Bitrate} = \frac{1}{t_{pw}} \quad \text{(eq. 3)}$$

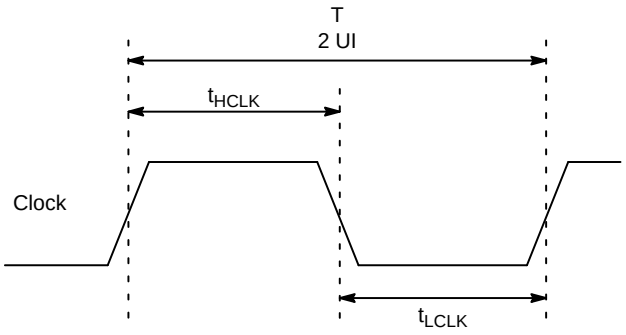

Figure 3. Clock Duty Cycle

Transmitter

Common Specifications

Table 2. COMMON SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit
TIMING PARAMETERS					
Zero Crossing Eye Width (Note 1)	t_{EYE_ZERO}	0.6			UI
Clock to Data Skew (Notes 1, 2)	t_{CHSKEW}	−0.2		0.2	UI
PHY-to-PHY Skew (Note 3)	$\|t_{PHYSKEW}\|$			2.2	UI
Mean Differential Skew (Note 4)	$t_{DIFFSKEW}$	−100		100	ps
AC PARAMETERS					
Single Ended Output Overshoot Peak (Note 6)	VOD_AC			1.15 × |VOD|	
Differential Output Peak to Peak (Note 6)	V_{DIFF_PKPK}			2.3 × |VOD|	
Output Common Mode Variation (Note 7)	V_{CM_AC}			50	mV
Output Pin Capacitance (Note 8)	C_{TX_PIN}			2.75	pF
DC PARAMETERS					
Output Leakage Current when Tri-state	I_{OUTZ}			10	μA

1. Taken from the 0 V differential crossing point.
2. Measured between Clock lane and any Data Lane in the same PHY; includes clock duty cycle, mean skew and total peak jitter at BER of 1E−9.
3. The absolute skew between any Clock lane in one PHY and any Data lane in other PHY between any two edges. The value is presented as a guideline and not a strict requirement, it can be relaxed when interfacing receivers with robust timing adjustment mechanisms.
4. Differential skew is defined as the skew between complementary outputs. It is measured as the time difference between the two complementary edges at mean VCM point. The parameter is closely related with V_{CM_AC} which must also be met.
5. Time required for outputs to go from any standby state to valid data/clock electrical levels.
6. Limits include effects of Min/Max Rx termination.
7. No center tap capacitance assumed at load.
8. The overall pin capacitance is defined by the driver output circuitry, bondpad and internal ESD protections. This value allows mainstream wire bond packages to be used while achieving the required performance across the complete link.

Clock to Data Skew

Clock-to-Data skew must be measured from the 0 V crossing point on Clock to the 0 V crossing point on any Data channel regardless of edge, as shown in Figure 4. This time is compared with the ideal Data transition point of 0.5 UI with the difference being the Clock-to-Data Skew (see Equation 4).

$$t_{CHSKEW}(ps) = \Delta t - \frac{t_{pw}}{2} \quad \text{(eq. 4)}$$

$$t_{CHSKEW}(UI) = \frac{\Delta t}{t_{pw}} - 0.5 = t_{MEANSKEW}(UI) \pm \frac{t_{TOTALJIT}(UI)}{2} \quad \text{(eq. 5)}$$

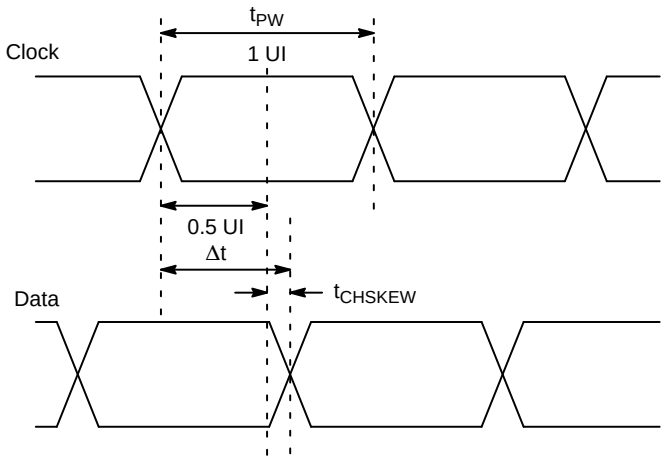

Figure 4. Clock-to-Data Skew Timing Diagram

Note that channel skew (t_{CHSKEW}) has the average mean skew ($t_{MEANSKEW}$) plus the peak total jitter ($\pm t_{TOTALJIT}/2$). These can be measured separately although the present specification only constraints the overall channel skew which is the ultimate parameter of interest for source synchronous interfaces.

Standby

When disabled the HiSPi transmitter outputs should transition into at least one of the following states:

- Tri-State (High impedance);
- All low (Low impedance to ground for p/n outputs);
- Locked Differential (Static differential output);

Which state(s) to support is application specific but it is expected that any compliant receiver will be able to withstand any of these states without compromising the proper operation of the link when normal streaming is resumed.

SLVS−200 Specifications

Table 3. SLVS−200 SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit
TIMING PARAMETERS					
Data Bit Rate (Notes 9, 10)	$1/t_{PW}$	200		1000	Mbps
DDR Clock Period (Note 10)	T	2		10	ns
Plateau Eye Width	$t_{EYE\_PLATEAU}$	0.35			UI
Rise Times (20% −80%) (Note 11)	t_R	150			ps
Fall Time (20% −80%) (Note 11)	t_F	150			ps
DC PARAMETERS					
SLVS DC Mean Common Mode Voltage (Note 12)	V_{CM}	155	200	250	mV
SLVS DC Mean Differential Output Voltage (Note 12)	$\|V_{OD}\|$	130	200	280	mV
Difference in V_{CM} between any Two Channels	$\|\Delta V_{CM}\|$			30	mV
Difference in V_{OD} between any Two Channels	$\|\Delta V_{OD}\|$			50	mV
Change in VCM between Logic 1 and 0	$\|\Delta V_{CM}\|_{0,1}$			25	mV
Change in |VOD| between Logic 1 and 0	$\|\Delta V_{OD}\|_{0,1}$			25	mV
Single-ended Output Impedance	R_O	40	50	70	Ω
Output Impedance Mismatch (Pullup vs. Pulldown)	ΔR_O			20	%

9. Equivalent to 1/UI where UI is the normalized mean time between consecutive clock edges.
10. Transmitters and Receivers are not required to support the full range of bit rates and related clock frequencies; any sub range is acceptable as long as the limits specified are not exceeded.
11. Rise and fall times measured between 20% to 80% positions on the differential waveform, as shown in Figure 8. The output signals must also meet the eye diagram mask which implicitly defines the maximum rise and fall times.
12. Limits include effects of Min/Max Rx termination.

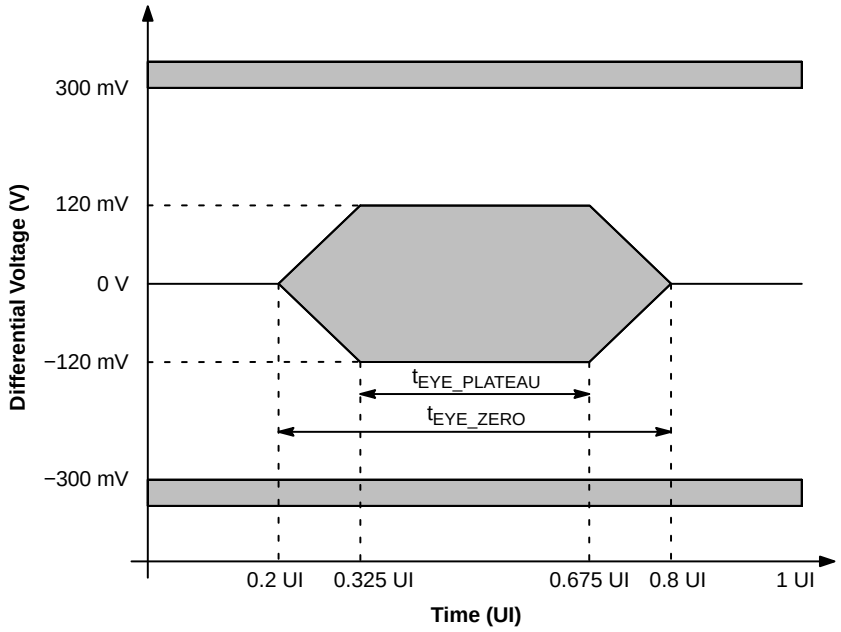

Figure 5. SLVS TX Eye Diagram Mask

SubLVDS Specifications

Table 4. SUBLVDS SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit
TIMING PARAMETERS					
Data Bit Rate (Note 13, 14)	$1/t_{PW}$	200		800	Mbps
DDR Clock Period (Note 14)	T	2.5		10	ns
Plateau Eye Width	$t_{EYE\_PLATEAU}$	0.35			UI
Rise Times (20% −80%) (Note 15)	t_R	150			ps
Fall Time (20% −80%) (Note 15)	t_F	150			ps
DC PARAMETERS					
SubLVDS DC Mean Common Mode Voltage (Note 16)	V_{CM}	750	900	1050	mV
SubLVDS DC Mean Differential Output Voltage (Note 16)	$\|V_{OD}\|$	100	150	200	mV
Difference in V_{CM} between any Two Channels	$\|\Delta V_{CM}\|$			50	mV
Difference in V_{OD} between any Two Channels	$\|\Delta V_{OD}\|$			50	mV
Change in VCM between Logic 1 and 0	$\|\Delta V_{CM}\|_{0,1}$			25	mV
Change in VOD between Logic 1 and 0	$\|\Delta V_{OD}\|_{0,1}$			25	mV
Single-ended Output Impedance	R_O	40		100	Ω
Output Impedance Mismatch (Pullup vs. Pulldown)	ΔR_O			20	%

13. Equivalent to 1/UI where UI is the normalized mean time between consecutive clock edges.
14. Transmitters and Receivers are not required to support the full range of bit rates and related clock frequencies; any sub range is acceptable as long as the limits specified are not exceeded.
15. Rise and fall times measured between 20% to 80% positions on the differential waveform, as shown Figure 8. The output signals must also meet the eye diagram mask which implicitly defines the maximum rise and fall times.
16. Limits include effects of Min/Max Rx termination.

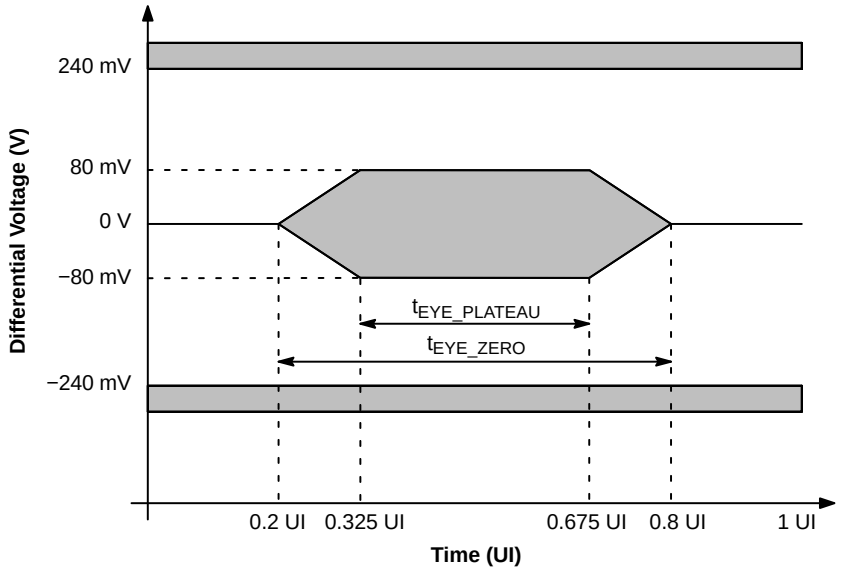

Figure 6. SubLVDS TX Eye Diagram Mask

Figure 5 and Figure 6 illustrate the eye diagram masks that must be met by a compliant transmitter while driving a nominal 100 Ω differential load with more than 20 dB return loss between DC and 1.5 × BaudRate. The grey areas represent keep out zones with the vertical limits defined by the stabilized differential output voltage values with additional margin for noise (supply, EMI, reflections, …).

The eye diagram mask applies to both clock and data streams. The former requires the measure to be performed with a maximum frequency square waveform pattern with no fixed timing reference, i.e the eye mask can be time shifted to better fit the superimposed pattern. The later requires a PRBS9 pattern to be transmitted with the clock lane serving as timing reference for the capture. This

reference shall be shifted by 0.5 UI to offset the intrinsic quadrature relation between data and clock, this can be achieved directly on the oscilloscope or by any other equivalent post processing method.

Voltage Levels and Slew Times

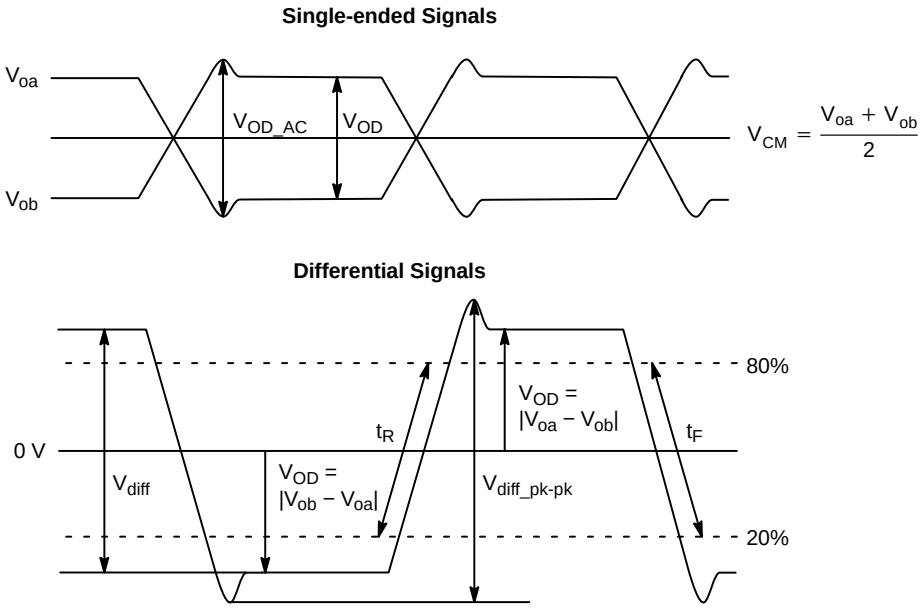

Figure 7. Voltage and Slew Times for Single-ended and Differential Signals

Differential Skew

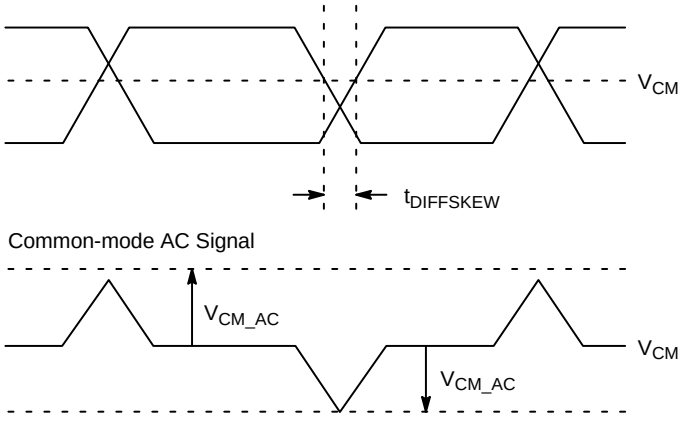

Figure 8. Differential Skew

The differential skew is measured on the two single-ended signals for any channel. The time is taken from a transition on V_{oa} signal to corresponding transition on V_{ob} signal at V_{CM} crossing point. Figure 8 also shows the corresponding AC V_{CM} common-mode signal. Differential skew between the V_{oa} and V_{ob} signals can cause spikes in the common-mode which the receiver needs to be able to reject. V_{CM_AC} is measured as the absolute peak deviation from the mean DC V_{CM} common-mode.

Receiver

Common Specifications

Table 5. COMMON SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit
TIMING PARAMETERS					
Setup Time (Note 17)	t_{SETUP}	0.15			UI
Hold Time (Note 17)	t_{HOLD}	0.15			UI
Zero Crossing Eye Width (Note 18)	t_{EYE_ZERO}	0.3			UI
AC PARAMETERS					
Load Capacitance per Pin (Note 19)	C_{RX_PIN}			2.5	pF
DC PARAMETERS					
Termination Load Resistance	R_L	80	100	125	Ω

17. Setup/Hold times are measured from zero crossings of data to/from clock when both are compliant with the specified receiver eye masks.
18. Taken from the 0 V differential crossing points.
19. The overall pin capacitance is defined by the receiver input circuitry, bondpad and internal ESD protections. This value allows mainstream wire bond packages to be used while achieving the required performance across the complete link.

SLVS−200 Specifications

Table 6. SLVS−200 SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit
TIMING PARAMETERS					
Data Bit Rate (Notes 20, 21)	$1/t_{PW}$	200		1000	Mbps
DDR Clock Period (Note 21)	T	2		10	ns
Plateau Eye Width	$t_{EYE\_PLATEAU}$	0.2			UI
DC PARAMETERS					
Input Voltage Receiver Range (Note 22)	V_{IN_DC}	−45		450	mV
Input Common-mode Receiver Range (Notes 22, 23)	V_{CMRX}	55		350	mV
Receiver Differential Input Voltage	$\|V_{ID}\|$	70			mV

20. Equivalent to 1/UI where UI is the normalized mean time between consecutive clock edges.
21. Transmitters and Receivers are not required to support the full range of bit rates and related clock frequencies; any sub range is acceptable as long as the limits specified are not exceeded.
22. A maximum of 50 mV ground potential difference between TX and RX is assumed.
23. Including V_{CM_AC}.

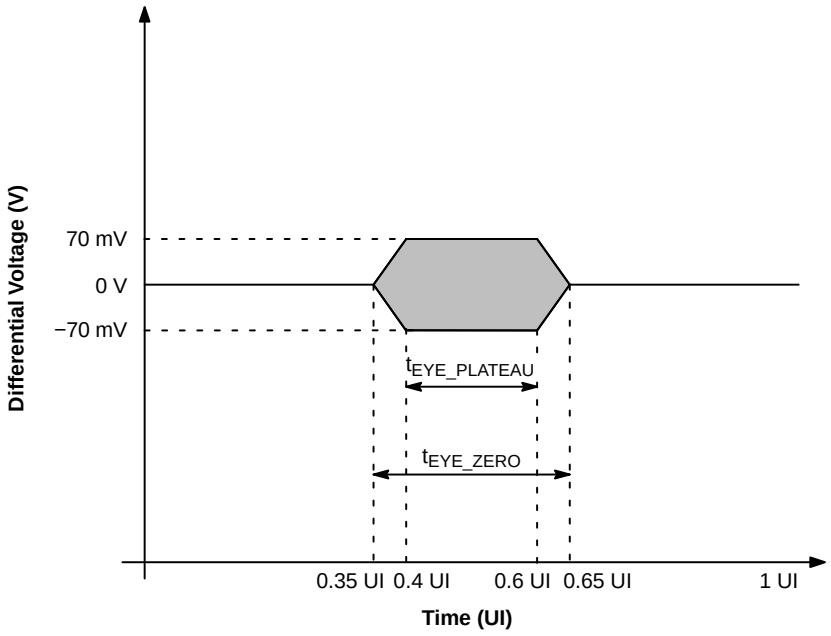

Figure 9. SLVS RX Eye Diagram Mask

SubLVDS Specifications

Table 7. SUBLVDS SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit
TIMING PARAMETERS					
Data Bit Rate (Note 24, 25)	$1/t_{PW}$	200		800	Mbps
DDR Clock Period (Note 25)	T	2.5		10	ns
Plateau Eye Width	$t_{EYE\_PLATEAU}$	0.15			UI
DC PARAMETERS					
Input Voltage Receiver Range (Note 26)	V_{IN_DC}	580		1220	mV
Input Common-mode Receiver Range (Notes 26, 27)	V_{CMRX}	650	900	1150	mV
Receiver Differential Input Voltage	$\|V_{ID}\|$	50			mV

24. Equivalent to 1/UI where UI is the normalized mean time between consecutive clock edges.
25. Transmitters and Receivers are not required to support the full range of bit rates and related clock frequencies; any sub range is acceptable as long as the limits specified are not exceeded.
26. A maximum of 50mV ground potential difference between TX and RX is assumed.
27. Including V_{CM_AC}.

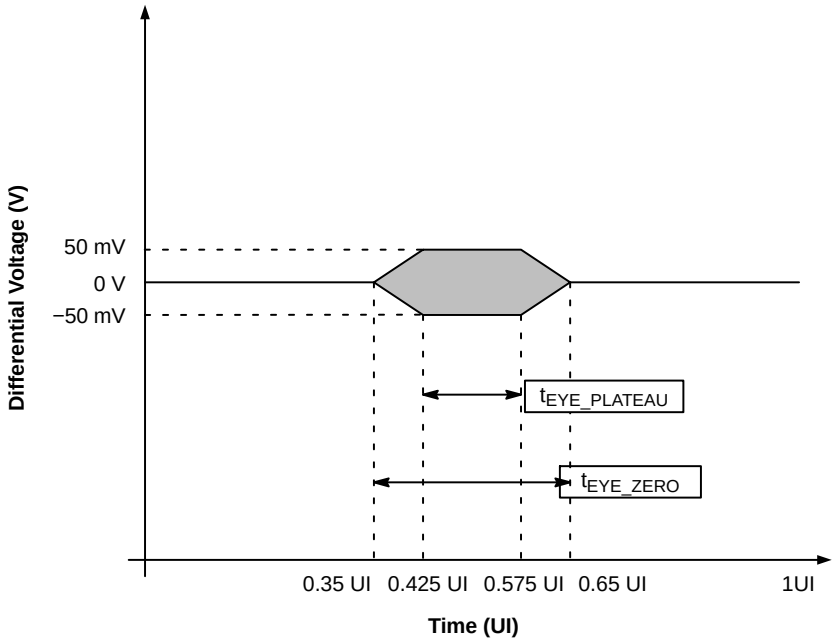

Figure 10. SubLVDS RX Eye Diagram Mask

The previous two figures illustrate the minimum eye opening required at the pins of the receiver to allow for proper operation of the link up to a bit error rate of $1e^{-9}$. For compliance test the input signal does not need to touch the vertices and edges of the mask but it should be a reasonably good approximation.

Transmission Line Interconnect System

The HiSPi Transmission Line Interconnect System (TLIS) consists of multiple unidirectional, point-to-point transmission lines. An illustrative four data lane system is shown bellow.

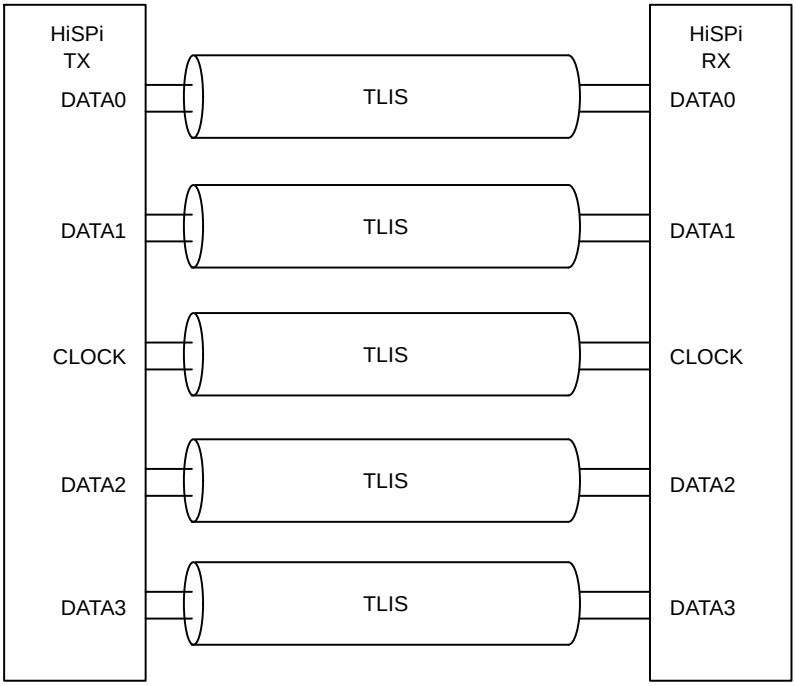

Figure 11. HiSPi Interconnect System

TLIS should be a differential transmission line with 100 Ω characteristic impedance.

Table 8.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DC PARAMETERS						
Differential Impedance	Z_0		90	100	110	Ω
Ground Shift	GM		−50		50	mV
TIMING PARAMETERS						
Intra Pair Skew					10	ps
Inter Pair Skew					50	ps
FREQUENCY PARAMETERS						
DC Insertion Loss	$S_{dd12, Sdd21}$	DC			0.4	dB
SLVS Insertion Loss	$S_{dd12, Sdd21}$	Freq = 0.5 × Bitrate			2	dB
		Freq = 1.5 × Bitrate			5	dB
subLVDS Insertion Loss	$S_{dd12, Sdd21}$	Freq = 0.5 × Bitrate			2	dB
		Freq = 1.5 × Bitrate			5	dB
Return Loss	$S_{dd11, Sdd22}$	Freq = Bitrate/2	15			dB
		Freq = 10 MHz	20			dB

All TLIS should be laid out using good signal integrity practices to minimize insertion losses and reflections, so as to avoid too much degradation of the signal. Good lane matching should also be used to minimize adding Clock-to-Data skew.

SYSTEM TRADE OFFS

HiSPi is expected to serve a broad range of applications and despite the electrical interface being quite generic the system may benefit from redistribution of the timing and amplitude budgets across transmitter, receiver and interconnect to achieve optimum performance.

The interconnect is undoubtedly the component that changes most across applications, in the form of different building materials, length requirements, noise environments, etc. Keeping this in mind, HiSPi offers the flexibility of trading interconnect attenuation for receiver sensitivity. This will allow applications to use longer and/or lower grade interconnects than the ones previously covered at the expense of more sensitive receivers and vice-versa.

Figures 12 and 13 show a possible compromise between TLIS Insertion Loss and RX sensitivity for SLVS and SubLVDS modes respectively. A marker is used to highlight the values for the two parameters based on the previous section.

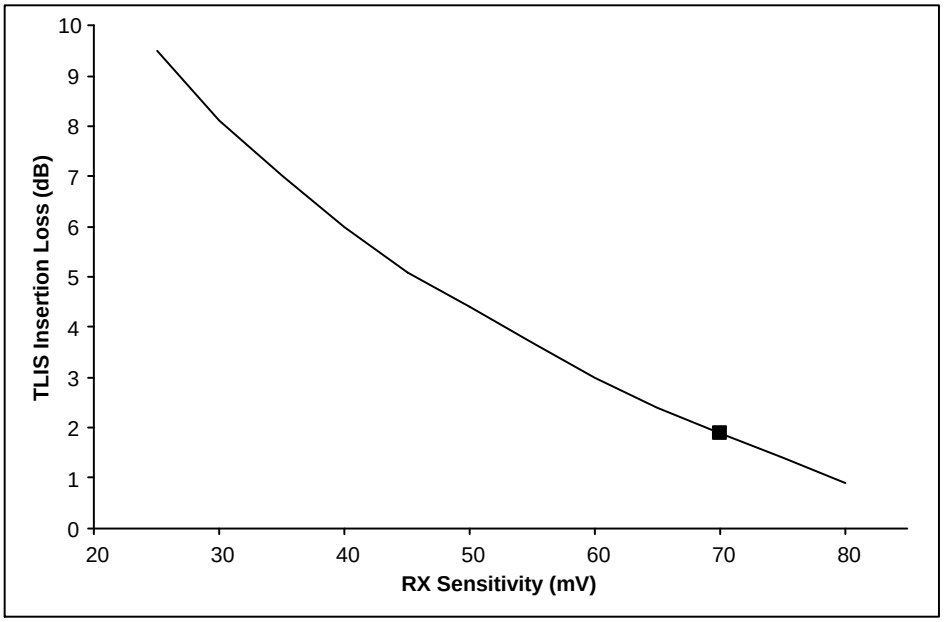

Figure 12. TLIS IL vs. RX Sensitivity for SLVS

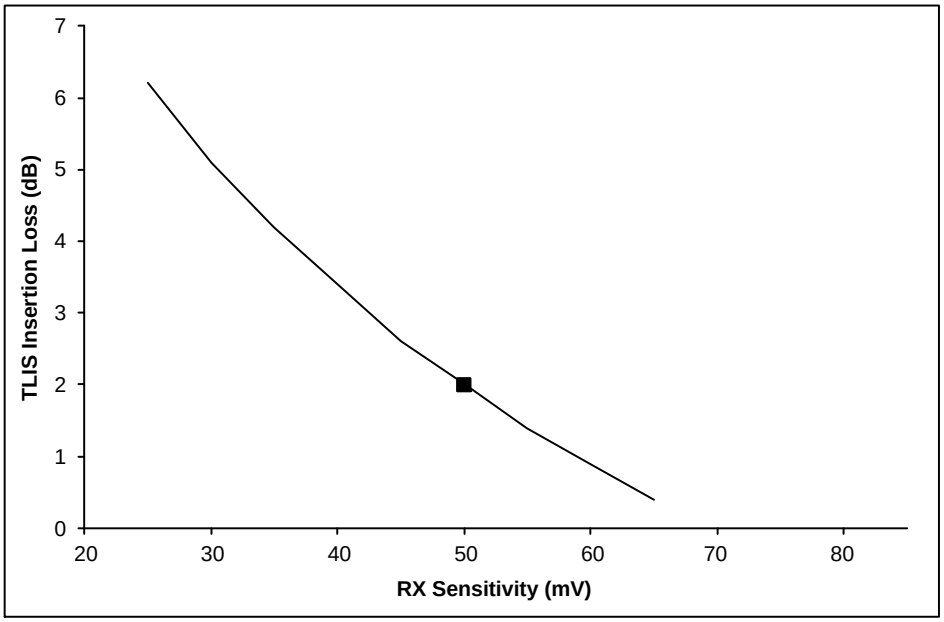

Figure 13. TLIS IL vs. RX Sensitivity for SubLVDS

TEST CONDITIONS [INFORMATIVE]

This section introduces some generic test circuits that can be used to characterize the HiSPi interface. The use of the circuits and methodologies described hereafter is not normative; other alternatives may be considered as long as the measured parameters do not deviate from the definitions presented in previous sections.

Transmitter Output Signal

The following test circuits are common to both SLVS and SubLVDS transmitters.

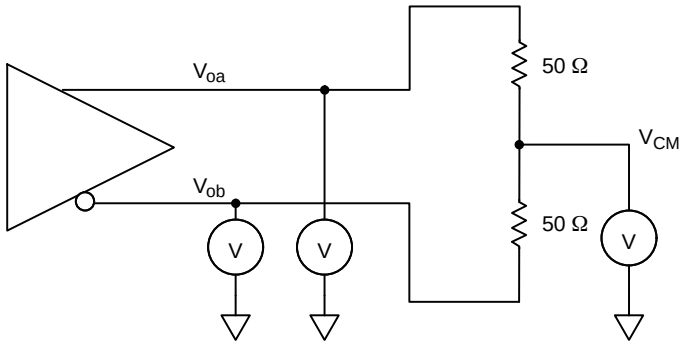

Figure 14. DC Test Circuit

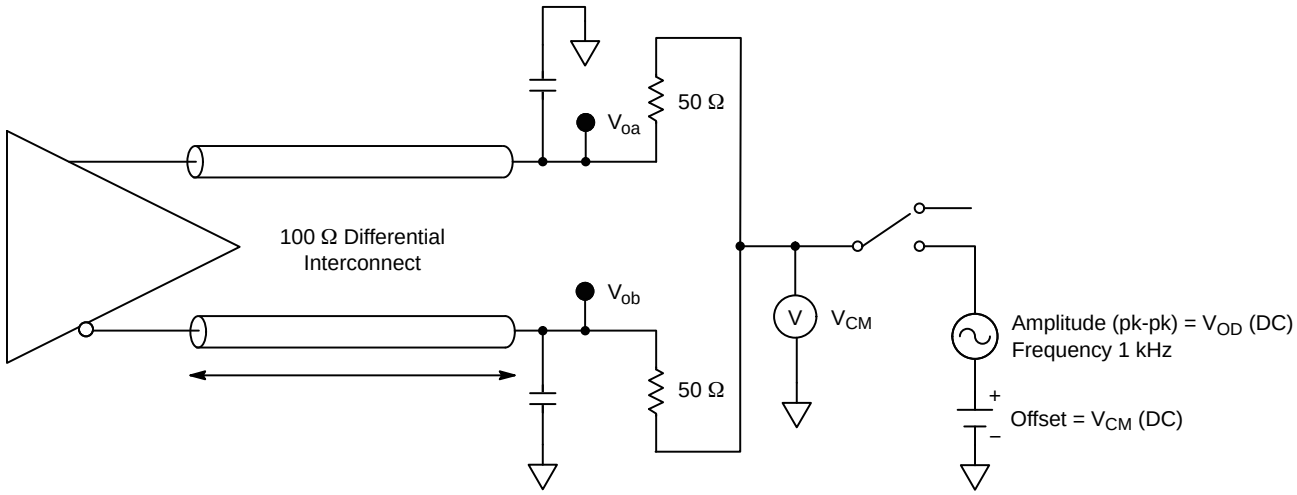

Figure 15. Test Circuit

Figure 15 presents a test circuit that may be used to measure driver output differential voltage and common mode voltage. Two similar high precision resistors (< ±1% tolerance) are connected in series and attached to driver output differential pins to provide proper termination and easy access to a center tap point where common mode voltage can be easily measured. For illustrative purposes, two 50 Ω resistors were used but any value within the previously defined R_L range can be used.

Ideally both V_{OD} and V_{CM} steady state values would not change with the transmitted logic value but in practice they do. This implies that both values are taken as the average of opposite logic level measures.

This specification also constraints variation between logic values to control EMI radiation and other adverse system properties.

$$V_{OD}(m) = |V_{oa}(m) - V_{ob}(m)| \quad \text{(eq. 6)}$$

where ‘m’ is either logic 1 or logic 0

$$|V_{OD}| = \frac{V_{OD}(1) + V_{OD}(0)}{2} \quad \text{(eq. 7)}$$

$$V_{diff} = V_{OD}(1) + V_{OD}(0) \quad \text{(eq. 8)}$$

$$V_{CM} = \frac{V_{CM}(1) + V_{CM}(0)}{2} \quad \text{(eq. 9)}$$

$$|\Delta V_{CM}|_{0,1} = |V_{CM}(1) - V_{CM}(0)| \quad \text{(eq. 10)}$$

$$|\Delta V_{OD}|_{0,1} = |V_{OD}(1) - V_{OD}(0)| \quad \text{(eq. 11)}$$

Both V_{OD} and V_{CM} are measured for all output channels. The worst case ΔV_{OD} is defined as the largest difference in

V_{OD} between all channels regardless of logic level. And the worst case ΔV_{CM} is similarly defined as the largest difference in V_{CM} between all channels regardless of logic level.

$$\Delta V_{CM} = MAX_{i=1:N}\left(V_{CM,i}(1),\ V_{CM,i}(0)\right) - MIN_{j=1:N}\left(V_{CM,j}(1),\ V_{CM,j}(0)\right) \quad \text{(eq. 12)}$$

$$\Delta V_{OD} = MAX_{i=1:N}\left(V_{OD,i}(1),\ V_{OD,i}(0)\right) - MIN_{j=1:N}\left(V_{OD,j}(1),\ V_{OD,j}(0)\right) \quad \text{(eq. 13)}$$

Figure 16 presents a test circuit that may be used to check parameters like V_{CM_AC} and the compliance against eye diagram masks defined for SLVS and subLVDS drivers. It is understandable that more often than not some short interconnect exists between the driver output pins and the test load as shown. Still, to ensure minimum impact of such interconnect on the transmitter measures it should be made as short as possible, impedance balanced and follow high speed design guidelines. Two generic capacitances are also included representing a lumped capacitance for soldering pads and oscilloscope probes. Test engineers must ensure that the overall load has more than 20 dB Return Loss from DC to $1.5 \times$ BaudRate so that reflections do not affect significantly the measures.

Judicious selection of timing critical test instruments such as oscilloscope and probes must be enforced. It is crucial that the bandwidth of both is sufficient to allow inclusion of at least the 5th harmonic with negligible attenuation where the fundamental frequency is half the bit rate for a NRZ signal. Also, the transition time of the test system must be at least 4x faster than the minimum rise/fall times expected for the test signal.

Transmitter eye diagram compliance must be checked with a sufficient number of bits to assess the target bit error rate (BER) while driving a PRBS9 pattern for data and maximum frequency square wave pattern for clock. A fail must be considered if the accumulated eye diagram touches any of the keep out regions in the mask.

Transmitter DC Impedance

Below is the test circuit for testing the single-ended DC impedance.

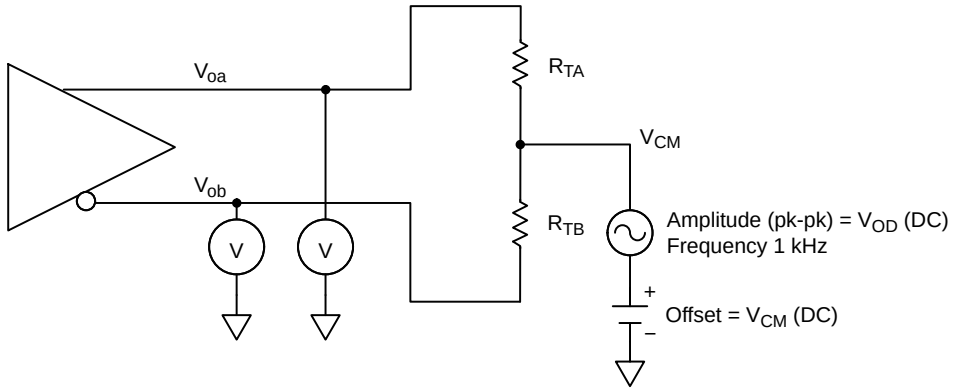

Figure 16. Single-ended Impedance Test Circuit

The HiSPi PHY should be configured to transmit a constant high or low logic output. For each logic level the output impedance can be measured by applying voltage V_{OS} of both a logic 1 and logic 0 level to the common-mode point between two 50 Ω resistors. By measuring the voltages V_{oa} and V_{ob} on the outputs for the two

$$R_{oa}(m) = \frac{R_{TA} \times \Delta V_{oa}}{\Delta V_{OS} - \Delta V_{oa}} \quad \text{(eq. 14)}$$

$$R_{ob}(m) = \frac{R_{TB} \times \Delta V_{ob}}{\Delta V_{OS} - \Delta V_{ob}} \quad \text{(eq. 15)}$$

where:
'm' is the logic lever 1 or 0
ΔV_{OS} is the difference between the two applied voltages.
$\Delta V_{oa,ob}$ is the difference in the measured voltages on the outputs

Receiver Input Signal

A compliant receiver must be able to properly recover with the target BER an input data stream shaped as close as possible to the receiver eye mask presented in section "Receiver". Such a signal may be generated with the help of an Arbitrary Waveform Generator (AWG), Data Timing Generator (DTG), Transition Time converters (TTC), Cable Emulators (CE) and is not required to touch any of the vertices or edges of the mask but be a good approximation instead.

A PRBS9 pattern should be used for data and should run for a time consistent with the target bit error rate. The cross checking of the pattern can be done internally on the DUT or through a loopback connection if transmitter capabilities are available.

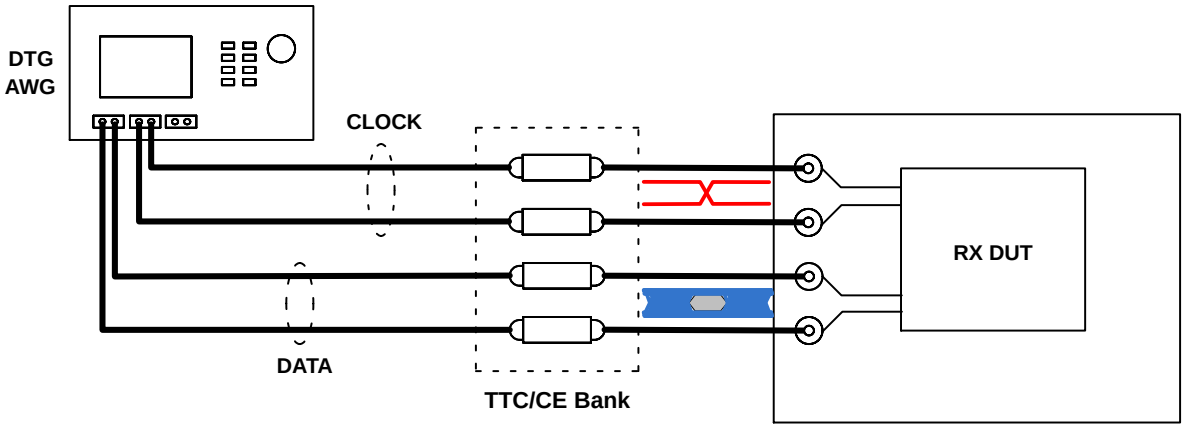

Figure 17. Test Setup for Receiver Testing

VERSION HISTORY

The most noticeable changes from HiSPi 2.0 are:

- Removed power supply scalability for SLVS electrical interface
- HiVCM LVDS support replaced by subLVDS (lower signal swing)
- Removed optional DLL section
- Removed image test modes section
- Removed power supplies and temperature references
- Added receiver and transmitter eye diagram masks
- Added pin capacitance specification parameters
- Constrained maximum bit rate in subLVDS mode to 800 Mbps
- Redefinition of some electrical specifications for SLVS and subLVDS modes
- Editorial changes

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