

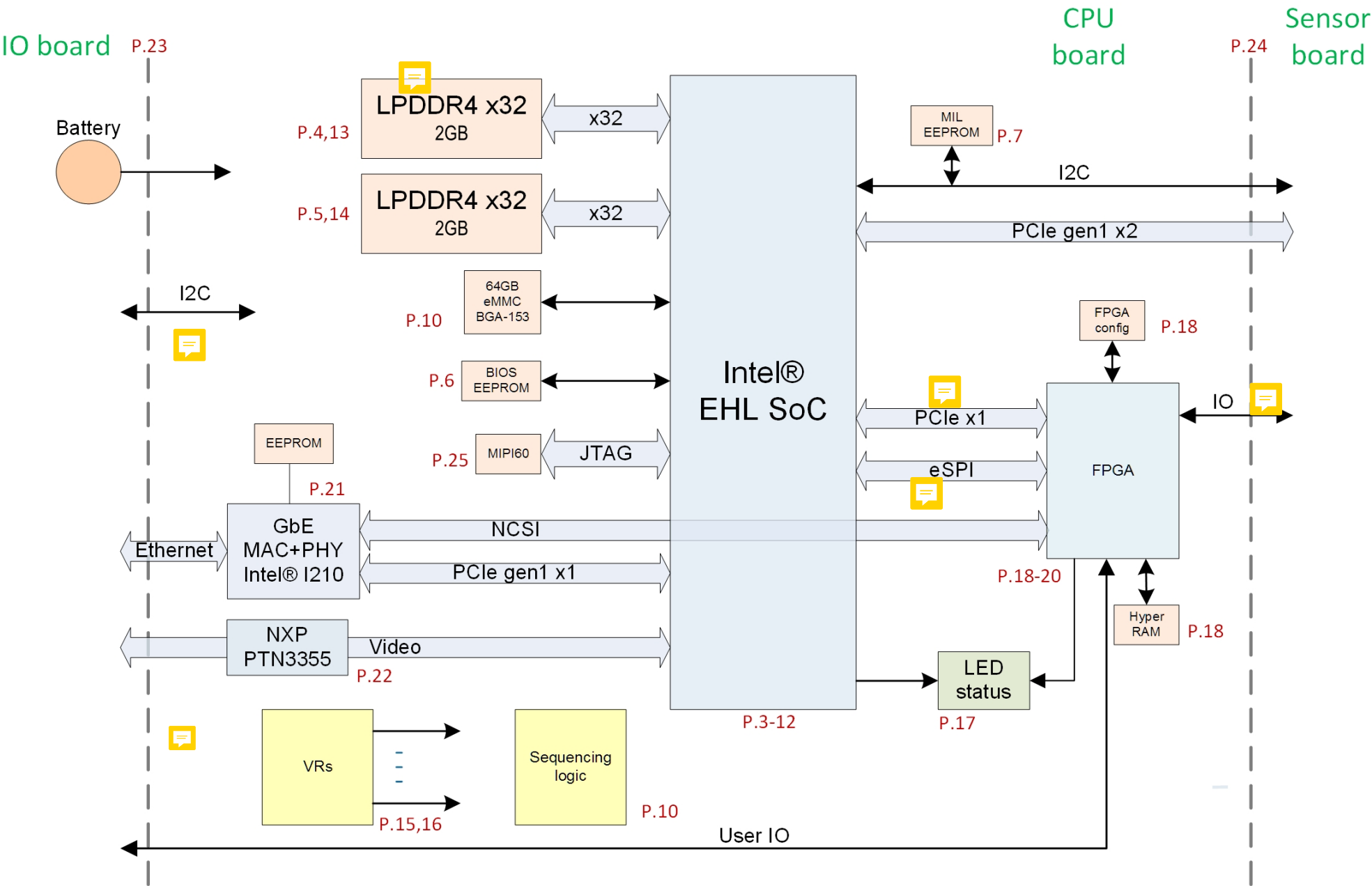
IRIS4 CPU Board


REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

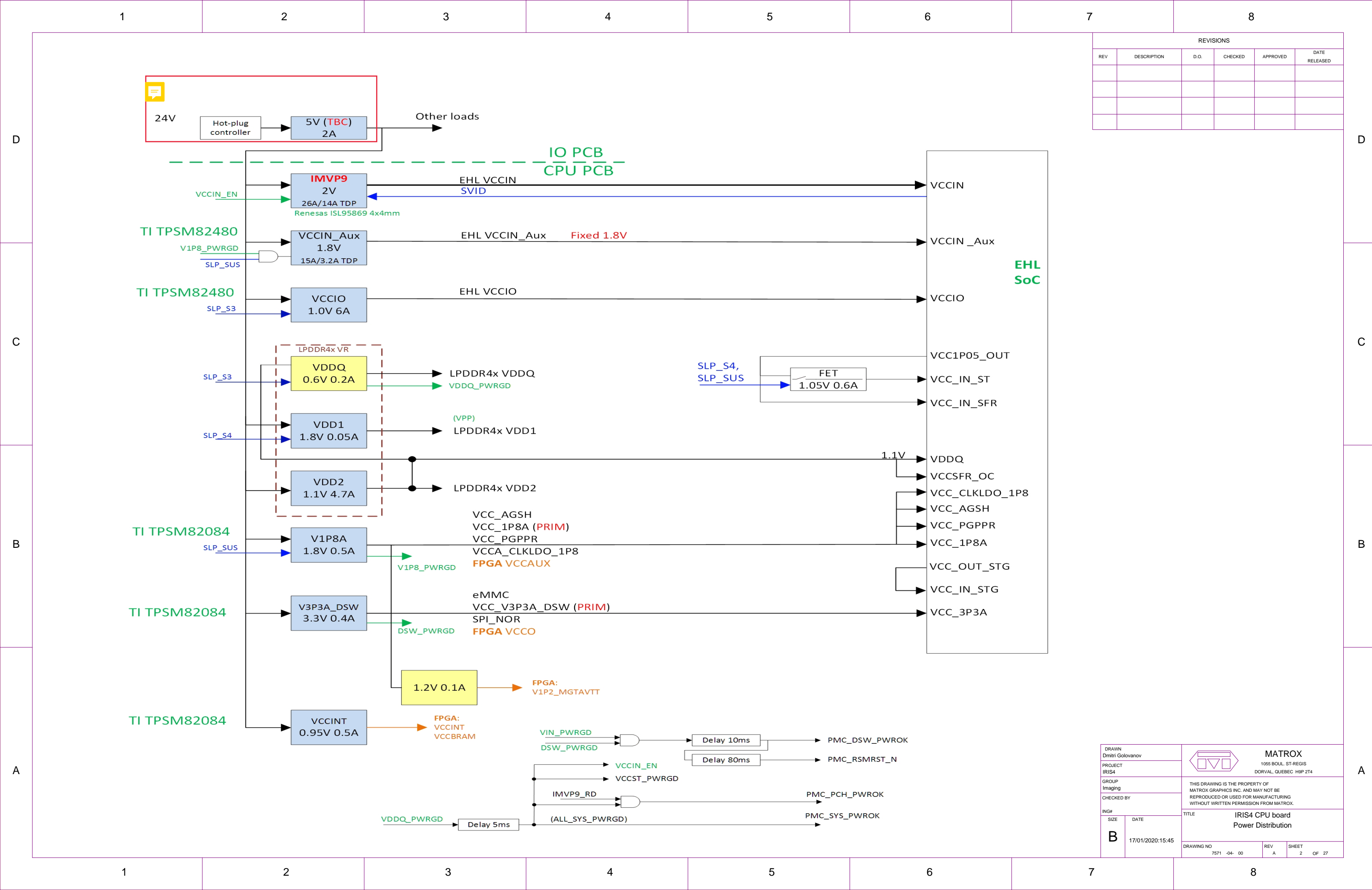
MATROX CONFIDENTIAL

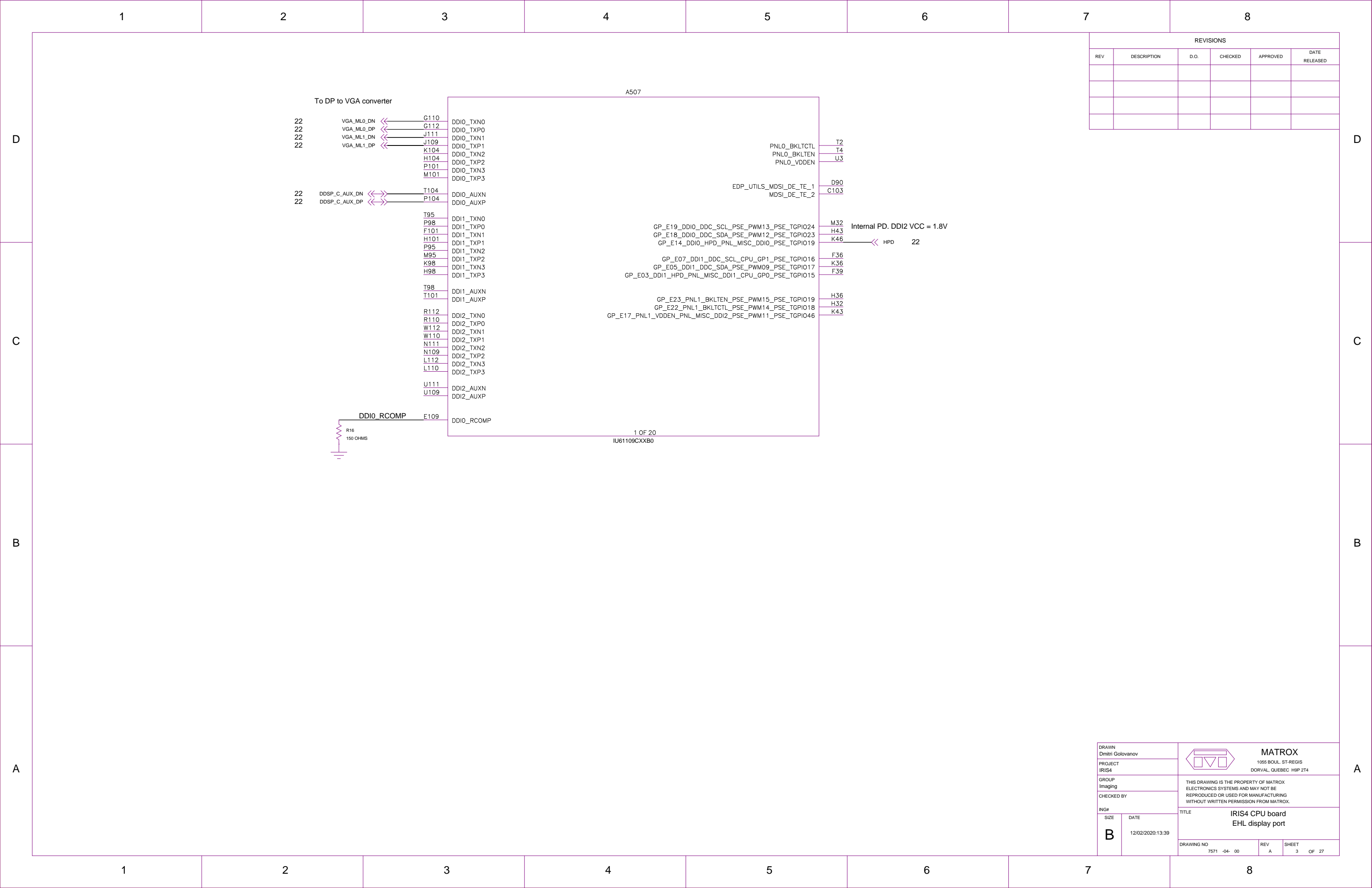
INDEX

- p.1 BLOCK_DIAGRAM
- p.2 POWER DISTRIBUTION
- p.3 EHL display port
- p.4 EHL DDR0
- p.5 EHL DR1
- p.6 EHL SPI
- p.7 EHL I2C IO
- p.8 EHL GPIO
- p.9 EHL PCIe USB
- p.10 EHL eMMC PMC
- p.11 EHL power
- p.12 EHL GND pins
- p.13 LPDDR4x channel A1
- p.14 LPDDR4x channel A2
- p.15 VR VCCIN IMVP9
- p.16 VRs
- p.17 LEDs
- p.18 FPGA config and PCIe
- p.19 FPGA IO
- p.20 FPGA power
- p.22 Ethernet controller
- p.22 VGA converter
- p.23 IO board connector
- p.24 Sensor board connector
- p.25 CPU debug port
- p.26 Mounting holes and test coupons
- p.27 Revision history



DRAWN Dmitri Golovanov		 MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY		TITLE IRIS4 CPU board Block_Diagram	
ING#		DRAWING NO	
SIZE B	DATE 21/01/2020:07:53	7571 -04- 00	REV A
			SHEET 1 OF 27





D

C

B

A

D

C

B

A

1

2

3

4

5

6

7

8

1

2

3

4

5

6

7

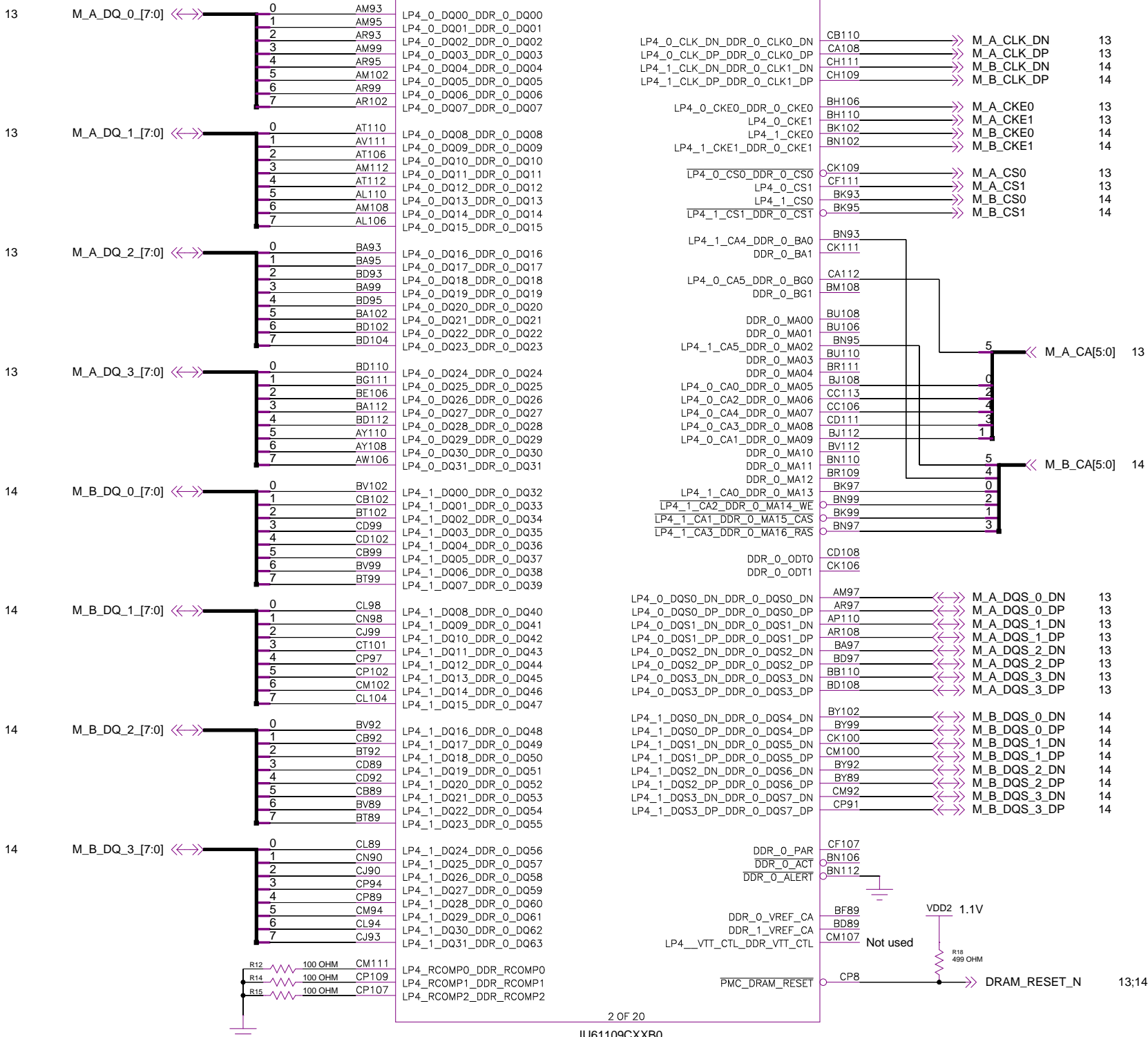
8


REVISIONS

REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

DDR sub-channels 0 and 1

A507



DRAWN Dmitri Golovanov		 MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY		TITLE IRIS4 CPU board EHL DDR0	
ING#			
SIZE B	DATE 12/02/2020:13:39		
		DRAWING NO 7571 -04- 00	REV A
		SHEET 4	OF 27

D

C

B

A

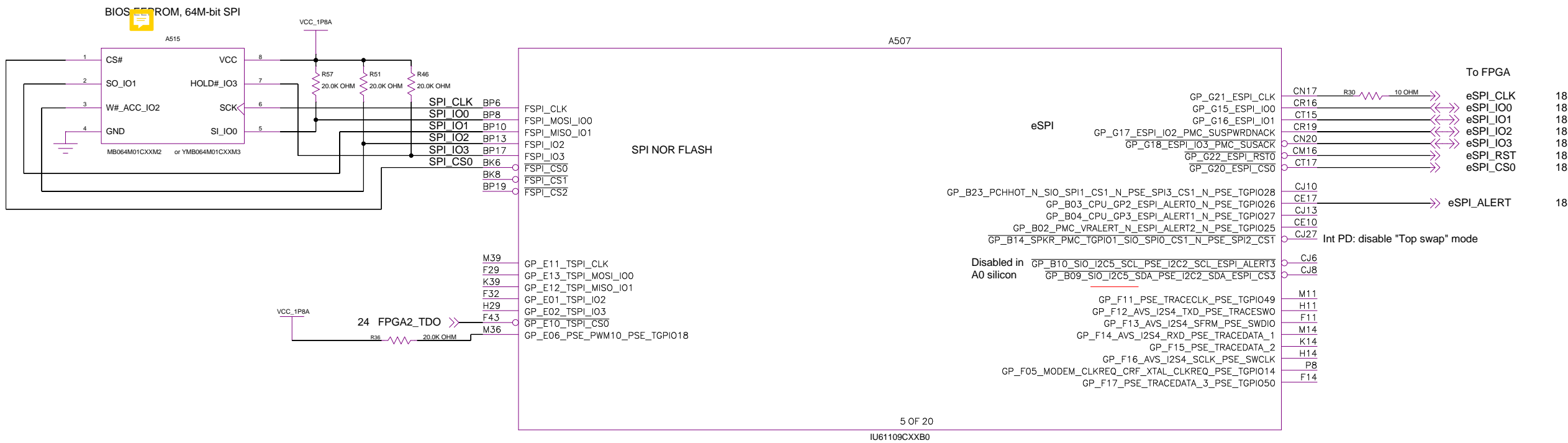
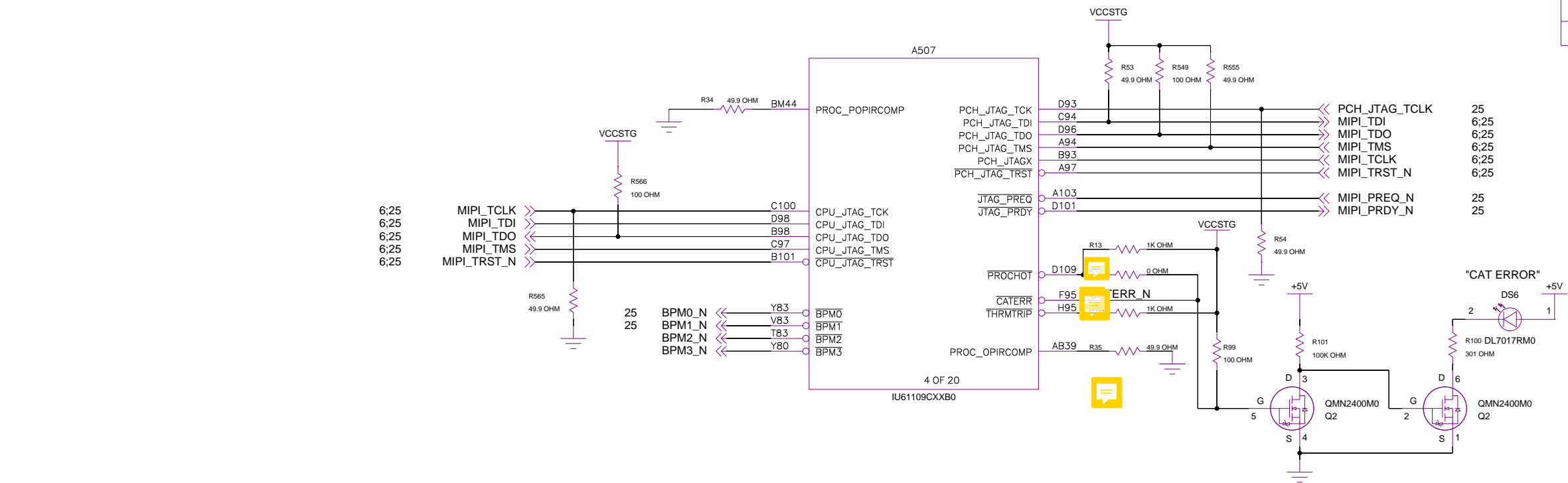
D


C

B

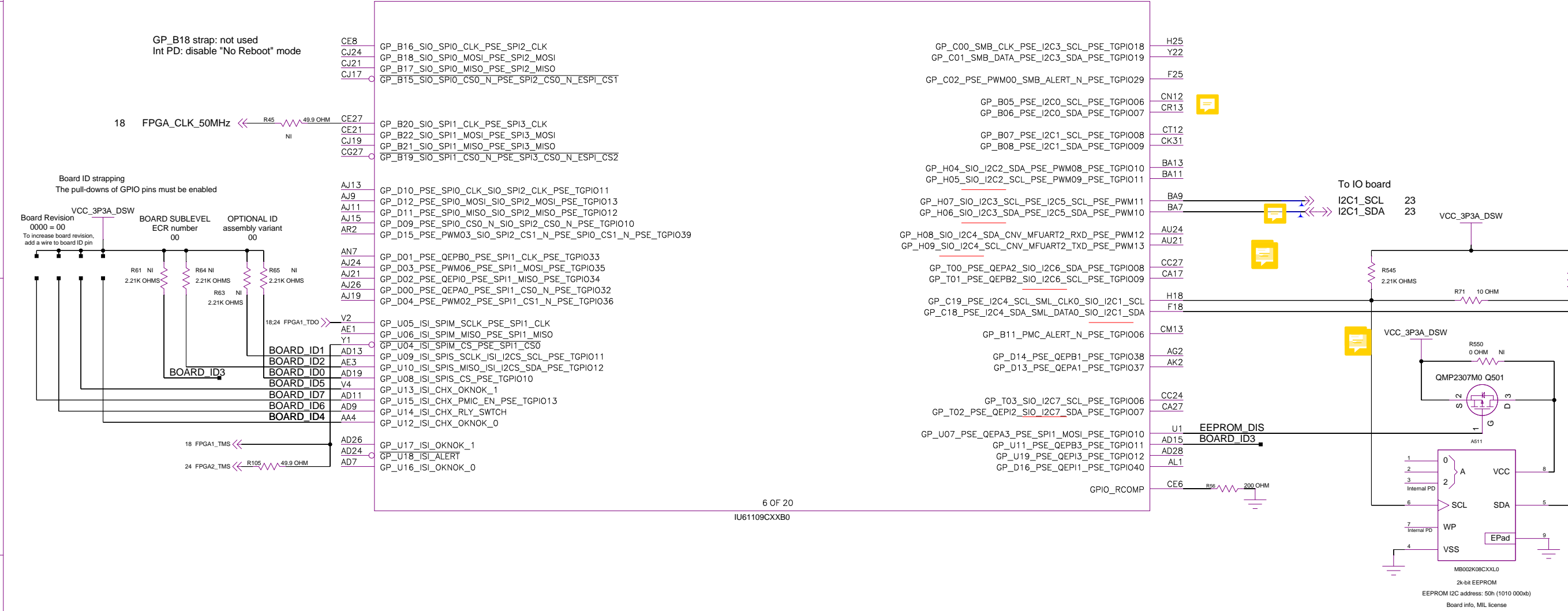
A


REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

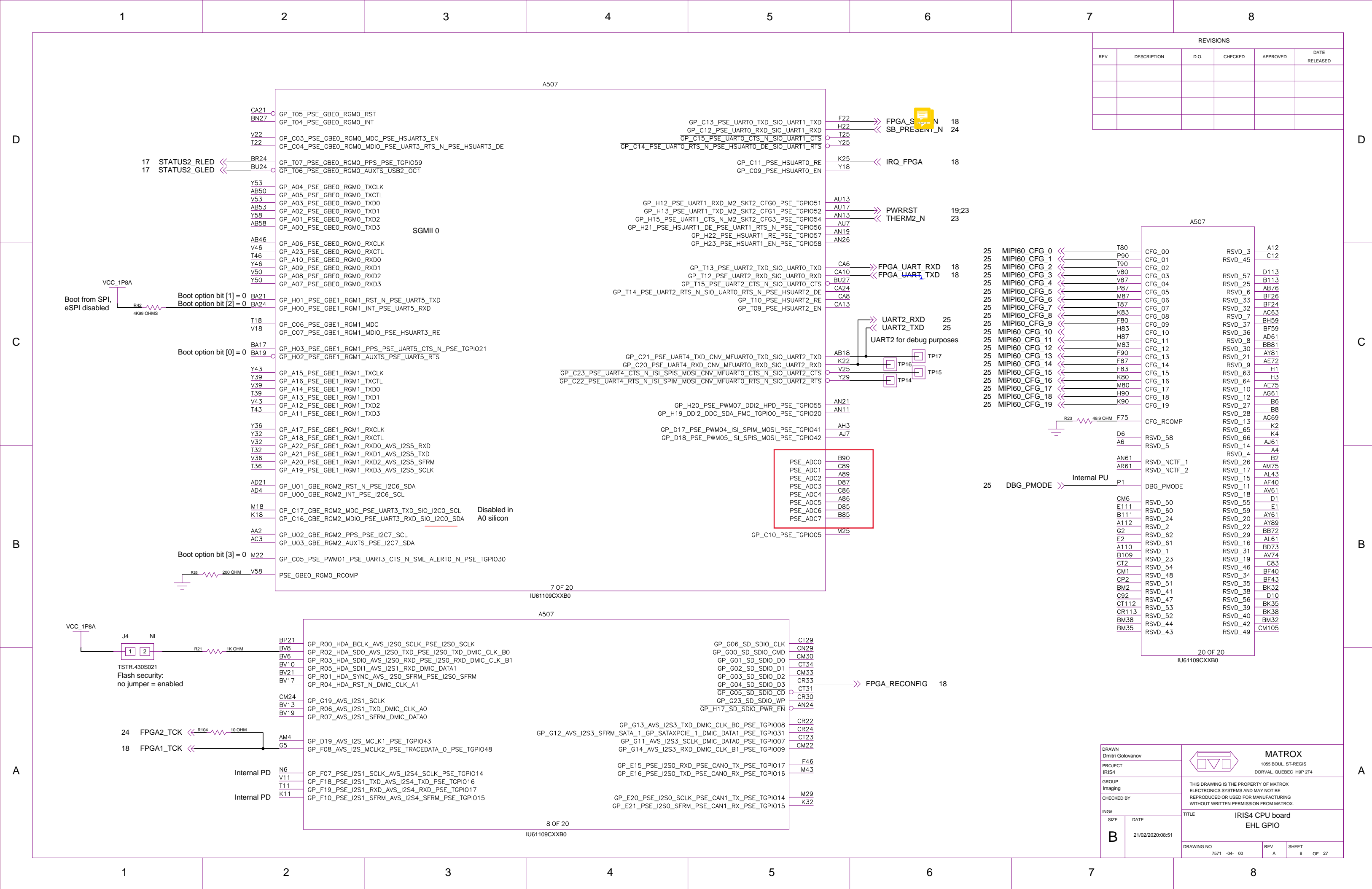


DRAWN Dmitri Golovanov				MATROX	
PROJECT IRIS4				1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.			
CHECKED BY					
ING#		TITLE IRIS4 CPU board EHL SPI and debug			
SIZE B	DATE 18/02/2020:08:31				
DRAWING NO 7571 -04- 00		REV A		SHEET 6 OF 27	

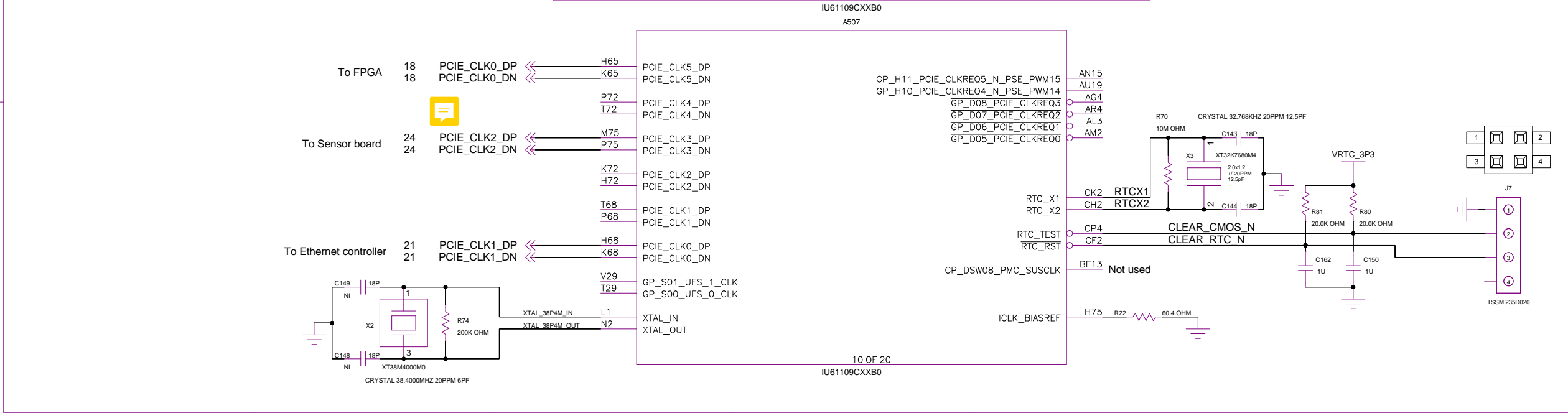
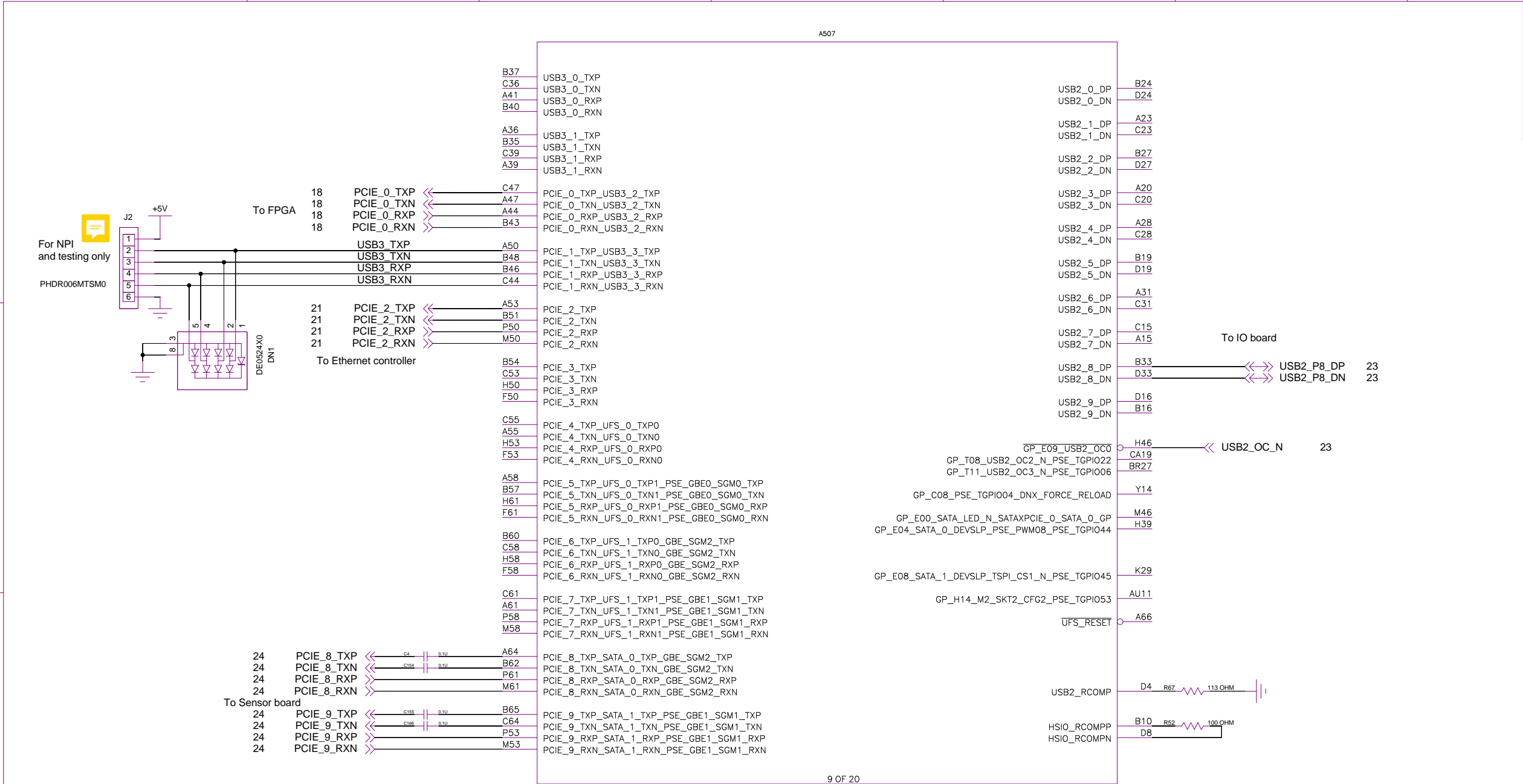
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED




DRAWN Dmitri Golovanov		 MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY		TITLE IRIS4 CPU board EHL IO I2C	
ING#		DRAWING NO	
SIZE B	DATE 21/02/2020:08:26	7571 -04- 00	REV A
			SHEET 7 OF 27



REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



DRAWN Dmitri Golovanov		 MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY		TITLE IRIS4 CPU board EHL PCIe USB	
ING#			
SIZE B	DATE 21/02/2020:08:18		
		DRAWING NO 7571 -04- 00	REV A
		SHEET 9 OF 27	

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

D

D

C

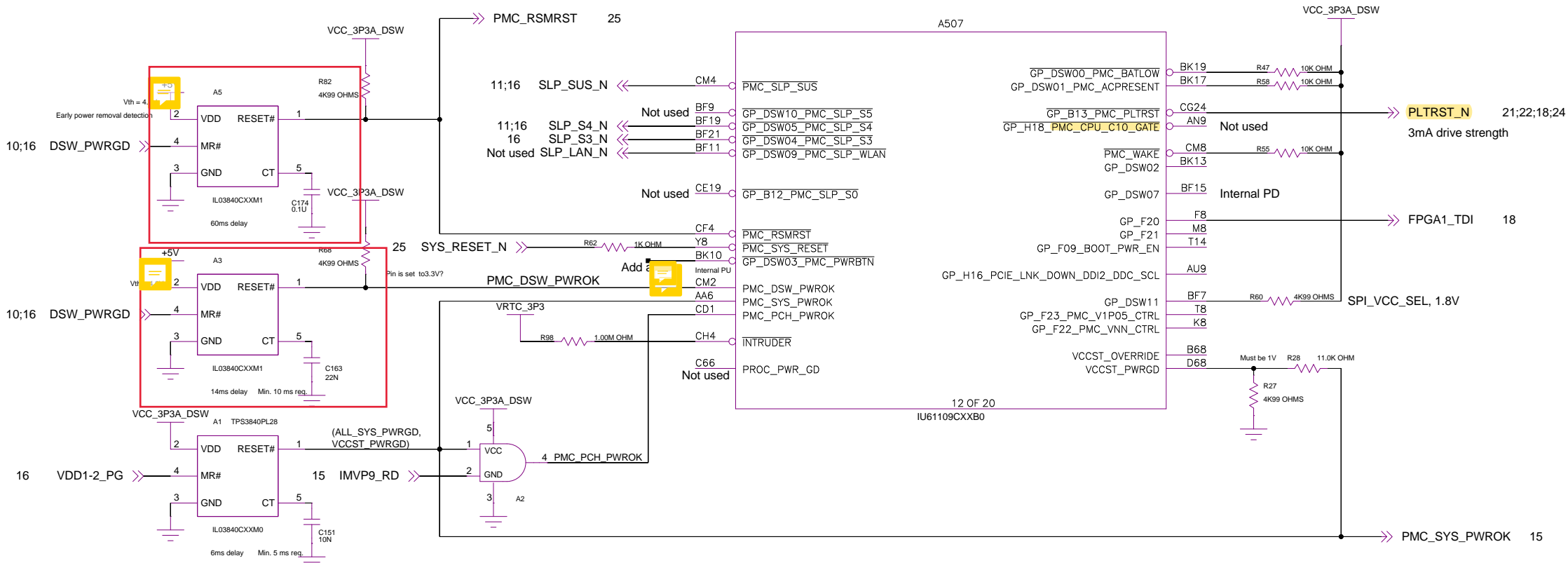
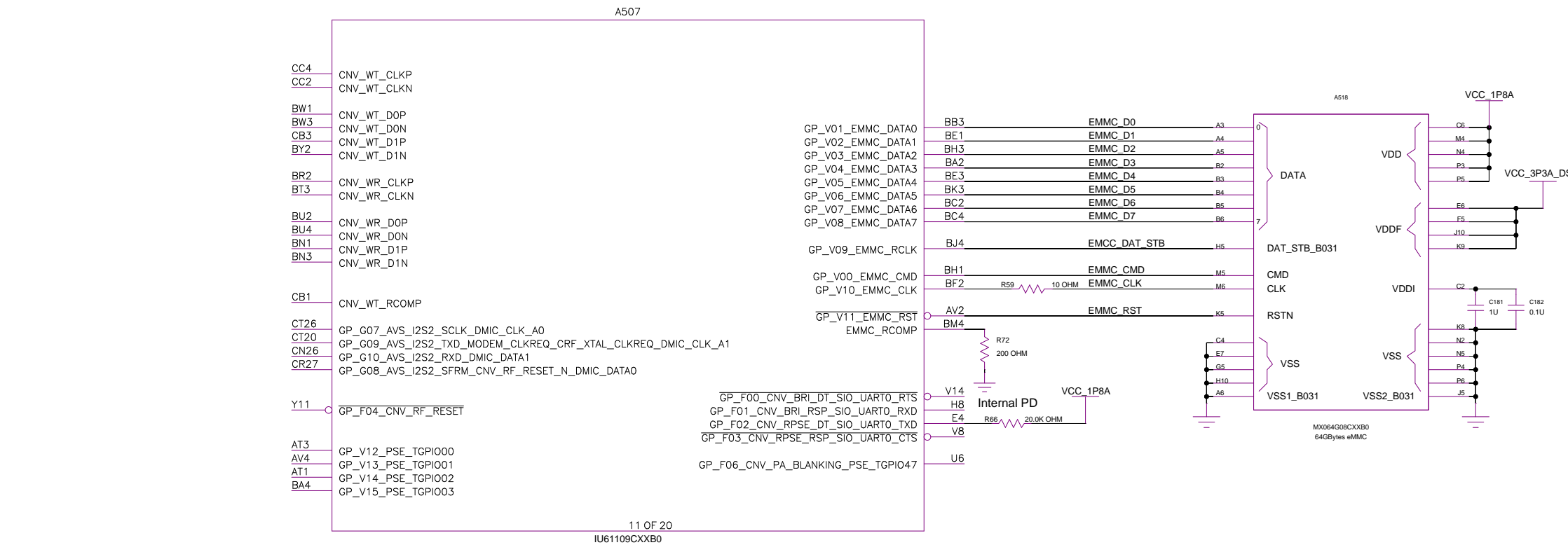
C


B

B

A

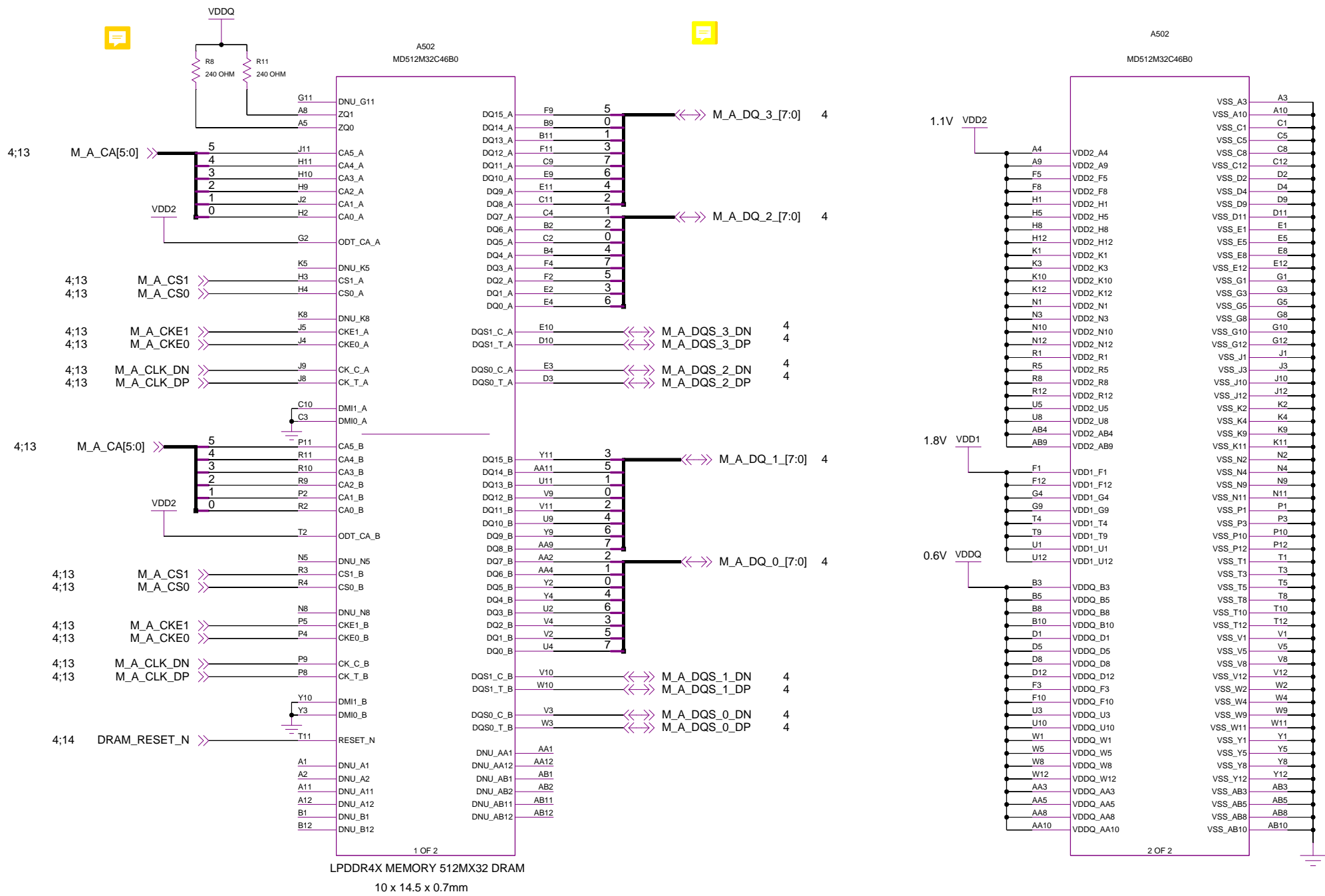
A




DRAWN Dmitri Golovanov		 MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX GRAPHICS INC. AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY			
ING#		TITLE IRIS4 CPU board EHL eMMC PMC	
SIZE B	DATE 21/02/2020 08:32		
		DRAWING NO 7571 -04- 00	REV A
		SHEET 10 OF 27	

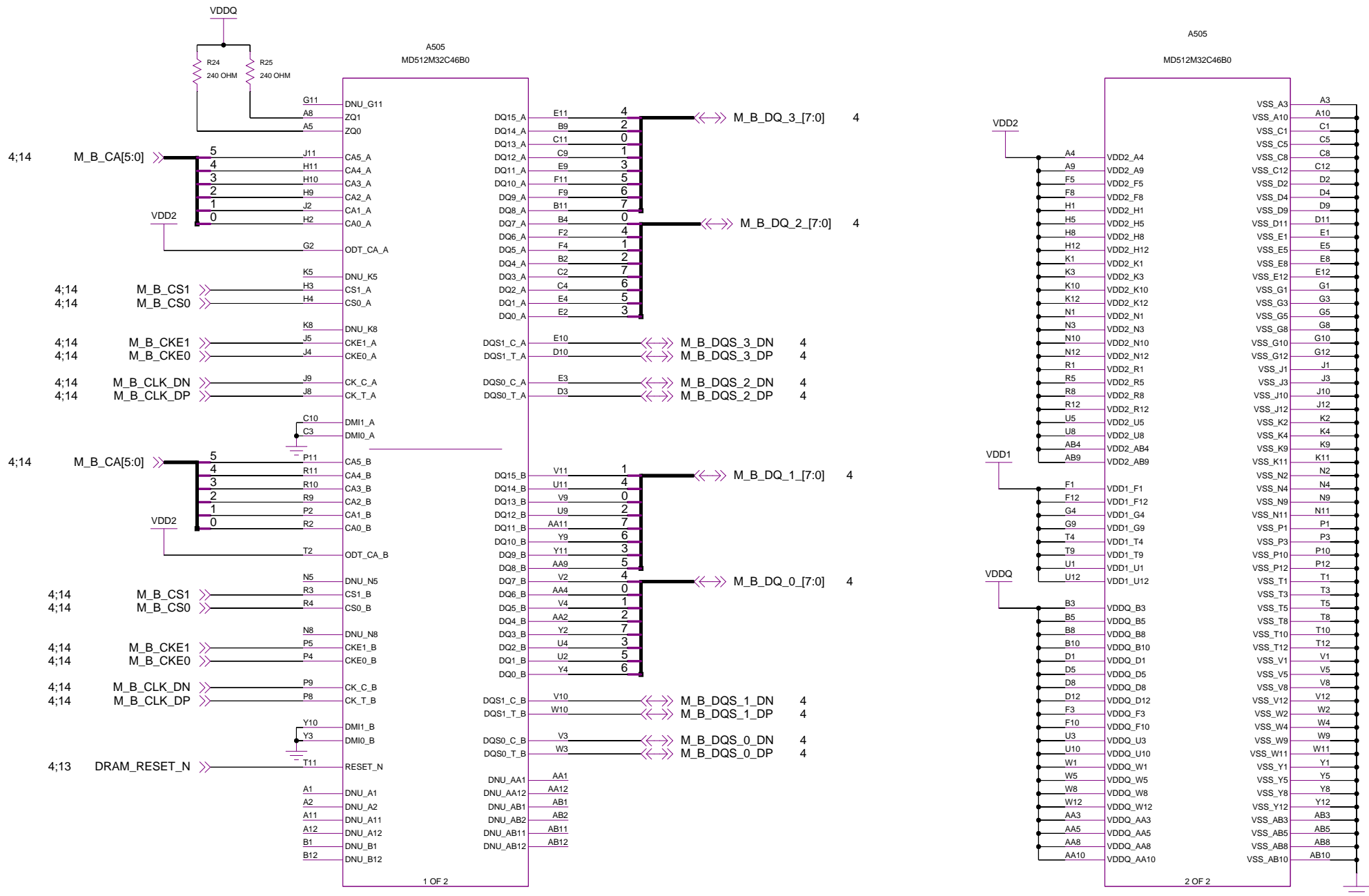
[illegible]


REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED




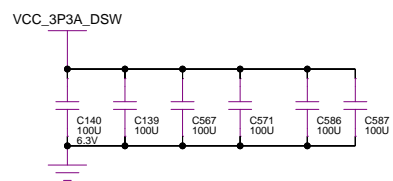
DRAWN Dmitri Golovanov		 MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY			
ING#		TITLE IRIS4 CPU board LPDDR4x sub-channel 0	
SIZE B	DATE 21/02/2020:07:58		
DRAWING NO 7571 -04- 00		REV A	SHEET 13 OF 27

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



DRAWN Dmitri Golovanov		 <div>MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4</div>	
PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY			
ING#		TITLE IRIS4 CPU board LPDDR4x sub-channel 1	
SIZE B	DATE 12/02/2020:13:39		
DRAWING NO 7571 -04- 00		REV A	SHEET 14 OF 27

DRAWN Dmitri Golovanov		 <p>MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4</p>	
PROJECT IRIS4			
GROUP Imaging		<p>THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.</p>	
CHECKED BY			
ING#		TITLE	
SIZE B	DATE 21/02/2020/07:44	IRIS4 CPU board VRs	
DRAWING NO		REV	SHEET
7571 -04- 00		A	16 OF 27



D

C

B

A

D

C

B

A

1

2

3

4

5

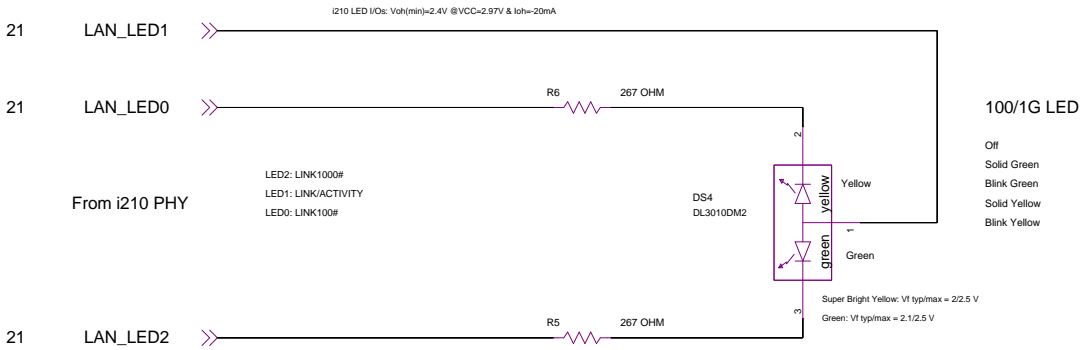
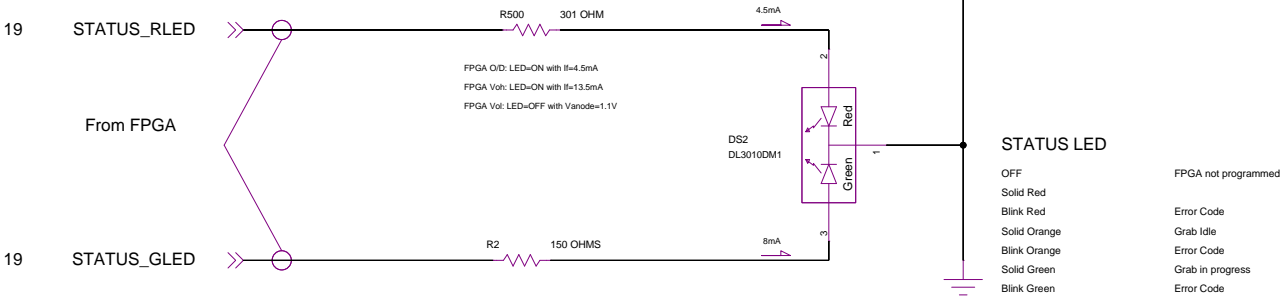
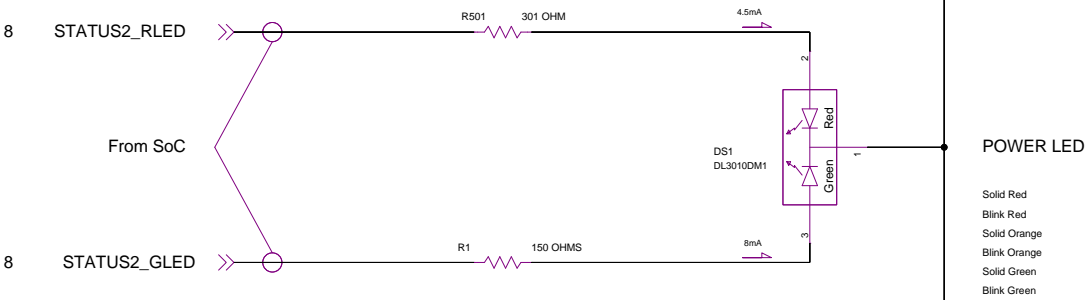
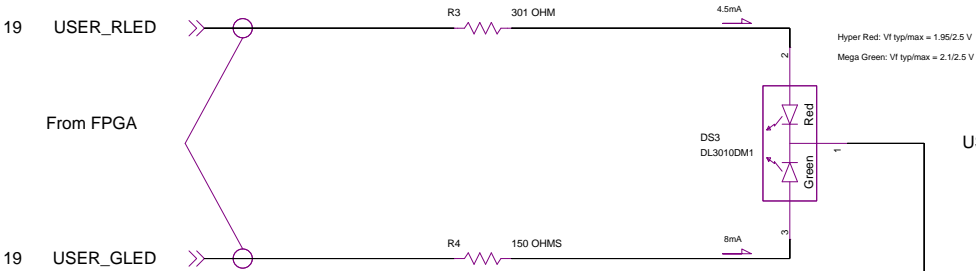
6


7

8

REVISIONS

REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



DRAWN Dmitri Golovanov		 MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
GROUP Imaging		TITLE IRIS4 CPU board LEDs	
CHECKED BY		DRAWING NO 7571 -04- 00	
ING#		REV A	SHEET 17 OF 27
SIZE B	DATE 12/02/2020:13:39		

1

2

3

4

5

6

7

8

D

C

B

A

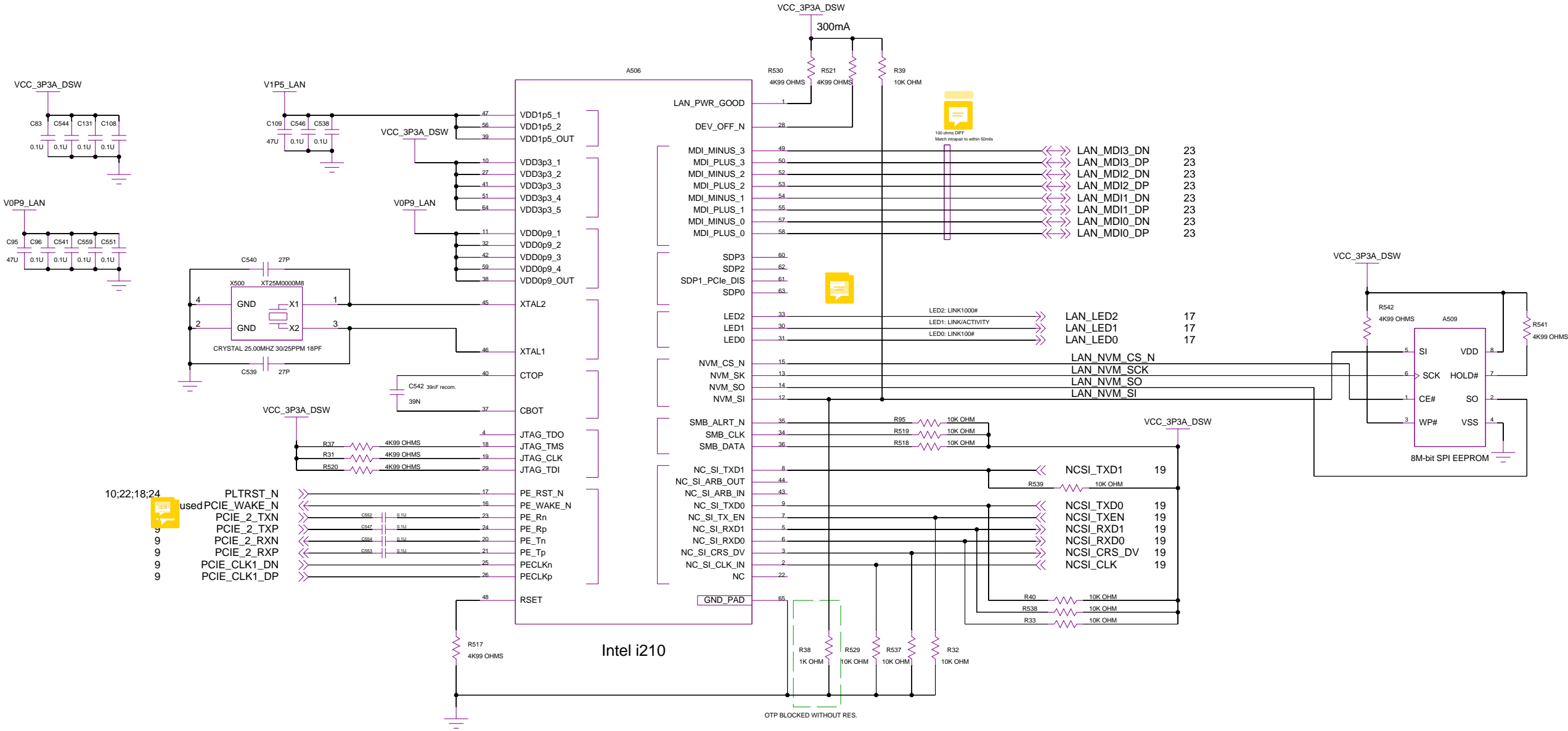
D


C

B

A

REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



DRAWN Dmitri Golovanov		 MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY		TITLE IRIS4 CPU board Ethernet controller	
ING#		DRAWING NO	
SIZE B	DATE 21/02/2020:09:17	7571 -04- 00	REV A
			SHEET 21 OF 27

D

C

B

A

D

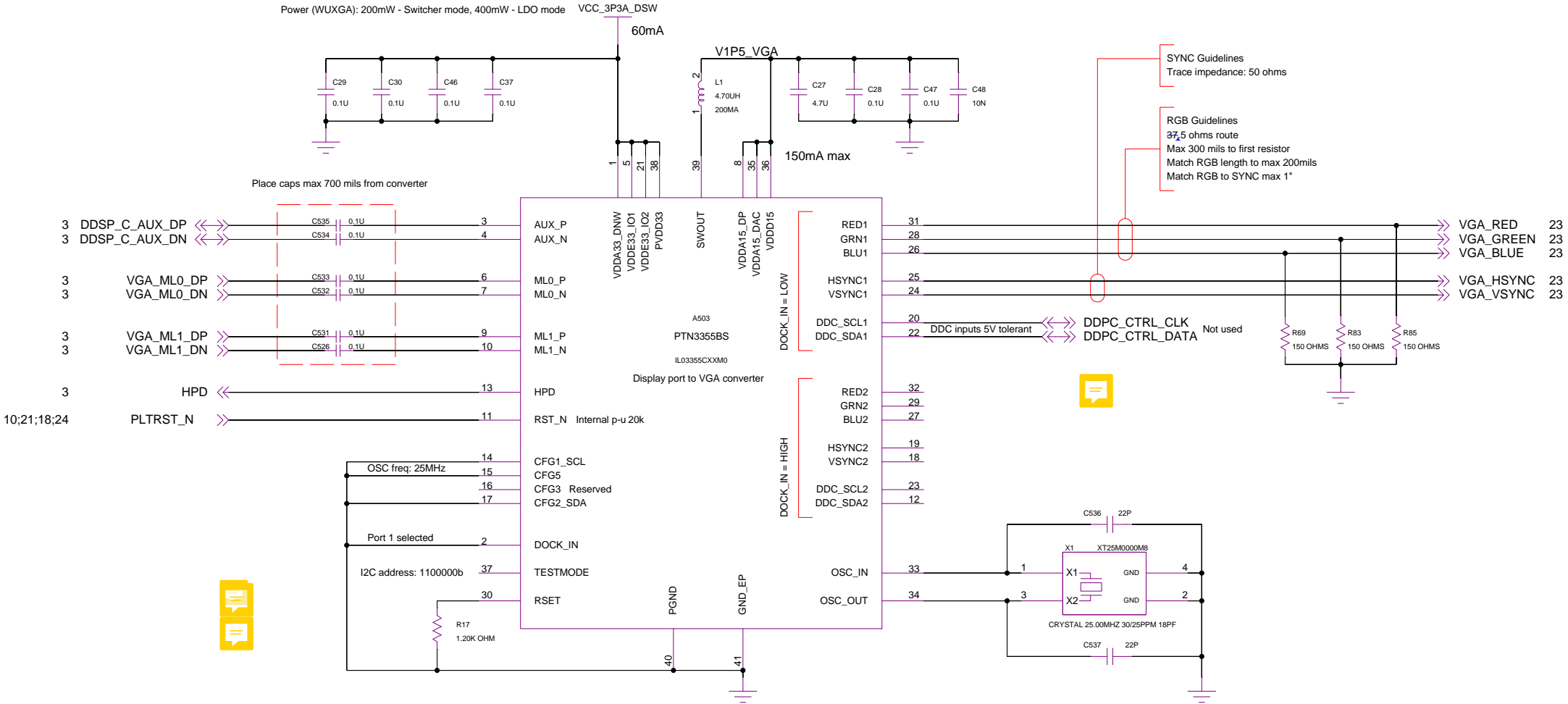
C


B

A

REVISIONS

REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



DRAWN Dmitri Golovanov		 MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX. ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY		TITLE IRIS4 CPU board VGA converter	
ING#	DATE	DRAWING NO	
B	13/02/2020:13:49	7571 -04- 00	REV A SHEET 22 OF 27

D

C

B

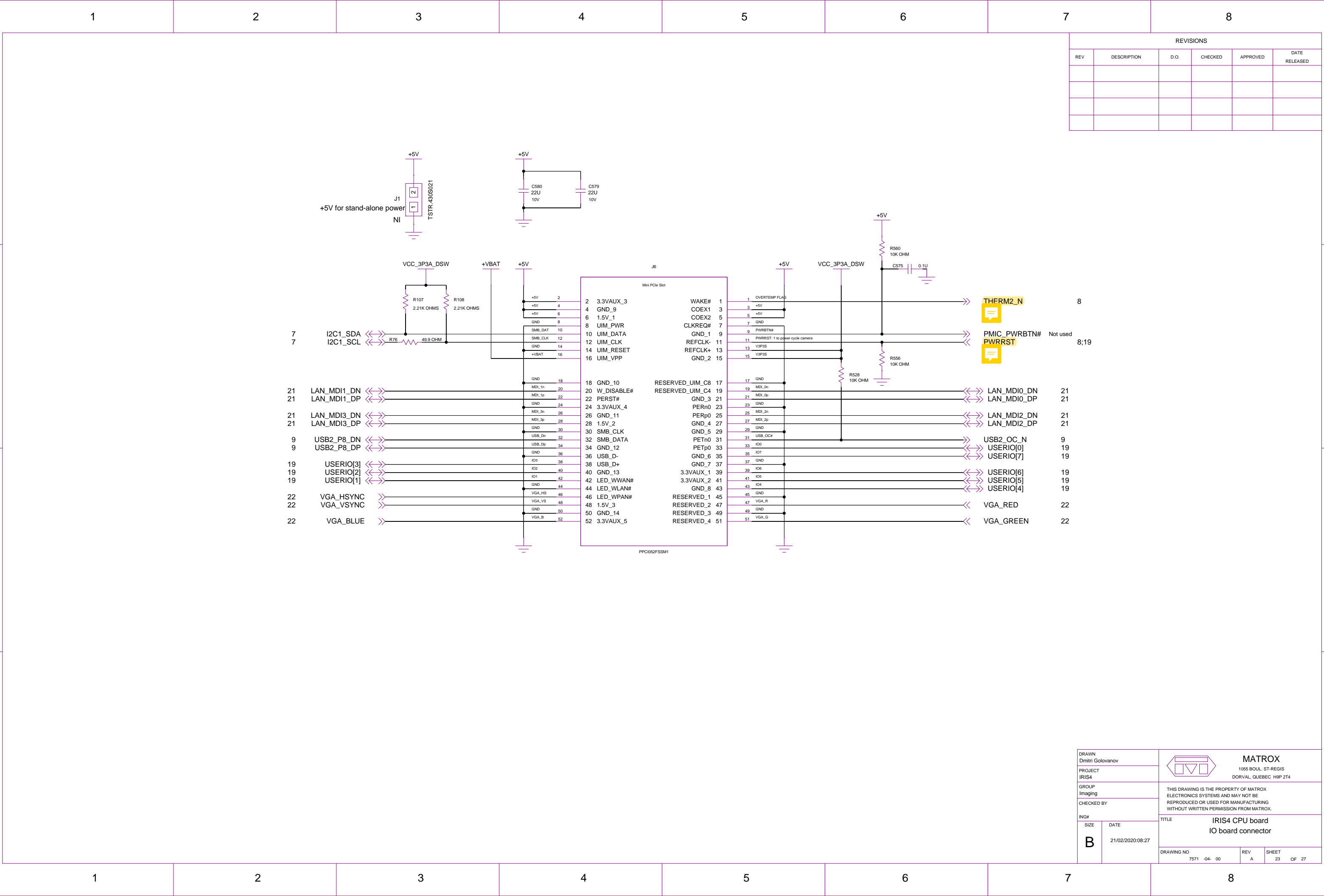
A

D

C


B

A



REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

8	THERM2_N	8
8;19	PMIC_PWRBTN# PWRRST	Not used
21	LAN_MDI0_DN	21
21	LAN_MDI0_DP	21
21	LAN_MDI2_DN	21
21	LAN_MDI2_DP	21
9	USB2_OC_N	9
19	USERIO[0]	19
19	USERIO[7]	19
19	USERIO[6]	19
19	USERIO[5]	19
19	USERIO[4]	19
22	VGA_RED	22
22	VGA_GREEN	22

DRAWN Dmitri Golovanov		 MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX. ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY		TITLE IRIS4 CPU board IO board connector	
ING#			
SIZE B	DATE 21/02/2020:08:27		
DRAWING NO 7571 -04- 00		REV A	SHEET 23 OF 27

D

C

B

A

D

C

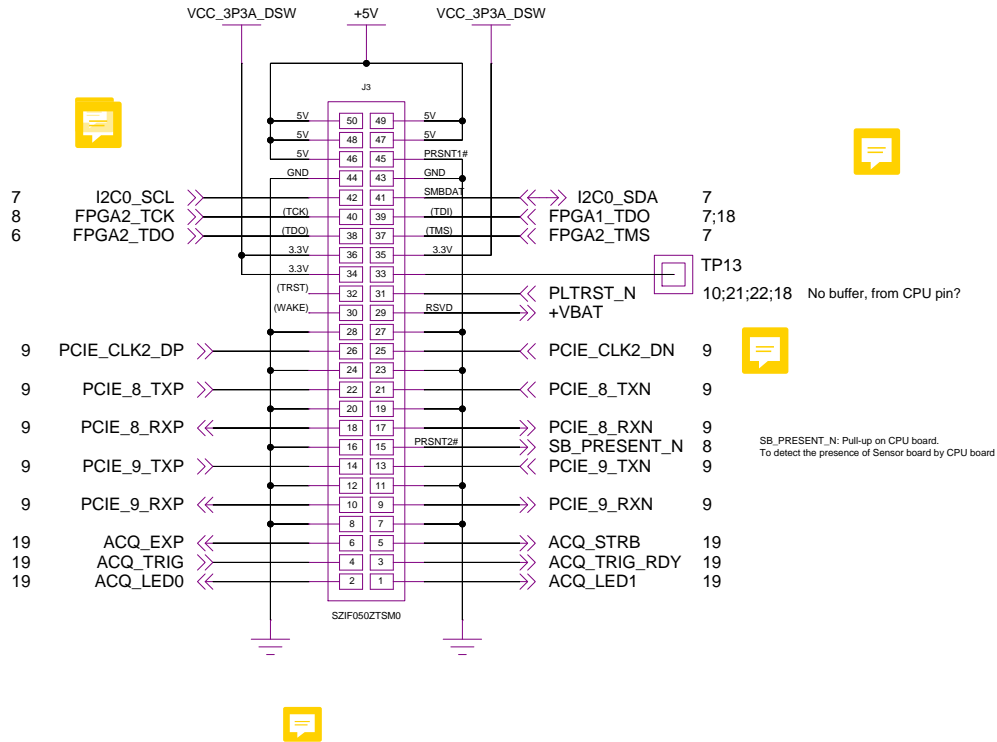
B

A

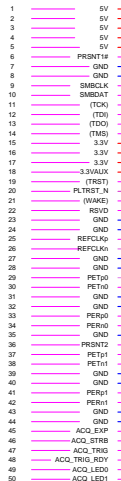
REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED



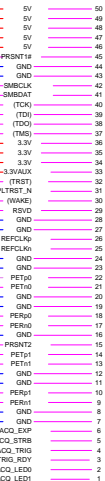
CPU Board ZIF pinout is inverted
Sensor board pos 1 aligned with CPU board pos 50
Connectors are head-to-head with latch on same side




Sensor board connector



CPU board connector



DRAWN Dmitri Golovanov				MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4				THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
GROUP Imaging		CHECKED BY		TITLE IRIS4 CPU board Sensor Board Connector	
ING#		DATE 20/02/2020:15:21		DRAWING NO 7571 -04- 00	
SIZE B		REV A		SHEET 24 OF 27	

D

C

B

A

D

C

B

A

1

2

3

4

5

6

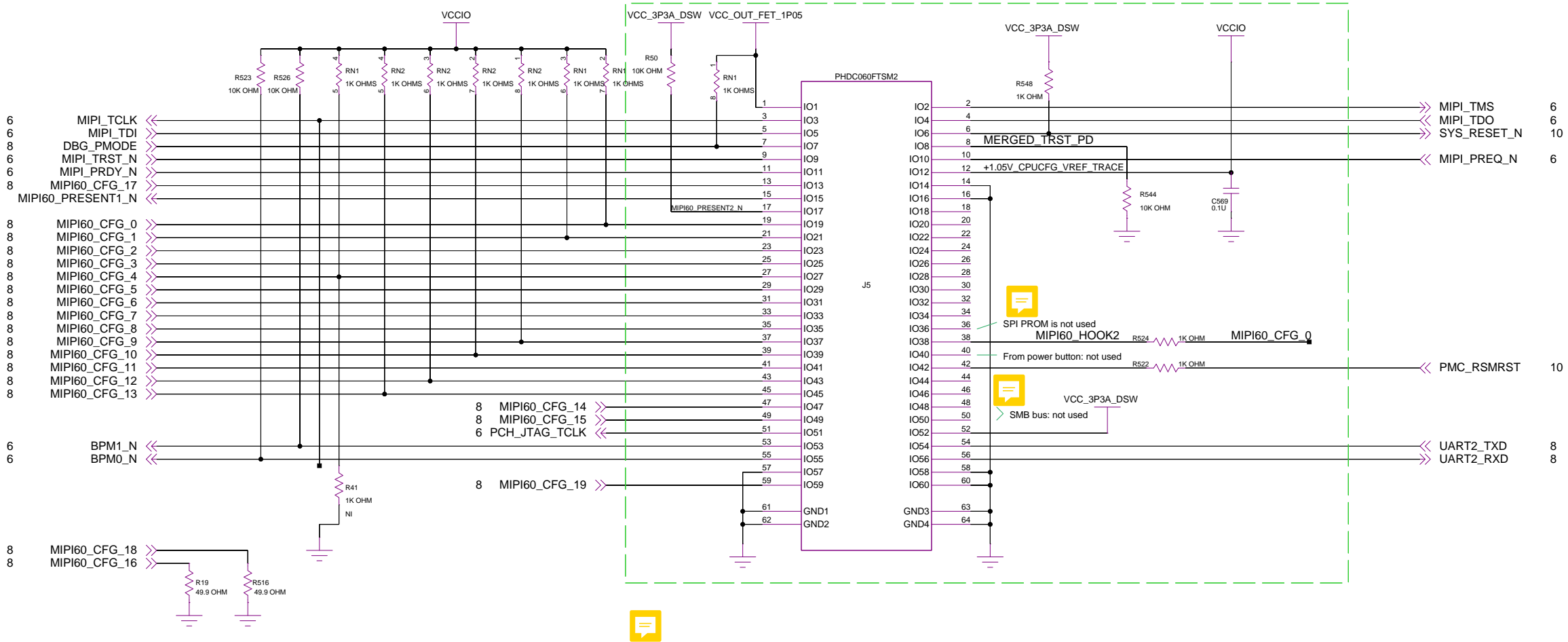
7

8


REVISIONS

REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

The MIPI 60 debug connector could be implemented on a break-away extension of the PCB, on prototype version only.
In this case, all components inside this outline will be disconnected from EHL SoC pins on production revision



SUB=XDP

DRAWN Dmitri Golovanov		 MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY		TITLE IRIS4 CPU board CPU debug port	
ING#			
SIZE B	DATE 12/02/2020:13:39		
DRAWING NO 7571 -04- 00		REV A	SHEET 25 OF 27

1

2

3

4

5

6

7

8

D

C

B

A

D

C

B

A

1

2

3

4

5

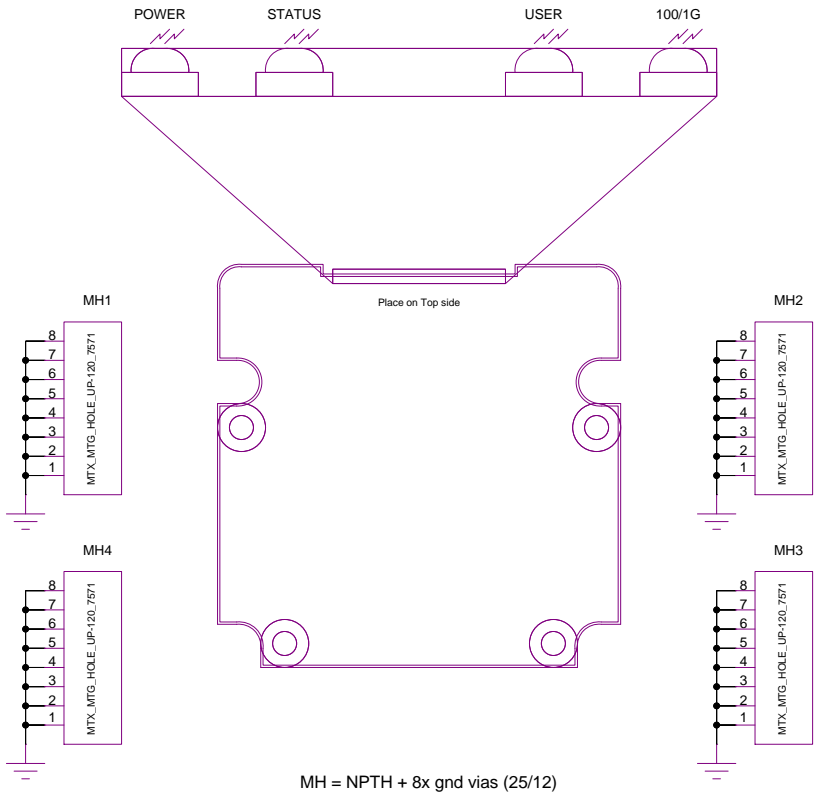
6

7

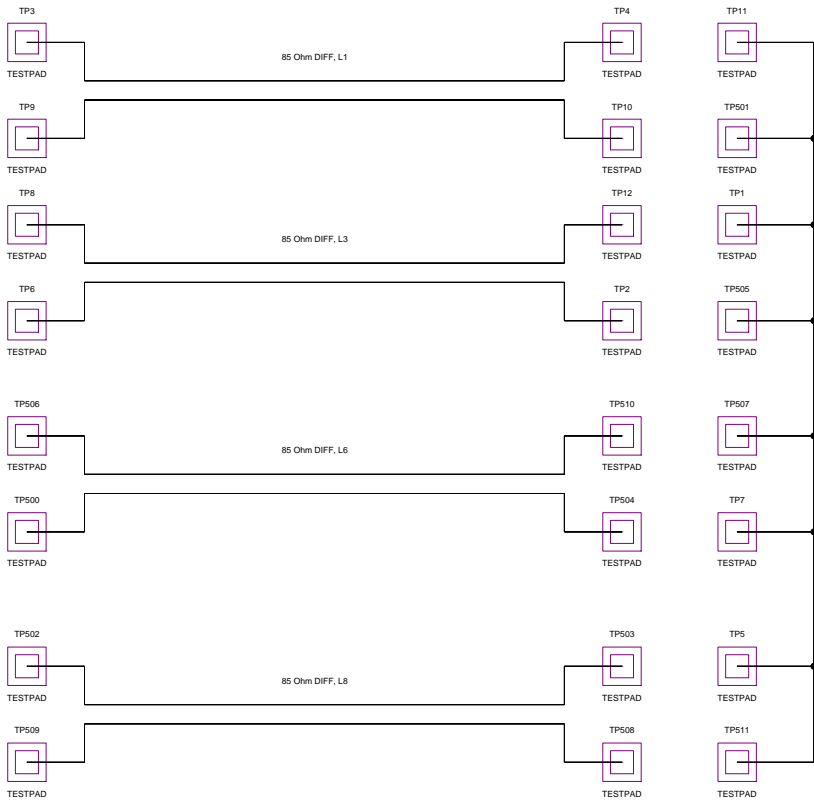
8

REVISIONS

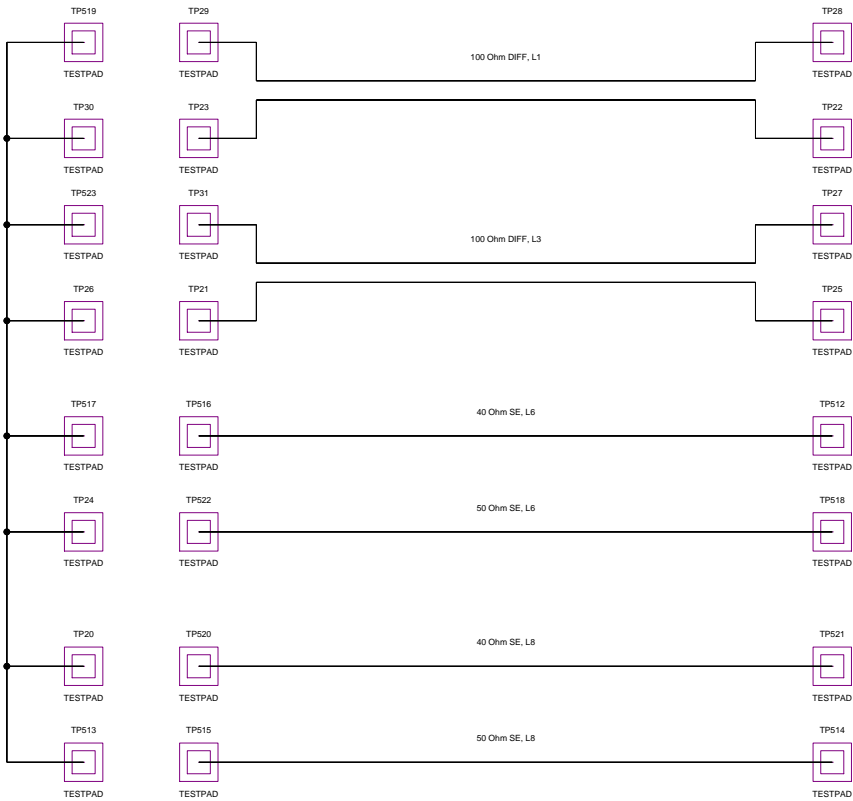
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED




Test coupons on panel upper cracker section
Route straight on full cracker length



Test coupons on panel lower cracker section
Route straight on full cracker length



DRAWN Dmitri Golovanov		 MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4			
GROUP Imaging		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	
CHECKED BY		TITLE IRIS4 CPU board Mounting holes and test coupons	
ING#			
SIZE B	DATE 31/01/2020:09:29		
		DRAWING NO 7571 -04- 00	REV A
		SHEET 26 OF 27	

1

2

3




4

5

6

7

8

	1	2	3	4	5	6	7	8																										
D							REVISIONS																											
							REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED																						
C																																		
B																																		
A																																		
						<table><tr><td colspan="2">DRAWN Dmitri Golovanov</td><td colspan="2" rowspan="4"><div>MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4</div></td></tr><tr><td colspan="2">PROJECT IRIS4</td><td rowspan="3">THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.</td></tr><tr><td colspan="2">GROUP Imaging</td></tr><tr><td colspan="2">CHECKED BY</td></tr><tr><td colspan="2">ING#</td><td colspan="2">TITLE IRIS4 CPU board Revision history</td></tr><tr><td>SIZE</td><td>DATE</td><td colspan="2"></td></tr><tr><td>B</td><td>17/01/2020:15:45</td><td colspan="2"></td></tr><tr><td colspan="2">DRAWING NO 7571 -04- 00</td><td>REV A</td><td>SHEET 27 OF 27</td></tr></table>		DRAWN Dmitri Golovanov		 <div>MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4</div>		PROJECT IRIS4		THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.	GROUP Imaging		CHECKED BY		ING#		TITLE IRIS4 CPU board Revision history		SIZE	DATE			B	17/01/2020:15:45			DRAWING NO 7571 -04- 00		REV A	SHEET 27 OF 27
DRAWN Dmitri Golovanov		 <div>MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4</div>																																
PROJECT IRIS4				THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONICS SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX.																														
GROUP Imaging																																		
CHECKED BY																																		
ING#		TITLE IRIS4 CPU board Revision history																																
SIZE	DATE																																	
B	17/01/2020:15:45																																	
DRAWING NO 7571 -04- 00		REV A	SHEET 27 OF 27																															
	1	2	3	4	5	6	7	8																										