ZC706 EVALUATION PLATFORM HW-Z7-ZC706 (XC7Z045-FFG900)

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		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
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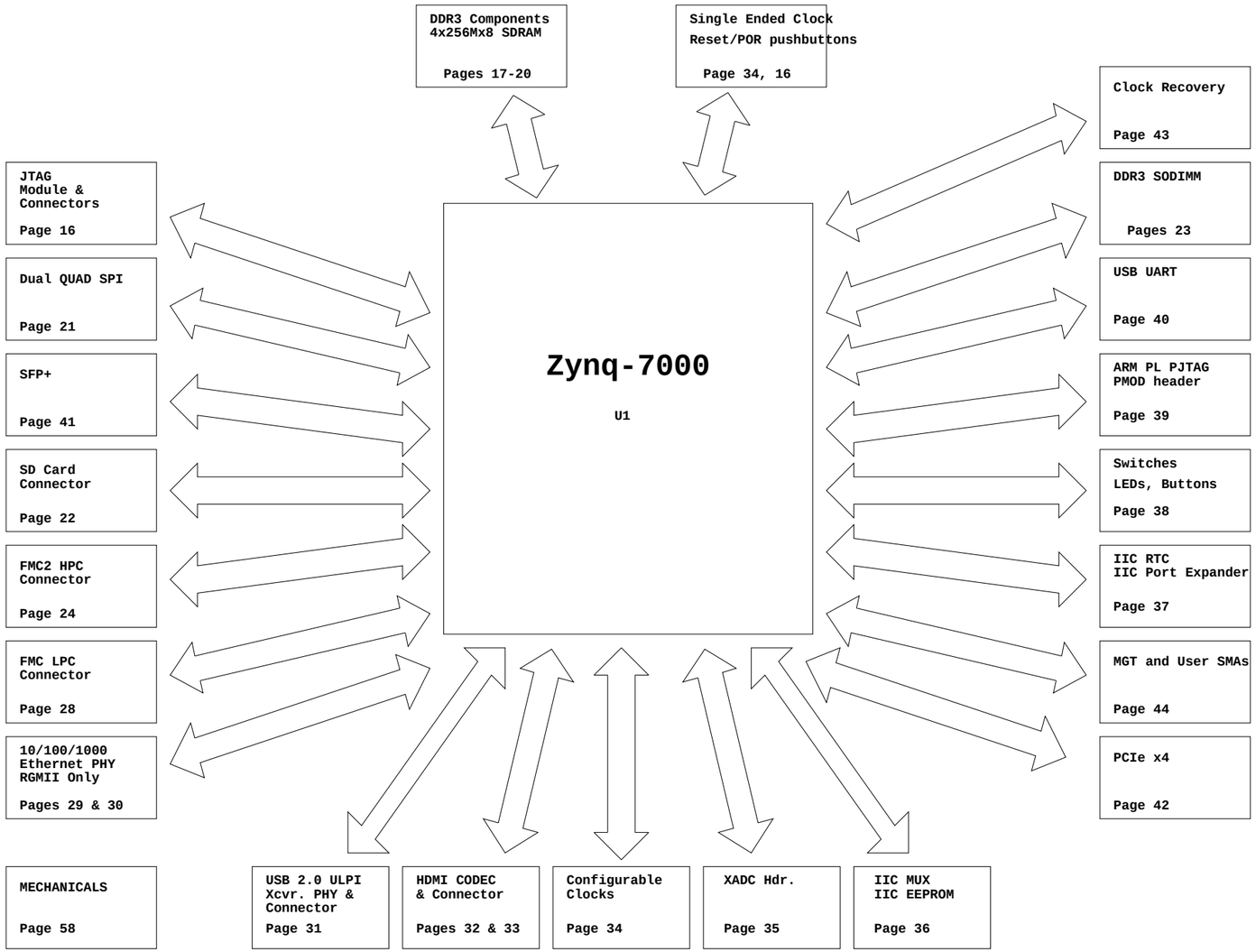

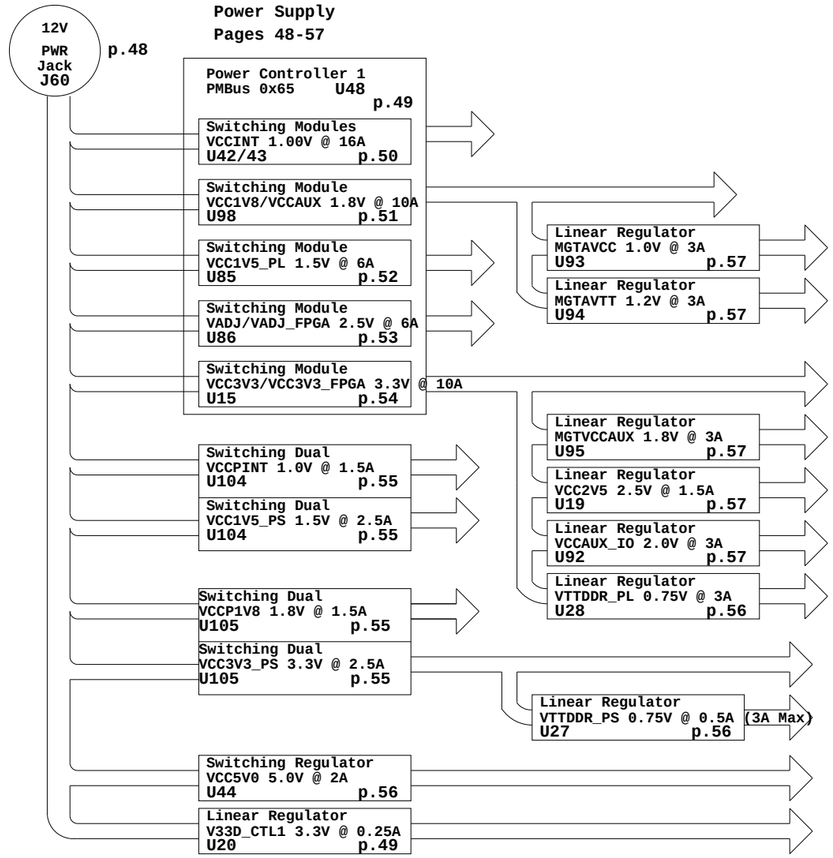

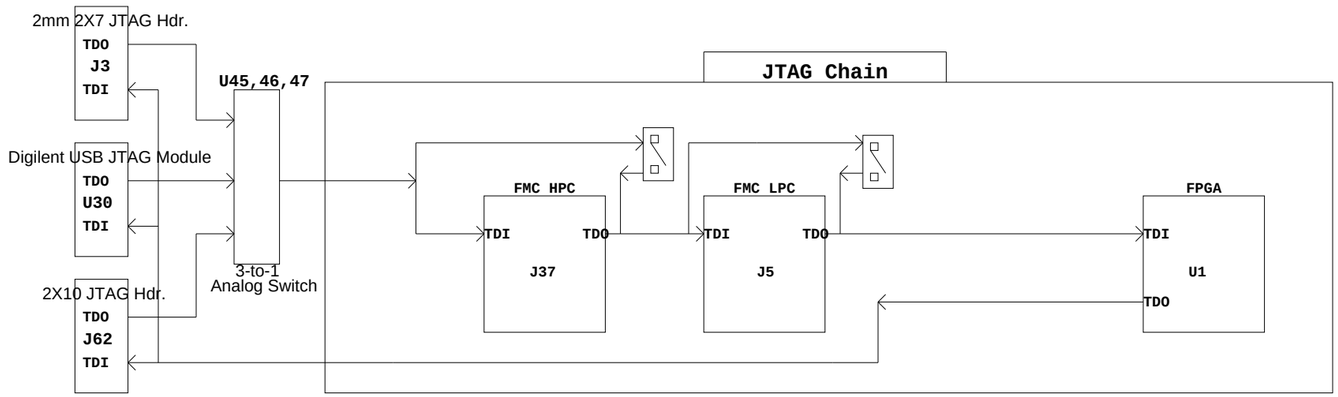

IIC Addressing

0b1110100	PCA9548
0b1011101	SI570
0bxxxxx00	FMC HPC
0bxxxxx00	FMC LPC
0b1010100	IIC EEPROM
0b0100001	IIC Port Expander
0b0111001	ADV7511
0b1100101	PMBUS Controller
0b1010001	IIC RTC
0b1010000	SFP+
0b1101000	SI5324
0b1010000 0b0011000	DDR3 SODIMM

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Title: ZC706 Block Diagram
SCHEM, ROHS COMPLIANT
ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

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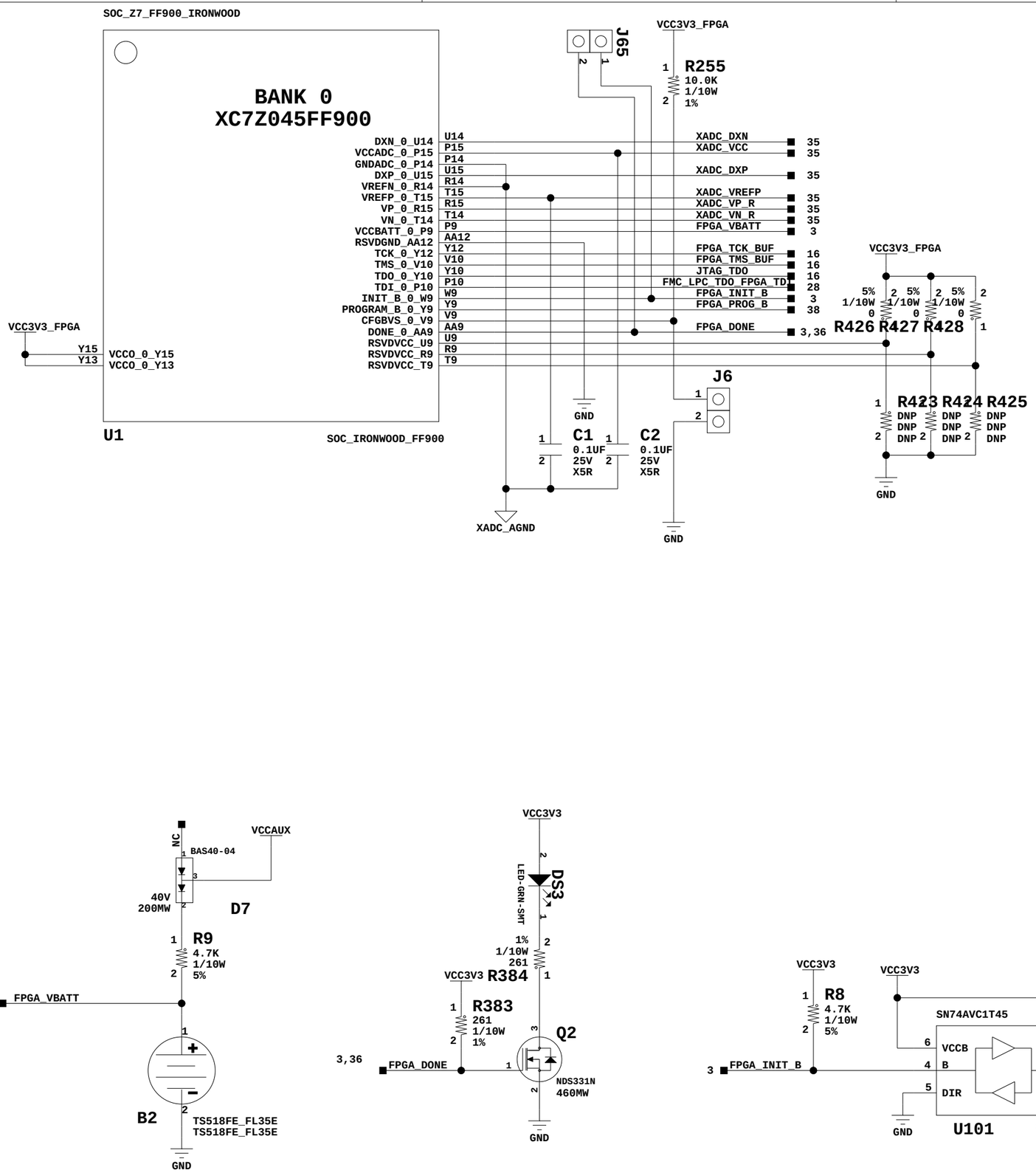

Zynq Bank 0, 9

Title:	Zynq Bank 0, 9 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
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SOC_Z7_FF900_IRONWOOD

BANK 10
XC7Z045FF900

IO_0_10_AA13	AA13		
IO_L1P_T0_10_AK13	AK13	PL_PJTAG_TCK	39
IO_L1N_T0_10_AK12	AK12	PL_PJTAG_TMS	39
IO_L2P_T0_10_AH18	AH18	PL_PJTAG_TDI	39
IO_L2N_T0_10_AJ18	AJ18	IIC_SDA_MAIN_LS	36
IO_L3P_T0_DQS_10_AJ14	AJ14	IIC_SCL_MAIN_LS	36
IO_L3N_T0_DQS_10_AJ13	AJ13	GPIO_DIP_SW3	38
IO_L4P_T0_10_AJ16	AJ16	FMC_LPC_LA11_P	28
IO_L4N_T0_10_AK16	AK16	FMC_LPC_LA11_N	28
IO_L5P_T0_10_AJ15	AJ15	FMC_LPC_LA04_P	28
IO_L5N_T0_10_AK15	AK15	FMC_LPC_LA04_N	28
IO_L6P_T0_10_AH17	AH17	FMC_LPC_LA13_P	28
IO_L6N_T0_VREF_10_AH16	AH16	FMC_LPC_LA13_N	28
IO_L7P_T1_10_AE12	AE12	FMC_LPC_LA02_P	28
IO_L7N_T1_10_AF12	AF12	FMC_LPC_LA02_N	28
IO_L8P_T1_10_AH14	AH14	FMC_LPC_LA09_P	28
IO_L8N_T1_10_AH13	AH13	FMC_LPC_LA09_N	28
IO_L9P_T1_DQS_10_AD14	AD14	FMC_LPC_LA08_P	28
IO_L9N_T1_DQS_10_AD13	AD13	FMC_LPC_LA08_N	28
IO_L10P_T1_10_AG12	AG12	FMC_LPC_LA03_P	28
IO_L10N_T1_10_AH12	AH12	FMC_LPC_LA03_N	28
IO_L11P_T1_SRCC_10_AE13	AE13	FMC_LPC_LA00_CC_P	28
IO_L11N_T1_SRCC_10_AF13	AF13	FMC_LPC_LA00_CC_N	28
IO_L12P_T1_MRCC_10_AF14	AF14	USRCLK_P	34
IO_L12N_T1_MRCC_10_AG14	AG14	USRCLK_N	34
IO_L13P_T2_MRCC_10_AG17	AG17	FMC_LPC_CLK0_M2C_P	28
IO_L13N_T2_MRCC_10_AG16	AG16	FMC_LPC_CLK0_M2C_N	28
IO_L14P_T2_SRCC_10_AF15	AF15	FMC_LPC_LA01_CC_P	28
IO_L14N_T2_SRCC_10_AG15	AG15	FMC_LPC_LA01_CC_N	28
IO_L15P_T2_DQS_10_AF18	AF18	FMC_LPC_LA14_P	28
IO_L15N_T2_DQS_10_AF17	AF17	FMC_LPC_LA14_N	28
IO_L16P_T2_10_AE16	AE16	FMC_LPC_LA05_P	28
IO_L16N_T2_10_AE15	AE15	FMC_LPC_LA05_N	28
IO_L17P_T2_10_AE18	AE18	FMC_LPC_LA16_P	28
IO_L17N_T2_10_AE17	AE17	FMC_LPC_LA16_N	28
IO_L18P_T2_10_AD16	AD16	FMC_LPC_LA12_P	28
IO_L18N_T2_10_AD15	AD15	FMC_LPC_LA12_N	28
IO_L19P_T3_10_AC14	AC14	FMC_LPC_LA10_P	28
IO_L19N_T3_VREF_10_AC13	AC13	FMC_LPC_LA10_N	28
IO_L20P_T3_10_AA15	AA15	FMC_LPC_LA07_P	28
IO_L20N_T3_10_AA14	AA14	FMC_LPC_LA07_N	28
IO_L21P_T3_DQS_10_AB12	AB12	FMC_LPC_LA06_P	28
IO_L21N_T3_DQS_10_AC12	AC12	FMC_LPC_LA06_N	28
IO_L22P_T3_10_AB15	AB15	FMC_LPC_LA15_P	28
IO_L22N_T3_10_AB14	AB14	FMC_LPC_LA15_N	28
IO_L23P_T3_10_AC17	AC17	GPIO_DIP_SW2	38
IO_L23N_T3_10_AC16	AC16	GPIO_DIP_SW1	38
IO_L24P_T3_10_AB17	AB17	GPIO_DIP_SW0	38
IO_L24N_T3_10_AB16	AB16	PMOD1_3_LS	39
IO_25_10_AA17	AA17	IIC_RTC_IRQ_1_B	37

PL_PJTAG_TDO_R — R154 22 1/10W 1% — PL_PJTAG_TDO 39

VADJ_FPGA

AA16	VCCO_10_AA16
AB13	VCCO_10_AB13
AD17	VCCO_10_AD17
AE14	VCCO_10_AE14
AG18	VCCO_10_AG18
AH15	VCCO_10_AH15
AJ12	VCCO_10_AJ12

U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK 11
XC7Z045FF900

IO_0_11_W23	W23	SI5324_RST_LS	47
IO_L1P_T0_11_AJ25	AJ25	SI5324_INT_ALM_LS	47
IO_L1N_T0_11_AK25	AK25	GPIO_SW_LEFT	38
IO_L2P_T0_11_AK22	AK22	PCIE_WAKE_B_LS	47
IO_L2N_T0_11_AK23	AK23	PCIE_PERST_LS	47
IO_L3P_T0_DQS_11_AJ21	AJ21	PMOD1_0_LS	39
IO_L3N_T0_DQS_11_AK21	AK21	PMOD1_1_LS	39
IO_L4P_T0_11_AJ23	AJ23	FMC_HPC_LA07_P	26
IO_L4N_T0_11_AJ24	AJ24	FMC_HPC_LA07_N	26
IO_L5P_T0_11_AH23	AH23	FMC_HPC_LA05_P	24
IO_L5N_T0_11_AH24	AH24	FMC_HPC_LA05_N	24
IO_L6P_T0_11_AG22	AG22	FMC_HPC_LA06_P	24
IO_L6N_T0_VREF_11_AH22	AH22	FMC_HPC_LA06_N	24
IO_L7P_T1_11_AC24	AC24	FMC_HPC_LA14_P	24
IO_L7N_T1_11_AD24	AD24	FMC_HPC_LA14_N	24
IO_L8P_T1_11_AG24	AG24	FMC_HPC_LA10_P	24
IO_L8N_T1_11_AG25	AG25	FMC_HPC_LA10_N	24
IO_L9P_T1_DQS_11_AF23	AF23	FMC_HPC_LA12_P	25
IO_L9N_T1_DQS_11_AF24	AF24	FMC_HPC_LA12_N	25
IO_L10P_T1_11_AD21	AD21	FMC_HPC_LA09_P	24
IO_L10N_T1_11_AE21	AE21	FMC_HPC_LA09_N	24
IO_L11P_T1_SRCC_11_AD23	AD23	FMC_HPC_LA11_P	26
IO_L11N_T1_SRCC_11_AE23	AE23	FMC_HPC_LA11_N	26
IO_L12P_T1_MRCC_11_AE22	AE22	FMC_HPC_CLK0_M2C_P	26
IO_L12N_T1_MRCC_11_AF22	AF22	FMC_HPC_CLK0_M2C_N	26
IO_L13P_T2_MRCC_11_AG21	AG21	FMC_HPC_LA01_CC_P	24
IO_L13N_T2_MRCC_11_AH21	AH21	FMC_HPC_LA01_CC_N	24
IO_L14P_T2_SRCC_11_AF20	AF20	FMC_HPC_LA00_CC_P	25
IO_L14N_T2_SRCC_11_AG20	AG20	FMC_HPC_LA00_CC_N	25
IO_L15P_T2_DQS_11_AJ20	AJ20	FMC_HPC_LA04_P	26
IO_L15N_T2_DQS_11_AK20	AK20	FMC_HPC_LA04_N	26
IO_L16P_T2_11_AK17	AK17	FMC_HPC_LA02_P	26
IO_L16N_T2_11_AK18	AK18	FMC_HPC_LA02_N	26
IO_L17P_T2_11_AH19	AH19	FMC_HPC_LA03_P	25
IO_L17N_T2_11_AJ19	AJ19	FMC_HPC_LA03_N	25
IO_L18P_T2_11_AF19	AF19	FMC_HPC_LA08_P	25
IO_L18N_T2_11_AG19	AG19	FMC_HPC_LA08_N	25
IO_L19P_T3_11_AB21	AB21	PMOD1_2_LS	39
IO_L19N_T3_VREF_11_AB22	AB22	HDMI_SPDIF_OUT_LS	38
IO_L20P_T3_11_W21	W21	GPIO_LED_RIGHT	38
IO_L20N_T3_11_Y21	Y21	GPIO_LED_LEFT	38
IO_L21P_T3_DQS_11_Y22	Y22	FMC_HPC_LA15_P	26
IO_L21N_T3_DQS_11_Y23	Y23	FMC_HPC_LA15_N	26
IO_L22P_T3_11_AA24	AA24	FMC_HPC_LA16_P	25
IO_L22N_T3_11_AB24	AB24	FMC_HPC_LA16_N	25
IO_L23P_T3_11_AA22	AA22	FMC_HPC_LA13_P	24
IO_L23N_T3_11_AA23	AA23	FMC_HPC_LA13_N	24
IO_L24P_T3_11_AC22	AC22	HDMI_R_D35	33
IO_L24N_T3_11_AC23	AC23	HDMI_INT	32
IO_25_11_AC21	AC21	HDMI_R_SPDIF	33

VADJ_FPGA

AB23	VCCO_11_AB23
AE24	VCCO_11_AE24
AF21	VCCO_11_AF21
AH25	VCCO_11_AH25
AJ22	VCCO_11_AJ22
AK19	VCCO_11_AK19
W22	VCCO_11_W22

U1 SOC_IRONWOOD_FF900

Zynq Bank 10, 11

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Title:	Zynq Bank 10, 11 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431760 1280681 0381513
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SOC_Z7_FF900_IRONWOOD

BANK 12
XC7Z045FF900

IO_0_12_Y25	Y25	HDMI_R_D21	33
IO_L1P_T0_12_Y30	Y30	FMC_LPC_LA33_P	28
IO_L1N_T0_12_AA30	AA30	FMC_LPC_LA33_N	28
IO_L2P_T0_12_AB29	AB29	FMC_LPC_LA30_P	28
IO_L2N_T0_12_AB30	AB30	FMC_LPC_LA30_N	28
IO_L3P_T0_DQS_12_Y26	Y26	FMC_LPC_LA32_P	28
IO_L3N_T0_DQS_12_Y27	Y27	FMC_LPC_LA32_N	28
IO_L4P_T0_12_Y28	Y28	HDMI_R_D28	33
IO_L4N_T0_12_AA29	AA29	HDMI_R_D22	33
IO_L5P_T0_12_AA27	AA27	HDMI_R_D31	33
IO_L5N_T0_12_AA28	AA28	HDMI_R_D18	33
IO_L6P_T0_12_AB25	AB25	HDMI_R_D10	33
IO_L6N_T0_VREF_12_AB26	AB26	HDMI_R_D17	33
IO_L7P_T1_12_AC26	AC26	HDMI_R_D19	33
IO_L7N_T1_12_AD26	AD26	HDMI_R_D16	33
IO_L8P_T1_12_AD30	AD30	HDMI_R_D23	33
IO_L8N_T1_12_AE30	AE30	HDMI_R_D20	33
IO_L9P_T1_DQS_12_AC29	AC29	FMC_LPC_LA31_P	28
IO_L9N_T1_DQS_12_AD29	AD29	FMC_LPC_LA31_N	28
IO_L10P_T1_12_AD25	AD25	FMC_LPC_LA28_P	28
IO_L10N_T1_12_AE26	AE26	FMC_LPC_LA28_N	28
IO_L11P_T1_SRCC_12_AB27	AB27	FMC_LPC_LA17_CC_P	28
IO_L11N_T1_SRCC_12_AC27	AC27	FMC_LPC_LA17_CC_N	28
IO_L12P_T1_MRCC_12_AC28	AC28	FMC_LPC_CLK1_M2C_P	28
IO_L12N_T1_MRCC_12_AD28	AD28	FMC_LPC_CLK1_M2C_N	28
IO_L13P_T2_MRCC_12_AE28	AE28	HDMI_R_D8	33
IO_L13N_T2_MRCC_12_AF28	AF28	HDMI_R_D29	33
IO_L14P_T2_SRCC_12_AE27	AE27	FMC_LPC_LA18_CC_P	28
IO_L14N_T2_SRCC_12_AF27	AF27	FMC_LPC_LA18_CC_N	28
IO_L15P_T2_DQS_12_AF29	AF29	FMC_LPC_LA25_P	28
IO_L15N_T2_DQS_12_AG29	AG29	FMC_LPC_LA25_N	28
IO_L16P_T2_12_AF30	AF30	FMC_LPC_LA24_P	28
IO_L16N_T2_12_AG30	AG30	FMC_LPC_LA24_N	28
IO_L17P_T2_12_AG26	AG26	FMC_LPC_LA20_P	28
IO_L17N_T2_12_AG27	AG27	FMC_LPC_LA20_N	28
IO_L18P_T2_12_AE25	AE25	FMC_LPC_LA29_P	28
IO_L18N_T2_12_AF25	AF25	FMC_LPC_LA29_N	28
IO_L19P_T3_12_AH28	AH28	FMC_LPC_LA21_P	28
IO_L19N_T3_VREF_12_AH29	AH29	FMC_LPC_LA21_N	28
IO_L20P_T3_12_AJ30	AJ30	FMC_LPC_LA26_P	28
IO_L20N_T3_12_AK30	AK30	FMC_LPC_LA26_N	28
IO_L21P_T3_DQS_12_AJ28	AJ28	FMC_LPC_LA27_P	28
IO_L21N_T3_DQS_12_AJ29	AJ29	FMC_LPC_LA27_N	28
IO_L22P_T3_12_AK27	AK27	FMC_LPC_LA22_P	28
IO_L22N_T3_12_AK28	AK28	FMC_LPC_LA22_N	28
IO_L23P_T3_12_AH26	AH26	FMC_LPC_LA19_P	28
IO_L23N_T3_12_AH27	AH27	FMC_LPC_LA19_N	28
IO_L24P_T3_12_AJ26	AJ26	FMC_LPC_LA23_P	28
IO_L24N_T3_12_AK26	AK26	FMC_LPC_LA23_N	28
IO_25_12_AA25	AA25	HDMI_R_D7	33

VADJ_FPGA

AA26	VCCO_12_AA26
AC30	VCCO_12_AC30
AD27	VCCO_12_AD27
AG28	VCCO_12_AG28
AK29	VCCO_12_AK29
Y29	VCCO_12_Y29

U1

SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK 13
XC7Z045FF900

IO_0_13_U21	U21	HDMI_R_VSYNC	33
IO_L1P_T0_13_P30	P30	FMC_HPC_LA28_P	26
IO_L1N_T0_13_R30	R30	FMC_HPC_LA28_N	26
IO_L2P_T0_13_T30	T30	FMC_HPC_LA24_P	26
IO_L2N_T0_13_U30	U30	FMC_HPC_LA24_N	26
IO_L3P_T0_DQS_13_N28	N28	HDMI_R_D33	33
IO_L3N_T0_DQS_13_P28	P28	HDMI_R_CLK	33
IO_L4P_T0_13_N29	N29	FMC_HPC_LA31_P	25
IO_L4N_T0_13_P29	P29	FMC_HPC_LA31_N	25
IO_L5P_T0_13_T29	T29	FMC_HPC_LA25_P	25
IO_L5N_T0_13_U29	U29	FMC_HPC_LA25_N	25
IO_L6P_T0_13_R28	R28	FMC_HPC_LA26_P	24
IO_L6N_T0_VREF_13_T28	T28	FMC_HPC_LA26_N	24
IO_L7P_T1_13_V28	V28	FMC_HPC_LA27_P	24
IO_L7N_T1_13_V29	V29	FMC_HPC_LA27_N	24
IO_L8P_T1_13_W29	W29	FMC_HPC_LA21_P	26
IO_L8N_T1_13_W30	W30	FMC_HPC_LA21_N	26
IO_L9P_T1_DQS_13_V27	V27	FMC_HPC_LA22_P	25
IO_L9N_T1_DQS_13_W28	W28	FMC_HPC_LA22_N	25
IO_L10P_T1_13_W25	W25	FMC_HPC_LA18_CC_P	24
IO_L10N_T1_13_W26	W26	FMC_HPC_LA18_CC_N	24
IO_L11P_T1_SRCC_13_U25	U25	FMC_HPC_LA20_P	25
IO_L11N_T1_SRCC_13_V26	V26	FMC_HPC_LA20_N	25
IO_L12P_T1_MRCC_13_U26	U26	FMC_HPC_CLK1_M2C_P	25
IO_L12N_T1_MRCC_13_U27	U27	FMC_HPC_CLK1_M2C_N	25
IO_L13P_T2_MRCC_13_R25	R25	FMC_HPC_LA29_P	25
IO_L13N_T2_MRCC_13_R26	R26	FMC_HPC_LA29_N	25
IO_L14P_T2_SRCC_13_R27	R27	GPIO_SW_RIGHT	38
IO_L14N_T2_SRCC_13_T27	T27	HDMI_R_D11	3
IO_L15P_T2_DQS_13_N26	N26	FMC_HPC_LA33_P	25
IO_L15N_T2_DQS_13_N27	N27	FMC_HPC_LA33_N	25
IO_L16P_T2_13_P25	P25	FMC_HPC_LA23_P	24
IO_L16N_T2_13_P26	P26	FMC_HPC_LA23_N	24
IO_L17P_T2_13_T24	T24	FMC_HPC_LA19_P	26
IO_L17N_T2_13_T25	T25	FMC_HPC_LA19_N	26
IO_L18P_T2_13_P23	P23	FMC_HPC_LA30_P	26
IO_L18N_T2_13_P24	P24	FMC_HPC_LA30_N	26
IO_L19P_T3_13_P21	P21	FMC_HPC_LA32_P	26
IO_L19N_T3_VREF_13_R21	R21	FMC_HPC_LA32_N	26
IO_L20P_T3_13_T22	T22	HDMI_R_D5	33
IO_L20N_T3_13_T23	T23	HDMI_R_D9	33
IO_L21P_T3_DQS_13_R22	R22	HDMI_R_HSYNC	33
IO_L21N_T3_DQS_13_R23	R23	HDMI_R_D6	33
IO_L22P_T3_13_U22	U22	HDMI_R_D32	33
IO_L22N_T3_13_V22	V22	HDMI_R_D30	33
IO_L23P_T3_13_U24	U24	HDMI_R_D4	33
IO_L23N_T3_13_V24	V24	HDMI_R_DE	33
IO_L24P_T3_13_V23	V23	FMC_HPC_LA17_CC_P	24
IO_L24N_T3_13_W24	W24	FMC_HPC_LA17_CC_N	24
IO_25_13_V21	V21	HDMI_R_D34	33

VADJ_FPGA

N30	VCCO_13_N30
P27	VCCO_13_P27
R24	VCCO_13_R24
T21	VCCO_13_T21
U28	VCCO_13_U28
V25	VCCO_13_V25

U1

SOC_IRONWOOD_FF900

Zynq Bank 12, 13

XILINX

Title:	Zynq Bank 12, 13 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431760 1280681 0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	5 of 58	Drawn By	BF

SOC_Z7_FF900_IRONWOOD

VTTVREF_SODIMM

C326
0.01UF
25V
X7R

GND

BANK 33
XC7Z045FF900

IO_0_VRN_33_L5	L5	VRN_33	
IO_L1P_T0_33_J4	J4	PL_DDR3_D3	6
IO_L1N_T0_33_J3	J3	PL_DDR3_DM0	23
IO_L2P_T0_33_L1	L1	PL_DDR3_D0	23
IO_L2N_T0_33_K1	K1	PL_DDR3_D4	23
IO_L3P_T0_DQS_33_K3	K3	PL_DDR3_DQS0_P	23
IO_L3N_T0_DQS_33_K2	K2	PL_DDR3_DQS0_N	23
IO_L4P_T0_33_L3	L3	PL_DDR3_D5	23
IO_L4N_T0_33_L2	L2	PL_DDR3_D1	23
IO_L5P_T0_33_K5	K5	PL_DDR3_D2	23
IO_L5N_T0_33_J5	J5	PL_DDR3_D6	23
IO_L6P_T0_33_K6	K6	PL_DDR3_D7	23
IO_L6N_T0_VREF_33_J6	J6		
IO_L7P_T1_33_G2	G2	GPIO_LED_CENTER	
IO_L7N_T1_33_F2	F2	PL_DDR3_DM1	38
IO_L8P_T1_33_H6	H6	PL_DDR3_D10	23
IO_L8N_T1_33_G6	G6	PL_DDR3_D8	23
IO_L9P_T1_DQS_33_J1	J1	PL_DDR3_DQS1_P	23
IO_L9N_T1_DQS_33_H1	H1	PL_DDR3_DQS1_N	23
IO_L10P_T1_33_H2	H2	PL_DDR3_D13	23
IO_L10N_T1_33_G1	G1	PL_DDR3_D12	23
IO_L11P_T1_SRCC_33_H4	H4	PL_DDR3_D9	23
IO_L11N_T1_SRCC_33_H3	H3	PL_DDR3_D11	23
IO_L12P_T1_MRCC_33_G5	G5	PL_DDR3_D14	23
IO_L12N_T1_MRCC_33_G4	G4	PL_DDR3_D15	23
IO_L13P_T2_MRCC_33_F5	F5	NC	
IO_L13N_T2_MRCC_33_E5	E5	PL_DDR3_D19	23
IO_L14P_T2_SRCC_33_F4	F4	PL_DDR3_D20	23
IO_L14N_T2_SRCC_33_F3	F3	PL_DDR3_D21	23
IO_L15P_T2_DQS_33_E6	E6	PL_DDR3_DQS2_P	23
IO_L15N_T2_DQS_33_D5	D5	PL_DDR3_DQS2_N	23
IO_L16P_T2_33_D4	D4	PL_DDR3_D18	23
IO_L16N_T2_33_D3	D3	PL_DDR3_D23	23
IO_L17P_T2_33_E3	E3	PL_DDR3_D17	23
IO_L17N_T2_33_E2	E2	PL_DDR3_D16	23
IO_L18P_T2_33_E1	E1	PL_DDR3_DM2	23
IO_L18N_T2_33_D1	D1	PL_DDR3_D22	23
IO_L19P_T3_33_C4	C4	PL_DDR3_D31	23
IO_L19N_T3_VREF_33_C3	C3		
IO_L20P_T3_33_B5	B5	PL_DDR3_D27	23
IO_L20N_T3_33_B4	B4	PL_DDR3_D26	23
IO_L21P_T3_DQS_33_A5	A5	PL_DDR3_DQS3_P	23
IO_L21N_T3_DQS_33_A4	A4	PL_DDR3_DQS3_N	23
IO_L22P_T3_33_C2	C2	PL_DDR3_DM3	23
IO_L22N_T3_33_C1	C1	PL_DDR3_D30	23
IO_L23P_T3_33_B2	B2	PL_DDR3_D25	23
IO_L23N_T3_33_B1	B1	PL_DDR3_D29	23
IO_L24P_T3_33_A3	A3	PL_DDR3_D28	23
IO_L24N_T3_33_A2	A2	PL_DDR3_D24	23
IO_25_VRP_33_L4	L4	VRP_33	6

VCC1V5_PL

B3	VCCO_33_B3
E4	VCCO_33_E4
F1	VCCO_33_F1
H5	VCCO_33_H5
J2	VCCO_33_J2
L6	VCCO_33_L6

U1

SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

VTTVREF_SODIMM

C713
0.01UF
25V
X7R

GND

BANK 34
XC7Z045FF900

IO_0_VRN_34_M12	M12	NC	
IO_L1P_T0_34_B10	B10	PL_DDR3_A8	23
IO_L1N_T0_34_A10	A10	PL_DDR3_A13	23
IO_L2P_T0_34_B9	B9	PL_DDR3_A1	23
IO_L2N_T0_34_A9	A9	PL_DDR3_A3	23
IO_L3P_T0_DQS_PUDC_B_34_A8	A8	PL_CPU_RESET	38
IO_L3N_T0_DQS_34_A7	A7	PL_DDR3_BA2	23
IO_L4P_T0_34_C7	C7	PL_DDR3_CKE1	23
IO_L4N_T0_34_B7	B7	PL_DDR3_A11	23
IO_L5P_T0_34_C6	C6	PL_DDR3_A15	23
IO_L5N_T0_34_B6	B6	PL_DDR3_A5	23
IO_L6P_T0_34_C9	C9	PL_DDR3_ODT1	23
IO_L6N_T0_VREF_34_C8	C8		
IO_L7P_T1_34_J11	J11	PL_DDR3_S0_B	
IO_L7N_T1_34_H11	H11	PL_DDR3_RAS_B	23
IO_L8P_T1_34_E11	E11	PL_DDR3_A2	23
IO_L8N_T1_34_D11	D11	PL_DDR3_A4	23
IO_L9P_T1_DQS_34_H12	H12	PL_DDR3_A12	23
IO_L9N_T1_DQS_34_G11	G11	PL_DDR3_A14	23
IO_L10P_T1_34_E10	E10	PL_DDR3_A0	23
IO_L10N_T1_34_D10	D10	PL_DDR3_CKE0	23
IO_L11P_T1_SRCC_34_G10	G10	PL_DDR3_CLK0_P	23
IO_L11N_T1_SRCC_34_F10	F10	PL_DDR3_CLK0_N	23
IO_L12P_T1_MRCC_34_D9	D9	PL_DDR3_CLK1_P	23
IO_L12N_T1_MRCC_34_D8	D8	PL_DDR3_CLK1_N	23
IO_L13P_T2_MRCC_34_H9	H9	SYSCLK_P	34
IO_L13N_T2_MRCC_34_G9	G9	SYSCLK_N	34
IO_L14P_T2_SRCC_34_F9	F9	PL_DDR3_A6	23
IO_L14N_T2_SRCC_34_E8	E8	PL_DDR3_A7	23
IO_L15P_T2_DQS_34_J8	J8	PL_DDR3_A9	23
IO_L15N_T2_DQS_34_H8	H8	PL_DDR3_S1_B	23
IO_L16P_T2_34_F8	F8	PL_DDR3_BA0	23
IO_L16N_T2_34_F7	F7	PL_DDR3_WE_B	23
IO_L17P_T2_34_E7	E7	PL_DDR3_CAS_B	23
IO_L17N_T2_34_D6	D6	PL_DDR3_A10	23
IO_L18P_T2_34_H7	H7	PL_DDR3_BA1	23
IO_L18N_T2_34_G7	G7	PL_DDR3_ODT0	23
IO_L19P_T3_34_L7	L7	PL_DDR3_D39	23
IO_L19N_T3_VREF_34_K7	K7		
IO_L20P_T3_34_J10	J10	PL_DDR3_D38	23
IO_L20N_T3_34_J9	J9	PL_DDR3_D35	23
IO_L21P_T3_DQS_34_L8	L8	PL_DDR3_DQS4_P	23
IO_L21N_T3_DQS_34_K8	K8	PL_DDR3_DQS4_N	23
IO_L22P_T3_34_K11	K11	PL_DDR3_D36	23
IO_L22N_T3_34_K10	K10	PL_DDR3_D32	23
IO_L23P_T3_34_L10	L10	PL_DDR3_D37	23
IO_L23N_T3_34_L9	L9	PL_DDR3_D33	23
IO_L24P_T3_34_L12	L12	PL_DDR3_DM4	23
IO_L24N_T3_34_K12	K12	PL_DDR3_D34	23
IO_25_VRP_34_M10	M10	PL_DDR3_TEMP_EVENT	23

VCC1V5_PL

A6	VCCO_34_A6
C10	VCCO_34_C10
D7	VCCO_34_D7
F11	VCCO_34_F11
G8	VCCO_34_G8
J12	VCCO_34_J12
K9	VCCO_34_K9

U1

SOC_IRONWOOD_FF900

VCC1V5_PL

R510
80.6
1/10W
1%

6 VRN_33

6 VRP_33

R511
80.6
1/10W
1%

GND

Zynq Bank 33, 34

XILINX

Title:	Zynq Bank 33, 34 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	6 of 58	Drawn By	BF

SOC_Z7_FF900_IRONWOOD

VTTVREF_SODIMM

C327
0.01UF
25V
X7R
GND

BANK 35
XC7Z045FF900

IO_0_VRN_35_K16	K16	VRN_35	
IO_L1P_T0_AD0P_35_L15	L15	XADC_VAUX0P_R	7
IO_L1N_T0_AD0N_35_L14	L14	XADC_VAUX0N_R	35
IO_L2P_T0_AD8P_35_J13	J13	XADC_VAUX8P_R	35
IO_L2N_T0_AD8N_35_H13	H13	XADC_VAUX8N_R	35
IO_L3P_T0_DQS_AD1P_35_L13	L13	XADC_AD1_R_P	35
IO_L3N_T0_DQS_AD1N_35_K13	K13	XADC_AD1_R_N	46
IO_L4P_T0_35_J14	J14	XADC_GPIO_3	46
IO_L4N_T0_35_H14	H14	XADC_GPIO_0	35
IO_L5P_T0_AD9P_35_K15	K15	GPIO_SW_CENTER	35
IO_L5N_T0_AD9N_35_J15	J15	XADC_GPIO_1	38
IO_L6P_T0_35_J16	J16	XADC_GPIO_2	35
IO_L6N_T0_VREF_35_H16	H16		35
IO_L7P_T1_AD2P_35_G17	G17	PL_DDR3_RESET_B	
IO_L7N_T1_AD2N_35_G16	G16	PL_DDR3_D43	23
IO_L8P_T1_AD10P_35_G15	G15	PL_DDR3_D44	23
IO_L8N_T1_AD10N_35_G14	G14	PL_DDR3_DM5	23
IO_L9P_T1_DQS_AD3P_35_G12	G12	PL_DDR3_DQS5_P	23
IO_L9N_T1_DQS_AD3N_35_F12	F12	PL_DDR3_DQS5_N	23
IO_L10P_T1_AD11P_35_F13	F13	PL_DDR3_D42	23
IO_L10N_T1_AD11N_35_E12	E12	PL_DDR3_D45	23
IO_L11P_T1_SRCC_35_E13	E13	PL_DDR3_D47	23
IO_L11N_T1_SRCC_35_D13	D13	PL_DDR3_D46	23
IO_L12P_T1_MRCC_35_F15	F15	PL_DDR3_D41	23
IO_L12N_T1_MRCC_35_F14	F14	PL_DDR3_D40	23
IO_L13P_T2_MRCC_35_E16	E16	PL_DDR3_D51	23
IO_L13N_T2_MRCC_35_E15	E15	PL_DDR3_D49	23
IO_L14P_T2_AD4P_SRCC_35_D15	D15	PL_DDR3_D48	23
IO_L14N_T2_AD4N_SRCC_35_D14	D14	PL_DDR3_D54	23
IO_L15P_T2_DQS_AD12P_35_F17	F17	PL_DDR3_DQS6_P	23
IO_L15N_T2_DQS_AD12N_35_E17	E17	PL_DDR3_DQS6_N	23
IO_L16P_T2_35_D16	D16	PL_DDR3_D50	23
IO_L16N_T2_35_C16	C16	PL_DDR3_DM6	23
IO_L17P_T2_AD5P_35_C17	C17	PL_DDR3_D52	23
IO_L17N_T2_AD5N_35_B16	B16	PL_DDR3_D53	23
IO_L18P_T2_AD13P_35_B17	B17	PL_DDR3_D55	23
IO_L18N_T2_AD13N_35_A17	A17	GPIO_LED_0	38
IO_L19P_T3_35_C14	C14	PL_DDR3_D62	23
IO_L19N_T3_VREF_35_C13	C13		
IO_L20P_T3_AD6P_35_C12	C12	PL_DDR3_D57	23
IO_L20N_T3_AD6N_35_B12	B12	PL_DDR3_D56	23
IO_L21P_T3_DQS_AD14P_35_B15	B15	PL_DDR3_DQS7_P	23
IO_L21N_T3_DQS_AD14N_35_A15	A15	PL_DDR3_DQS7_N	23
IO_L22P_T3_AD7P_35_C11	C11	PL_DDR3_DM7	23
IO_L22N_T3_AD7N_35_B11	B11	PL_DDR3_D61	23
IO_L23P_T3_35_B14	B14	PL_DDR3_D63	23
IO_L23N_T3_35_A14	A14	PL_DDR3_D59	23
IO_L24P_T3_AD15P_35_A13	A13	PL_DDR3_D60	23
IO_L24N_T3_AD15N_35_A12	A12	PL_DDR3_D58	23
IO_25_VRP_35_M16	M16	VRP_35	7

VCC1V5_PL

A16	VCCO_35_A16
B13	VCCO_35_B13
D17	VCCO_35_D17
E14	VCCO_35_E14
H15	VCCO_35_H15
L16	VCCO_35_L16

U1

SOC_IRONWOOD_FF900

VCC1V5_PL

R105
80.6
1/10W
1%

7 VRN_35

7 VRP_35

R104
80.6
1/10W
1%

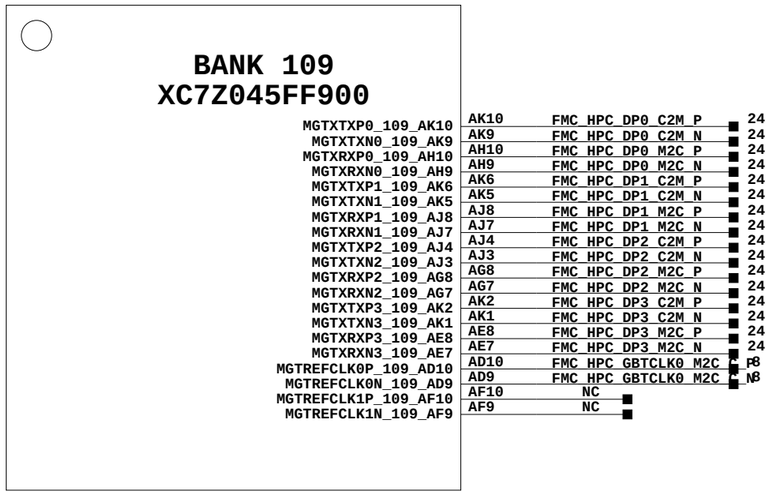
GND

Zynq Bank 35

XILINX

Title:	Zynq Bank 35 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	7 of 58	Drawn By	BF

SOC_Z7_FF900_IRONWOOD

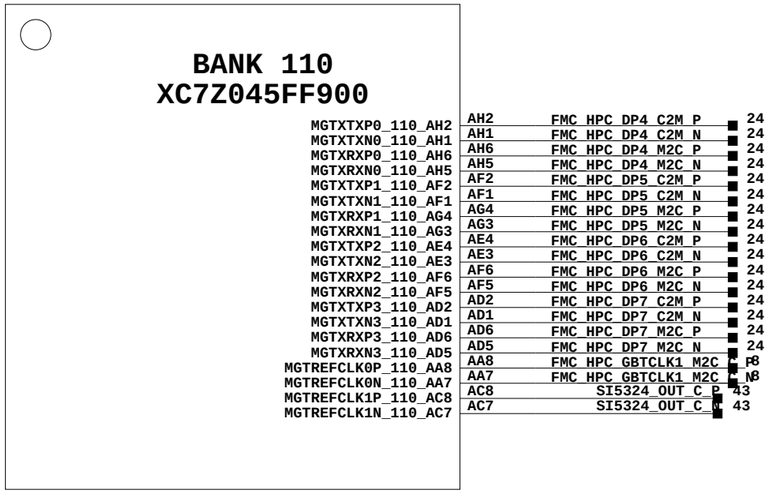


AK10	FMC_HPC_DP0_C2M_P	24
AK9	FMC_HPC_DP0_C2M_N	24
AH10	FMC_HPC_DP0_M2C_P	24
AH9	FMC_HPC_DP0_M2C_N	24
AK6	FMC_HPC_DP1_C2M_P	24
AK5	FMC_HPC_DP1_C2M_N	24
AJ8	FMC_HPC_DP1_M2C_P	24
AJ7	FMC_HPC_DP1_M2C_N	24
AJ4	FMC_HPC_DP2_C2M_P	24
AJ3	FMC_HPC_DP2_C2M_N	24
AG8	FMC_HPC_DP2_M2C_P	24
AG7	FMC_HPC_DP2_M2C_N	24
AK2	FMC_HPC_DP3_C2M_P	24
AK1	FMC_HPC_DP3_C2M_N	24
AE8	FMC_HPC_DP3_M2C_P	24
AE7	FMC_HPC_DP3_M2C_N	24
AD10	FMC_HPC_GBTCLK0_M2C_P	8
AD9	FMC_HPC_GBTCLK0_M2C_N	8
AF10	NC	
AF9	NC	

U1

SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD



AH2	FMC_HPC_DP4_C2M_P	24
AH1	FMC_HPC_DP4_C2M_N	24
AH6	FMC_HPC_DP4_M2C_P	24
AH5	FMC_HPC_DP4_M2C_N	24
AF2	FMC_HPC_DP5_C2M_P	24
AF1	FMC_HPC_DP5_C2M_N	24
AG4	FMC_HPC_DP5_M2C_P	24
AG3	FMC_HPC_DP5_M2C_N	24
AE4	FMC_HPC_DP6_C2M_P	24
AE3	FMC_HPC_DP6_C2M_N	24
AF6	FMC_HPC_DP6_M2C_P	24
AF5	FMC_HPC_DP6_M2C_N	24
AD2	FMC_HPC_DP7_C2M_P	24
AD1	FMC_HPC_DP7_C2M_N	24
AD6	FMC_HPC_DP7_M2C_P	24
AD5	FMC_HPC_DP7_M2C_N	24
AA8	FMC_HPC_GBTCLK1_M2C_P	8
AA7	FMC_HPC_GBTCLK1_M2C_N	8
AC8	SI5324_OUT_C_P	43
AC7	SI5324_OUT_C_N	43

U1

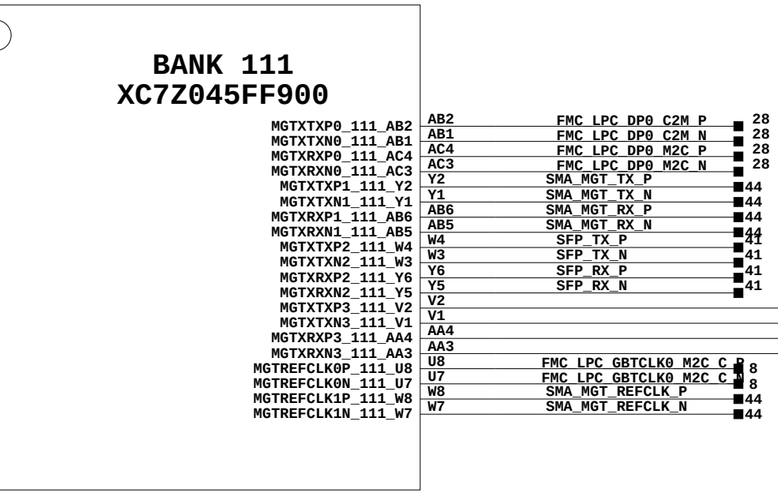
SOC_IRONWOOD_FF900

C647
0.1UF
25V
X5R

C648
0.1UF
25V
X5R

28	FMC_LPC_GBTCLK0_M2C_P	FMC_LPC_GBTCLK0_M2C_C_P	8
28	FMC_LPC_GBTCLK0_M2C_N	FMC_LPC_GBTCLK0_M2C_C_N	8

SOC_Z7_FF900_IRONWOOD



AB2	FMC_LPC_DP0_C2M_P	28
AB1	FMC_LPC_DP0_C2M_N	28
AC4	FMC_LPC_DP0_M2C_P	28
AC3	FMC_LPC_DP0_M2C_N	28
Y2	SMA_MGT_TX_P	44
Y1	SMA_MGT_TX_N	44
AB6	SMA_MGT_RX_P	44
AB5	SMA_MGT_RX_N	44
W4	SFP_TX_P	41
W3	SFP_TX_N	41
Y6	SFP_RX_P	41
Y5	SFP_RX_N	41
V2		
V1		
AA4		
AA3		
U8	FMC_LPC_GBTCLK0_M2C_C_P	8
U7	FMC_LPC_GBTCLK0_M2C_C_N	8
W8	SMA_MGT_REFCLK_P	44
W7	SMA_MGT_REFCLK_N	44

C653
0.1UF
25V
X5R

C652
0.1UF
25V
X5R

U1

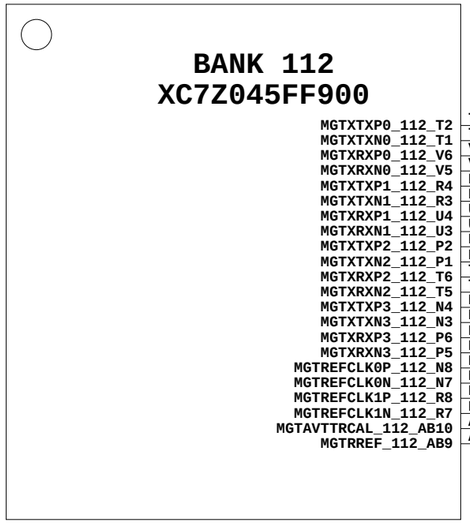
SOC_IRONWOOD_FF900

C643
0.1UF
25V
X5R

C644
0.1UF
25V
X5R

24	FMC_HPC_GBTCLK1_M2C_P	FMC_HPC_GBTCLK1_M2C_C_P	8
24	FMC_HPC_GBTCLK1_M2C_N	FMC_HPC_GBTCLK1_M2C_C_N	8

SOC_Z7_FF900_IRONWOOD



T2	PCIE_TX3_P	42
T1	PCIE_TX3_N	42
V6	PCIE_RX3_P	42
V5	PCIE_RX3_N	42
R4	PCIE_TX2_P	42
R3	PCIE_TX2_N	42
U4	PCIE_RX2_P	42
U3	PCIE_RX2_N	42
P2	PCIE_TX1_P	42
P1	PCIE_TX1_N	42
T6	PCIE_RX1_P	42
T5	PCIE_RX1_N	42
N4	PCIE_TX0_P	42
N3	PCIE_TX0_N	42
P6	PCIE_RX0_P	42
P5	PCIE_RX0_N	42
N8	PCIE_CLK_QO_P	42
N7	PCIE_CLK_QO_N	42
R8	NC	
R7	NC	
AB10		
AB9		

MGTAVTT

R252
100
1/10W
1%

U1

SOC_IRONWOOD_FF900

C646
0.1UF
25V
X5R

C645
0.1UF
25V
X5R

24	FMC_HPC_GBTCLK0_M2C_P	FMC_HPC_GBTCLK0_M2C_C_P	8
24	FMC_HPC_GBTCLK0_M2C_N	FMC_HPC_GBTCLK0_M2C_C_N	8

Zynq MGT Banks

XILINX

Title:	Zynq MGT Banks SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
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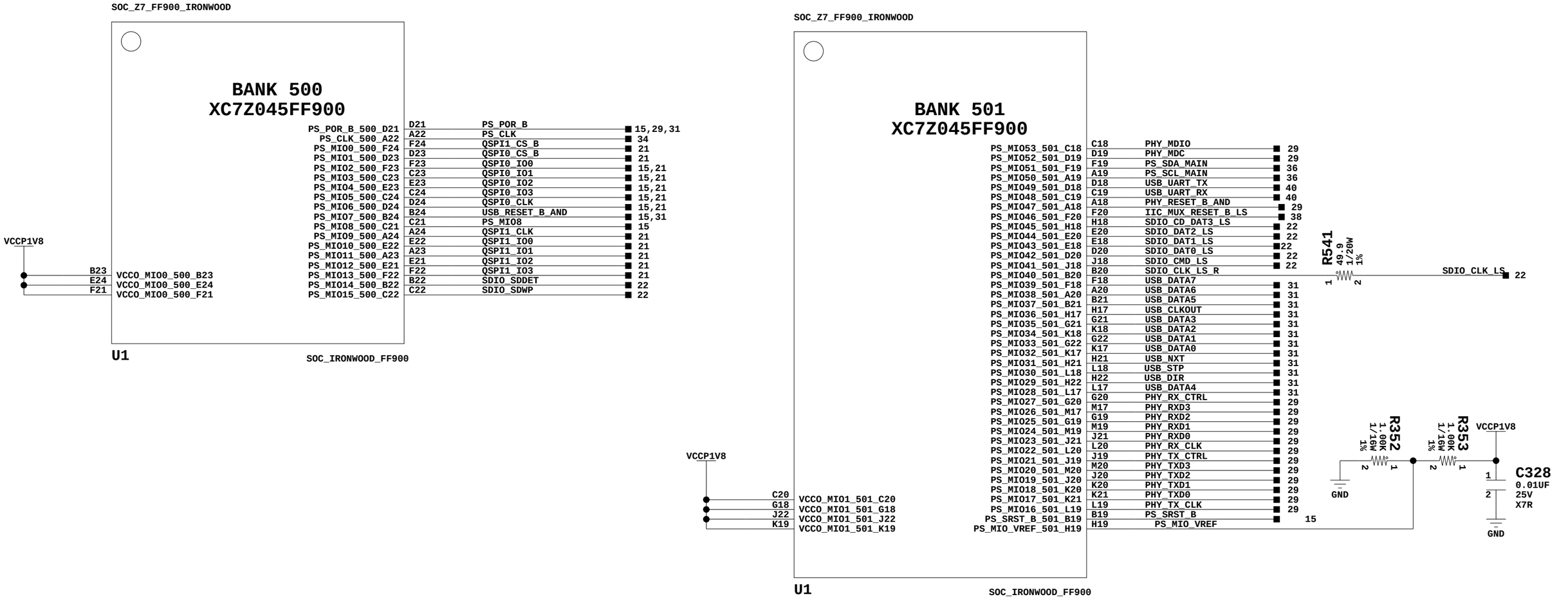

Zynq Banks 500, 501

XILINX

Title:	Zynq Banks 500, 501 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
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SOC_Z7_FF900_IRONWOOD

BANK 502
XC7Z045FF900

PS_DDR_DRST_B_502_F25	F25	PS_DDR3_RESET_B	17,18,19,20
PS_DDR_DQ1_502_E25	E25	PS_DDR3_DQ3	17
PS_DDR_DQ0_502_A25	A25	PS_DDR3_DQ1	17
PS_DDR_DQ3_502_D25	D25	PS_DDR3_DQ6	17
PS_DDR_DQ2_502_B27	B27	PS_DDR3_DQ7	17
PS_DDR_DM0_502_C27	C27	PS_DDR3_DM0	17
PS_DDR_DQS_N0_502_B26	B26	PS_DDR3_DQS0_N	17
PS_DDR_DQS_P0_502_C26	C26	PS_DDR3_DQS0_P	17
PS_DDR_DQ5_502_E26	E26	PS_DDR3_DQ0	17
PS_DDR_DQ4_502_B25	B25	PS_DDR3_DQ5	17
PS_DDR_DQ7_502_E27	E27	PS_DDR3_DQ2	17
PS_DDR_DQ6_502_D26	D26	PS_DDR3_DQ4	17
PS_DDR_DQ9_502_A27	A27	PS_DDR3_DQ8	17
PS_DDR_DQ8_502_A29	A29	PS_DDR3_DQ10	18
PS_DDR_DQ11_502_A28	A28	PS_DDR3_DQ9	18
PS_DDR_DQ10_502_A30	A30	PS_DDR3_DQ13	18
PS_DDR_DM1_502_B30	B30	PS_DDR3_DM1	18
PS_DDR_DQS_N1_502_B29	B29	PS_DDR3_DQS1_N	18
PS_DDR_DQS_P1_502_C29	C29	PS_DDR3_DQS1_P	18
PS_DDR_DQ13_502_D30	D30	PS_DDR3_DQ12	18
PS_DDR_DQ12_502_C28	C28	PS_DDR3_DQ11	18
PS_DDR_DQ15_502_D29	D29	PS_DDR3_DQ14	18
PS_DDR_DQ14_502_D28	D28	PS_DDR3_DQ15	18
PS_DDR_A13_502_H23	H23	PS_DDR3_A13	17,18,19,20
PS_DDR_A14_502_J24	J24	PS_DDR3_A14	17,18,19,20
PS_DDR_A11_502_H24	H24	PS_DDR3_A11	17,18,19,20
PS_DDR_A12_502_K23	K23	PS_DDR3_A12	17,18,19,20
PS_DDR_A9_502_J23	J23	PS_DDR3_A9	17,18,19,20
PS_DDR_A10_502_G26	G26	PS_DDR3_A10	17,18,19,20
PS_DDR_A7_502_K22	K22	PS_DDR3_A7	17,18,19,20
PS_DDR_A8_502_F27	F27	PS_DDR3_A8	17,18,19,20
PS_DDR_A5_502_G24	G24	PS_DDR3_A5	17,18,19,20
PS_DDR_A6_502_H26	H26	PS_DDR3_A6	17,18,19,20
PS_DDR_A3_502_G25	G25	PS_DDR3_A3	17,18,19,20
PS_DDR_A4_502_J26	J26	PS_DDR3_A4	17,18,19,20
PS_DDR_VRP_502_M21	M21	PS_VRP	10
PS_DDR_VRN_502_N21	N21	PS_VRN	10
PS_DDR_CKP_502_K25	K25	PS_DDR3_CLK_P	17,18,19,20
PS_DDR_CKN_502_J25	J25	PS_DDR3_CLK_N	17,18,19,20
PS_DDR_A2_502_L27	L27	PS_DDR3_A2	17,18,19,20
PS_DDR_A1_502_K26	K26	PS_DDR3_A1	17,18,19,20
PS_DDR_A0_502_L25	L25	PS_DDR3_A0	17,18,19,20
PS_DDR_BA2_502_M25	M25	PS_DDR3_BA2	17,18,19,20
PS_DDR_BA1_502_M26	M26	PS_DDR3_BA1	17,18,19,20
PS_DDR_BA0_502_M27	M27	PS_DDR3_BA0	17,18,19,20
PS_DDR_ODT_502_L23	L23	PS_DDR3_ODT	17,18,19,20
PS_DDR_CS_B_502_N22	N22	PS_DDR3_CS_B	17,18,19,20
PS_DDR_CKE_502_M22	M22	PS_DDR3_CKE	17,18,19,20
PS_DDR_WE_B_502_N23	N23	PS_DDR3_WE_B	17,18,19,20
PS_DDR_CAS_B_502_M24	M24	PS_DDR3_CAS_B	17,18,19,20
PS_DDR_RAS_B_502_N24	N24	PS_DDR3_RAS_B	17,18,19,20
PS_DDR_DQ16_502_H27	H27	PS_DDR3_DQ16	19
PS_DDR_DQ17_502_G27	G27	PS_DDR3_DQ17	19
PS_DDR_DQ18_502_H28	H28	PS_DDR3_DQ18	19
PS_DDR_DQ19_502_E28	E28	PS_DDR3_DQ19	19
PS_DDR_DM2_502_H29	H29	PS_DDR3_DM2	19
PS_DDR_DQS_P2_502_G29	G29	PS_DDR3_DQS2_P	19
PS_DDR_DQS_N2_502_F29	F29	PS_DDR3_DQS2_N	19
PS_DDR_DQ20_502_E30	E30	PS_DDR3_DQ20	19
PS_DDR_DQ21_502_F28	F28	PS_DDR3_DQ21	19
PS_DDR_DQ22_502_G30	G30	PS_DDR3_DQ22	19
PS_DDR_DQ23_502_F30	F30	PS_DDR3_DQ23	19
PS_DDR_DQ24_502_J29	J29	PS_DDR3_DQ27	20
PS_DDR_DQ25_502_K27	K27	PS_DDR3_DQ24	20
PS_DDR_DQ26_502_J30	J30	PS_DDR3_DQ25	20
PS_DDR_DQ27_502_J28	J28	PS_DDR3_DQ26	20
PS_DDR_DM3_502_K28	K28	PS_DDR3_DM3	20
PS_DDR_DQS_P3_502_L28	L28	PS_DDR3_DQS3_P	20
PS_DDR_DQS_N3_502_L29	L29	PS_DDR3_DQS3_N	20
PS_DDR_DQ28_502_K30	K30	PS_DDR3_DQ28	20
PS_DDR_DQ29_502_M29	M29	PS_DDR3_DQ29	20
PS_DDR_DQ30_502_L30	L30	PS_DDR3_DQ30	20
PS_DDR_DQ31_502_M30	M30	PS_DDR3_DQ31	20
PS_DDR_VREF0_502_L22	L22		
PS_DDR_VREF1_502_L24	L24		

VCC1V5_PS

A26	VCCO_DDR_502_A26
C30	VCCO_DDR_502_C30
D27	VCCO_DDR_502_D27
G28	VCCO_DDR_502_G28
H25	VCCO_DDR_502_H25
K29	VCCO_DDR_502_K29
L26	VCCO_DDR_502_L26
M23	VCCO_DDR_502_M23

U1

SOC_IRONWOOD_FF900

VTTVREF_PS

C330
0.01UF
25V
X7R

GND

VTTVREF_PS

C329
0.01UF
25V
X7R

GND

VCC1V5_PS

R107
80.6
1/10W
1%

PS_VRN 10
PS_VRP 10

R106
80.6
1/10W
1%

GND

Zynq Bank 502

XILINX

Title:	Zynq Bank 502 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
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*See Notes at bottom left of page

SOC_Z7_FF900_IRONWOOD

BANK VCCAUX
XC7Z045FF900

VCCAUX_Y11 Y11
VCCAUX_W10 W10
VCCAUX_U10 U10
VCCAUX_R10 R10
VCCAUX_N10 N10
VCCAUX_M11 M11

VCCAUX

U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK VCCPAUX
XC7Z045FF900

VCCPAUX_U20 U20
VCCPAUX_R20 R20
VCCPAUX_P19 P19
VCCPAUX_N20 N20

VCCP1V8

U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK VCCPLL
XC7Z045FF900

VCCPLL_N18 N18

VCCPLL
VCCP1V8
FERRITE-120
L8
2A
C725 0.47UF 10V X5R
C267 10UF 4V X5R
GND

U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK VCCPINT
XC7Z045FF900

VCCPINT_U18 U18
VCCPINT_T19 T19
VCCPINT_T17 T17
VCCPINT_R18 R18
VCCPINT_P17 P17
VCCPINT_N16 N16

VCCPINT

U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK VCCINT
XC7Z045FF900

VCCINT_Y17 Y17
VCCINT_W16 W16
VCCINT_W14 W14
VCCINT_W12 W12
VCCINT_V15 V15
VCCINT_V13 V13
VCCINT_U16 U16
VCCINT_U12 U12
VCCINT_T13 T13
VCCINT_R16 R16
VCCINT_R12 R12
VCCINT_P13 P13
VCCINT_N14 N14
VCCINT_N12 N12
VCCINT_M15 M15
VCCINT_M13 M13

VCCINT

U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK VCCBRAM
XC7Z045FF900

VCCBRAM_W20 W20
VCCBRAM_W18 W18
VCCBRAM_V19 V19
VCCBRAM_V17 V17

VCCINT

U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK MGTAVTT
XC7Z045FF900

MGTAVTT_Y4 Y4
MGTAVTT_W2 W2
MGTAVTT_V4 V4
MGTAVTT_U2 U2
MGTAVTT_T4 T4
MGTAVTT_R2 R2
MGTAVTT_P4 P4
MGTAVTT_N2 N2
MGTAVTT_AK8 AK8
MGTAVTT_AK4 AK4
MGTAVTT_AJ6 AJ6
MGTAVTT_AJ2 AJ2
MGTAVTT_AH4 AH4
MGTAVTT_AG6 AG6
MGTAVTT_AG2 AG2
MGTAVTT_AF4 AF4
MGTAVTT_AE2 AE2
MGTAVTT_AD4 AD4
MGTAVTT_AC2 AC2
MGTAVTT_AB4 AB4
MGTAVTT_AA2 AA2

MGTAVTT

U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK VCCAUX_IO_G0
XC7Z045FF900

VCCAUX_IO_G0_V11 V11
VCCAUX_IO_G0_T11 T11
VCCAUX_IO_G0_P11 P11

VCCAUX_IO

U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK MGTAVCC
XC7Z045FF900

MGTAVCC_Y8 Y8
MGTAVCC_W6 W6
MGTAVCC_U6 U6
MGTAVCC_R6 R6
MGTAVCC_P8 P8
MGTAVCC_N6 N6
MGTAVCC_AJ10 AJ10
MGTAVCC_AH8 AH8
MGTAVCC_AG10 AG10
MGTAVCC_AF8 AF8
MGTAVCC_AE6 AE6
MGTAVCC_AE10 AE10
MGTAVCC_AD8 AD8
MGTAVCC_AC6 AC6
MGTAVCC_AC10 AC10
MGTAVCC_AB8 AB8
MGTAVCC_AA6 AA6

MGTAVCC

U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK MGTVCCAUX
XC7Z045FF900

MGTVCCAUX_V7 V7
MGTVCCAUX_T7 T7

MGTVCCAUX

GND

U1 SOC_IRONWOOD_FF900

Increase width of VCCPLL route as wide as possible

Reduce the length of VCCPLL route as much as possible

Place C725 inside VIA field for short connection to VCCPLL and

Place C726 inside open space cross adjacent to N18 for short connection to VCCPLL

Zynq Power Pins

XILINX

Title:	Zynq Power Pins SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
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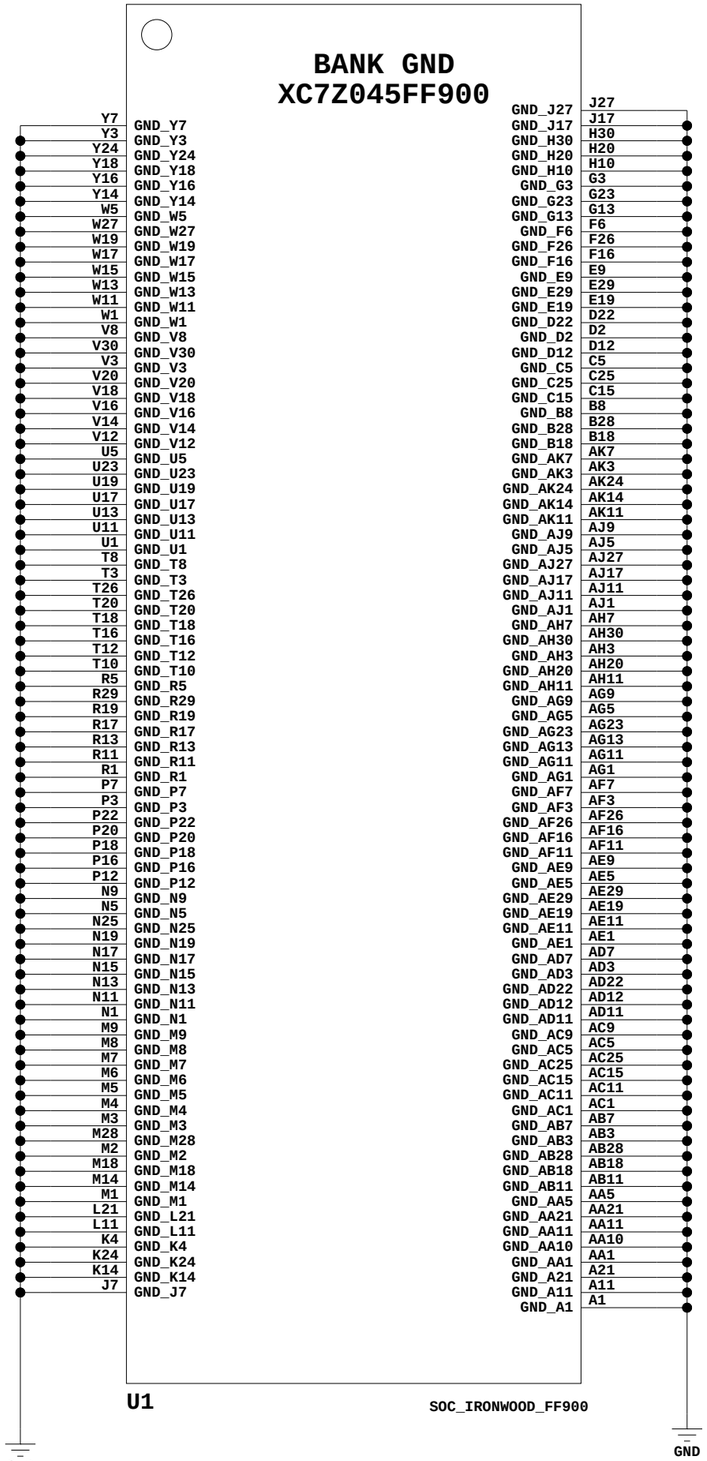
SOC_Z7_FF900_IRONWOOD



Zynq GND

XILINX

Title:	Zynq GND SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431760 1280681 0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
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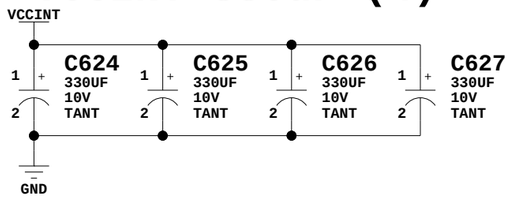
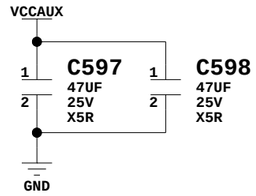
BYPASS CAPACITORS

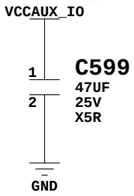
VCCINT 330uF (4)



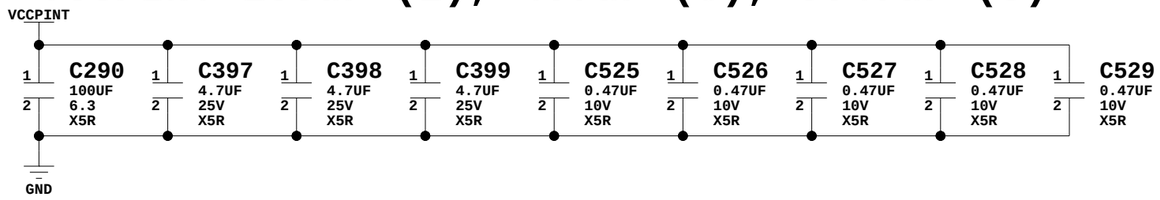
VCCAUX 47uF (2)



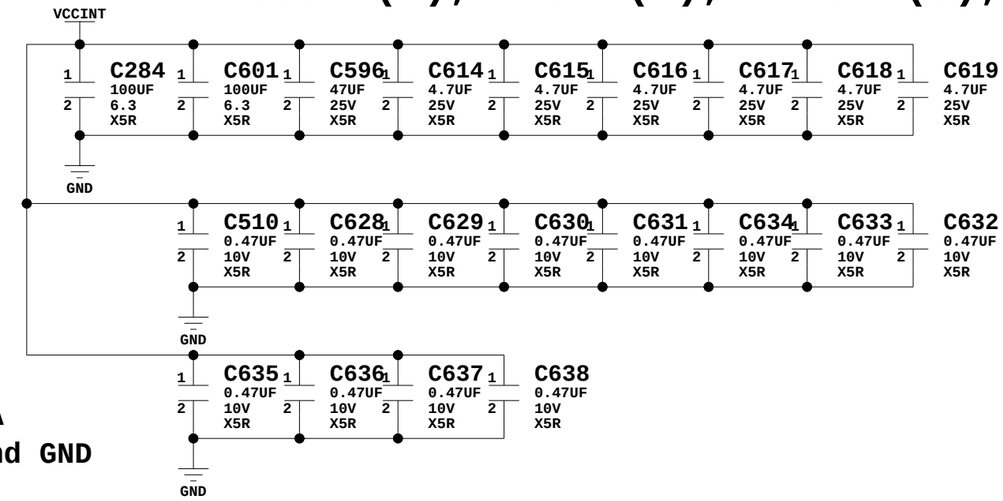
VCCAUX_IO 47uF (1)



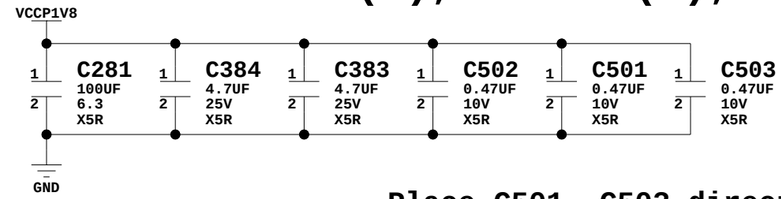
VCCPINT 100uF (1), 4.7uF (3), 0.47uF (5)



VCCBRAM 100uF (2), 47uF (1), 4.7uF (6), 0.47uF (12)

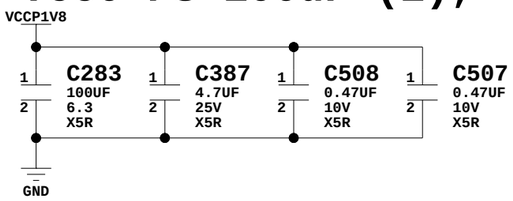


VCCPAUX 100uF (1), 4.7uF (2), 0.47uF (3)

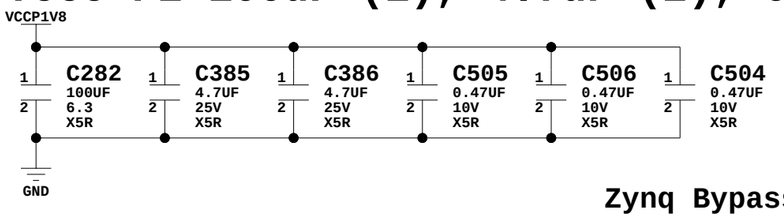


Place C501, C503 directly underneath the FPGA as short as possible connection to VCCPAUX and GND

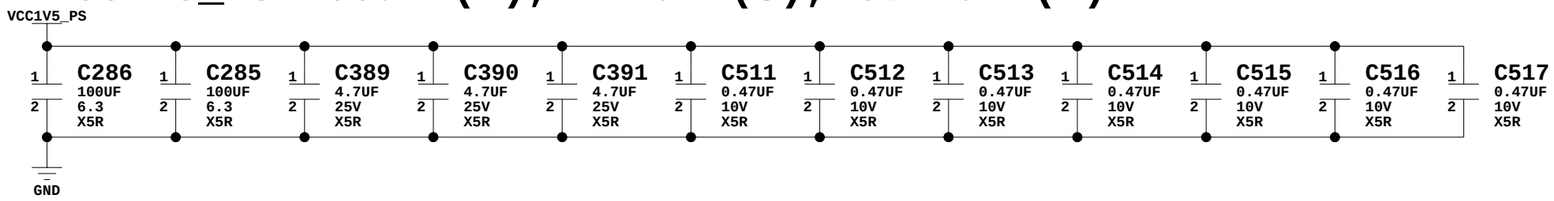
VCC0 PS 100uF (1), 4.7uF (1), 0.47uF (2)



VCCO P1 100uF (1), 4.7uF (2), 0.47uF (3)



VCC1V5_PS 100uF (2), 4.7uF (3), 0.47uF (7)



Zynq Bypass Capacitors Page 1

XILINX

Title:	Zynq Bypass Capacitors Page 1 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
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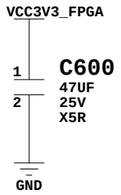
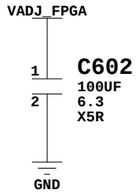
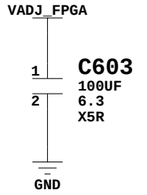
Bank 0 VCC3V3 100uF (1)



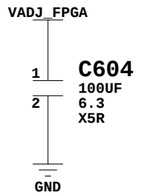
Bank 9 VADJ_FPGA 100uF (1)



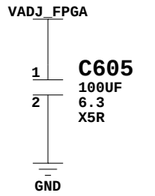
Bank 10 VADJ_FPGA 100uF (1)



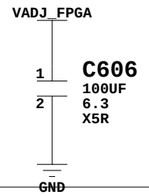
Bank 11 VADJ_FPGA 100uF (1)



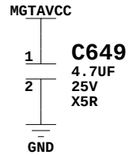
Bank 12 VADJ_FPGA 100uF (1)



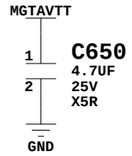
Bank 13 VADJ_FPGA 100uF (1)



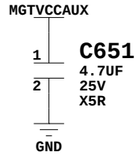
MGTAVCC 4.7uF (1)



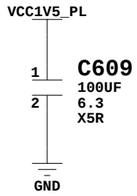
MGTAVTT 4.7uF (1)



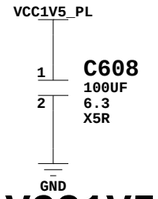
MGTVCCAUX 4.7uF (1)



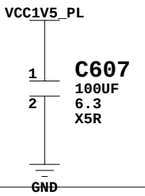
Bank 33 VCC1V5_PL 100uF (1)



Bank 34 VCC1V5_PL 100uF (1)



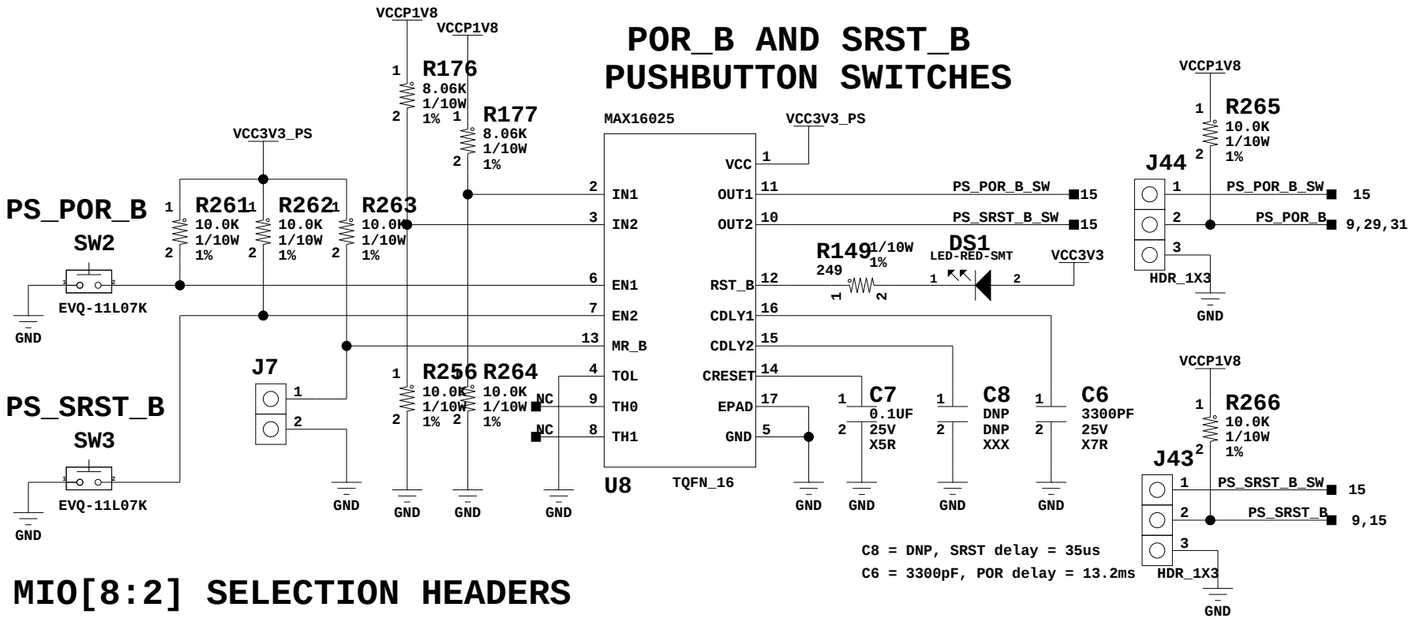
Bank 35 VCC1V5_PL 100uF (1)

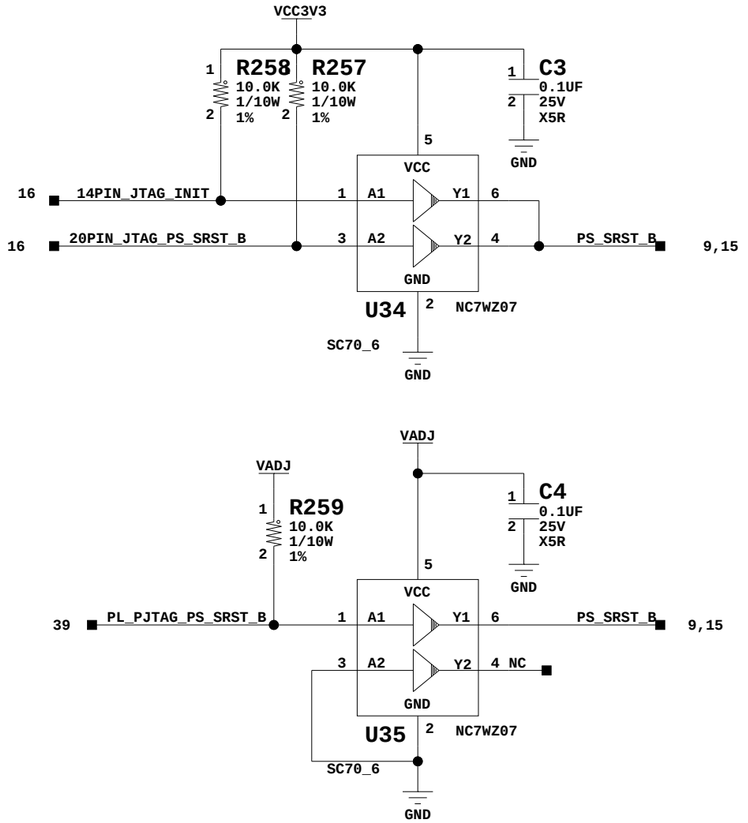


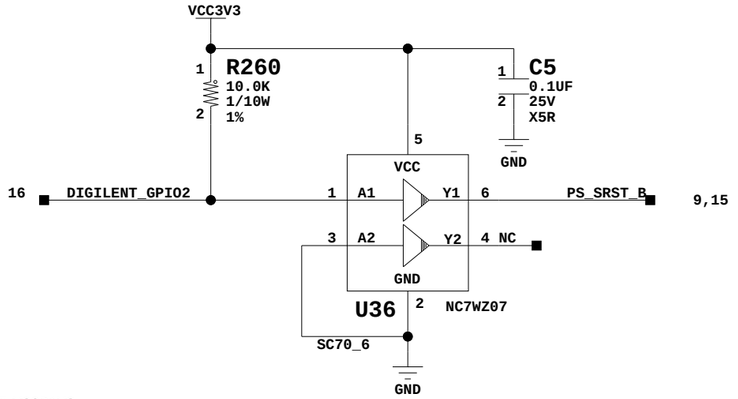
Zynq Bypass Capacitors Page 2

XILINX

Title:	Zynq Bypass Capacitors Page 2 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	14 of 58	Drawn By	BF

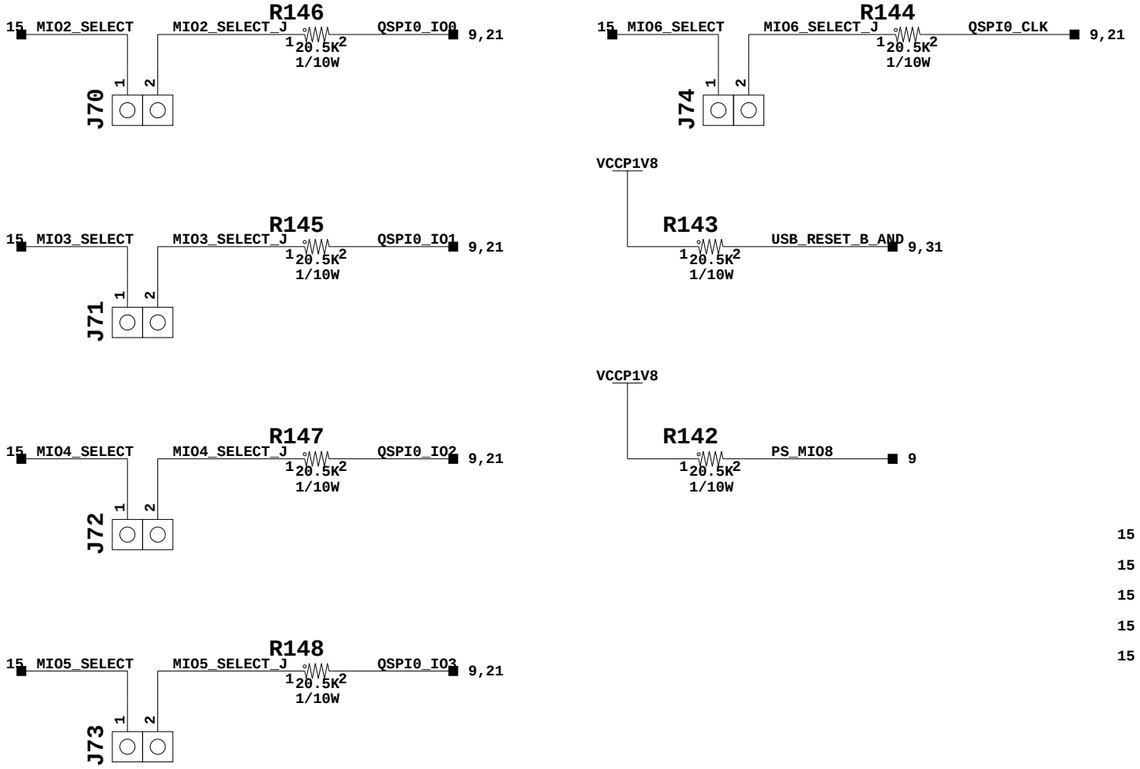


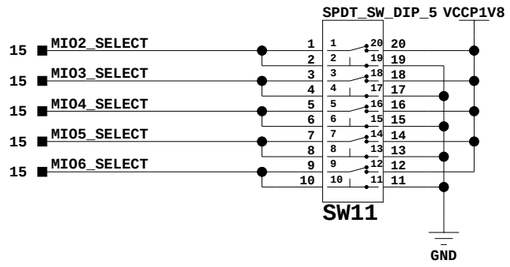




MIO[8:2] SELECTION HEADERS

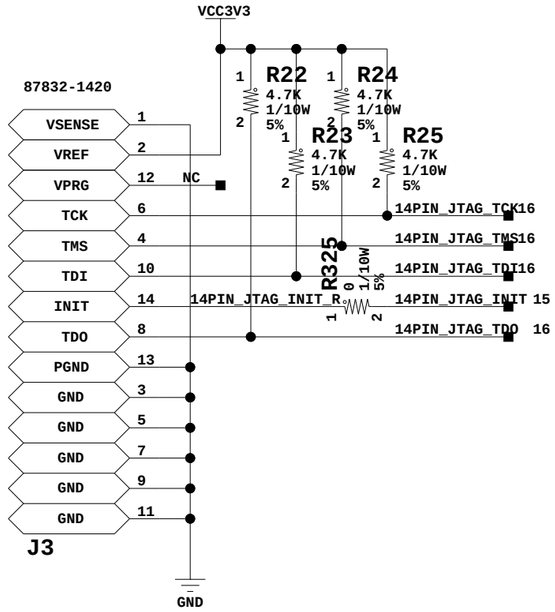
20.5K resistors must be placed near middle of QSPI traces

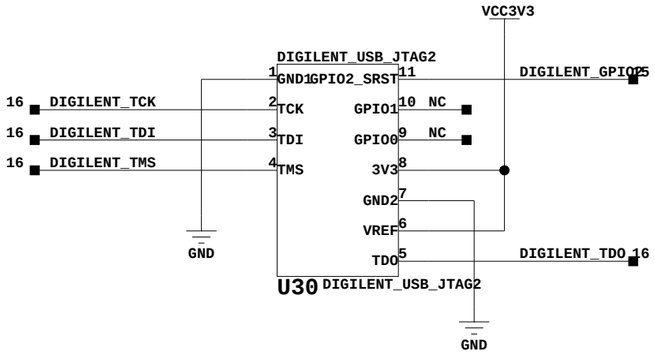


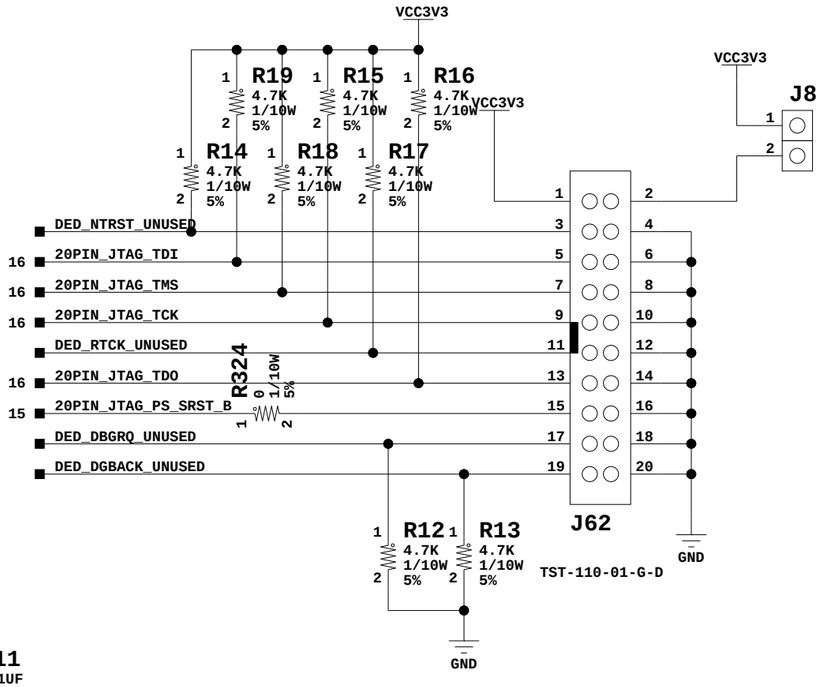


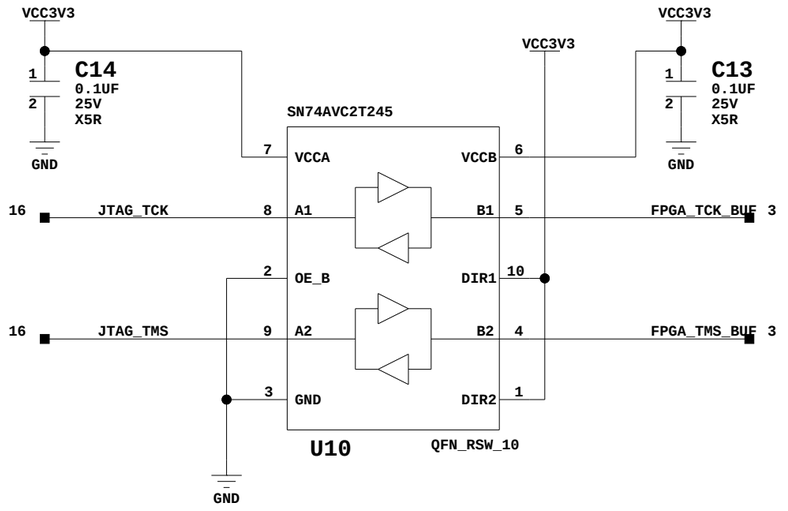
Power Supervisor, Zynq Config Pins, Re

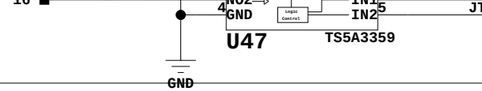
Title: Power Supervisor, Zynq Config Pins, Reset SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 2-21-2013_17:14	Ver: 1.2
Sheet Size: B	Rev: 03
Sheet 15 of 58	Drawn By BF

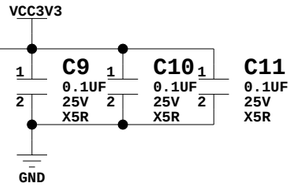


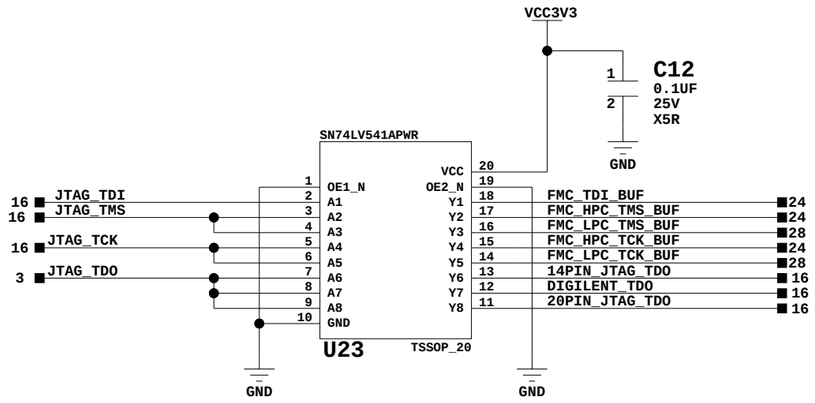








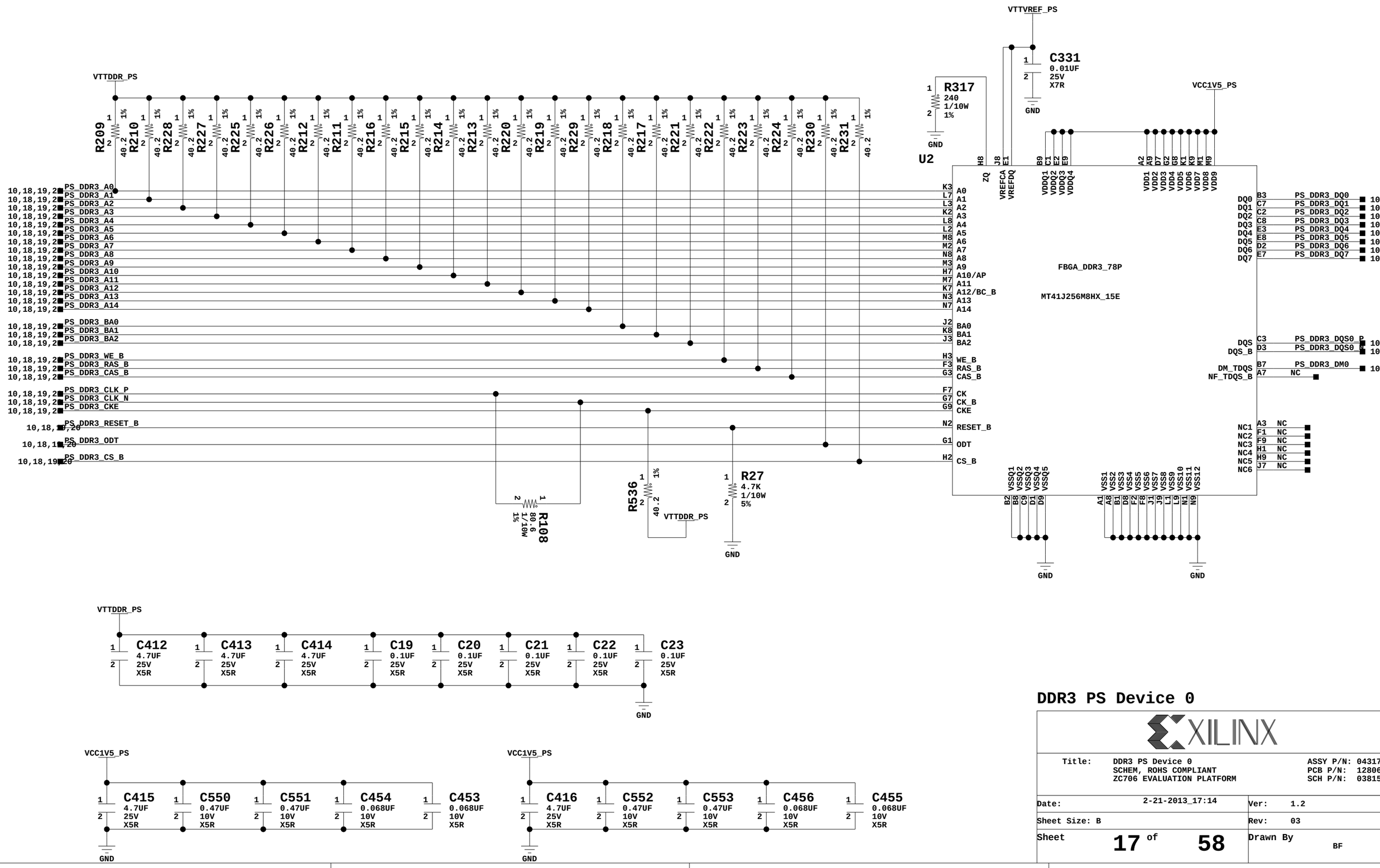




JTAG Buffer, USB JTAG Module, JTAG Hdr

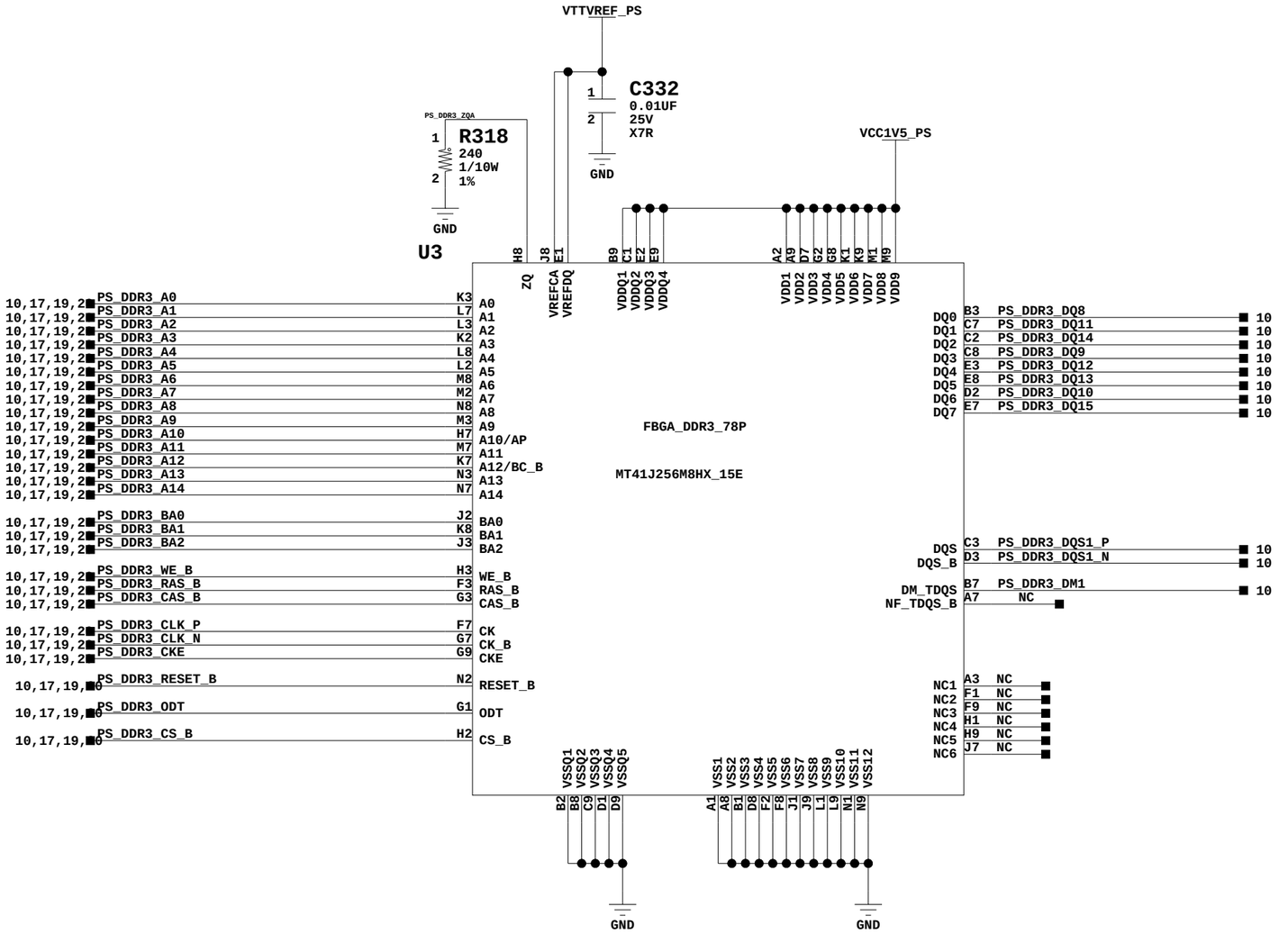
XILINX

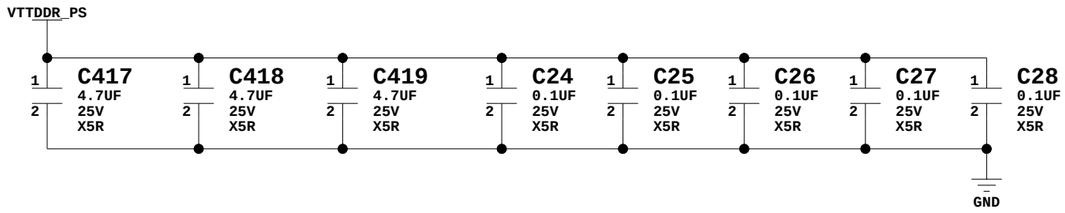
Title:	JTAG Buffer, USB JTAG Module, JTAG Hdr SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431760 1280681 0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	16 of 58	Drawn By	BF

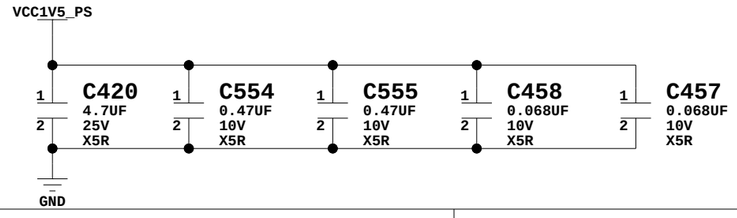


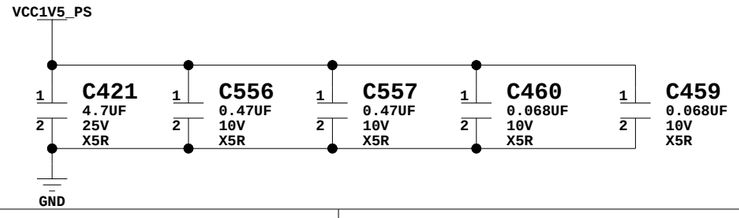
DDR3 PS Device 0

Title:	DDR3 PS Device 0 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431760 1280681 0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	17 of 58	Drawn By	BF



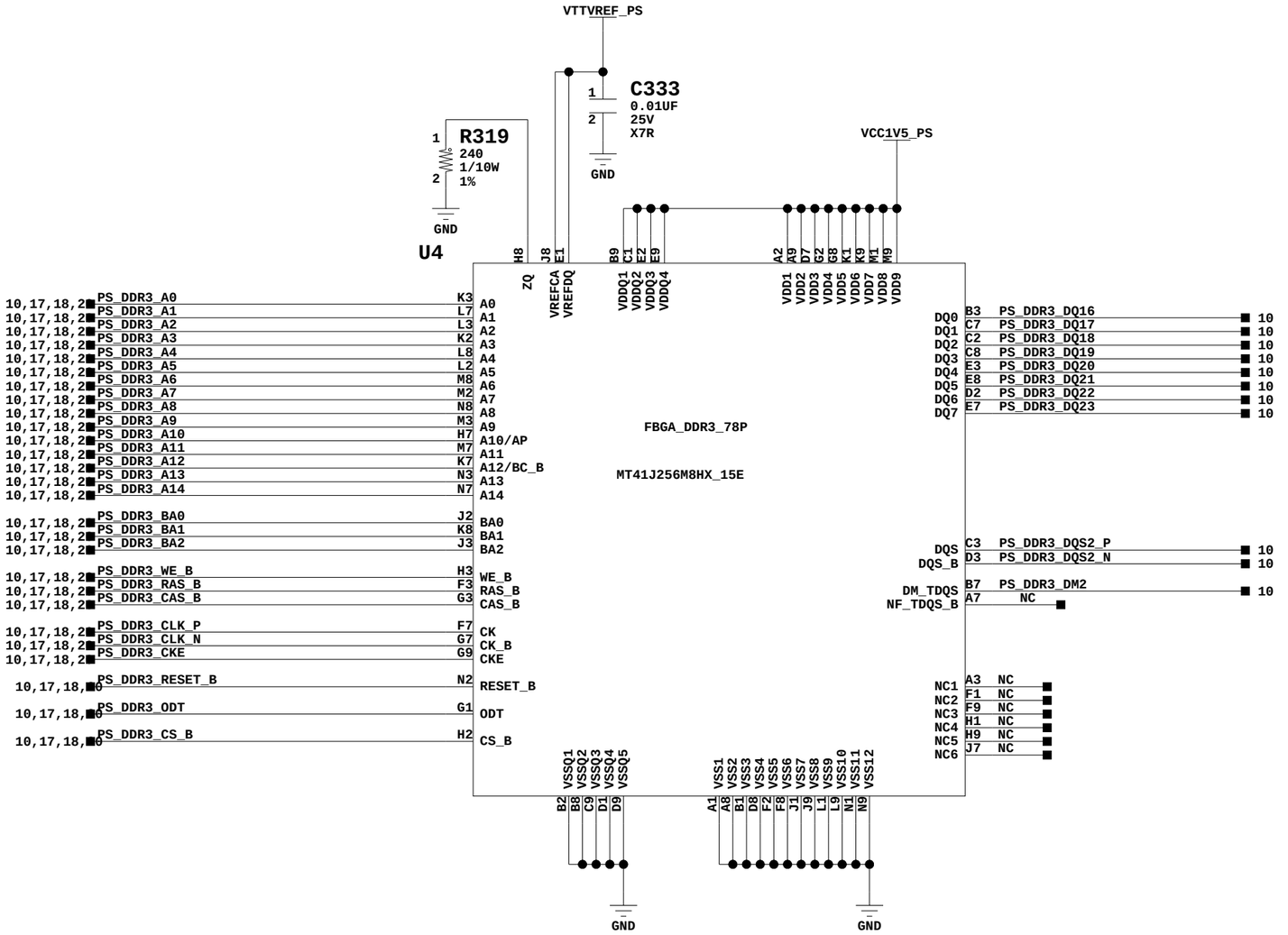


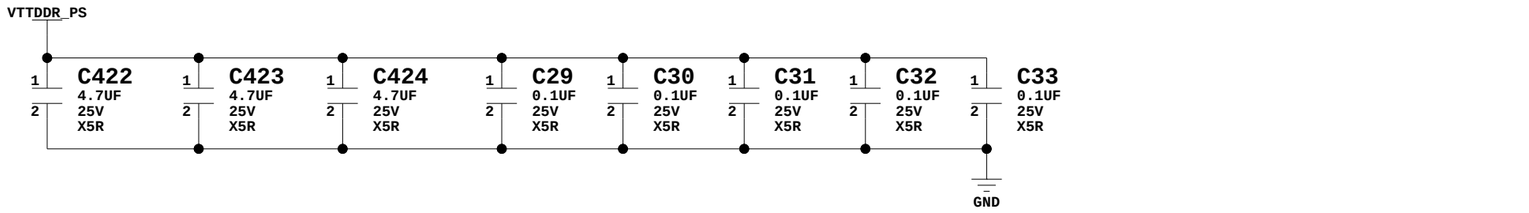


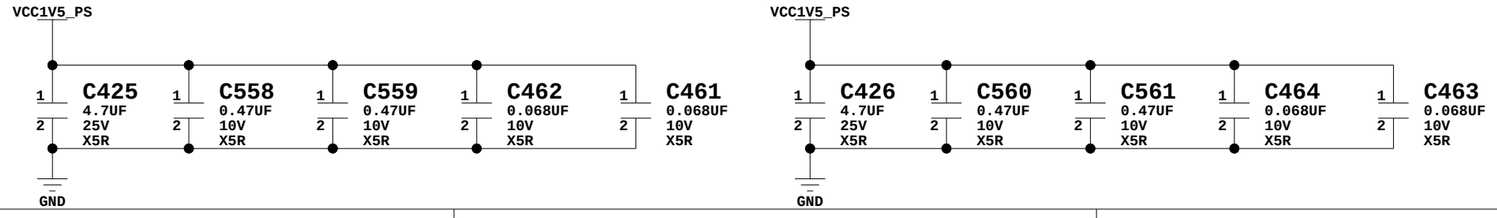


DDR3 PS Device 1

Title:	DDR3 PS Device 1 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	18 of 58	Drawn By	BF

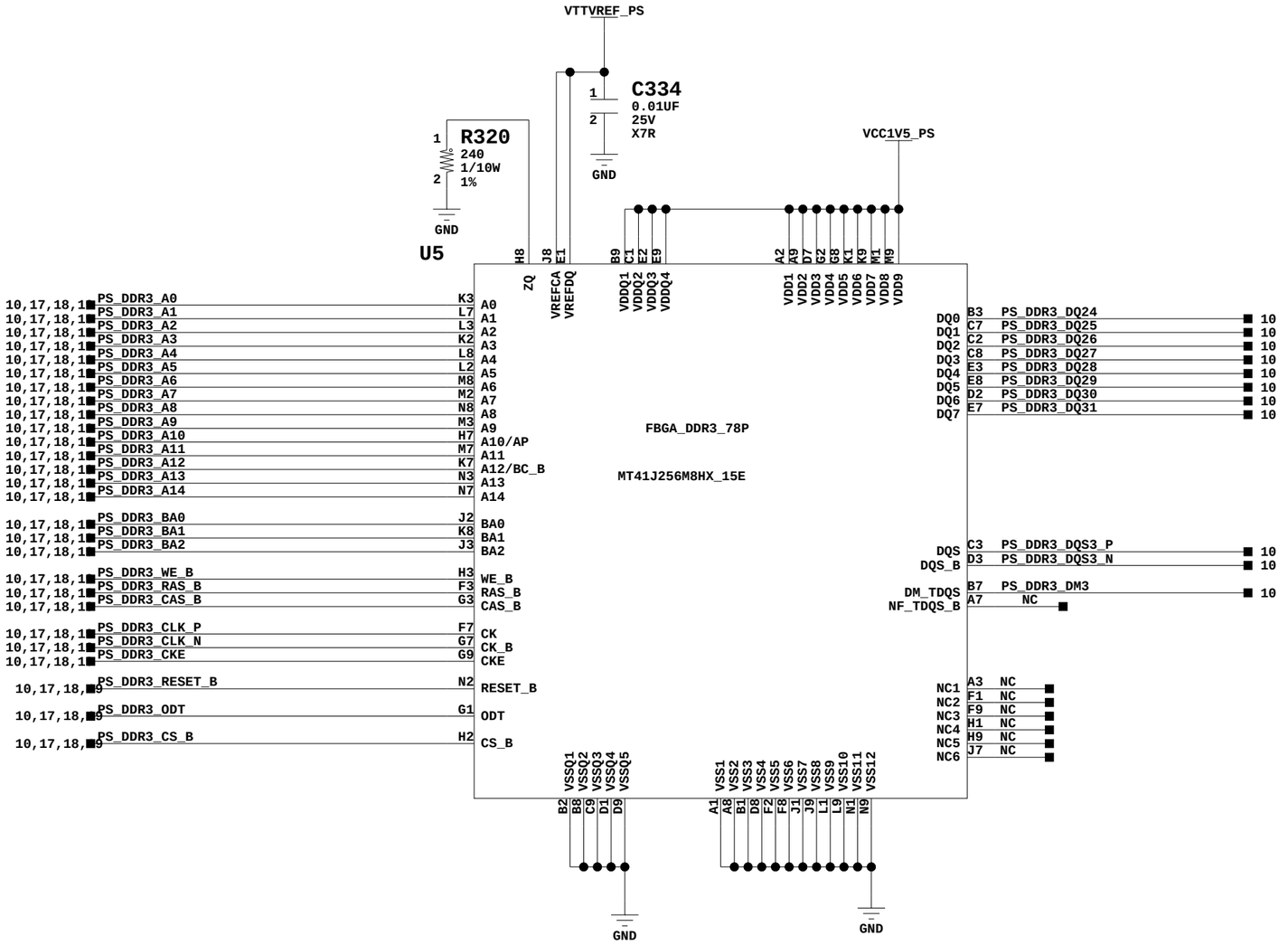


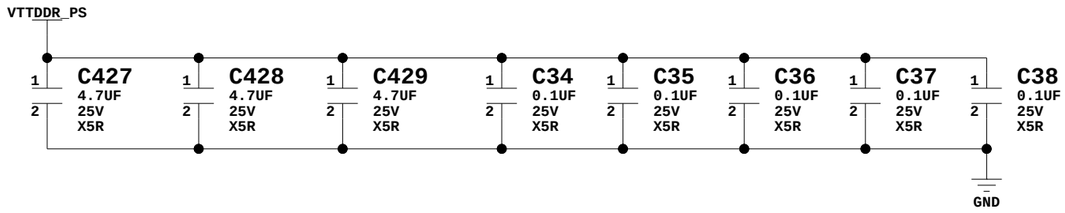


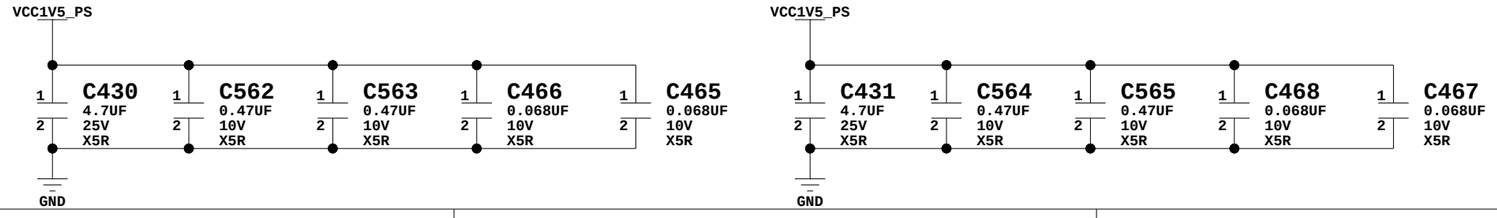


DDR3 PS Device 2

Title:	DDR3 PS Device 2 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	19 of 58	Drawn By	BF

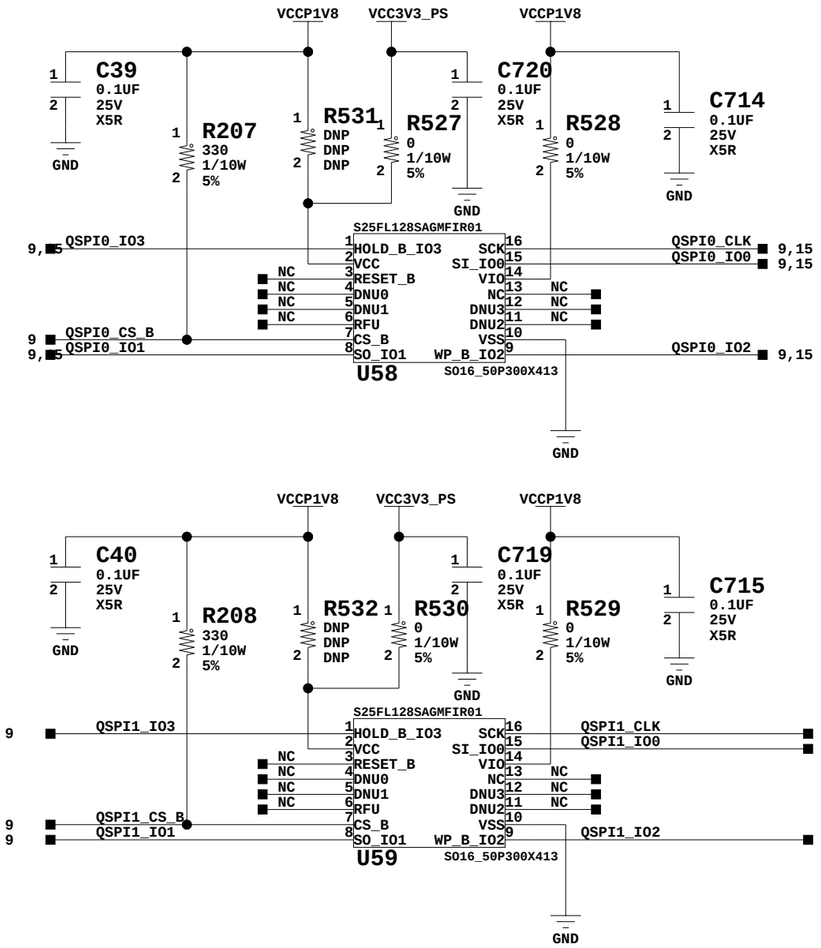






DDR3 PS Device 3

Title:	DDR3 PS Device 3 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431760 1280681 0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	20 of 58	Drawn By	BF

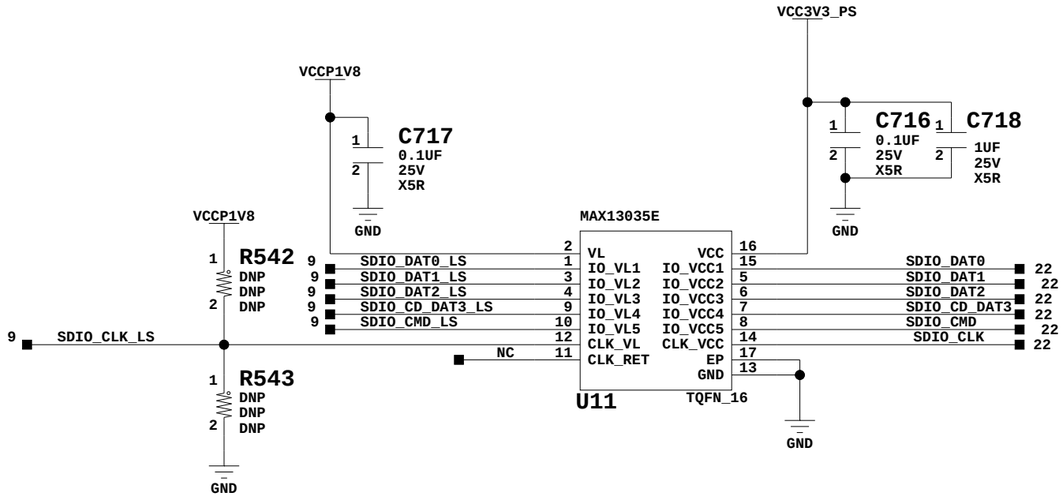


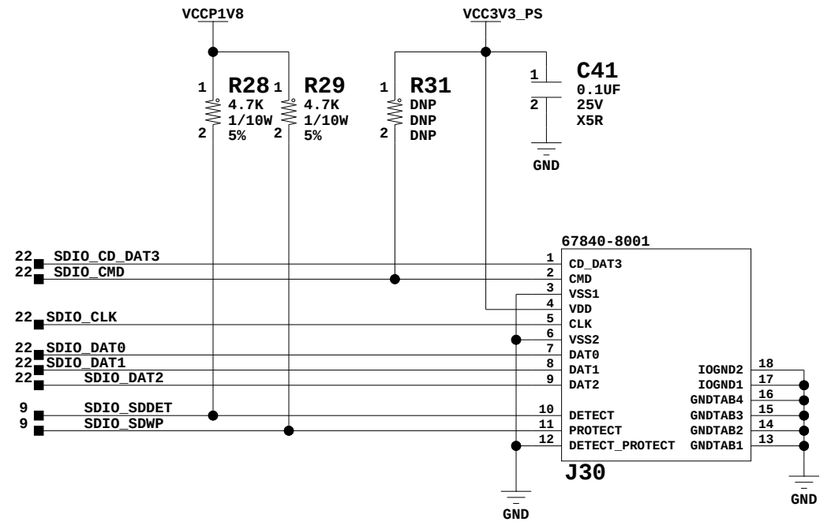
Dual Quad SPIs

Dual Quad SPIs

XILINX

Title:	Dual Quad SPIs SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	21 of 58	Drawn By	BF

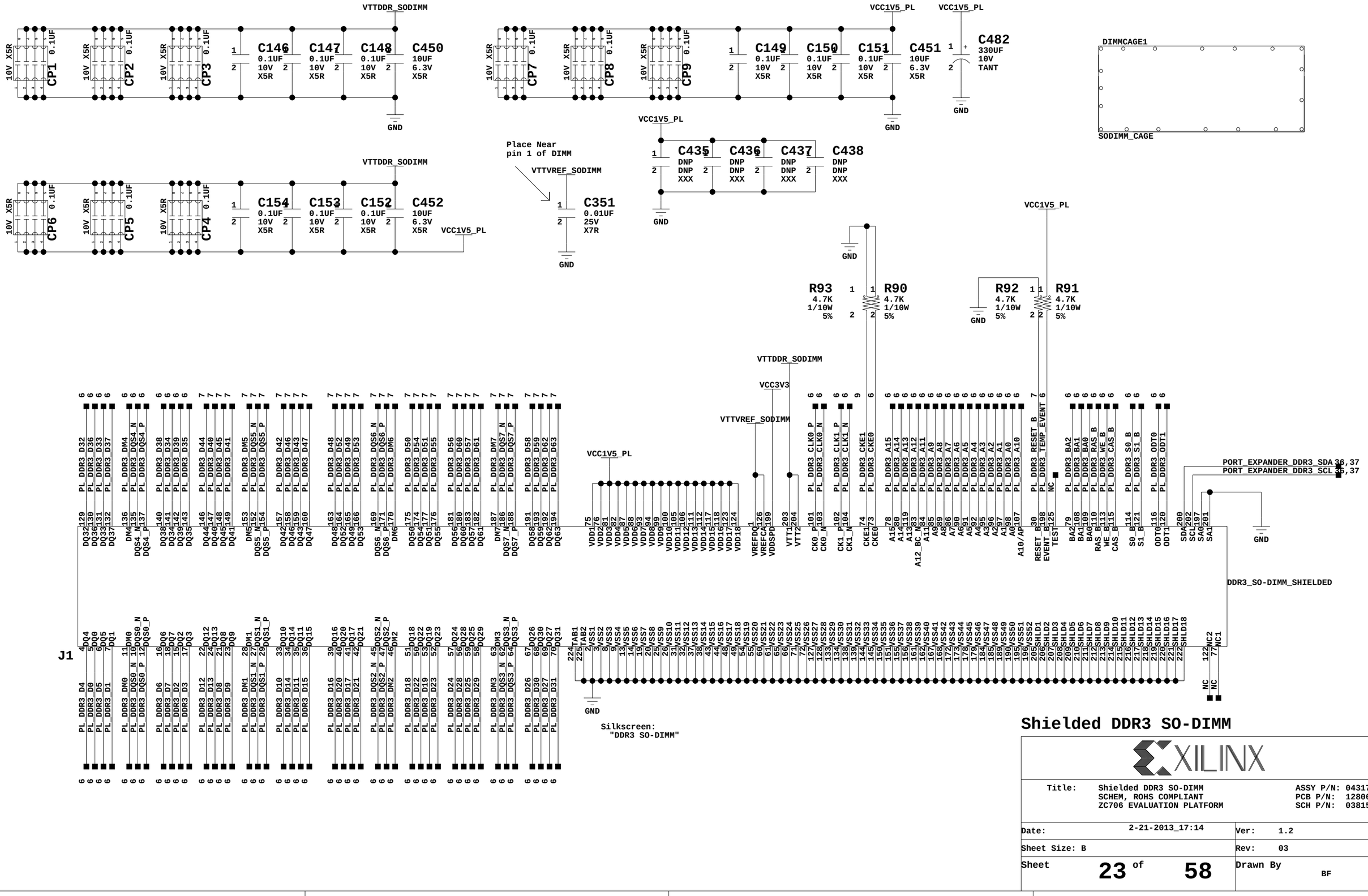




SD Card Connector

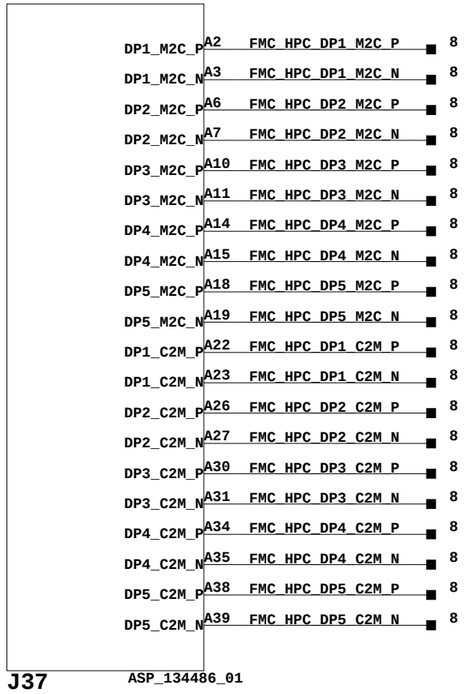
XILINX

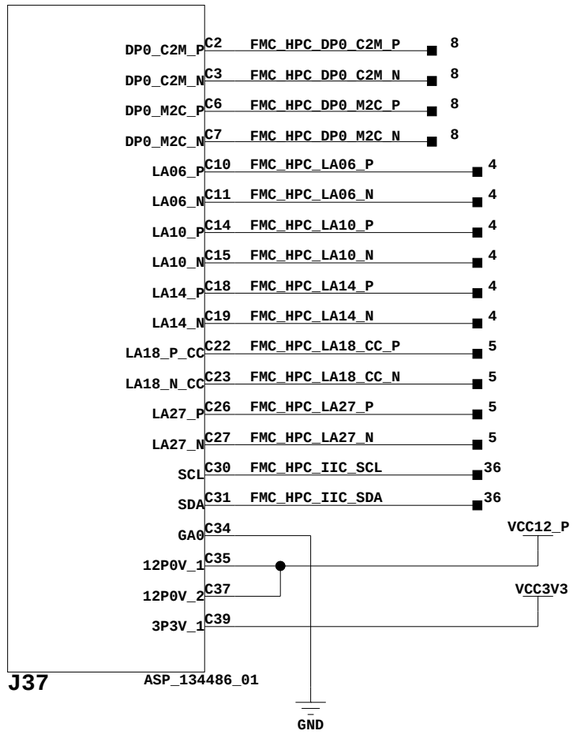
Title:	SD Card Connector SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	22 of 58	Drawn By	BF

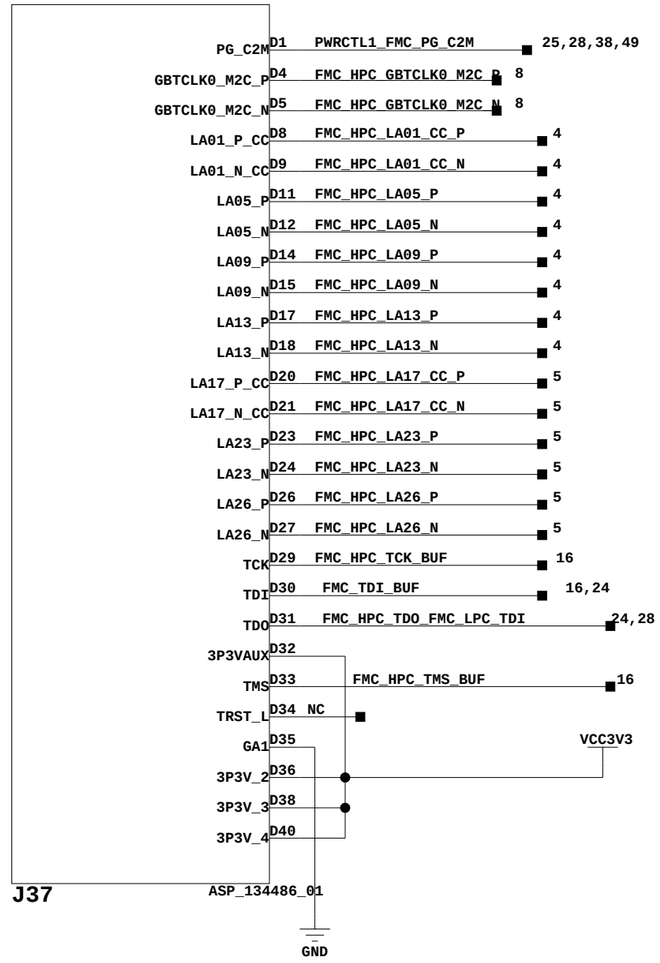


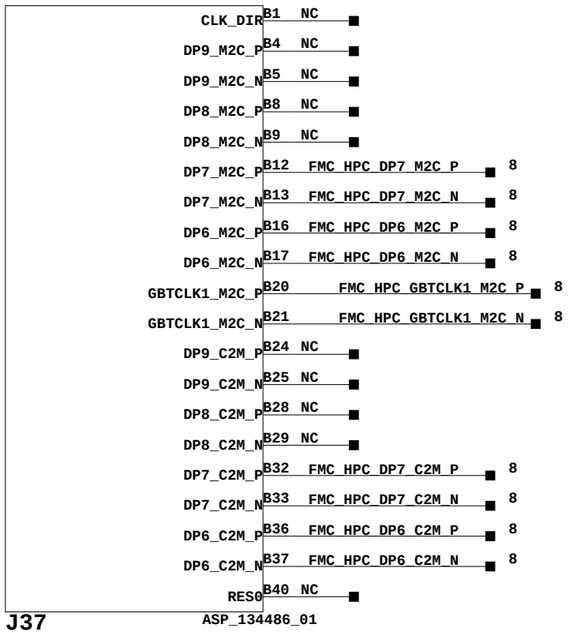
Shielded DDR3 SO-DIMM

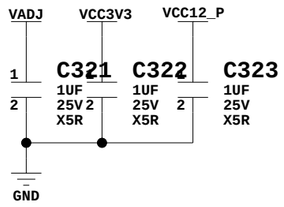
Title:	Shielded DDR3 SO-DIMM SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	23 of 58	Drawn By	BF

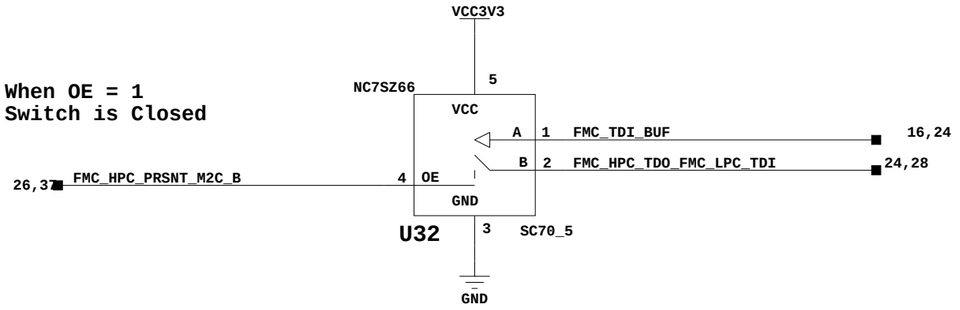






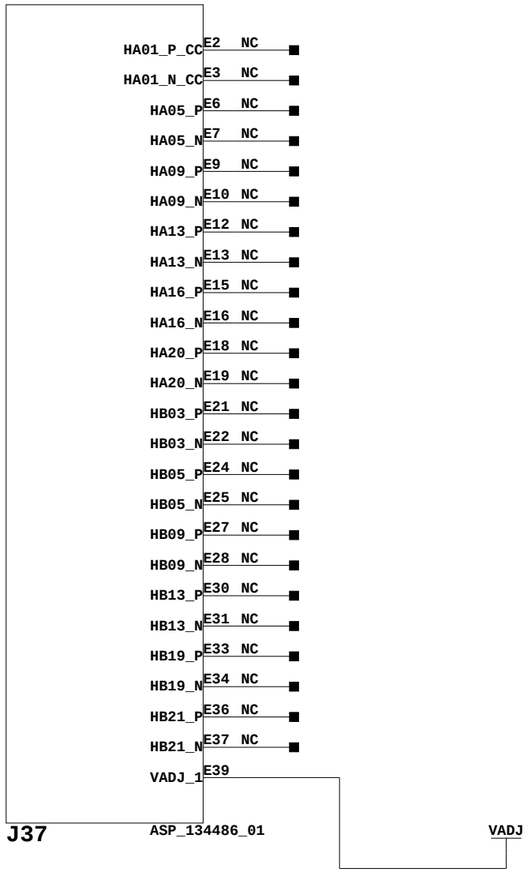


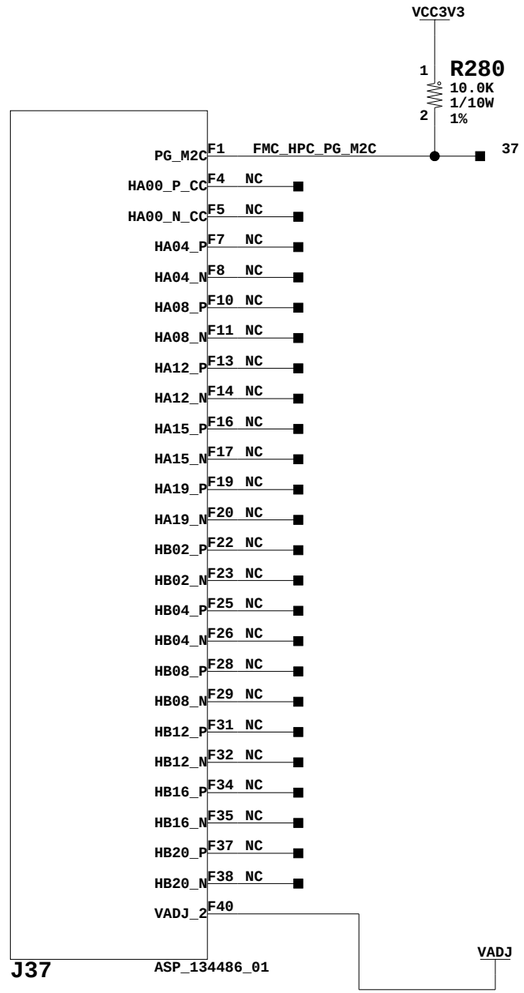


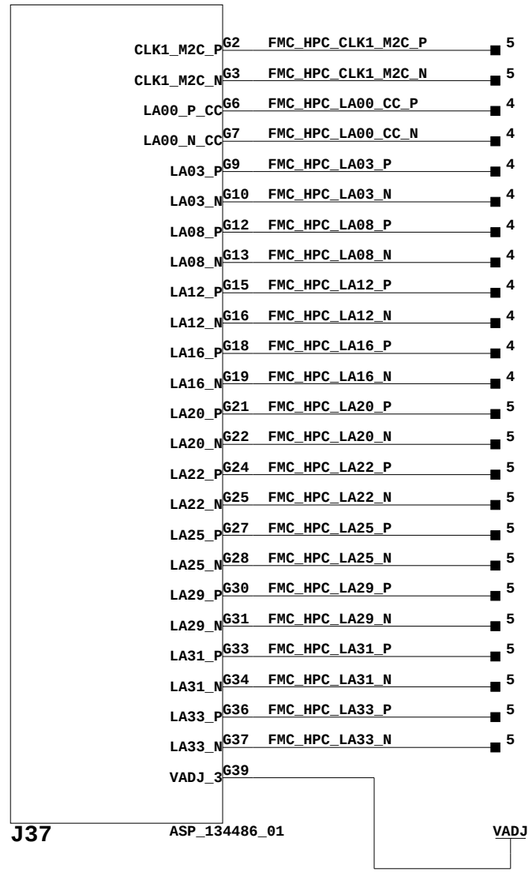


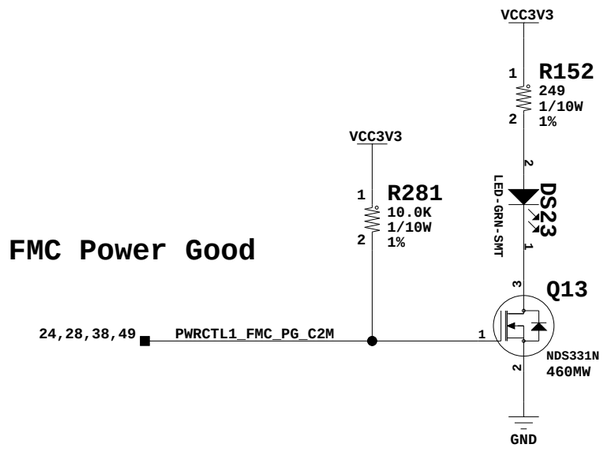
ANSI/VITA 57.1 - Revised 2010
FMC HPC Header, Rows A, B, C, D

Title:	FMC HPC Header, Rows A, B, C, D SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431760 1280681 0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	24 of 58	Drawn By	BF





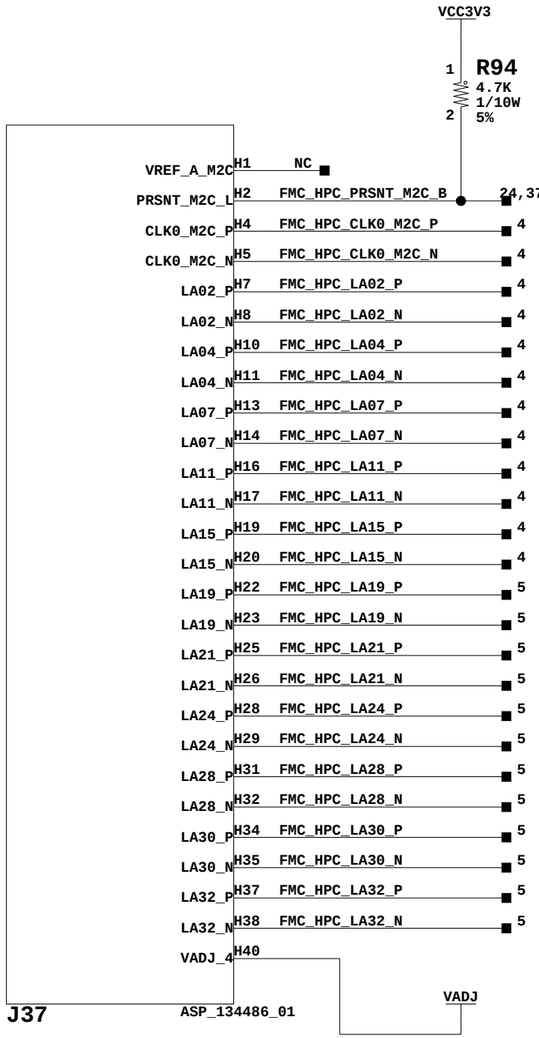


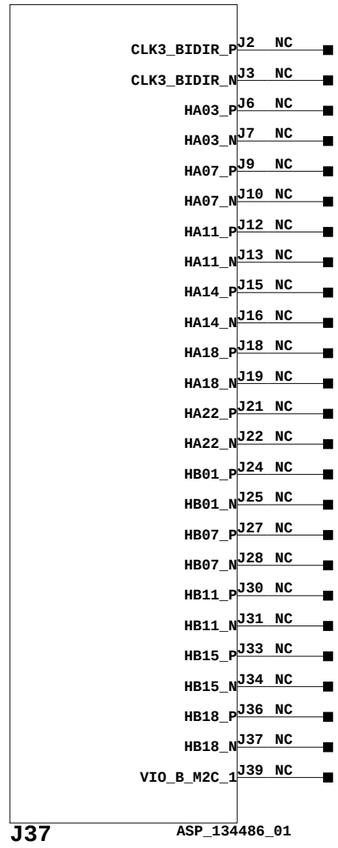


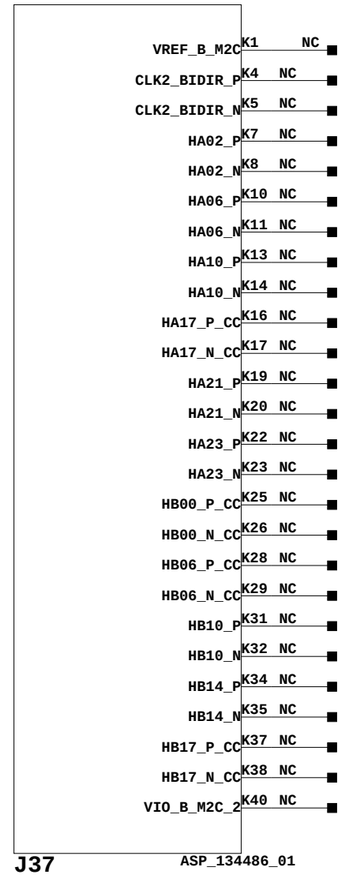
ANSI/VITA 57.1 - Revised 2010
FMC HPC Header, Rows E, F, G

XILINX

Title:	FMC HPC Header, Rows E, F, G SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	25 of 58	Drawn By	BF



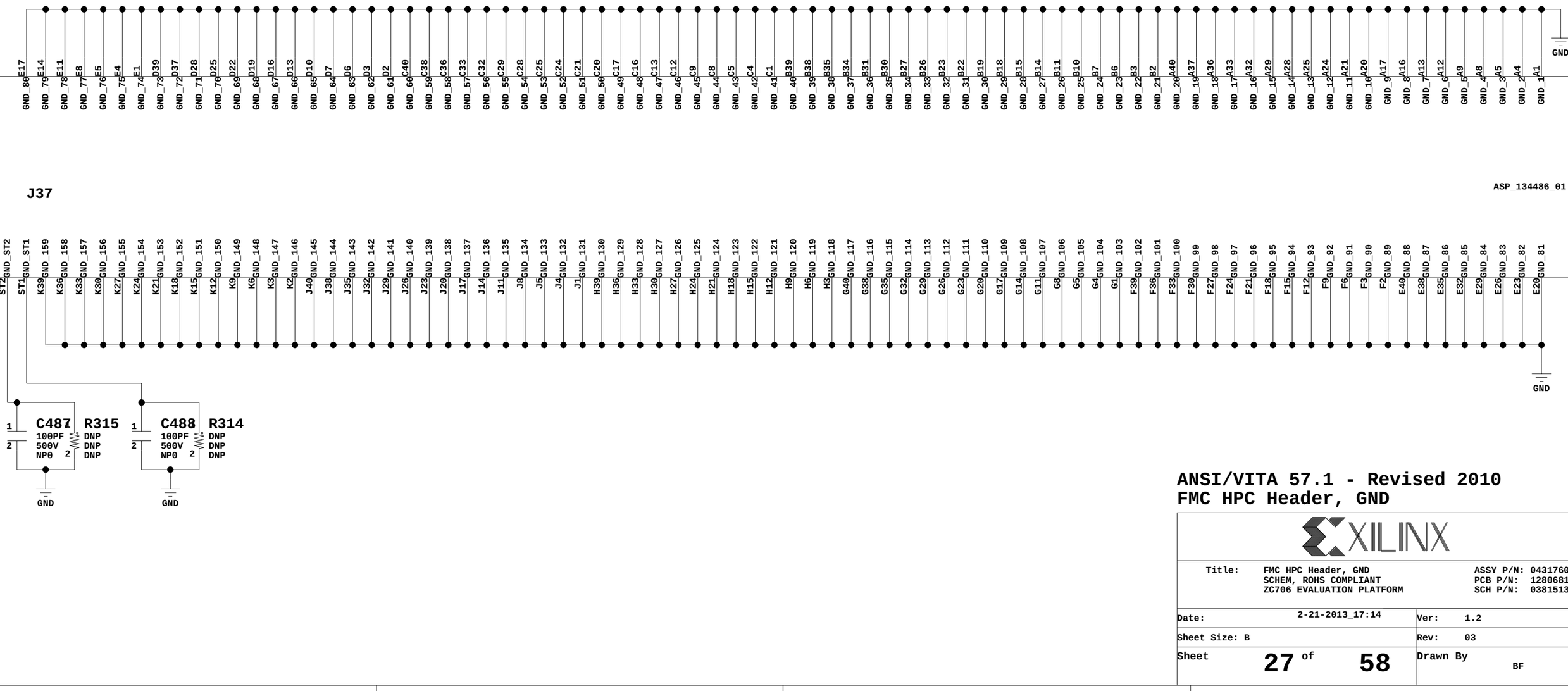




ANSI/VITA 57.1 - Revised 2010
FMC HPC Header, Rows H, J, K

XILINX

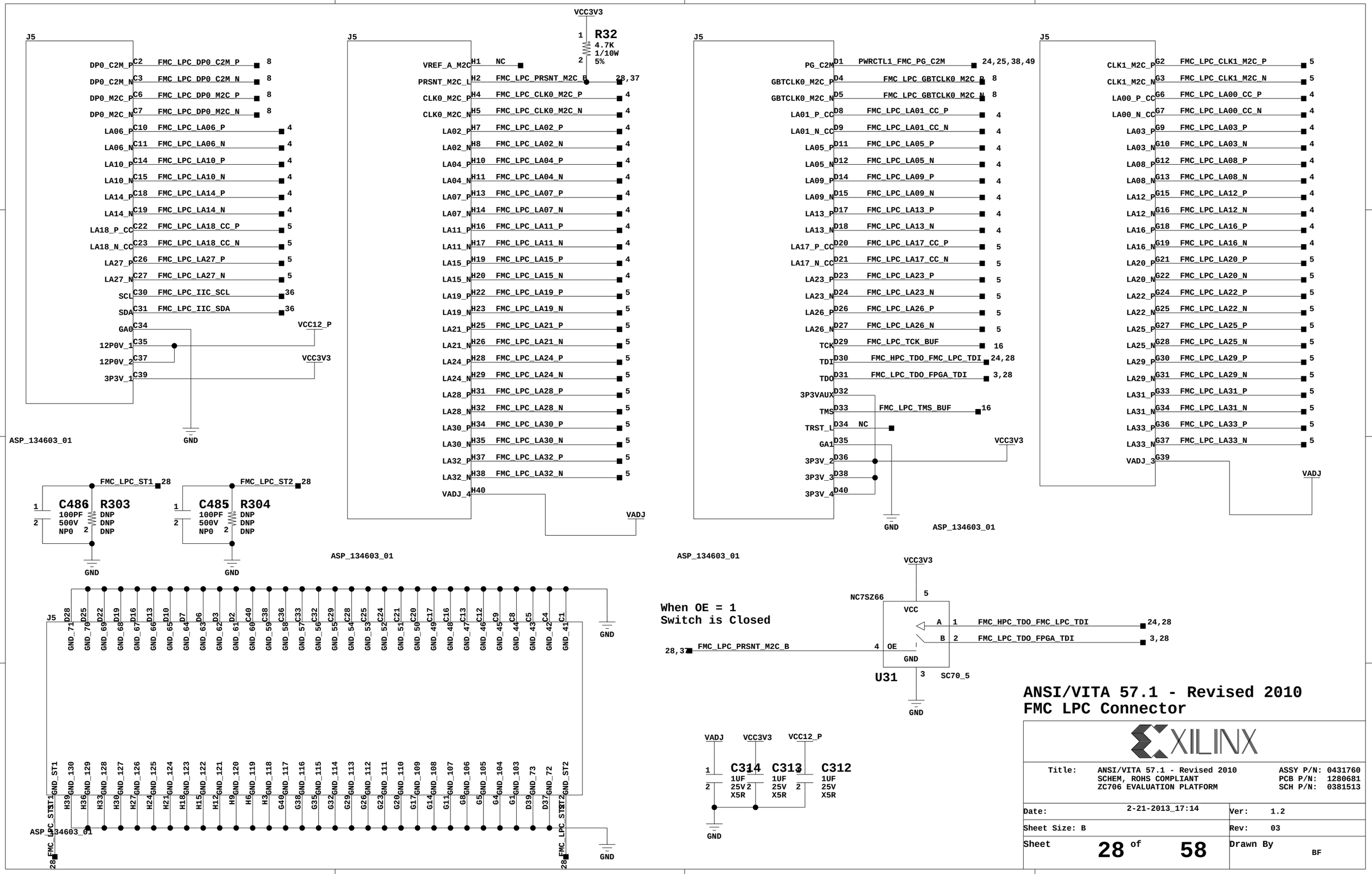
Title:	FMC HPC Header, Rows H, J, K SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	26 of 58	Drawn By	BF



ANSI/VITA 57.1 - Revised 2010
FMC HPC Header, GND

XILINX

Title:	FMC HPC Header, GND SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431760 1280681 0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	27 of 58	Drawn By	BF



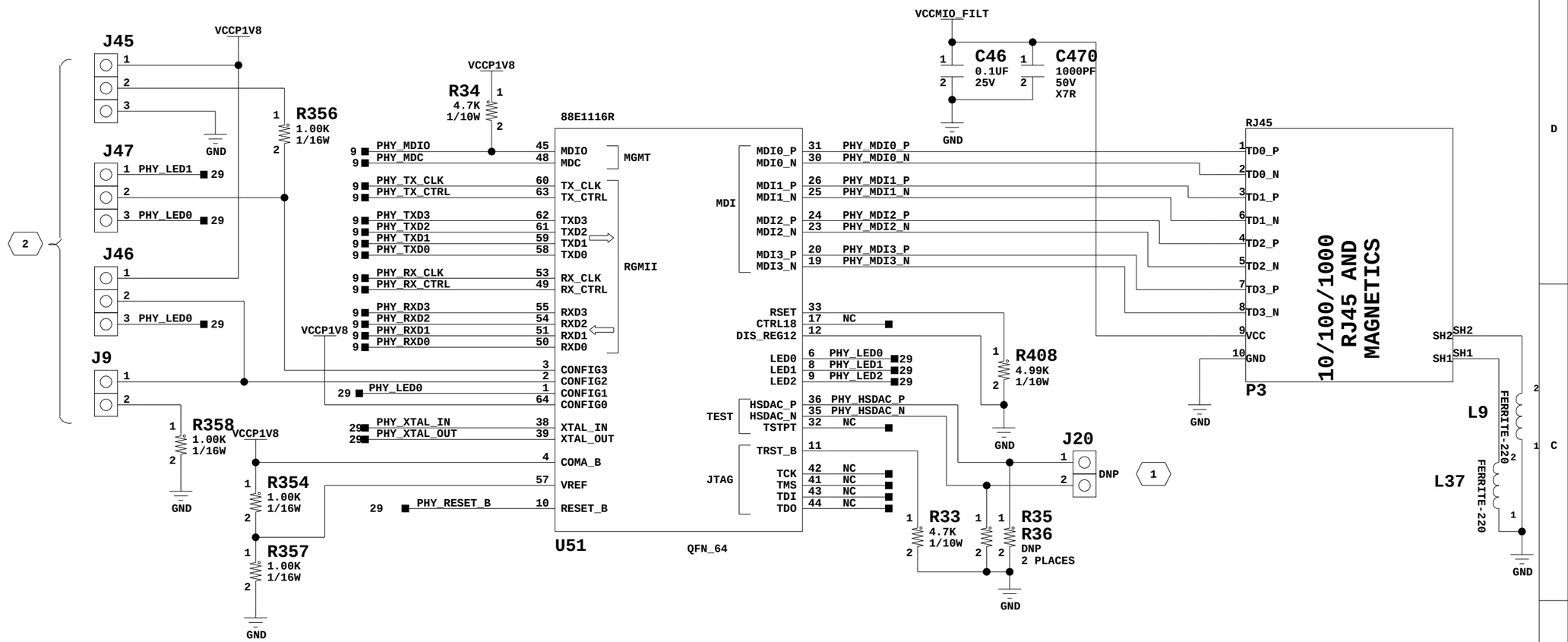
ANSI/VITA 57.1 - Revised 2010
FMC LPC Connector

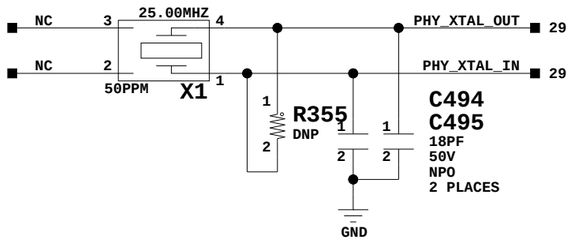
XILINX

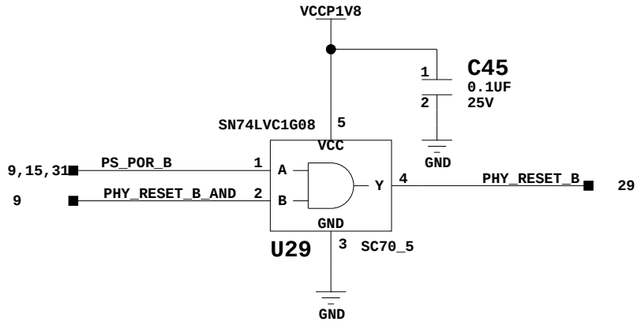
Title:	ANSI/VITA 57.1 - Revised 2010 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	28 of 58	Drawn By	BF

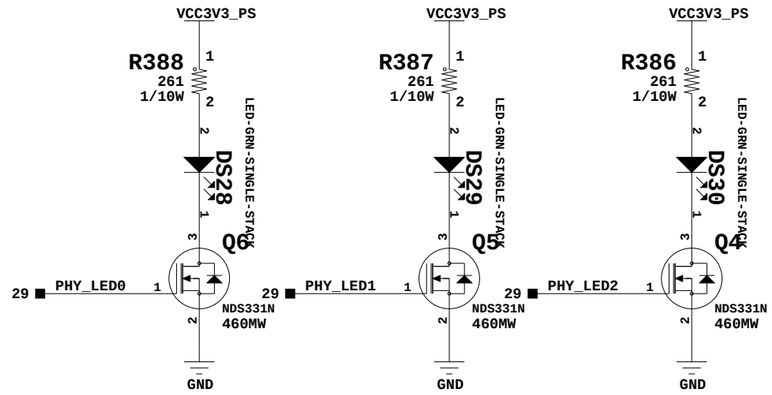
CONFIGURATION MAPPING

PIN	SETTING	CONFIGURATION	
CONFIG0	VCCO_MIO1	PHYAD[1]=1	PHYAD[0]=1
CONFIG1	EPHY_LED0	PHYAD[3]=0	PHYAD[2]=1
CONFIG2	GND	ENA_XC=0	PHYAD[4]=0
	EPHY_LED0	ENA_XC=0	PHYAD[4]=1
	VCCO_MIO1	ENA_XC=1	PHYAD[4]=1
CONFIG3	GND	RGMII_TX=0	RGMII_RX=0
	EPHY_LED0	RGMII_TX=0	RGMII_RX=1
	EPHY_LED1	RGMII_TX=1	RGMII_RX=0
	VCCO_MIO1	RGMII_TX=1	RGMII_RX=1









2 SEE CONFIGURATION MAPPING TABLE FOR JUMPER SETTINGS

1 TEST PORT: IF USING THE TEST PORT INSTALL 49.9 OHM PULLDOWN RESITORS ON HSDAC_P AND HSDAC_N.

GEM / MDIO

XILINX

Title:	GEM / MDIO SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
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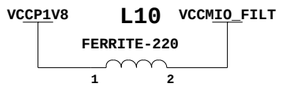
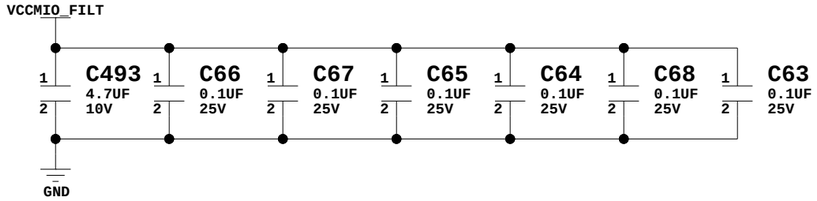
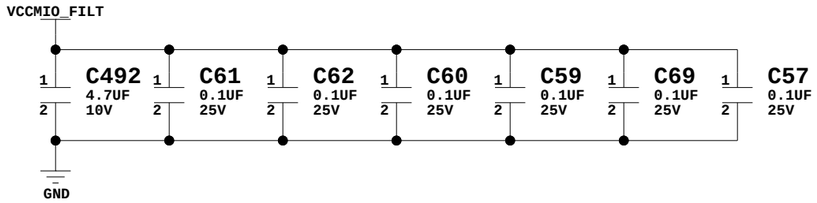
GEM / MDIO - POWER & DECOUPLING



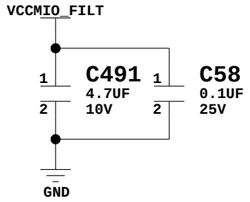
AVDDX, AVDDR, AVDDC



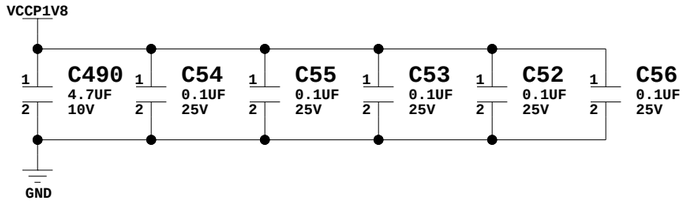
AVDD



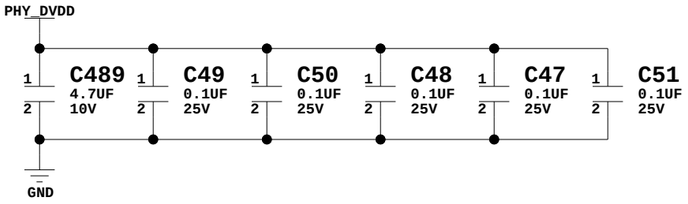
MAGNETICS / RJ45

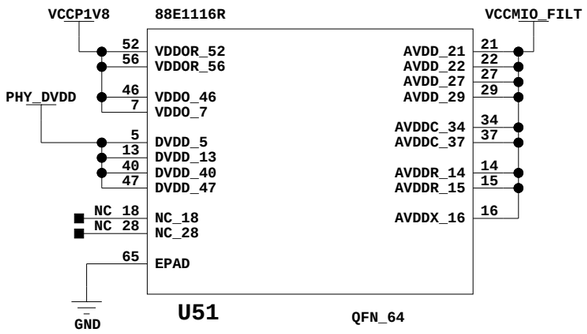


VDDO, VDDOR



DVDD





GEM / MDIO

XILINX

Title:	GEM / MDIO SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
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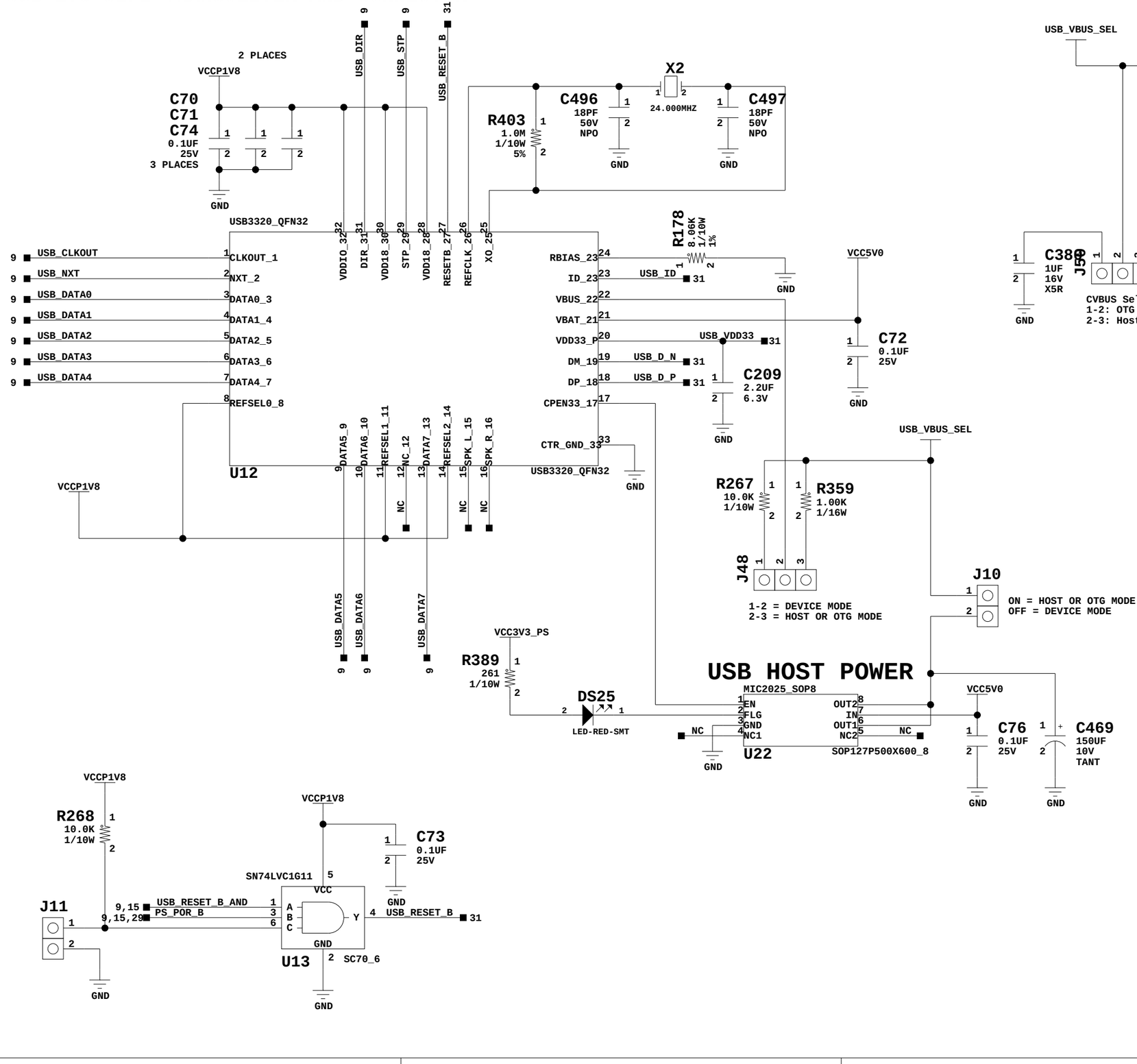
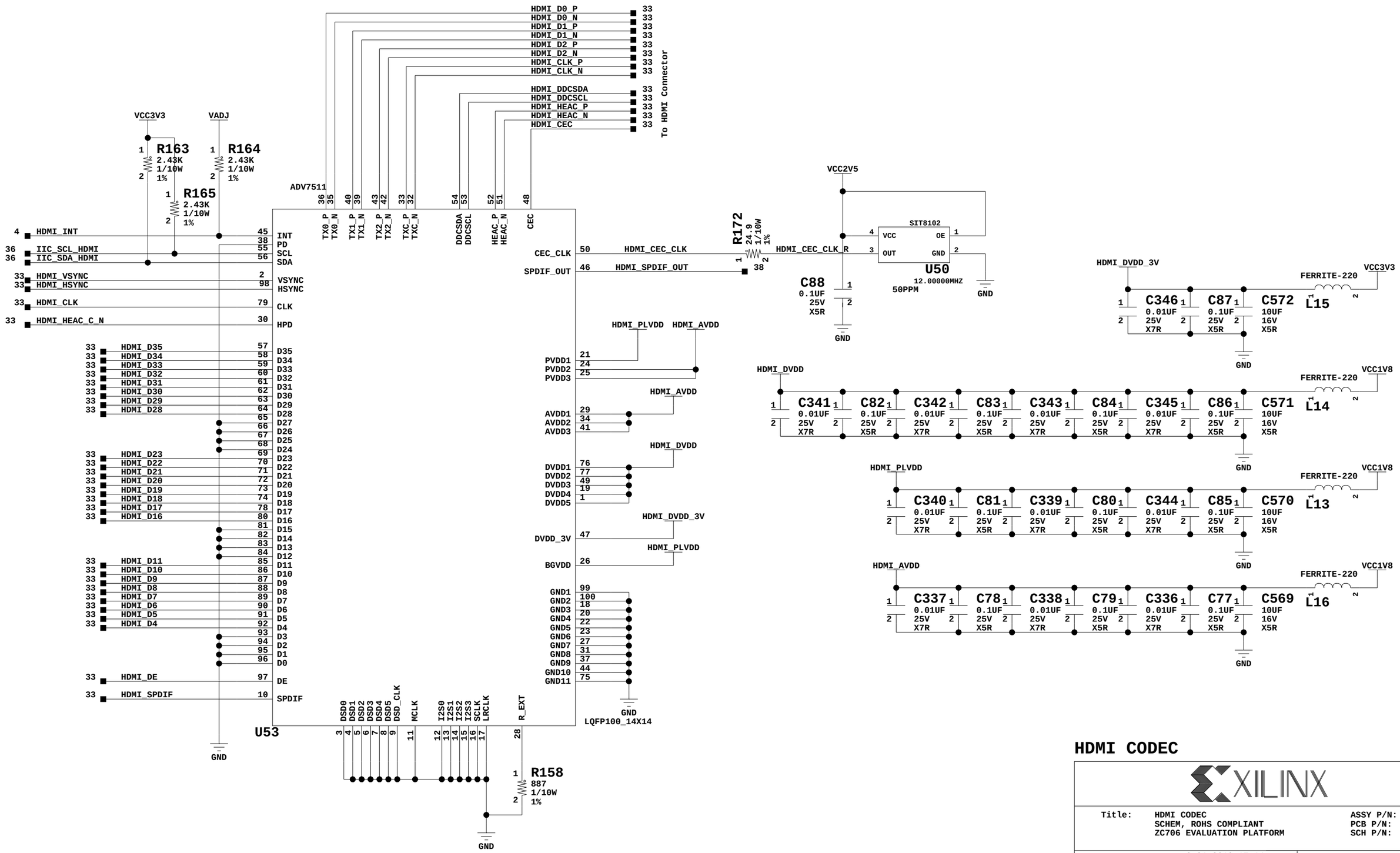
USB 2.0 ULPI TRANSCEIVER AND CONNECTOR



USB ULPI

XILINX

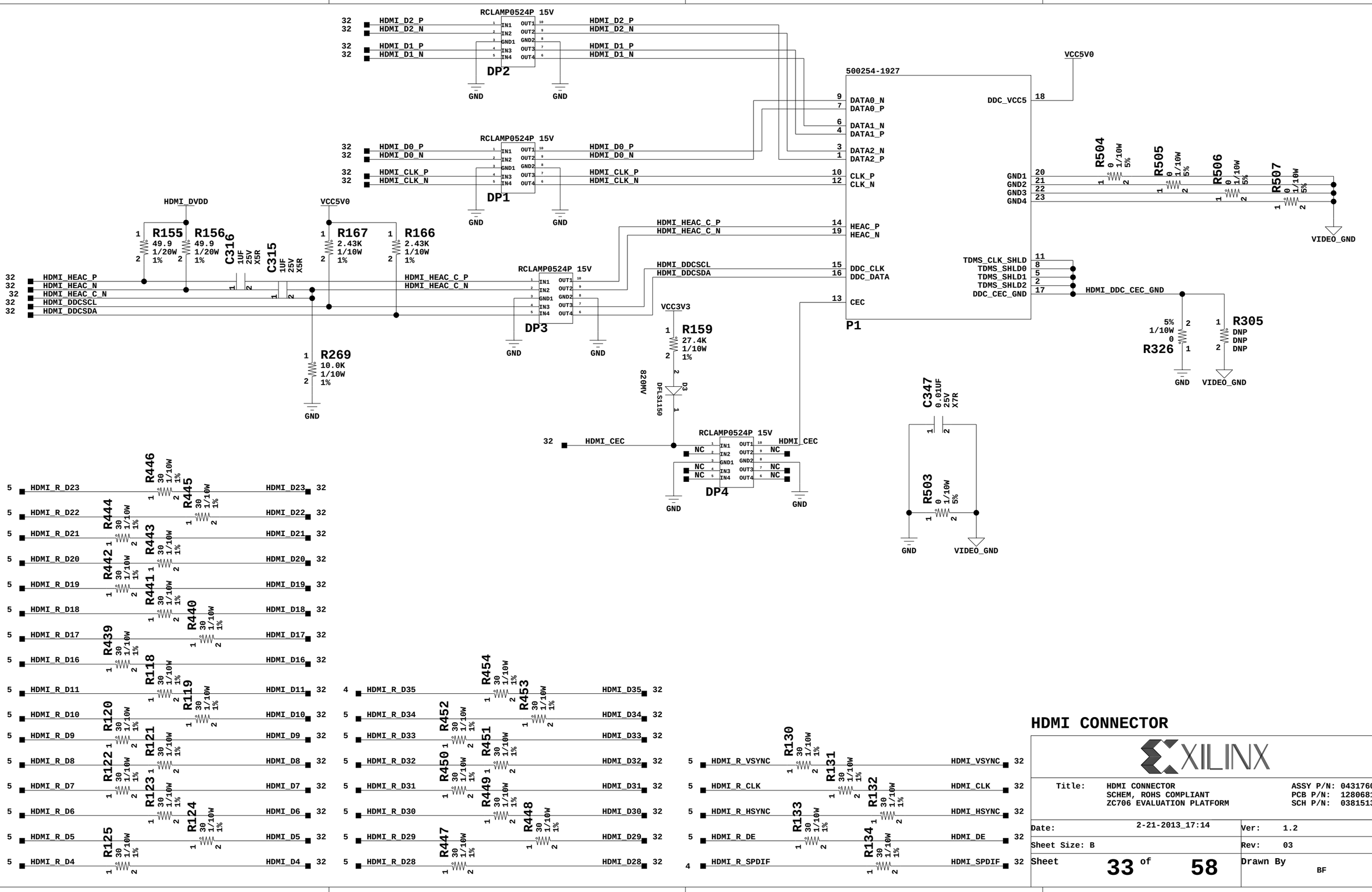
Title:	USB ULPI SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	31 of 58	Drawn By	BF



HDMI CODEC

XILINX

Title:	HDMI CODEC SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size:	B	Rev:	03
Sheet	32 of 58	Drawn By	BF


RCLAMP0524P 15V
DP2
DP1
DP3
DP4
GND
VIDEO_GND
HDMI_DVDD
VCC5V0
VCC3V3
500254-1927
P1
DDC_VCC5
GND1
GND2
GND3
GND4
DATA0_N
DATA0_P
DATA1_N
DATA1_P
DATA2_N
DATA2_P
CLK_P
CLK_N
HEAC_P
HEAC_N
DDC_CLK
DDC_DATA
CEC
TDMS_CLK_SHLD
TDMS_SHLD0
TDMS_SHLD1
TDMS_SHLD2
DDC_CEC_GND
HDMI_DDC_CEC_GND
HDMI_D2_P
HDMI_D2_N
HDMI_D1_P
HDMI_D1_N
HDMI_D0_P
HDMI_D0_N
HDMI_CLK_P
HDMI_CLK_N
HDMI_HEAC_P
HDMI_HEAC_N
HDMI_HEAC_C_P
HDMI_HEAC_C_N
HDMI_DDCSCL
HDMI_DDCSDA
HDMI_CEC
R155 49.9 1/20W 1%
R156 49.9 1/20W 1%
R167 2.43K 1/10W 1%
R166 2.43K 1/10W 1%
R269 10.0K 1/10W 1%
R159 27.4K 1/10W 1%
C316 1UF 25V X5R
C315 1UF 25V X5R
C347 0.01UF 25V X7R
R504 0 1/10W 5%
R505 0 1/10W 5%
R506 0 1/10W 5%
R507 0 1/10W 5%
R326 0 1/10W 5%
R305 DNP
R503 0 1/10W 5%
820MV
DFLS150
D3
HDMI_R_D23
HDMI_R_D22
HDMI_R_D21
HDMI_R_D20
HDMI_R_D19
HDMI_R_D18
HDMI_R_D17
HDMI_R_D16
HDMI_R_D11
HDMI_R_D10
HDMI_R_D9
HDMI_R_D8
HDMI_R_D7
HDMI_R_D6
HDMI_R_D5
HDMI_R_D4
HDMI_R_D35
HDMI_R_D34
HDMI_R_D33
HDMI_R_D32
HDMI_R_D31
HDMI_R_D30
HDMI_R_D29
HDMI_R_D28
HDMI_R_VSYNC
HDMI_R_CLK
HDMI_R_HSYNC
HDMI_R_DE
HDMI_R_SPDIF
R446 R445 R444 R443 R442 R441 R440 R439 R118 R119 R120 R121 R122 R123 R124 R125
R454 R453 R452 R451 R450 R449 R448 R447
R130 R131 R132 R133 R134
HDMI CONNECTOR
XILINX
Title: HDMI CONNECTOR
SCHEM, ROHS COMPLIANT
ZC706 EVALUATION PLATFORM
ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513
Date: 2-21-2013_17:14
Ver: 1.2
Sheet Size: B
Rev: 03
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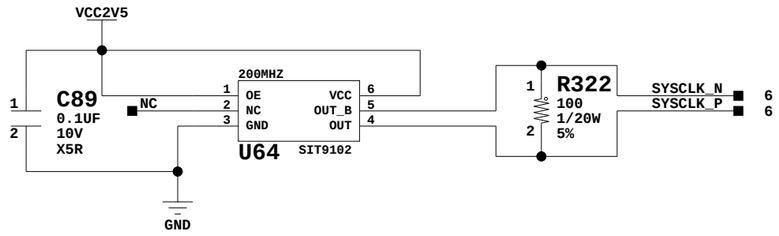
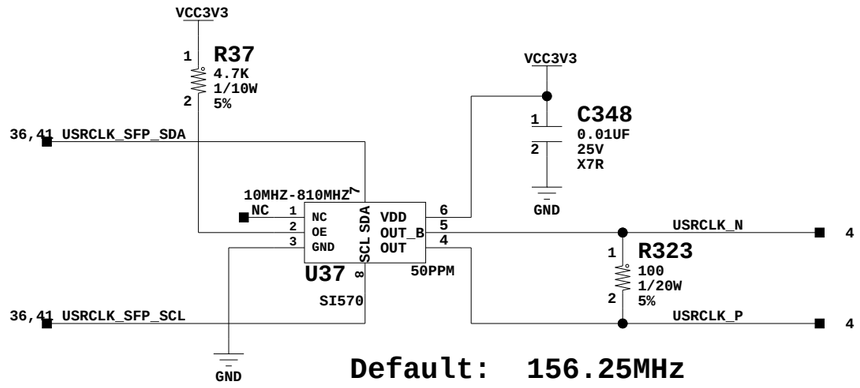
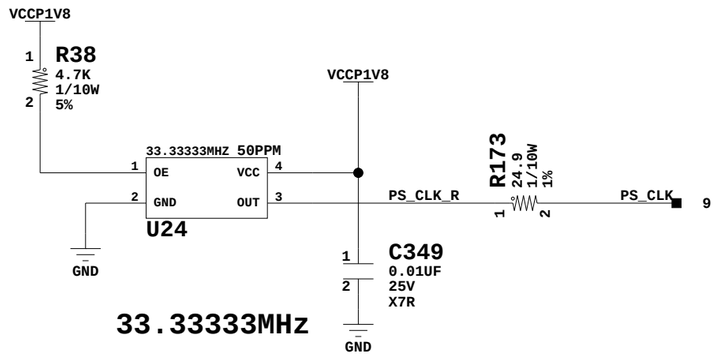
Drawn By BF

SIT9102AI-243N25E200.0000





Default: 156.25MHz



Clocks

XILINX

Title:	Clocks SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
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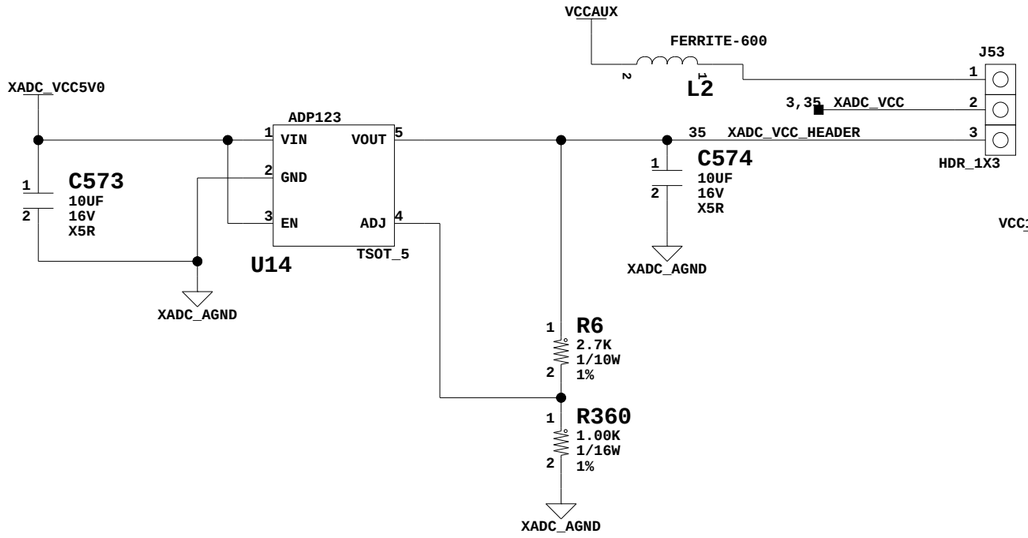
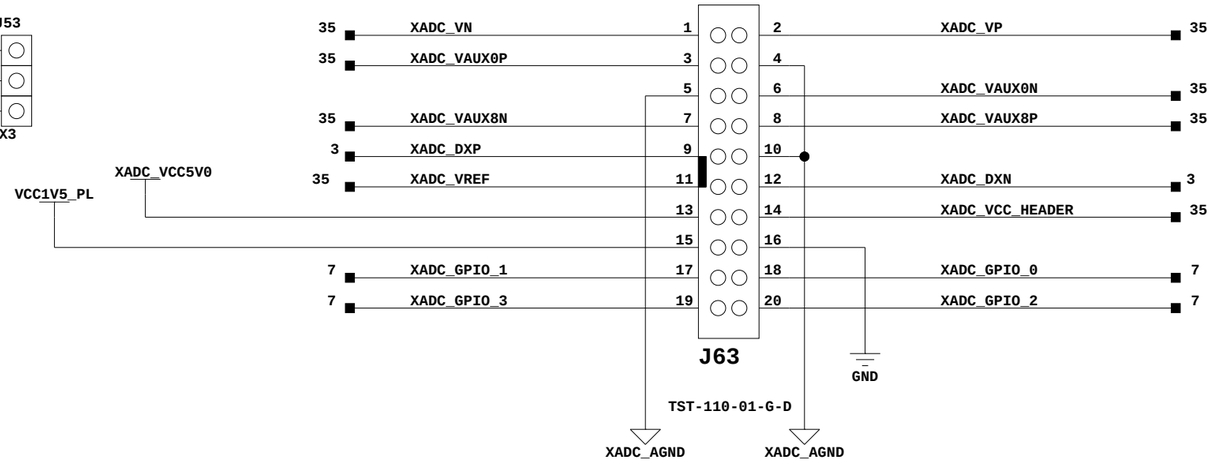
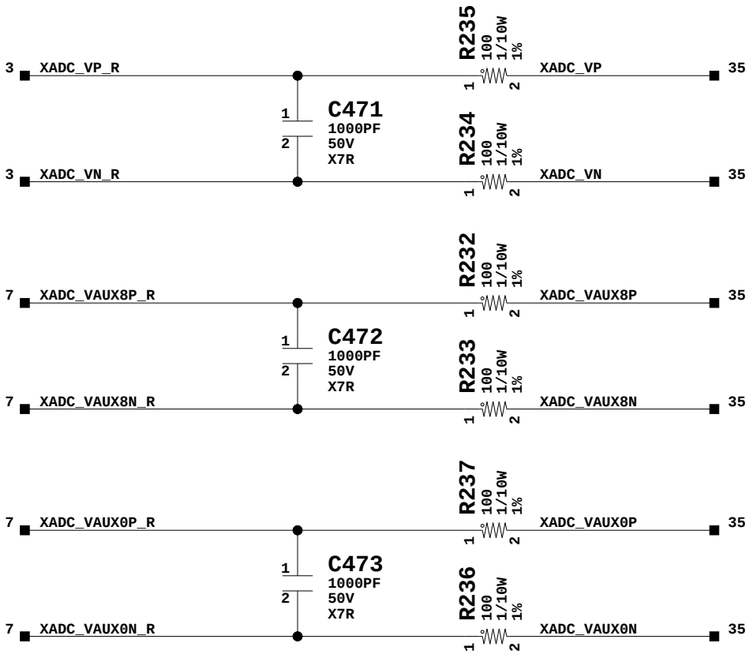
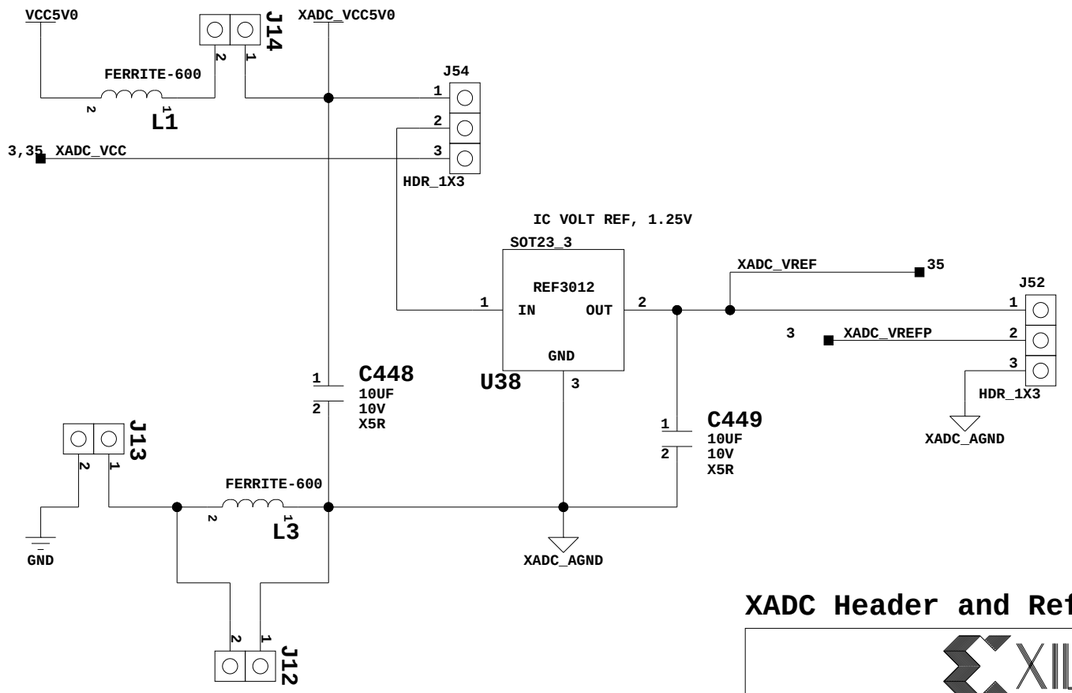




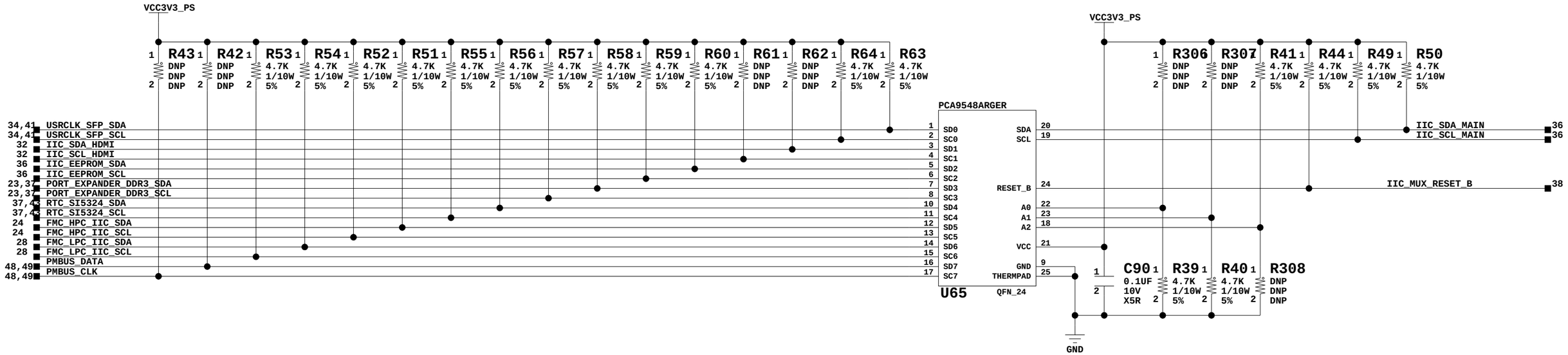




XADC Header and Reference

XILINX

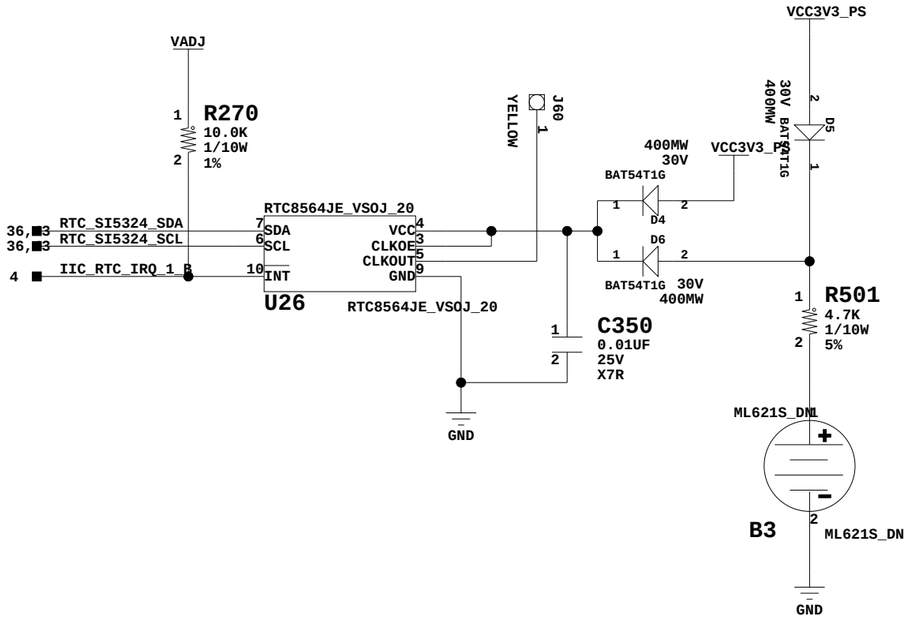
Title:	XADC Header and Reference SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	35 of 58	Drawn By	BF

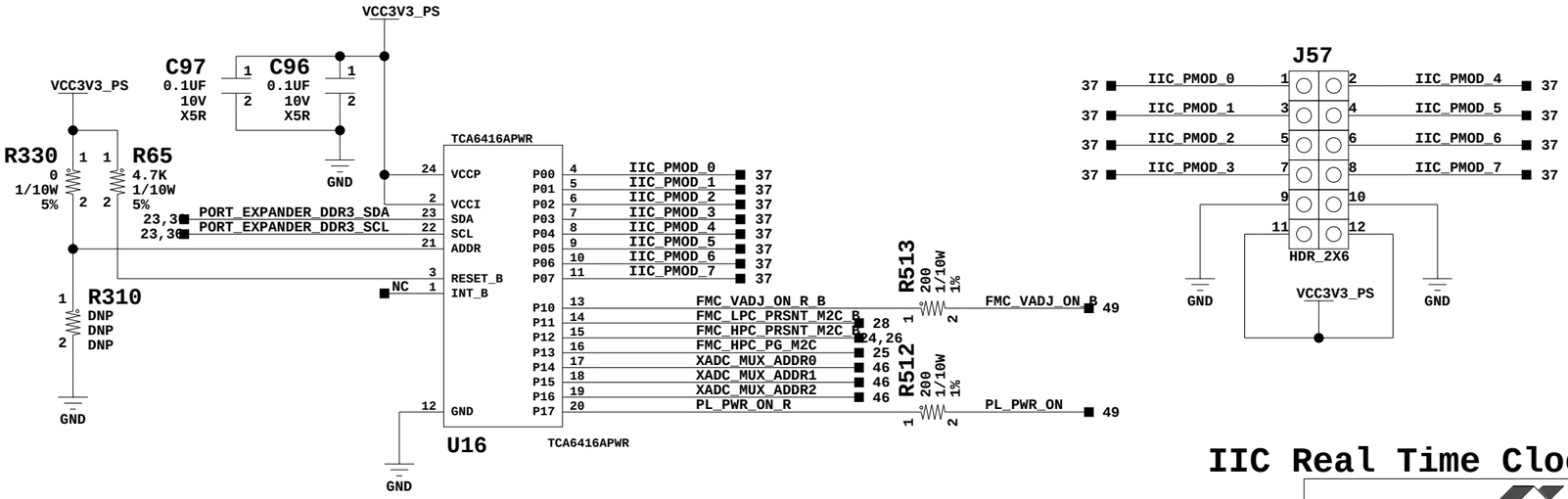


IIC MUX, EEPROM

XILINX

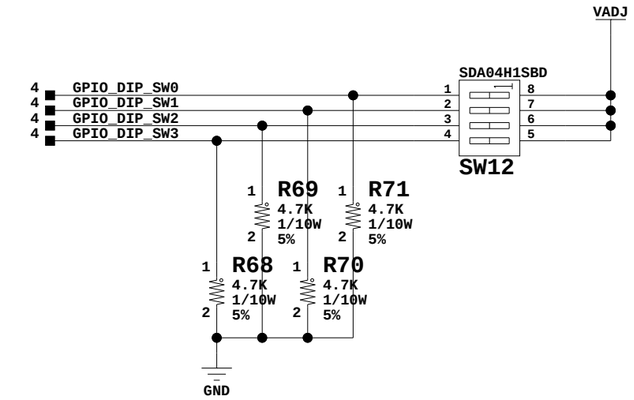
Title:	IIC MUX, EEPROM SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	36 of 58	Drawn By	BF

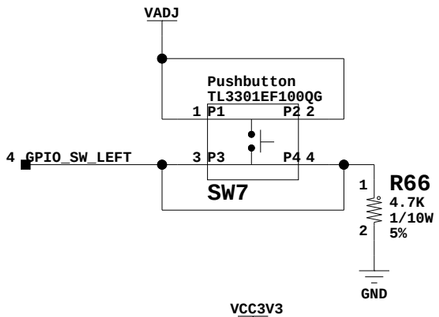


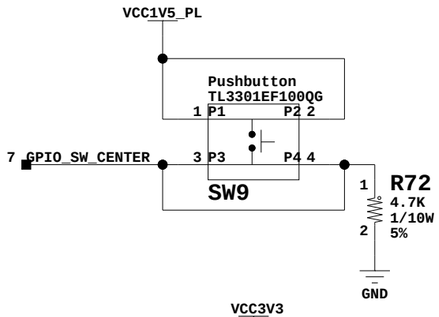


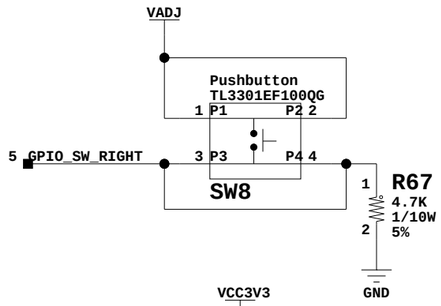
IIC Real Time Clock, Port Expander

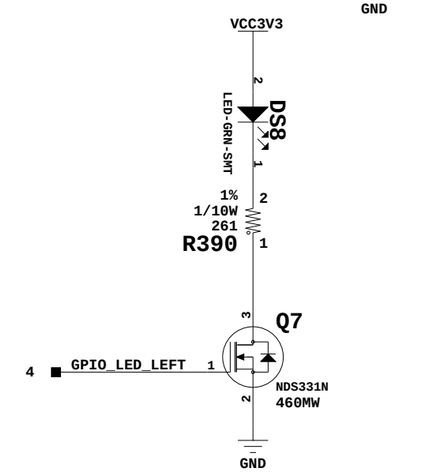
Title:	IIC Real Time Clock, Port Expander SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431760 1280681 0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	37 of 58	Drawn By	BF

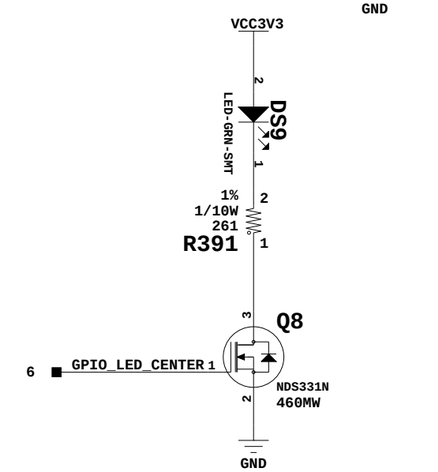


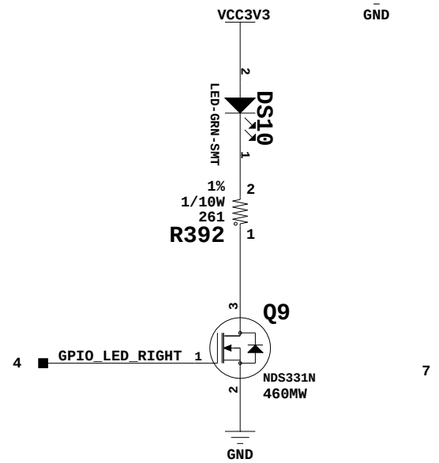


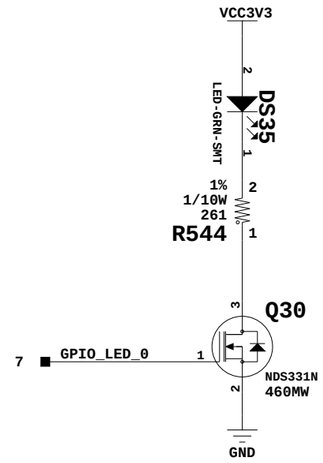


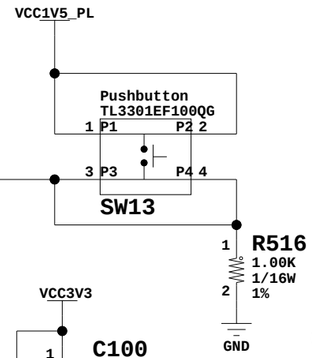


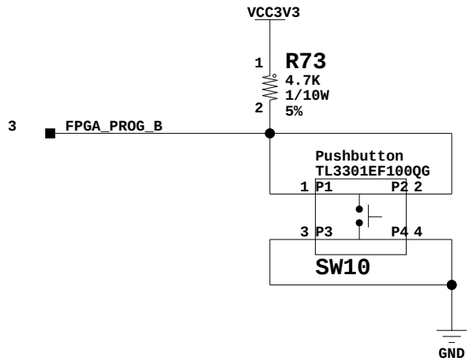


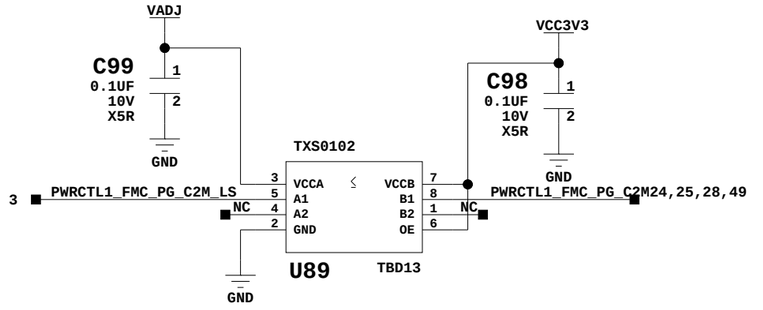


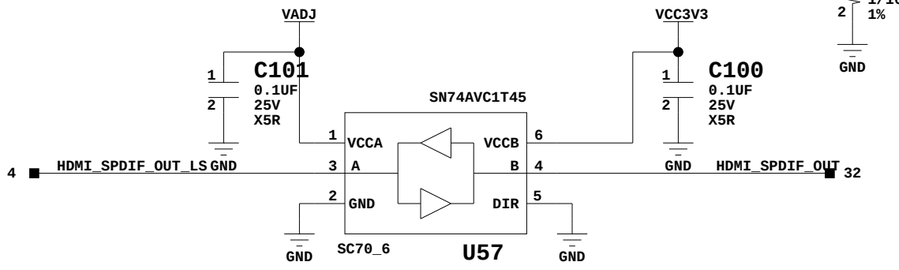








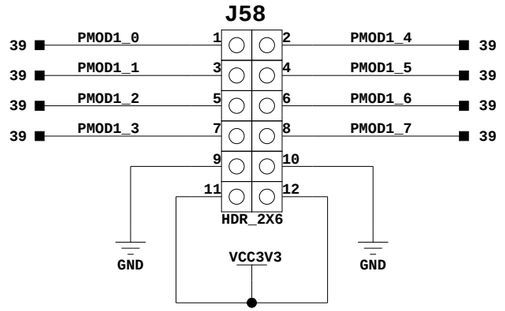


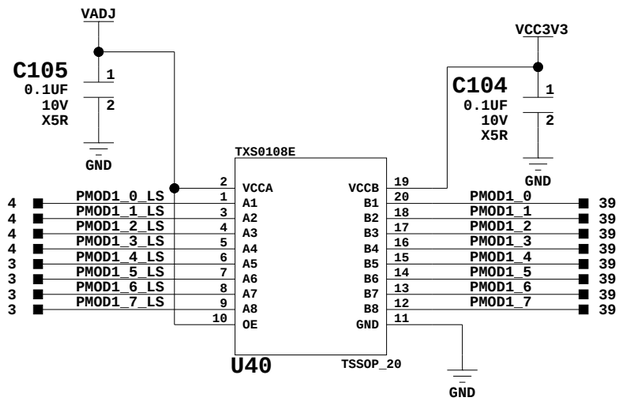


GPIO, Level Shifters

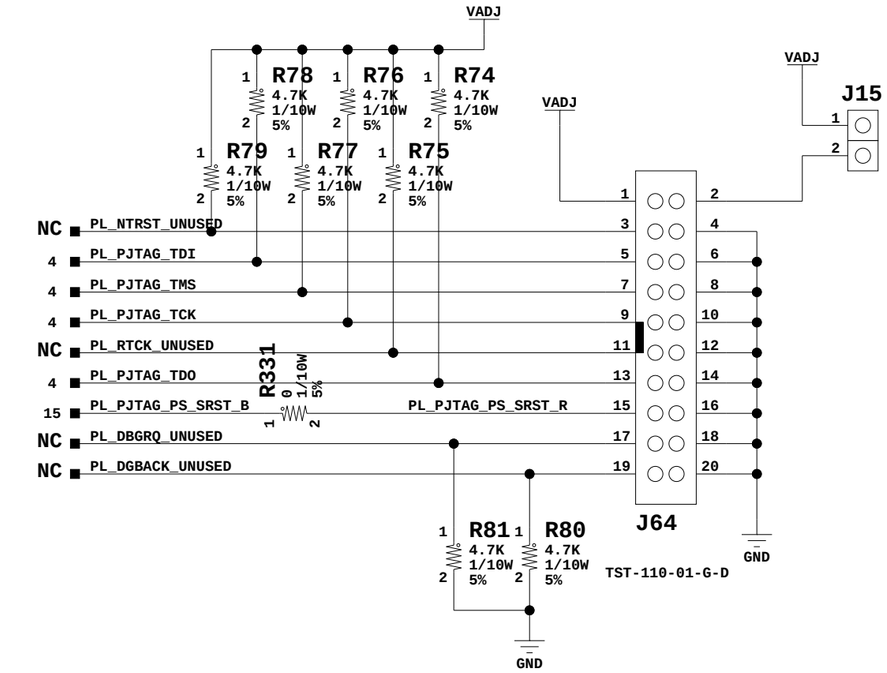
XILINX

Title:	GPIO, Level Shifters SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	38 of 58	Drawn By	BF



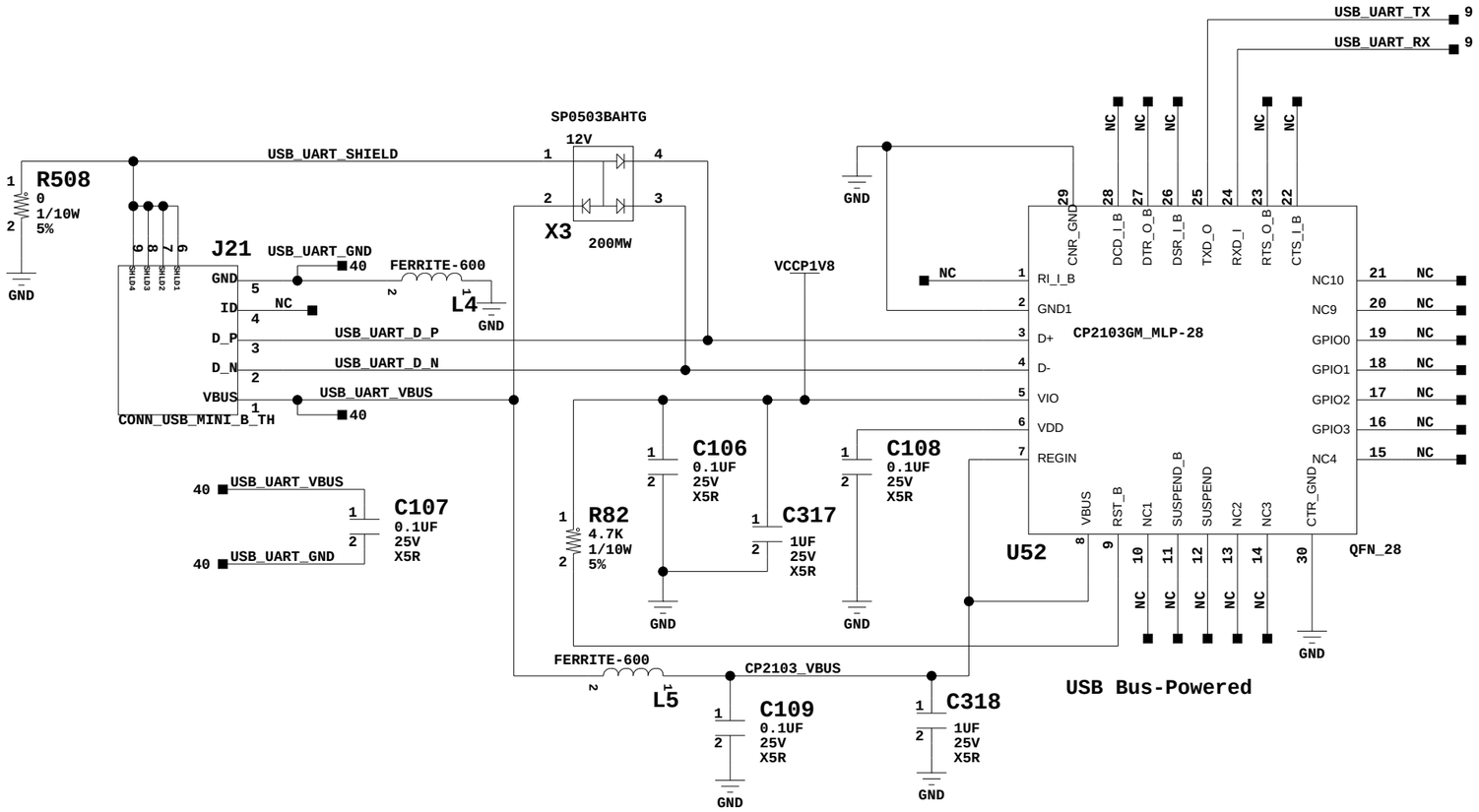


ARM PJTAG Header



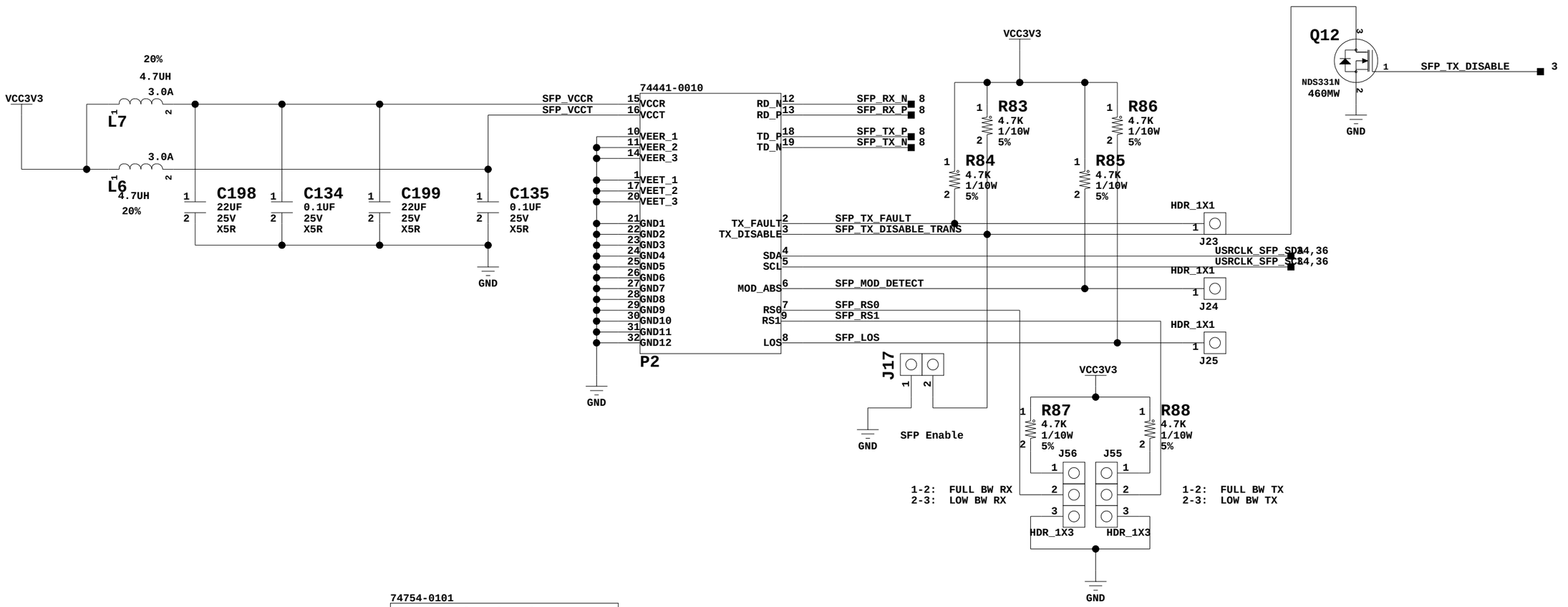
ARM PJTAG Header, PMOD1

Title:	ARM PJTAG Header, PMOD1 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	39 of 58	Drawn By	BF



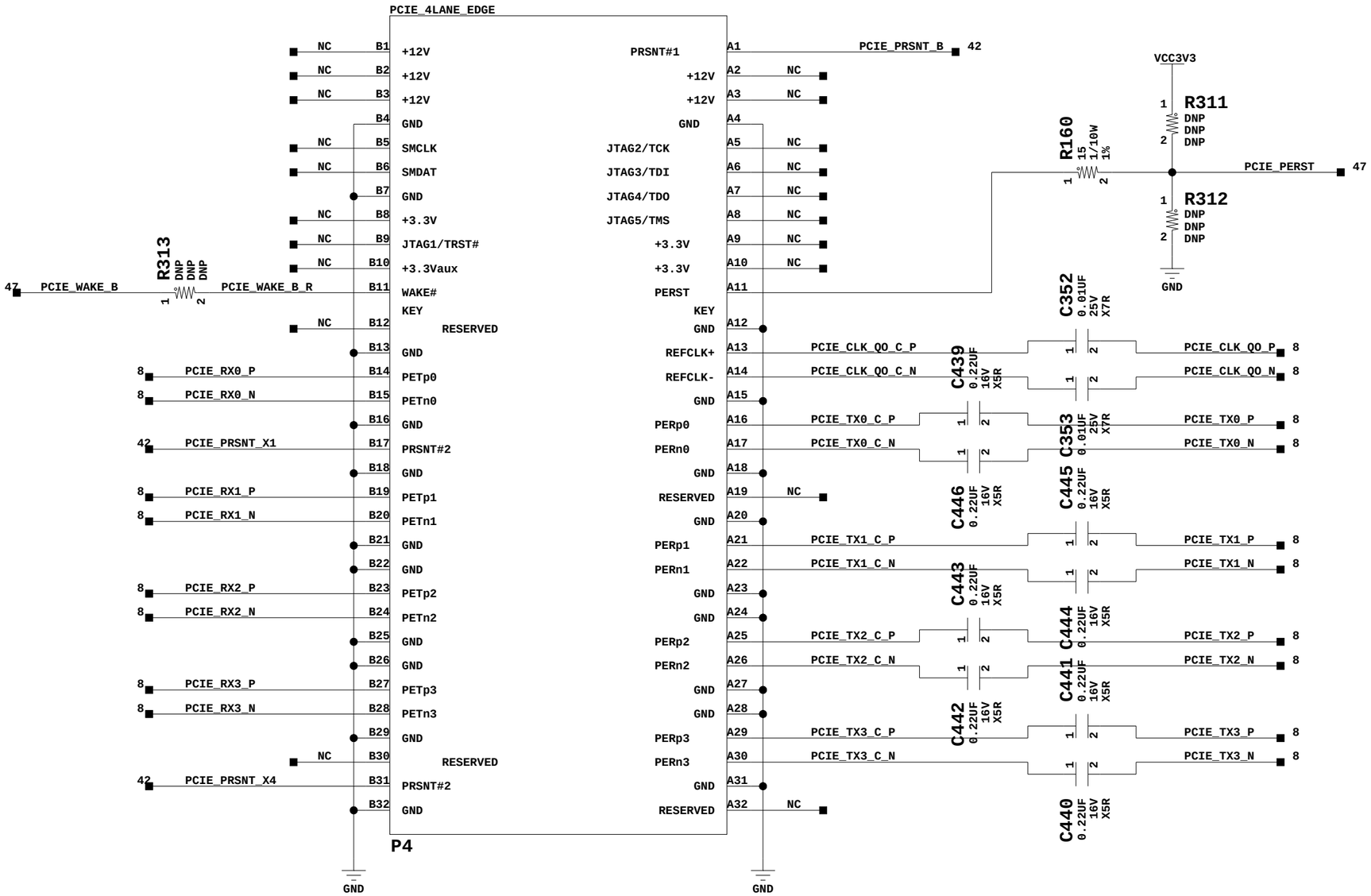
USB UART

Title:	USB UART SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	40 of 58	Drawn By	BF



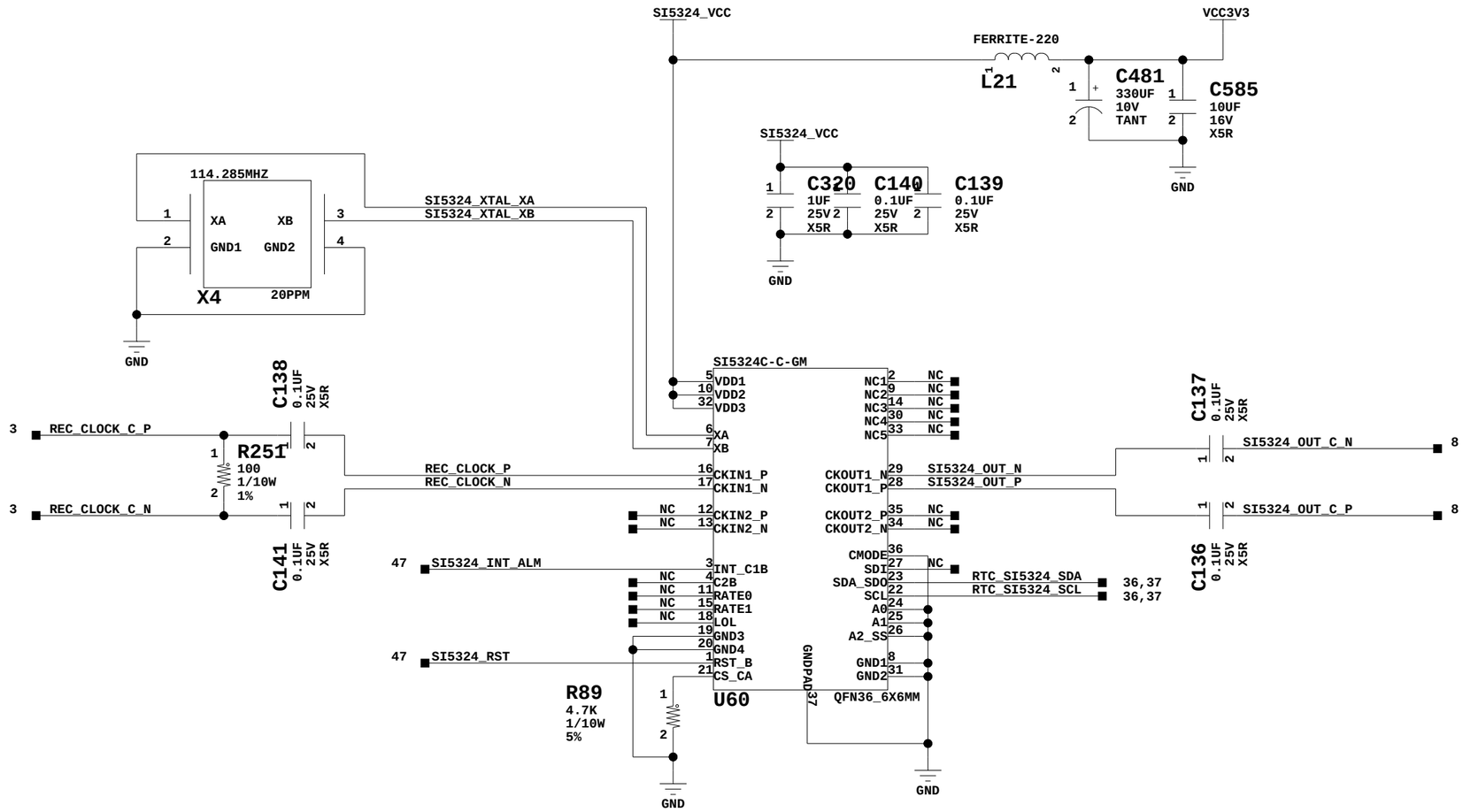
SFP+ Connector and Cage

Title:	SFP+ Connector and Cage SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	41 of 58	Drawn By	BF



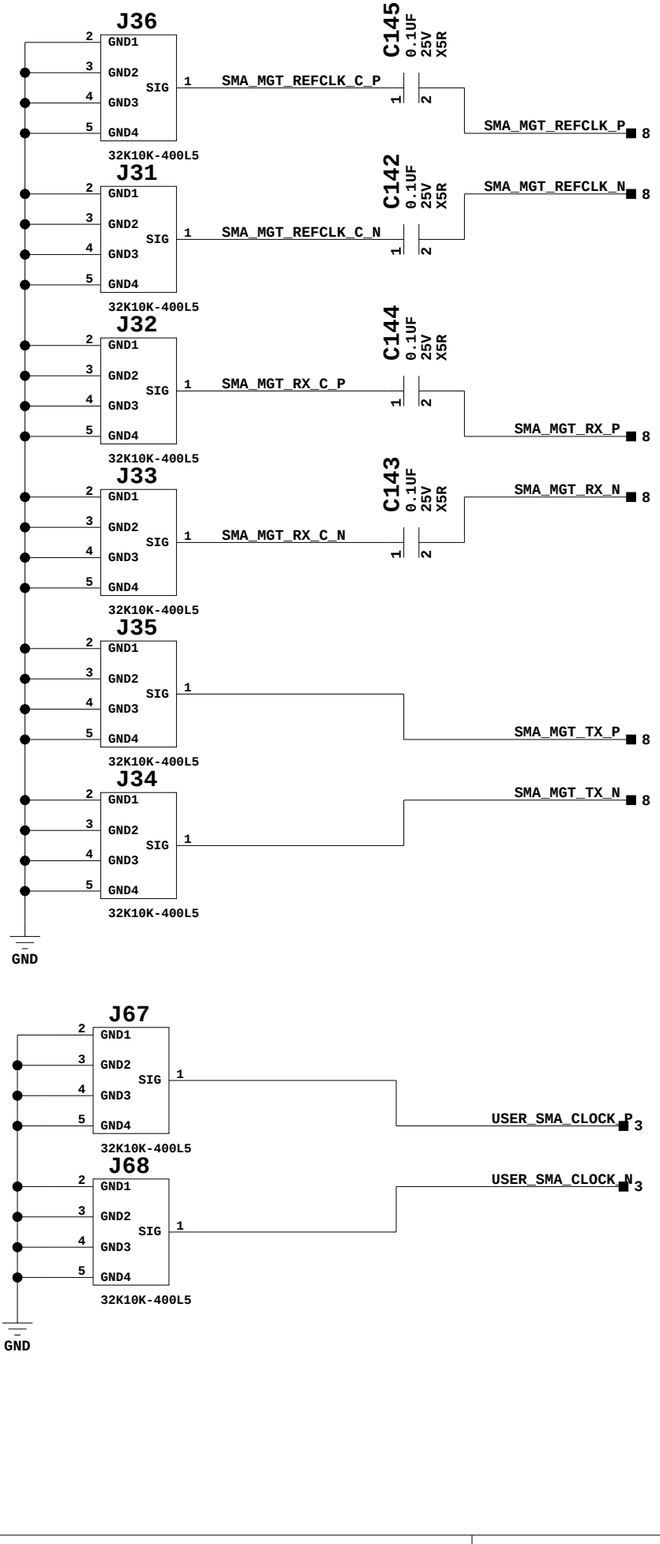
PCIe x4 Card edge

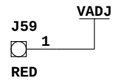
Title:	PCIe x8 Card edge SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	42 of 58	Drawn By	BF



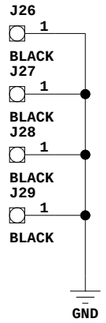
5324 Clock Recovery

Title:	5324 Clock Recovery SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	43 of 58	Drawn By	BF





Place near FMC connectors



SMA and Testpoints

XILINX

Title:	SMA and Testpoints SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
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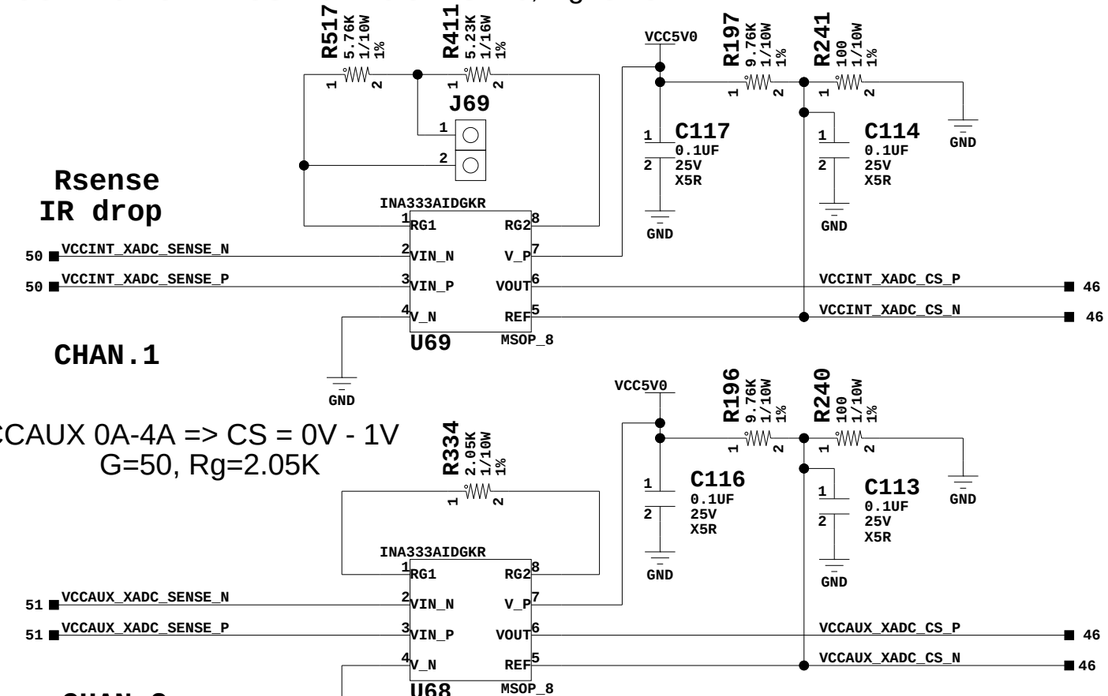
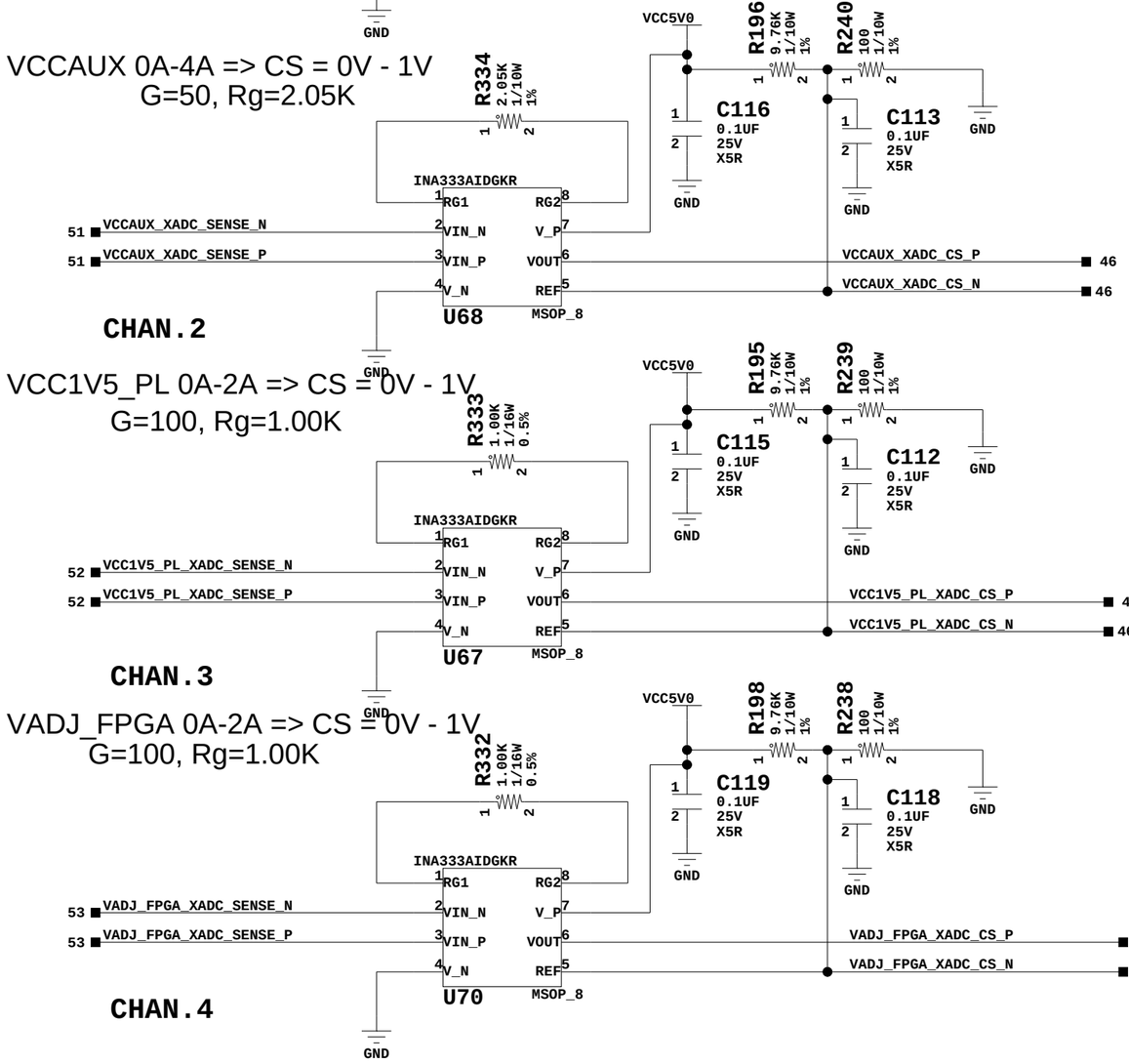
XADC I/F MONITORING CIRCUIT PAGE 1

CONTROLLER #1

VCCINT 0A-16A => CS = 0V - 0.8V G=10, Rg=11K
VCCINT 0A-8A => CS = 0V - 0.8V G=20, Rg=5.23K



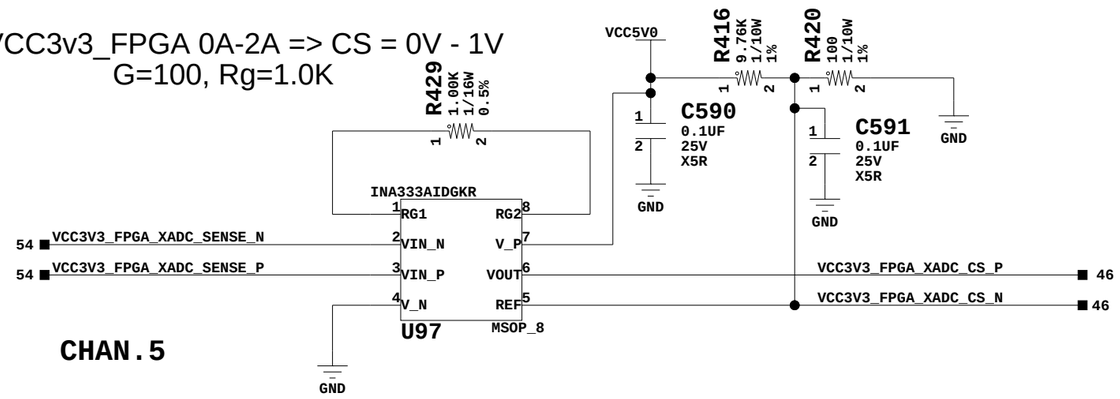
VCCAUX 0A-4A => CS = 0V - 1V
G=50, Rg=2.05K



VCC1V5_PL 0A-2A => CS = 0V - 1V
G=100, Rg=1.00K

VADJ_FPGA 0A-2A => CS = 0V - 1V
G=100, Rg=1.00K

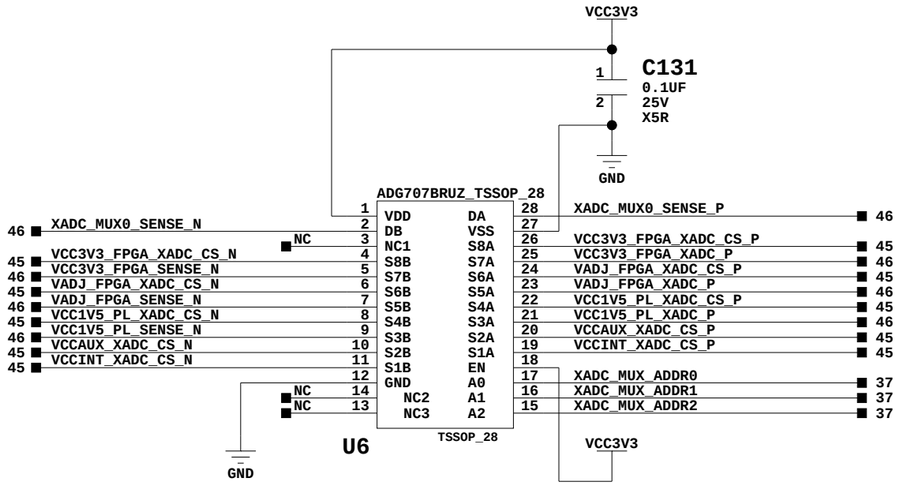
VCC3v3_FPGA 0A-2A => CS = 0V - 1V
G=100, Rg=1.0K

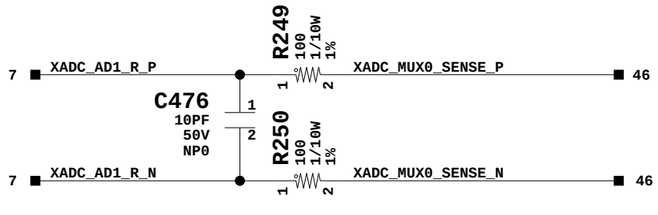


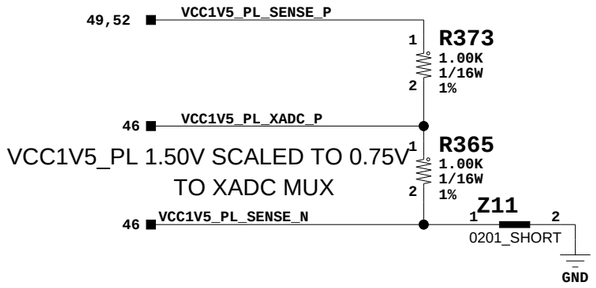
XADC I/F Monitoring Page 1

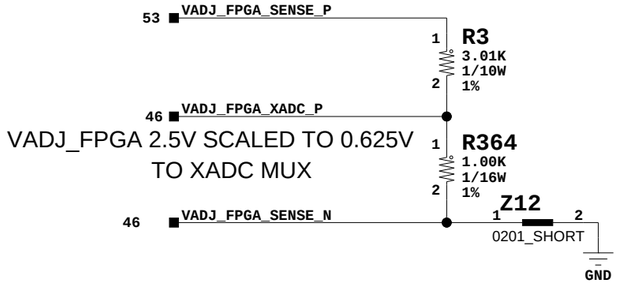
Title:	XADC I/F Monitoring Page 1 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	45 of 58	Drawn By	BF

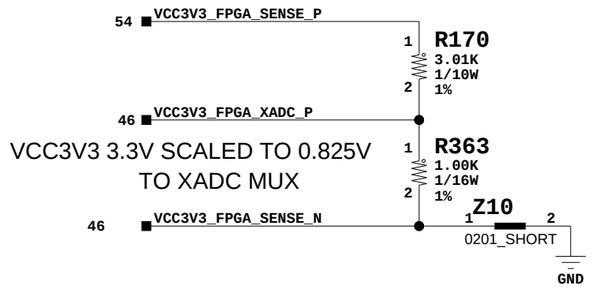
XADC I/F MONITORING CIRCUIT PAGE 2







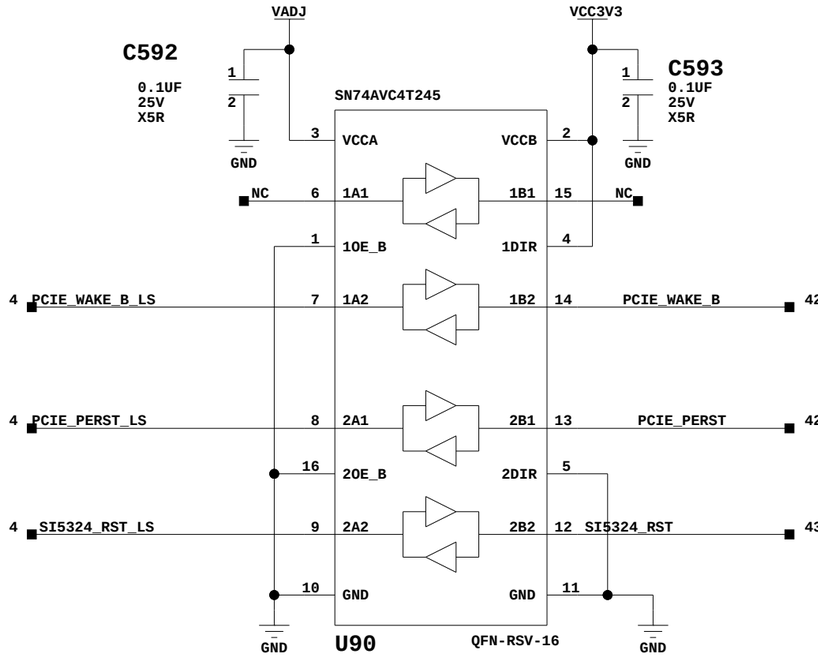


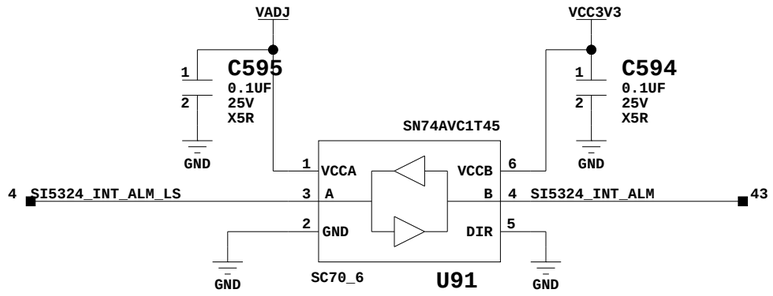


XADC I/F Monitoring Page 2

XILINX

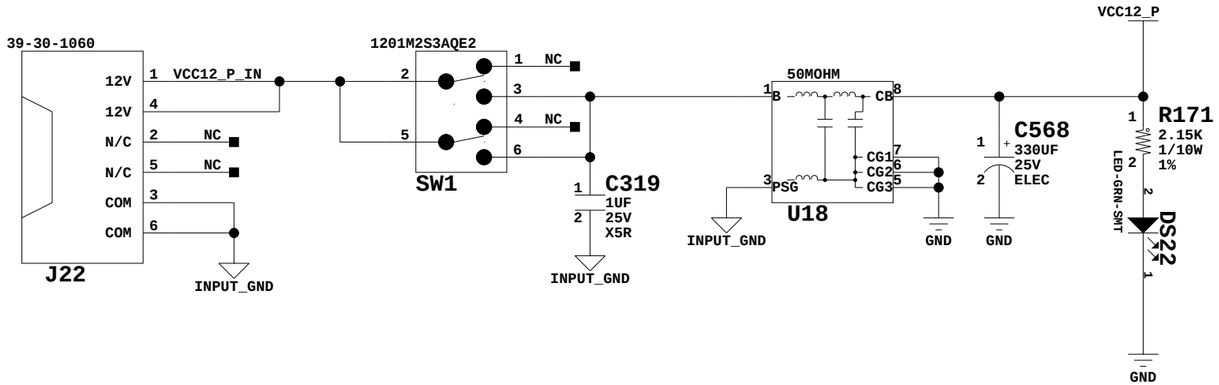
Title:	XADC I/F Monitoring Page 3 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	46 of 58	Drawn By	BF

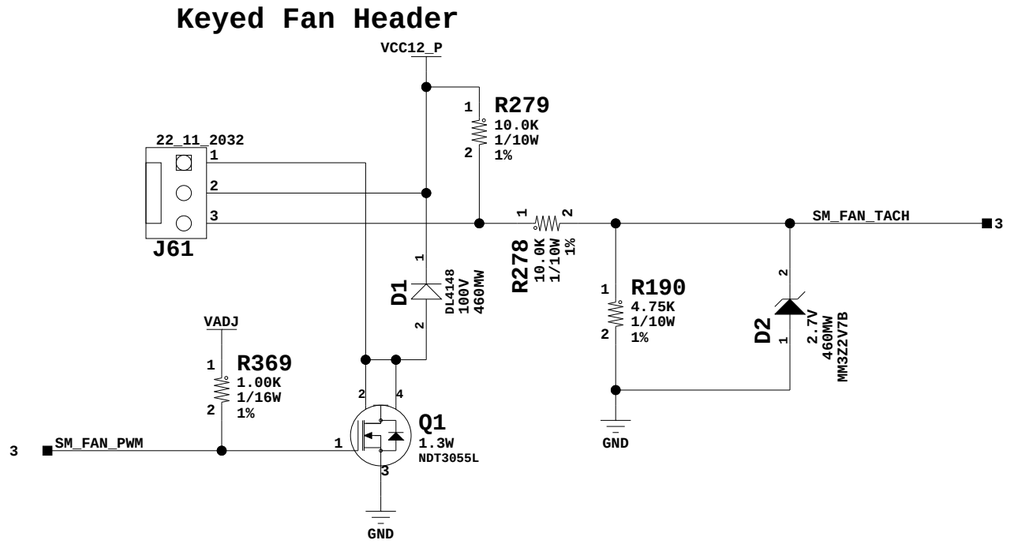


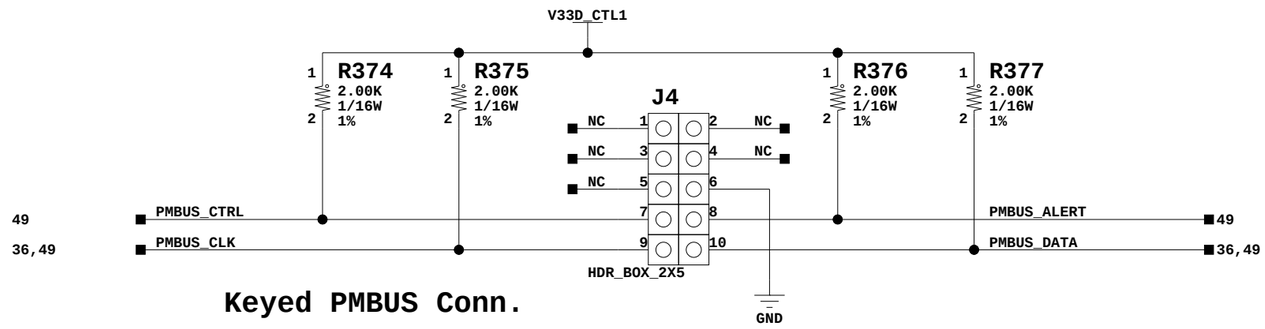


Level Shifters

Title:	Level Shifters SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431760 1280681 0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	47 of 58	Drawn By	BF







Keyed PMBUS Conn.

Power Connectors

Title:	Power Connectors SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 2-21-2013_17:14		Ver: 1.2
Sheet Size: B		Rev: 03
Sheet 48 of 58		Drawn By BF

PMBus Addr 101

VOLTAGE SENSE FILTERS

Tap into GND close to the SENSE_P pin

CURRENT SENSE

CURRENT SENSE FILTERS

Tap into GND close to the SENSE_P pin

VOLTAGE SENSE

RAIL ENABLES

MARGIN TRIM

MARGIN R4's

MARGIN C1's

U48

UCD90120ARGC_VQFN64

VQFN_64

PLACE CLOSE TO PINS44,45

U20

SOT223_6

TPS79433DCQR

250MA

POWER CONTROLLER 1

XILINX

Title:	POWER CONTROLLER 1 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size:	B	Rev:	03
Sheet	49 of 58	Drawn By	BF

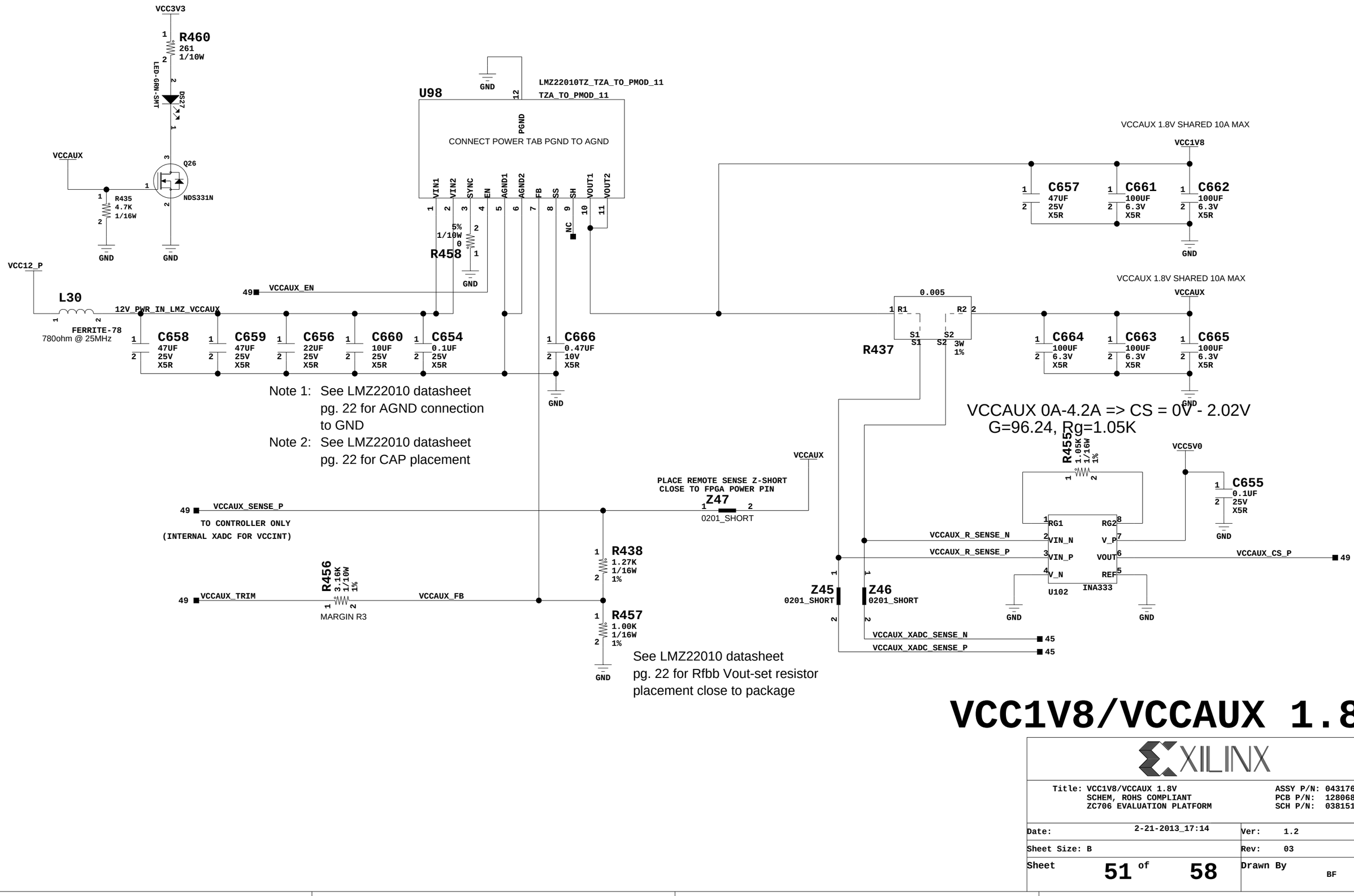
APPROX. 2 SQ. IN. CU HEATSINKING REQ'D AT 2 x 8A NO AIRFLOW

VCC12_P
L24
FERRITE-78
12V_PWR_IN_LMZ_VCCINT
C212 47UF 25V X5R
C211 47UF 25V X5R
C200 22UF 25V X5R
C269 10UF 25V X5R
C168 0.1UF 25V X5R
C213 47UF 25V X5R
C214 47UF 25V X5R
C201 22UF 25V X5R
C270 10UF 25V X5R
C169 0.1UF 25V X5R
GND
U43
LMZ22008TZ_TZA_TO_PMOD_11
TZA_TO_PMOD_11
PGND
CONNECT POWER TAB PGND TO AGND
VIN1 VIN2 SYNC EN AGND1 AGND2 FB SS SH VOUT1 VOUT2
5% 1/10W 0 R341
NC NC
VCCINT_SHARE
U42
LMZ22008TZ_TZA_TO_PMOD_11
TZA_TO_PMOD_11
PGND
CONNECT POWER TAB PGND TO AGND
VIN1 VIN2 SYNC EN AGND1 AGND2 FB SS SH VOUT1 VOUT2
5% 1/10W 0 R342
C566 0.47UF 10V X5R
49 VCCINT_EN
C210 47UF 25V X5R
C305 100UF 6.3V X5R
C304 100UF 6.3V X5R
C303 100UF 6.3V X5R
C302 100UF 6.3V X5R
C306 100UF 6.3V X5R
VCCINT_REG_OUT
0.005 R111 3W 1%
S1 S1 S2 S2
C300 100UF 6.3V X5R
C299 100UF 6.3V X5R
C298 100UF 6.3V X5R
C297 100UF 6.3V X5R
C301 100UF 6.3V X5R
VCCINT 1.0V 16A MAX
VCCINT
D8 1N5335BRLG 3.9V 320MA
GND
49 VCCINT_SENSE_P
TO CONTROLLER ONLY
(INTERNAL XADC FOR VCCINT)
Z24 0201_SHORT
REMOTE SENSE Z-SHORT PLACED
CLOSE TO FPGA POWER PIN
R316 1.69K 1/10W 1%
R193 9.09K 1/10W 1%
49 VCCINT_TRIM
VCCINT_VFB
MARGIN R3
R254 6.49K 1/10W 1%
R253 1.78K 1/10W 1%
VCCINT 0A-16A => CS = 0V - 2.02V
G=25.27, Rg=4.12K
R103 4.12K 1/10W 1%
VCC5V0
C167 0.1UF 25V
RG1 RG2 VIN_N V_P VIN_P VOUT V_N REF
INA333 U76
VCCINT_R_SENSE_N
VCCINT_R_SENSE_P
VCCINT_CS_P 49
Z21 0201_SHORT
Z22 0201_SHORT
VCCINT_XADC_SENSE_N 45
VCCINT_XADC_SENSE_P 45
VCC3V3
R394 261 1/10W
LED-GRN-SMT
DS11
VCCINT
Q15 NDS331N
R95 4.7K 1/16W
V33D_CTL1
LOW-POWER MODE SELECT
LOW_PWR_SEL = HI = 0.9V VCCINT
LOW_PWR_SEL = LOW = 1.0V VCCINT
49 LOW_PWR_SEL
R96 4.7K 1/16W
VCC A B OE GND
U33 NC7SZ66 SC70_5

VCCINT 1.0V

XILINX

Title: VCCINT 1.0V SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	50 of 58	Drawn By	BF



VCC1V8/VCCAUX 1.8V

XILINX

Title: VCC1V8/VCCAUX 1.8V SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	51 of 58	Drawn By	BF

VCC12_P

L26

12V_PWR_IN_TPS84K_VCC1V5_PL

FERRITE-78

C174 0.1UF 25V X5R

C228 47UF 25V X5R

C224 47UF 25V X5R

C203 22UF 25V X5R

C272 10UF 25V X5R

GND

See TPS84621 datasheet
pg. 23 for PGND-AGND short

Z2 0603_SHORT

VCC1V5_PL

Z31 0201_SHORT

REMOTE SENSE Z-SHORT PLACED

CLOSE TO FPGA POWER PIN

46,49 VCC1V5_PL_SENSE_P

49 VCC1V5_PL_TRIM

R184 3.74K 1/10W 1%

MARGIN R3

R4 953 1/10W 1%

AGND

VCC3V3

R293 10.0K 1/10W 1%

TPS84621RUQ_BQFN_47

VOUT8 PH7 AGND4 SENSE+ VADJ VIN PVIN3 PVIN2 PVIN1 PGND3

46 45 44 43 42 41 40 39 38

R345 200K 1/10W 1%

RTCLK_VCC1V5_PL

VCC1V5_PL_POWER_GOOD

1	AGND1		PGND2	37	
2	AGND2		PGND1	36	
NC 3	DNC1		RT_CLK	35	
NC 4	DNC2		AGND3	34	
NC 5	DNC3		PWRGD	33	
NC 6	SS_TR		DNC13	32 NC	
7	STSEL		DNC12	31 NC	
8	INH_UVLO1		DNC11	30 NC	
9	INH_UVLO2		VOUT7	29	
10	PH1		VOUT6	28	
11	PH2		VOUT5	27	
12	PH3		VOUT4	26	
13	PH4		VOUT3	24	
14	PH5		VOUT2	24	
NC 15	DNC4		DNC10	23 NC	

DNC5 PH6 DNC6 DNC7 DNC8 VOUT1 DNC9

16 17 18 19 20 21 22

NC NC NC NC NC

U85 BQFN_47

VCC1V5_PL_PH_ISLAND

49 VCC1V5_PL_EN

VCC1V5_PL_REG_OUT

C176 0.1UF 25V X5R

C229 47UF 25V X5R

C230 47UF 25V X5R

C231 47UF 25V X5R

GND

VCC3V3

R396 261 1/10W

LED-GRN-SMT

DS13

VCC1V5_PL

Q17

NDS331N

R98 4.7K 1/16W

GND GND

AGND

VCC1V5_PL 1.50V 6A MAX

VCC1V5_PL

R136

I1 I1 I2 I2

V1 V1 V2 V2

0.005 2W 1%

C226 47UF 25V X5R

C227 47UF 25V X5R

C225 47UF 25V X5R

GND

VCC1V5_PL 0A-3.8A => CS = 0V - 2.01V
G=105.93, Rg=953

VCC5V0

R5 953 1/10W 1%

C175 0.1UF 25V

GND

Z29 0201_SHORT

45 VCC1V5_PL_XADC_SENSE_N

45 VCC1V5_PL_XADC_SENSE_P

Z30 0201_SHORT

XADC TAP

VCC1V5_PL_R_SENSE_N

VCC1V5_PL_R_SENSE_P

1	RG1	RG2	8
2	VIN_N	V_P	7
3	VIN_P	VOUT	6
4	V_N	REF	5

U78 INA333

VCC1V5_PL_CS_P 49

GND GND

VCC1V5_PL 1.5V

XILINX

Title: VCC1V5_PL 1.5V SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
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VADJ (Default 2.5V)

VCC12_P

L28 FERRITE-78

12V_PWR_IN_TPS84K_VADJ

C180 0.1UF 25V X5R

C241 47UF 25V X5R

C240 47UF 25V X5R

C205 22UF 25V X5R

C274 10UF 25V X5R

GND

Z4 0603_SHORT

See TPS84621 datasheet pg. 23 for PGND-AGND short

REMOTE SENSE Z-SHORT PLACED

CLOSE TO FPGA POWER PIN

VADJ_FPGA

Z38 0201_SHORT

V33D_CTL1

C181 0.1UF 25V X5R

46 VADJ_FPGA_SENSE_P

49 VADJ_FPGA_TRIM

R2 2.21K 1/10W 1%

MARGIN R3

VADJ_FPGA_VADJ

R153 649 1/10W 1%

49 VADJ_FPGA_SCALED_P

VADJ 2.5V SCALED TO 2.0V TO CONTROLLER

R372 1.00K 1/16W 1%

(SCALE FACTOR = 0.800)

Place Scaling resistors near U48

TPS84621RUQ_BQFN_47

VOUT8 PH7 AGND4 SENSE+ VADJ VIN PVIN3 PVIN2 PVIN1 PGND3

AGND1 AGND2 DNC1 DNC2 DNC3 SS_TR STSEL INH_UVLO1 INH_UVLO2 PH1 PH2 PH3 PH4 PH5 DNC4

PGND2 PGND1 RT_CLK AGND3 PWRGD DNC13 DNC12 DNC11 VOUT7 VOUT6 VOUT5 VOUT4 VOUT3 VOUT2 DNC10

DNC5 PH6 DNC6 DNC7 DNC8 VOUT1 DNC9

U86 BQFN_47

VADJ_PH_ISLAND

SEE FMC VADJ VOLTAGE SELECT-->

RTCLK_VADJ

VADJ_FPGA_POWER_GOOD

R295 1% 1/10W 10.0K

VCC3V3

49 VADJ_FPGA_EN

IDTQS3VH253QG8

EA_B S1 I3A I2A I1A I0A YA GND VCC EB_B S0 I3B I2B I1B I0B YB

U66

49 VADJ_SEL1

VADJ_SEL0 49

NC

R349 200K 1/10W 1%

R348 200K 1/10W 1%

R347 200K 1/10W 1%

R410 453 1/10W 1%

R188 715 1/10W 1%

R1 316 1/10W 1%

AGND

GND

VADJ 2.50V @ Shared 6A MAX

VADJ

C183 0.1UF 25V X5R

C245 47UF 25V X5R

C247 47UF 25V X5R

C246 47UF 25V X5R

FMC VADJ VOLTAGE SELECT

FMC_VADJ_SEL[1	0]	ADJ (V)
0	0	2.5V
0	1	1.8V
1	0	3.3V
1	1	NOT USED

VCC3V3

R398 261 1/10W

LED-GRN-SMT DS15

VADJ_FPGA

Q19 NDS331N

R100 4.7K 1/16W

GND

AGND

VADJ_FPGA 2.50V @ Shared 6A MAX

VADJ_FPGA

R138 0.005 2W 1%

V1 V2

C244 47UF 25V X5R

C243 47UF 25V X5R

C242 47UF 25V X5R

VADJ 0A-1.1A => CS = 0V - 2.01V

G=365.96, Rg=274

VCC5V0

R7 274 1/10W 1%

C182 0.1UF 25V X5R

XADC TAP

45 VADJ_FPGA_XADC_SENSE_N

45 VADJ_FPGA_XADC_SENSE_P

Z39 0201_SHORT

Z40 0201_SHORT

VADJ_FPGA_R_SENSE_N

VADJ_FPGA_R_SENSE_P

RG1 VIN_N VIN_P V_N RG2 V_P VOUT REF

U80 INA333

VADJ_FPGA_CS_P 49

Title:	VADJ (Default 2.5V) SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM
ASSY P/N:	0431760
PCB P/N:	1280681
SCH P/N:	0381513
Date:	2-21-2013_17:14
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Sheet Size:	B
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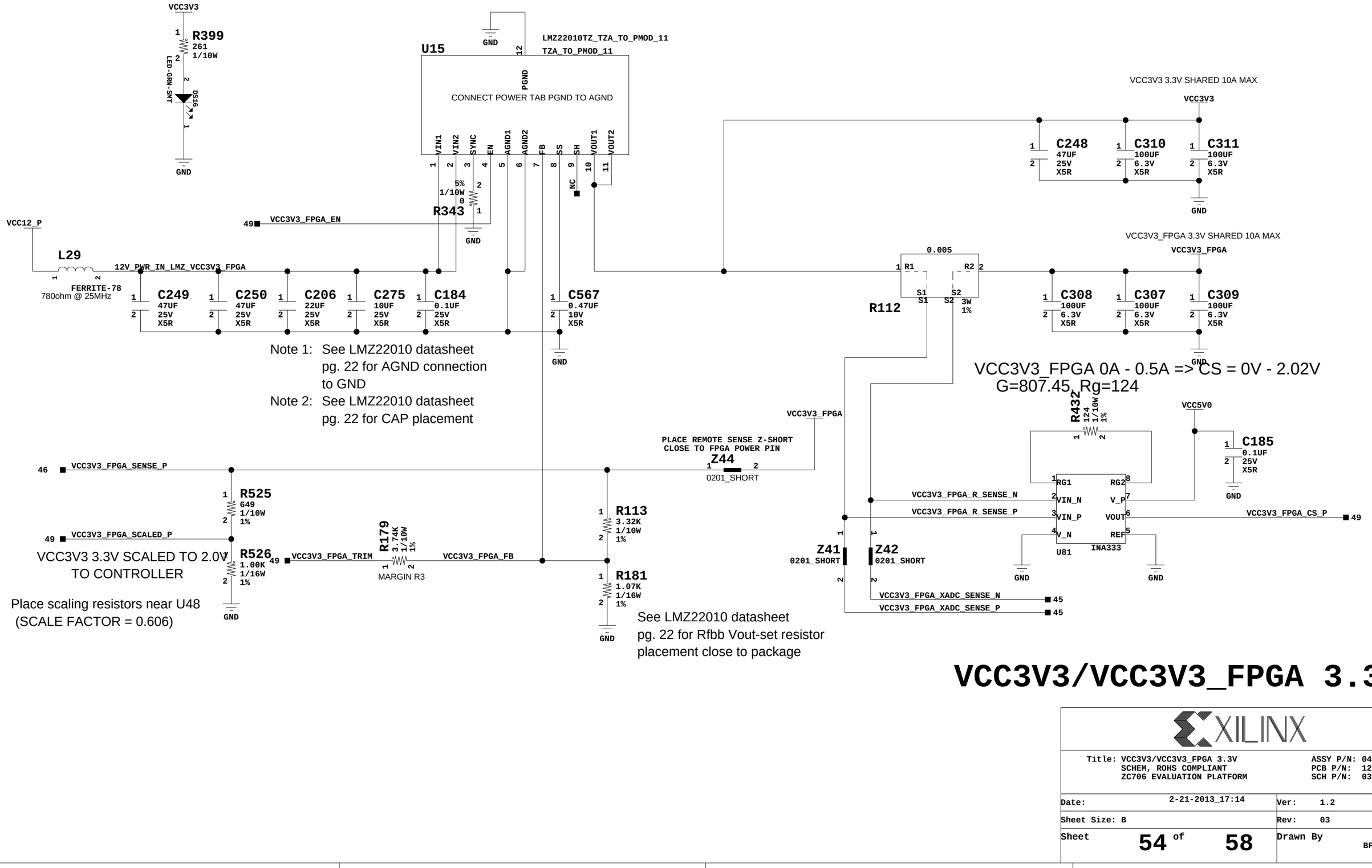
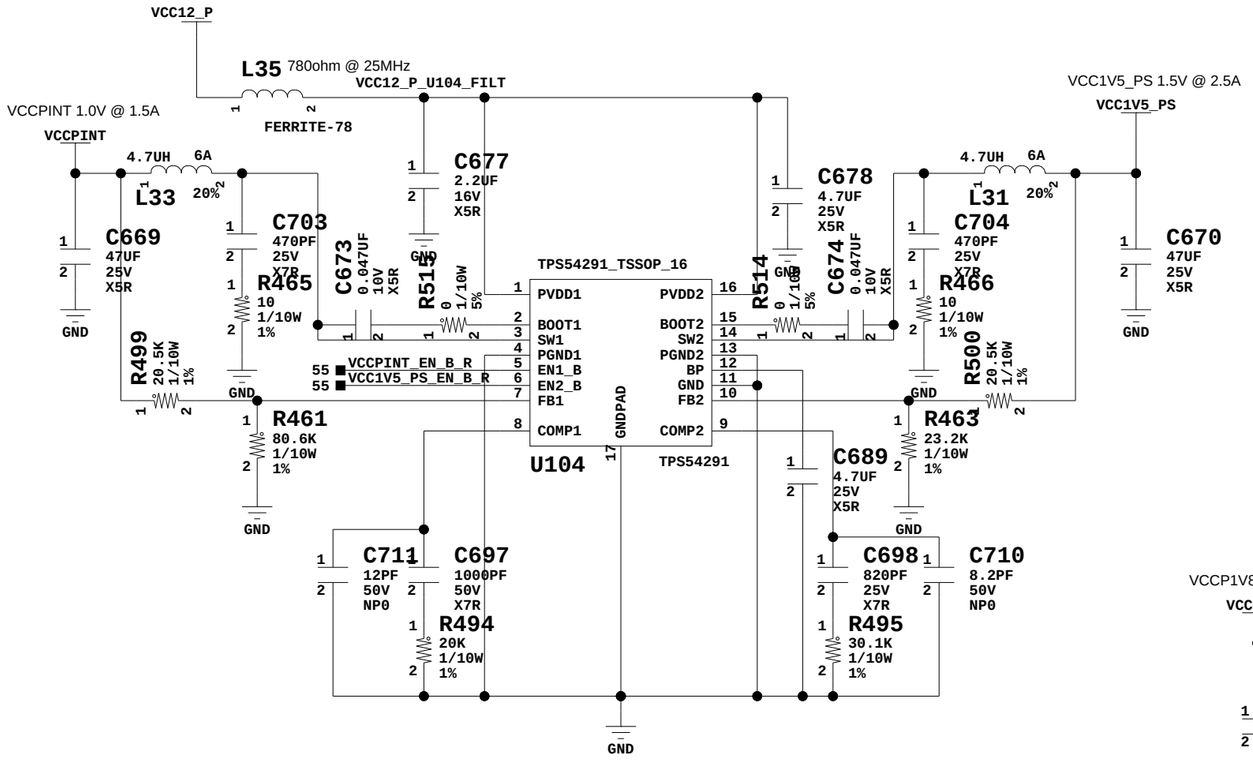
Drawn By	BF

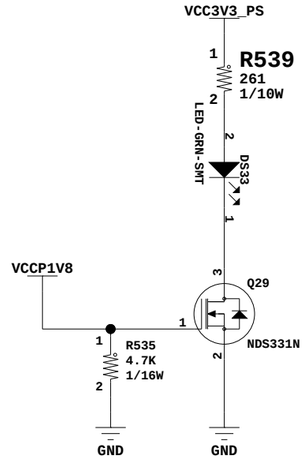


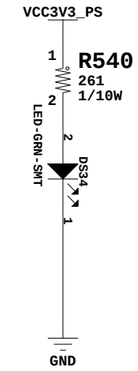
VCC3V3/VCC3V3_FPGA 3.3V

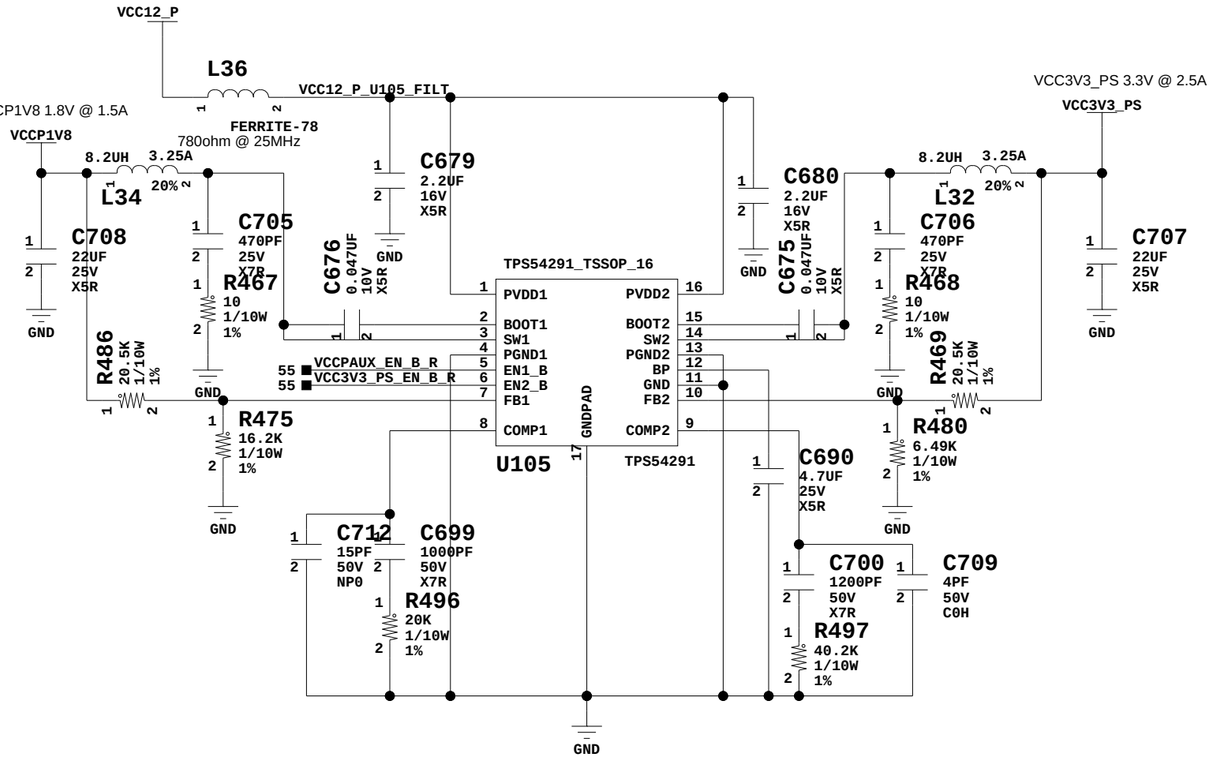
XILINX

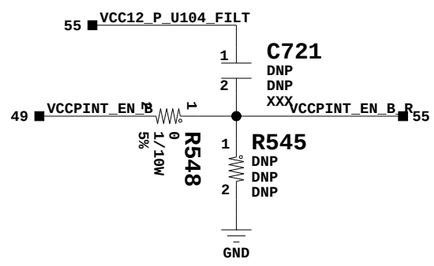
Title: VCC3V3/VCC3V3_FPGA 3.3V SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
Sheet	54 of 58	Drawn By	BF

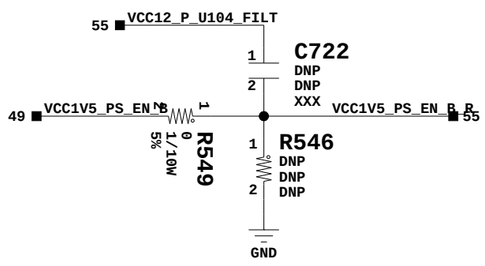


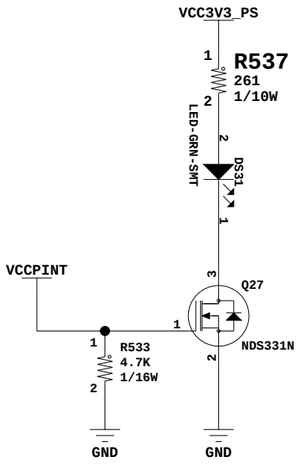


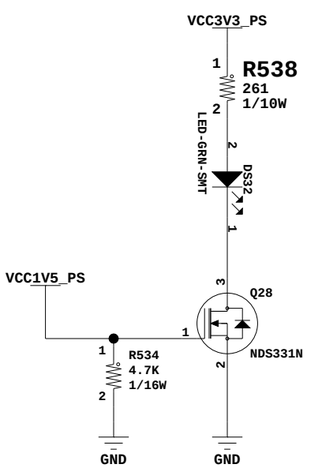


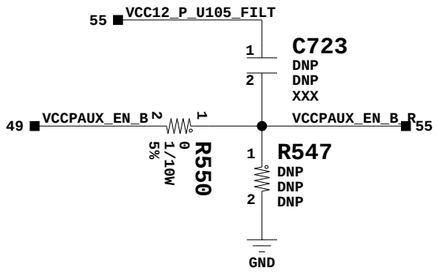


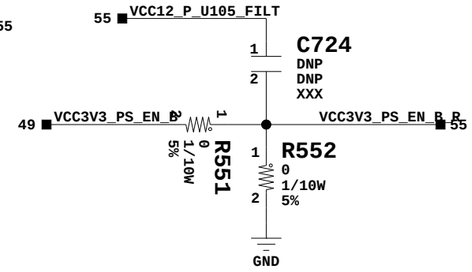












Dual switching supplies

XILINX

Title:	Dual switching supplies ZC706 EVALUATION PLATFORM SCHEM, ROHS COMPLIANT	ASSY P/N: PCB P/N: SCH P/N:	0431760 1280681 0381513
Date:	2-21-2013_17:14	Ver:	1.2
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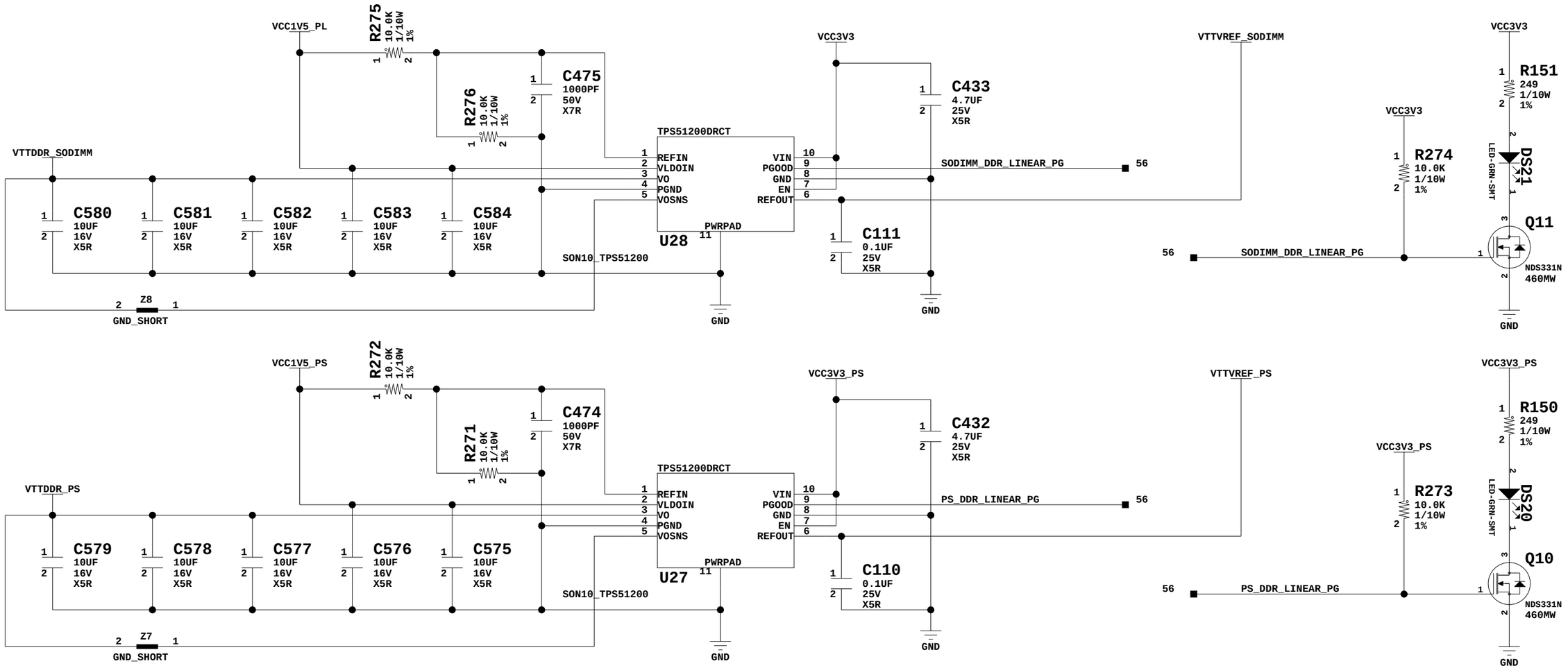

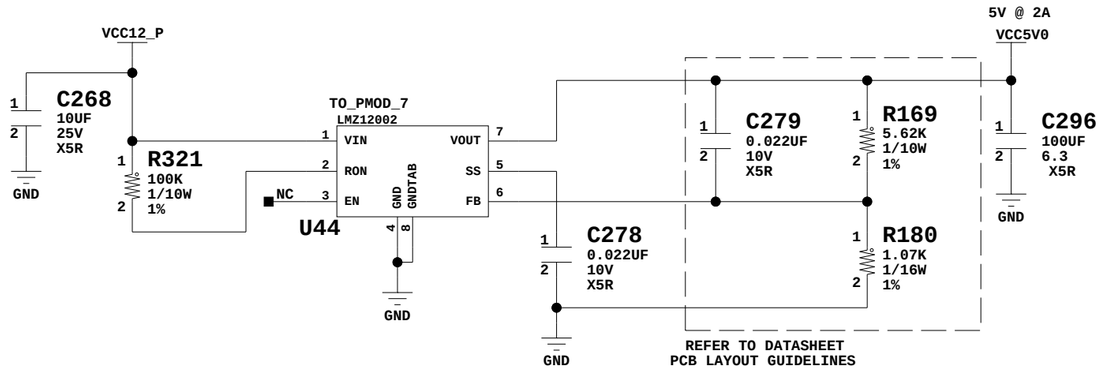

Linear Power Supplies Page 1

XILINX

Title:	Linear Power Supplies Page 1 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
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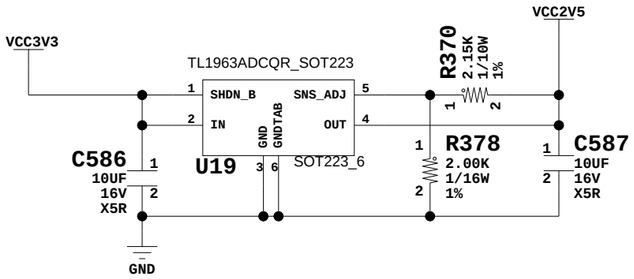
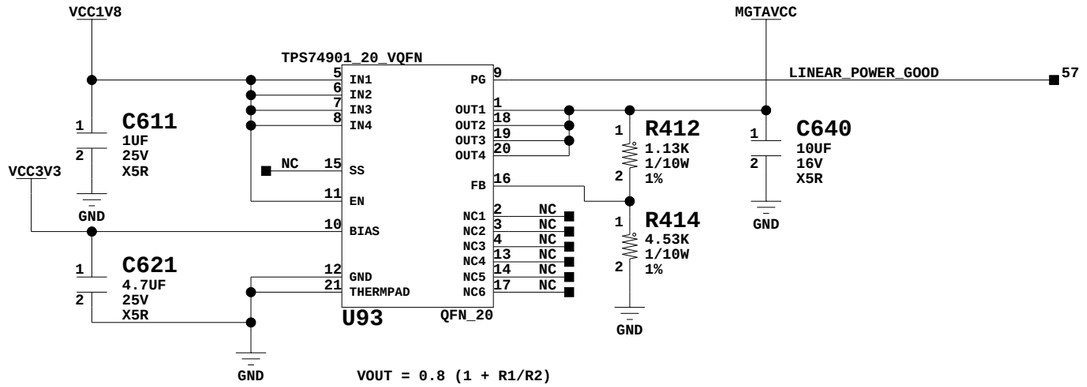
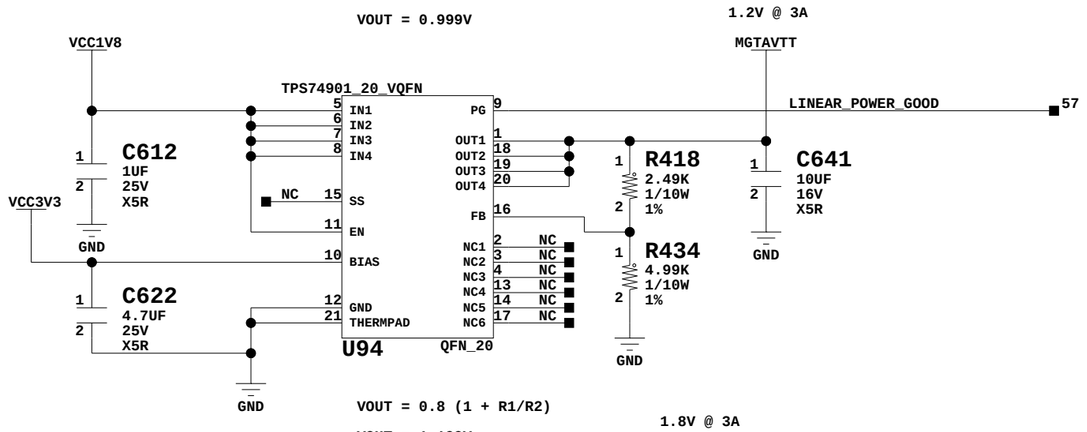
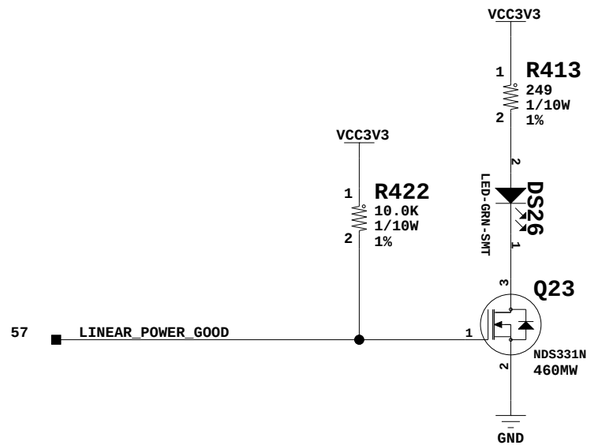
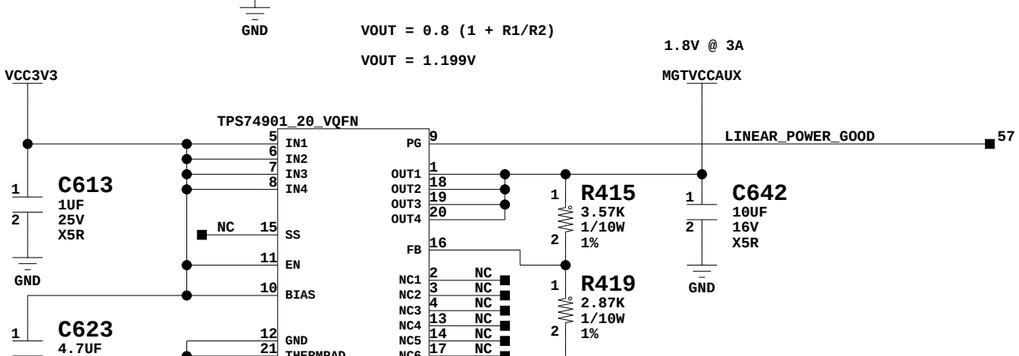
VCC2V5 2.5V 1.5A MAX

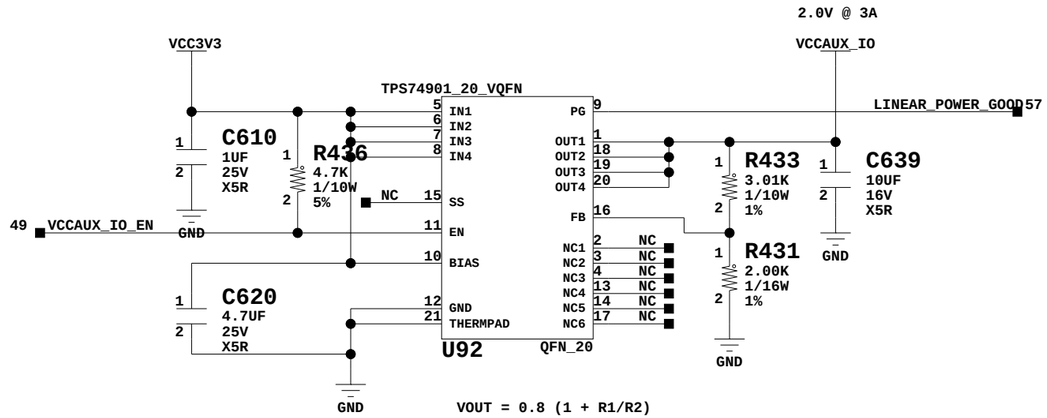












Linear Power Supplies Page 2

Title:	Linear Power Supplies Page 2 ZC706 EVALUATION PLATFORM SCHEM, ROHS COMPLIANT	ASSY P/N:	0431760
		PCB P/N:	1280681
		SCH P/N:	0381513
Date:	2-21-2013_17:14	Ver:	1.2
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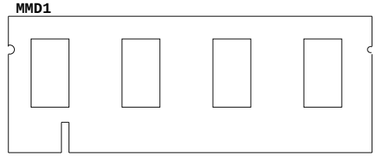
HS1

12V Fan / Heatsink

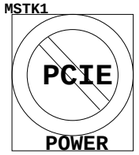
12VDC

MMD1



DDR3_SODIMM

MSTK1



PCIE_POWER_STICKER

CBL3

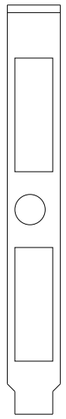
110V Prong

IEC320-C13

PC_POWER_CABLE

Power Cord

PL1



ZC706_PCIE_PLATE

PB1

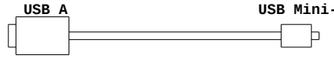
12v Power Brick

PWR_BRICK_12V

CBL1

USB A

USB Mini-B



USB Mini-B Cable

USB_MINIB_CABLE

CBL4

USB A

USB Mini-B

USB Micro-B Cable

USB_MICRO_CABLE

CBL2

4-Pin ATX Power

6-Pin Molex Mini-fit Jr.

PCIe Adapter Cable

PCIE_ADAPTER_CABLE

NOTE: These two standoffs are shorter and must be connected to MH4 and MH5 to level the board properly

MS01

STANDOFF_0P625

MW1

WASHER_FLAT_4

MRB1

RUBBER_BUMPER

MS1

MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MS12

MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MH_125_250

MH1

GND

MS2

MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MH_125_250

MH2

GND

NOTE: No standoff foot on MH2

MS03

STANDOFF_0P625

MW3

WASHER_FLAT_4

MRB3

RUBBER_BUMPER

MS3

MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MS14

MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MH_125_250

MH3

GND

MS04

STANDOFF_0P500

MW4

WASHER_FLAT_4

MRB4

RUBBER_BUMPER

MS4

MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MS15

MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MH_125_250

MH4

GND

MS05

STANDOFF_0P500

MW5

WASHER_FLAT_4

MRB5

RUBBER_BUMPER

MS5

MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MS16

MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MH_125_250

MH5

GND

MS06

STANDOFF_0P625

MW6

WASHER_FLAT_4

MRB6

RUBBER_BUMPER

MS6

MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MS17

MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MH_125_250

MH6

GND

MJB1 MJB2 MJB3 MJB4 MJB5 MJB6 MJB7 MJB8

JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN

MJB9 MJB10 MJB11 MJB12 MJB13 MJB14 MJB15 MJB16

JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN

MJB17 MJB18 MJB19 MJB20 MJB21 MJB22

JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN

Mechanical Components

XILINX

Title:	Mechanical Components SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431760 1280681 0381513
Date:	2-21-2013_17:14	Ver:	1.2
Sheet Size: B		Rev:	03
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