

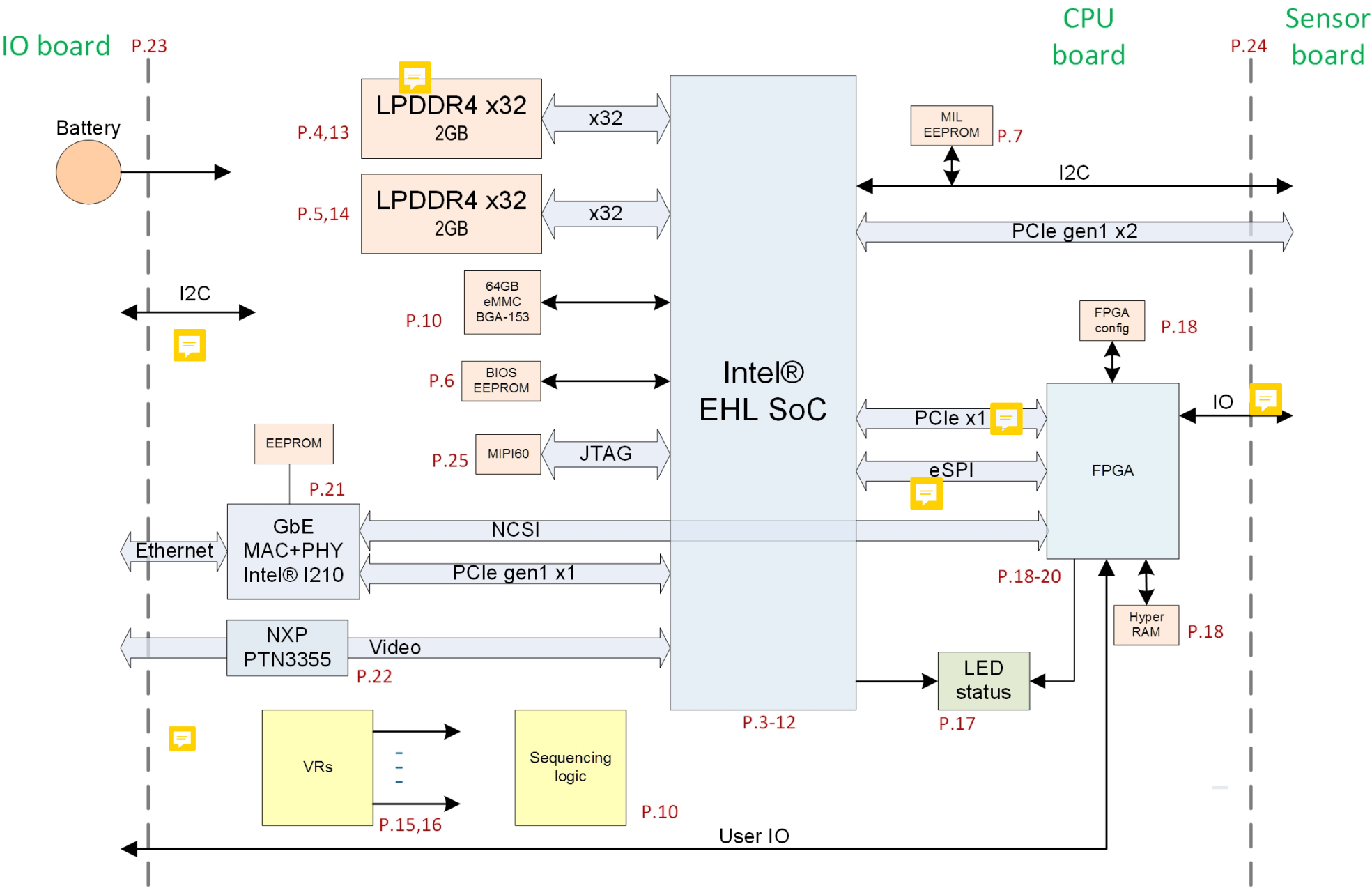
IRIS4 CPU Board


REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

MATROX CONFIDENTIAL

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DRAWN Dmitri Golovanov		 MATROX 1055 BOUL. ST-REGIS DORVAL, QUEBEC H9P 2T4	
PROJECT IRIS4			
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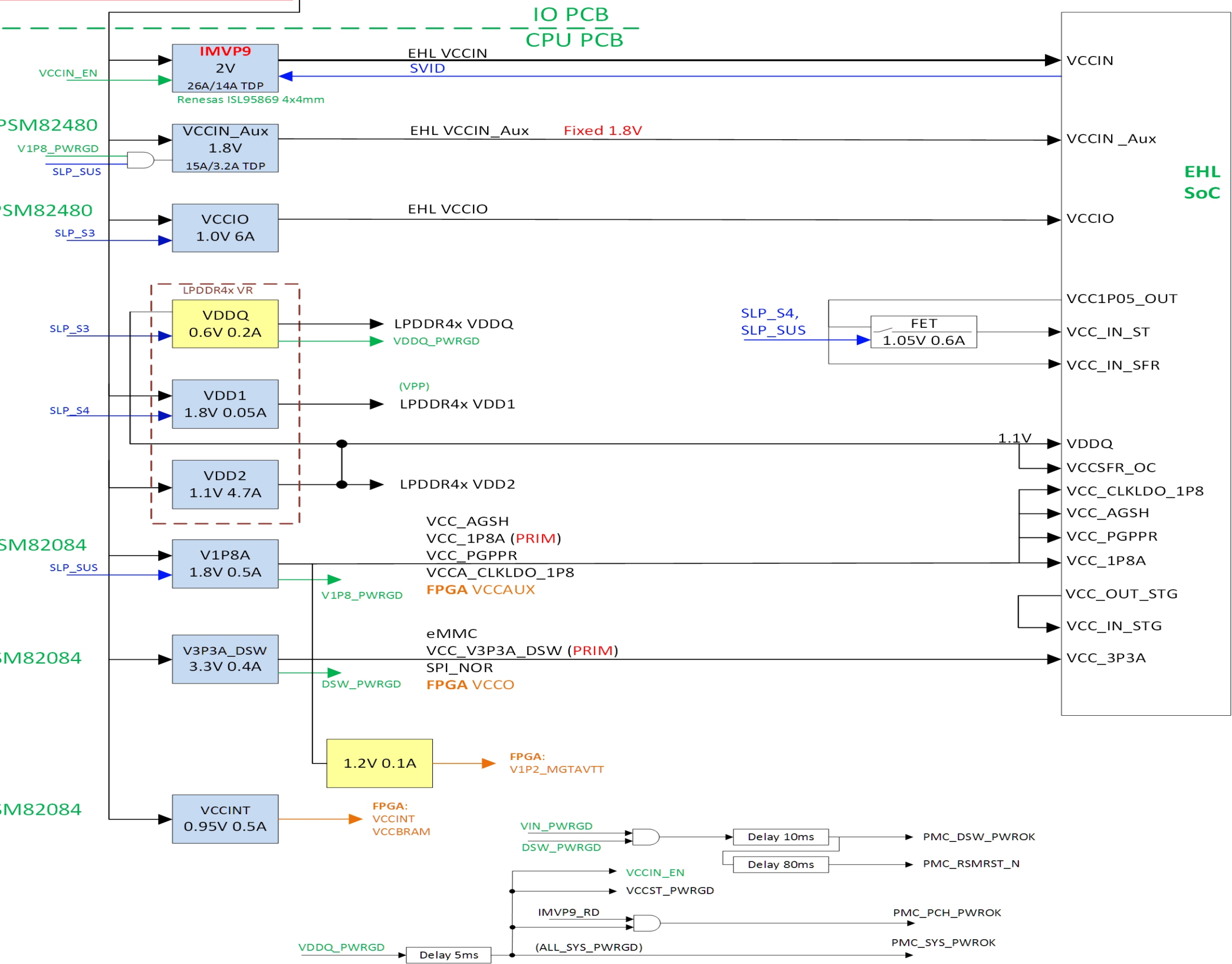
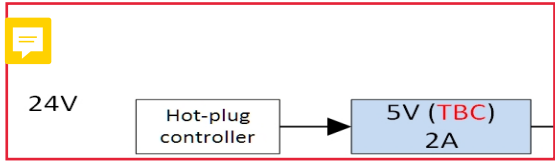
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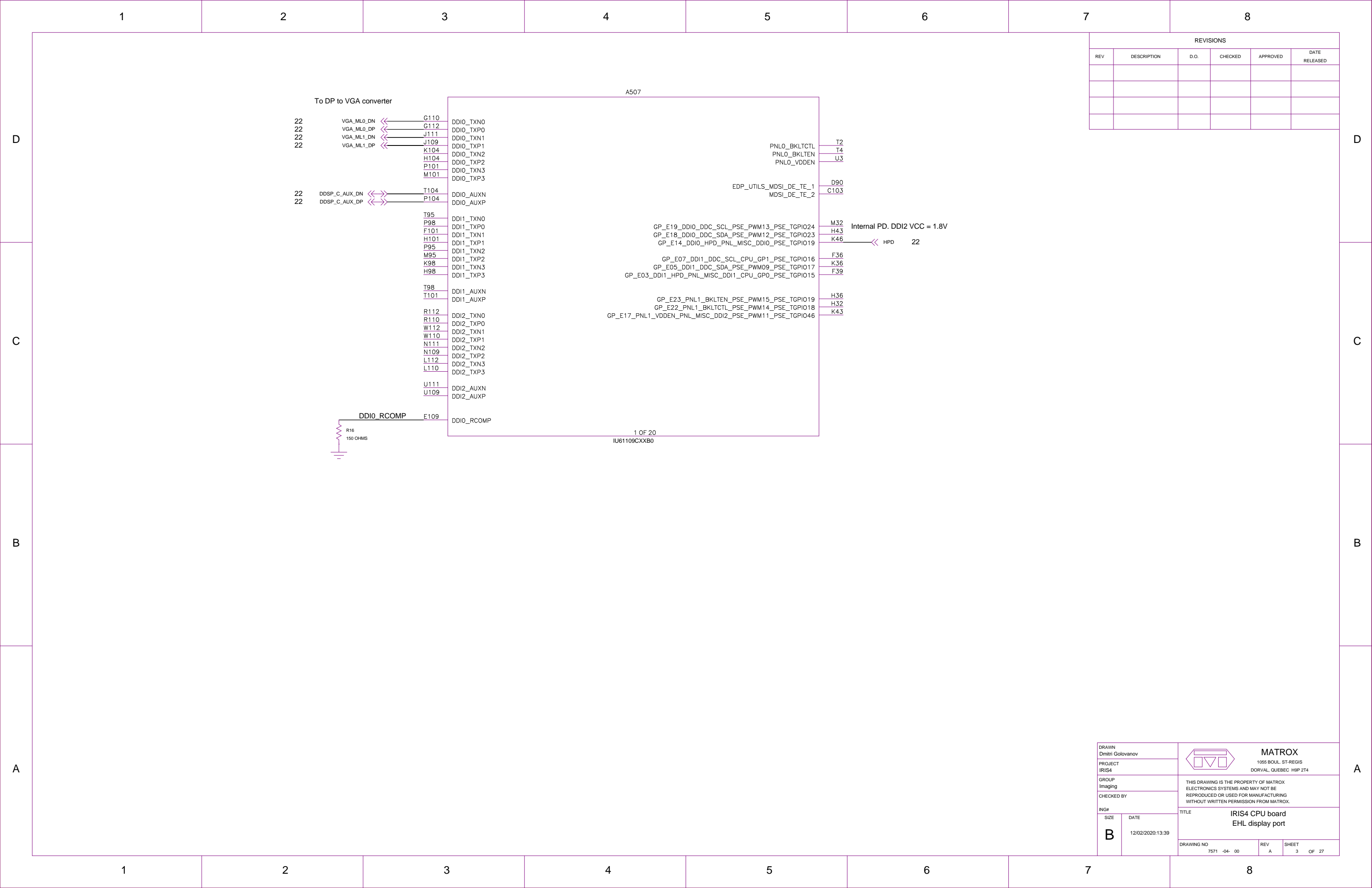
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Power Distribution**

DRAWING NO
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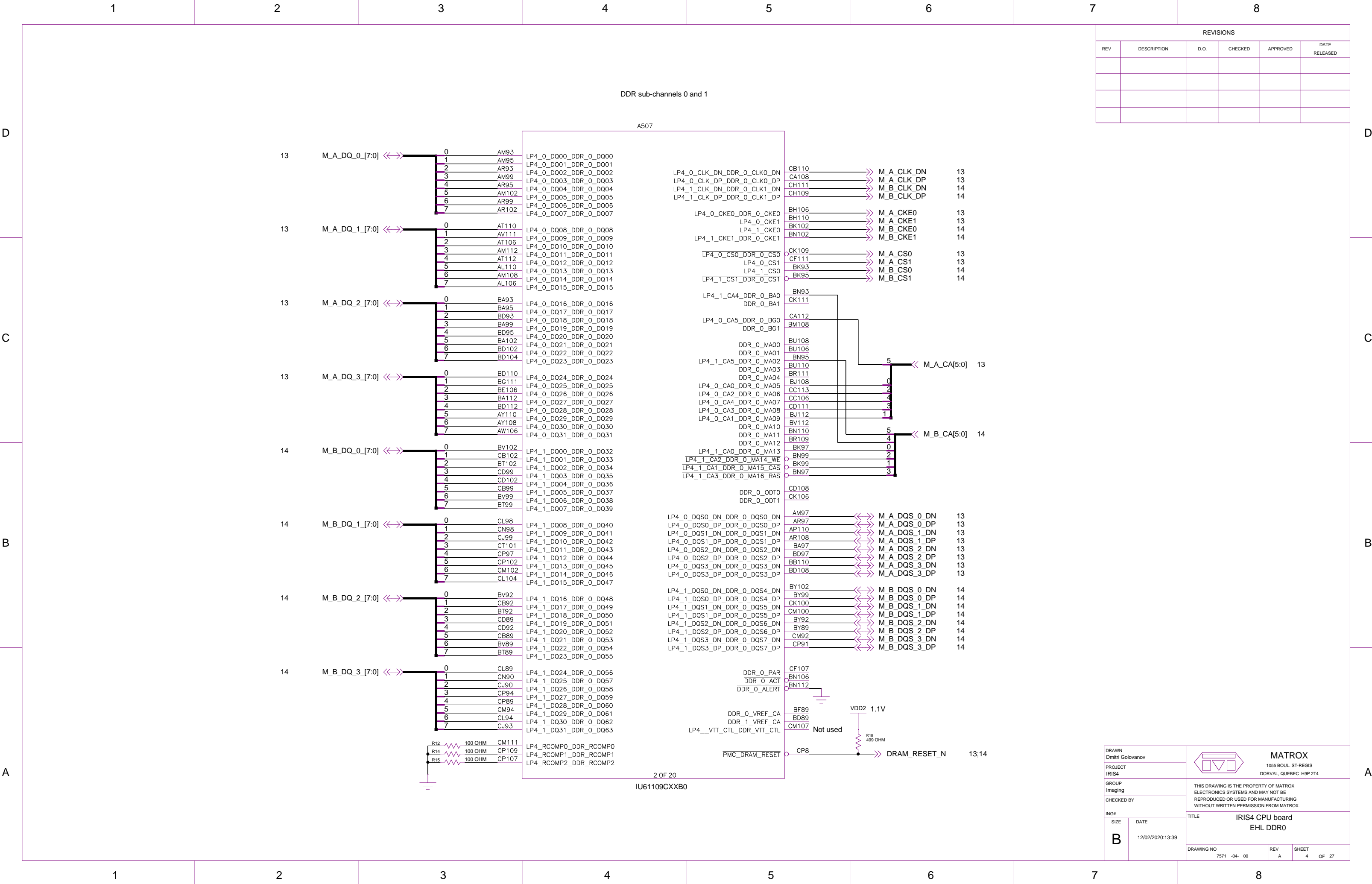
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DRAWN
Dmitri Golovanov

PROJECT
IRIS4


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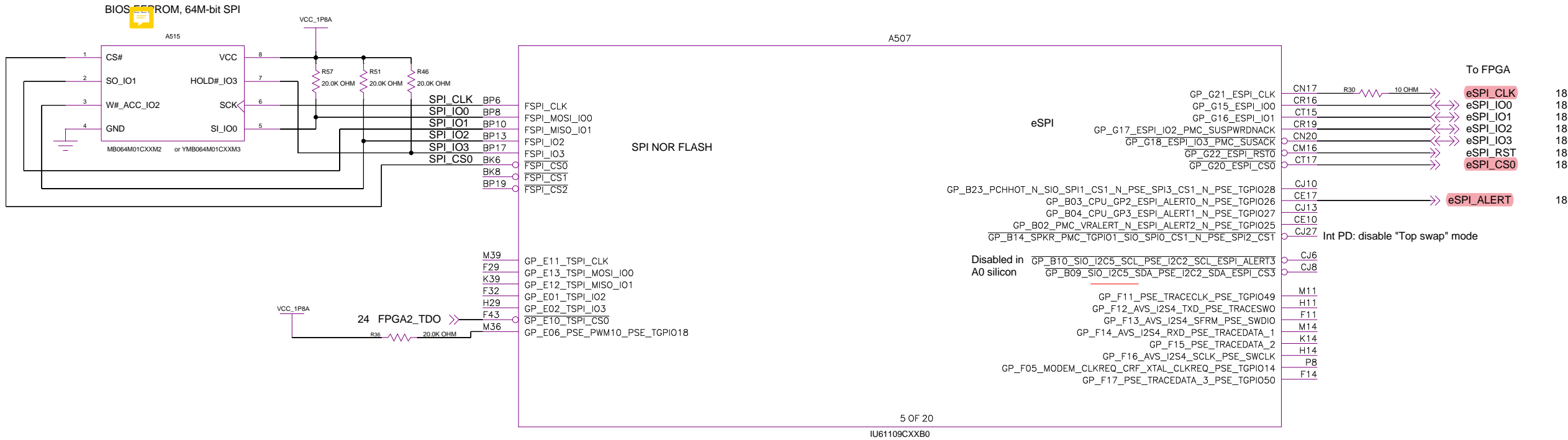
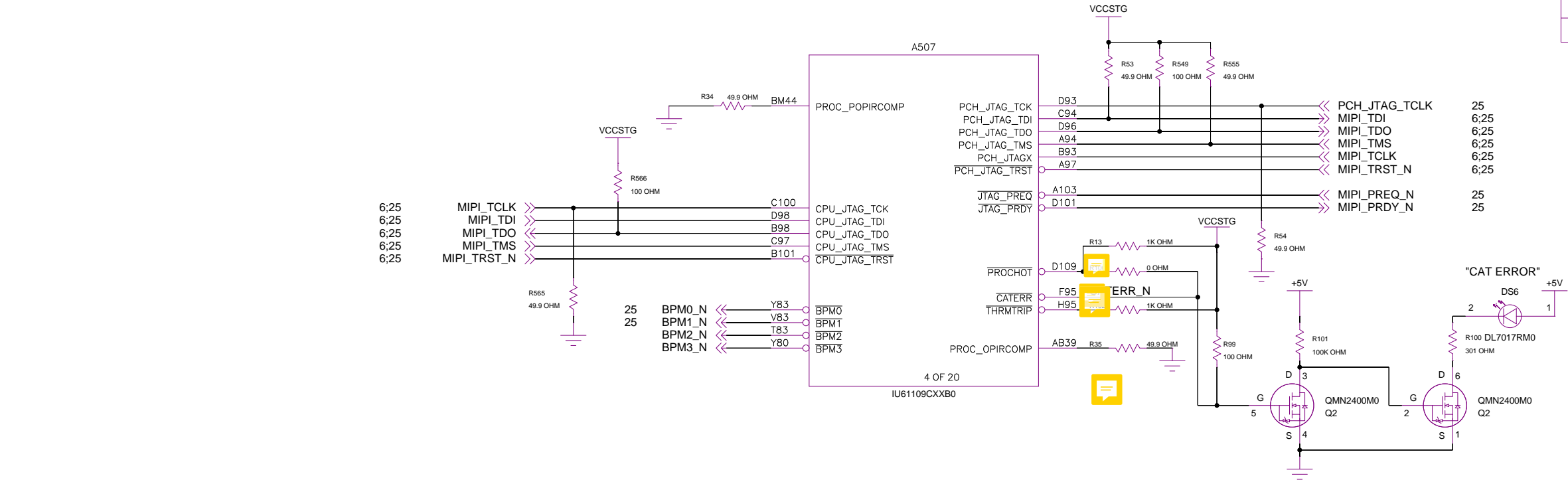
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EHL DDR0**


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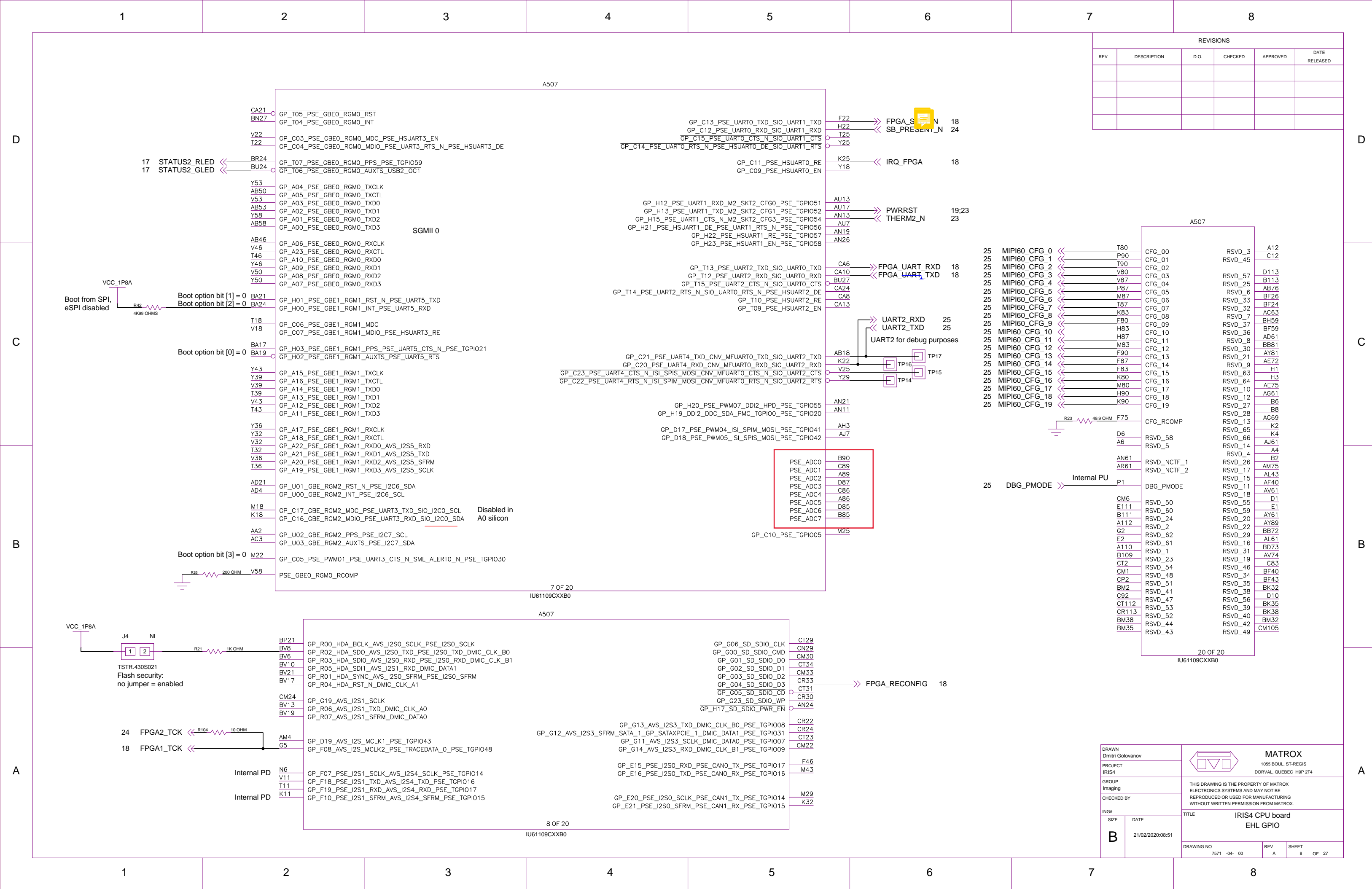
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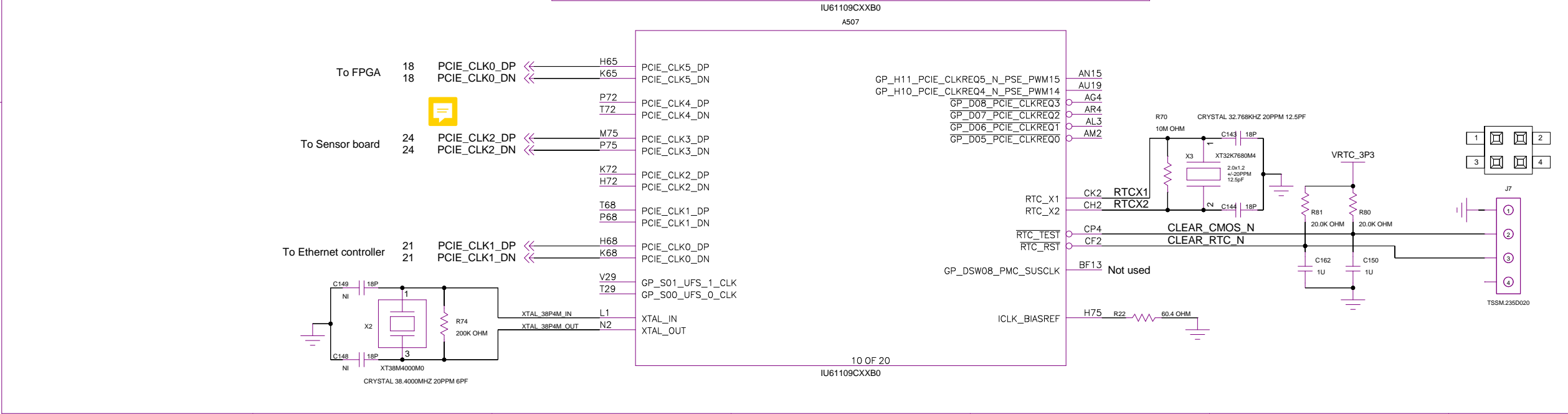
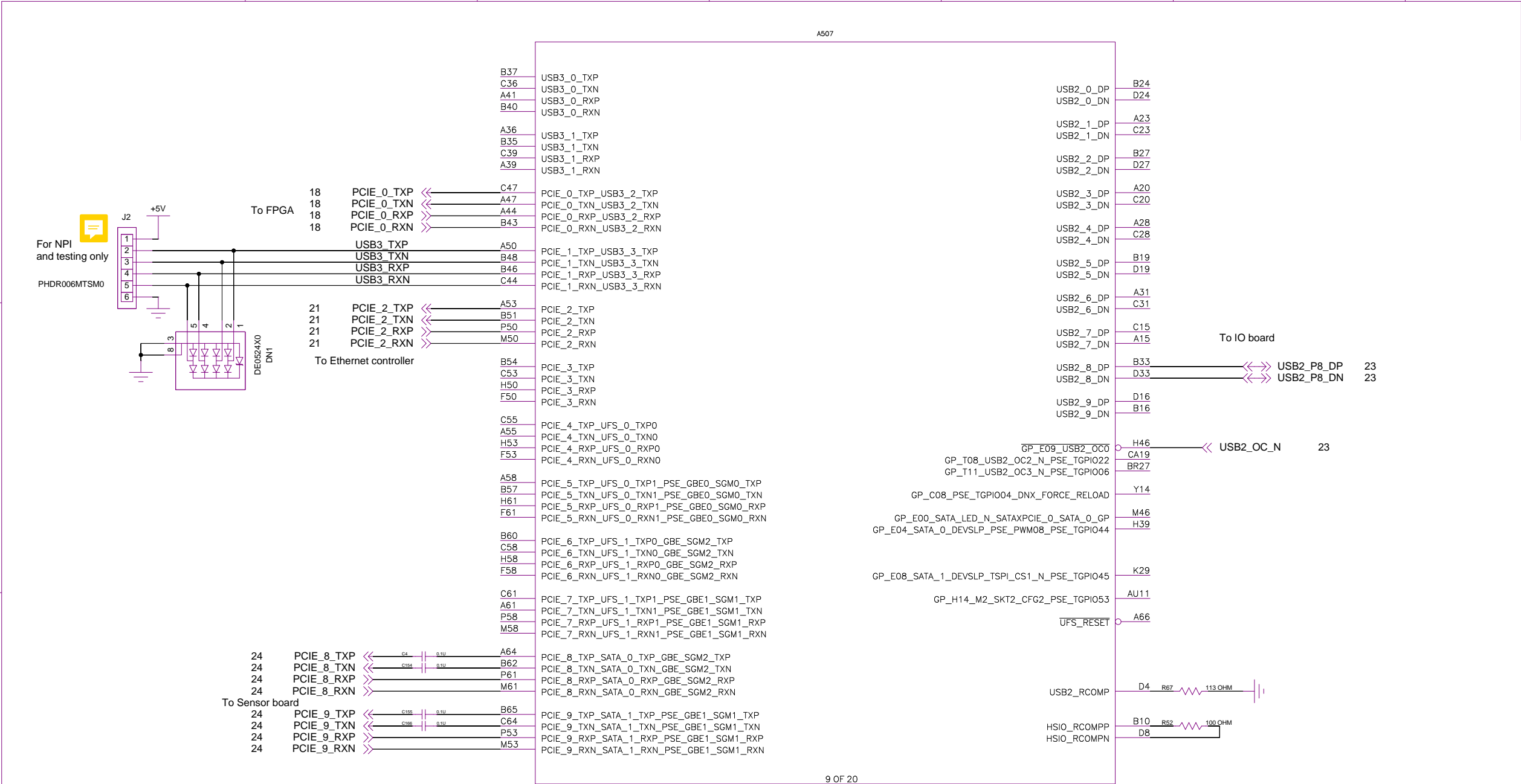
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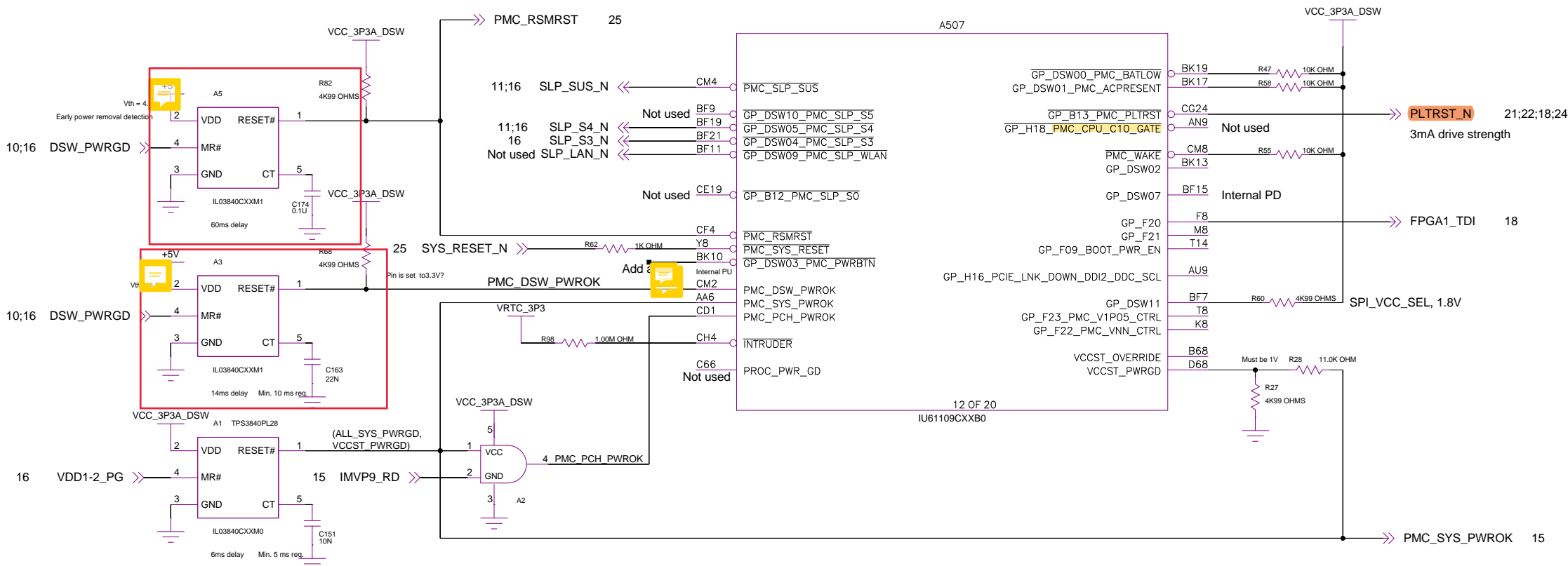
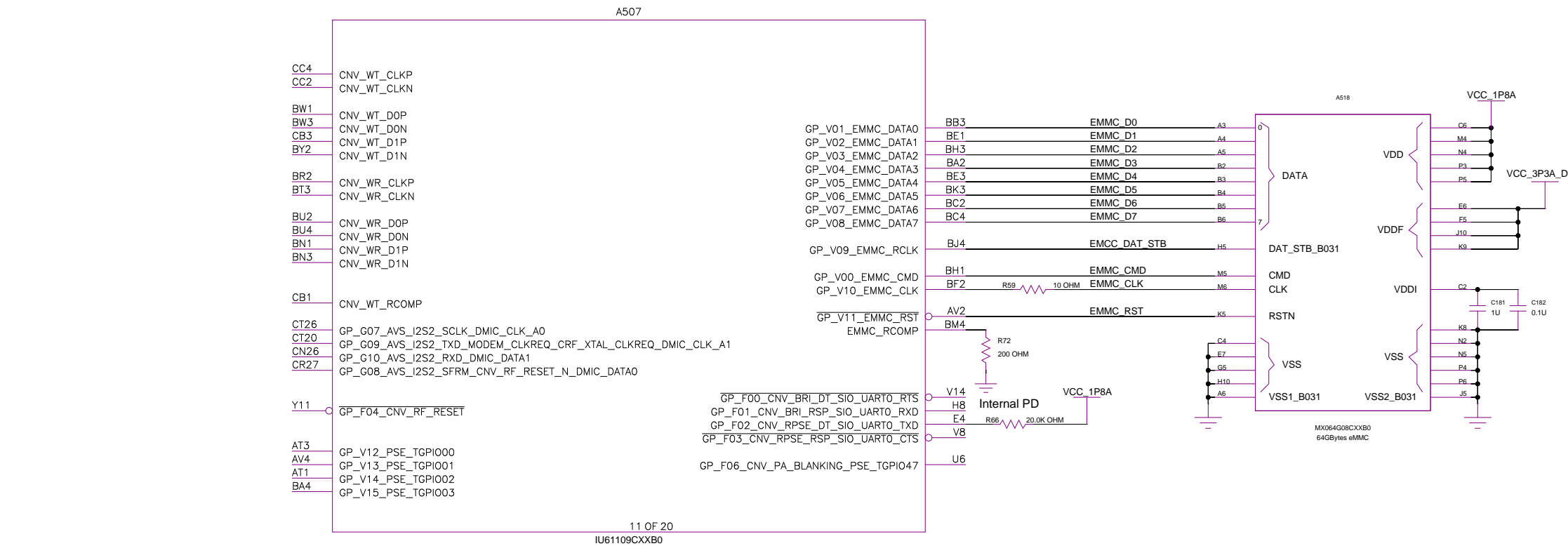



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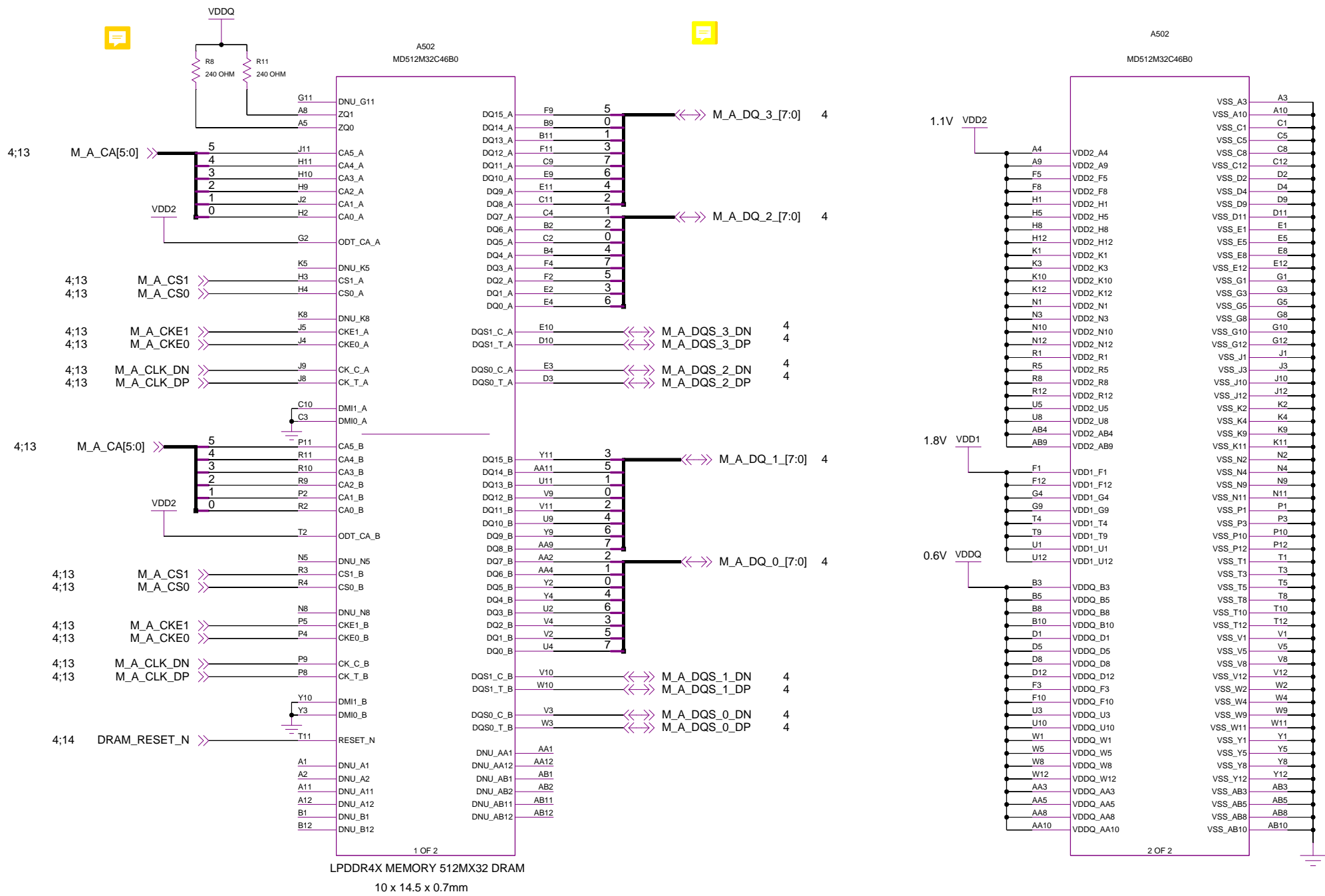
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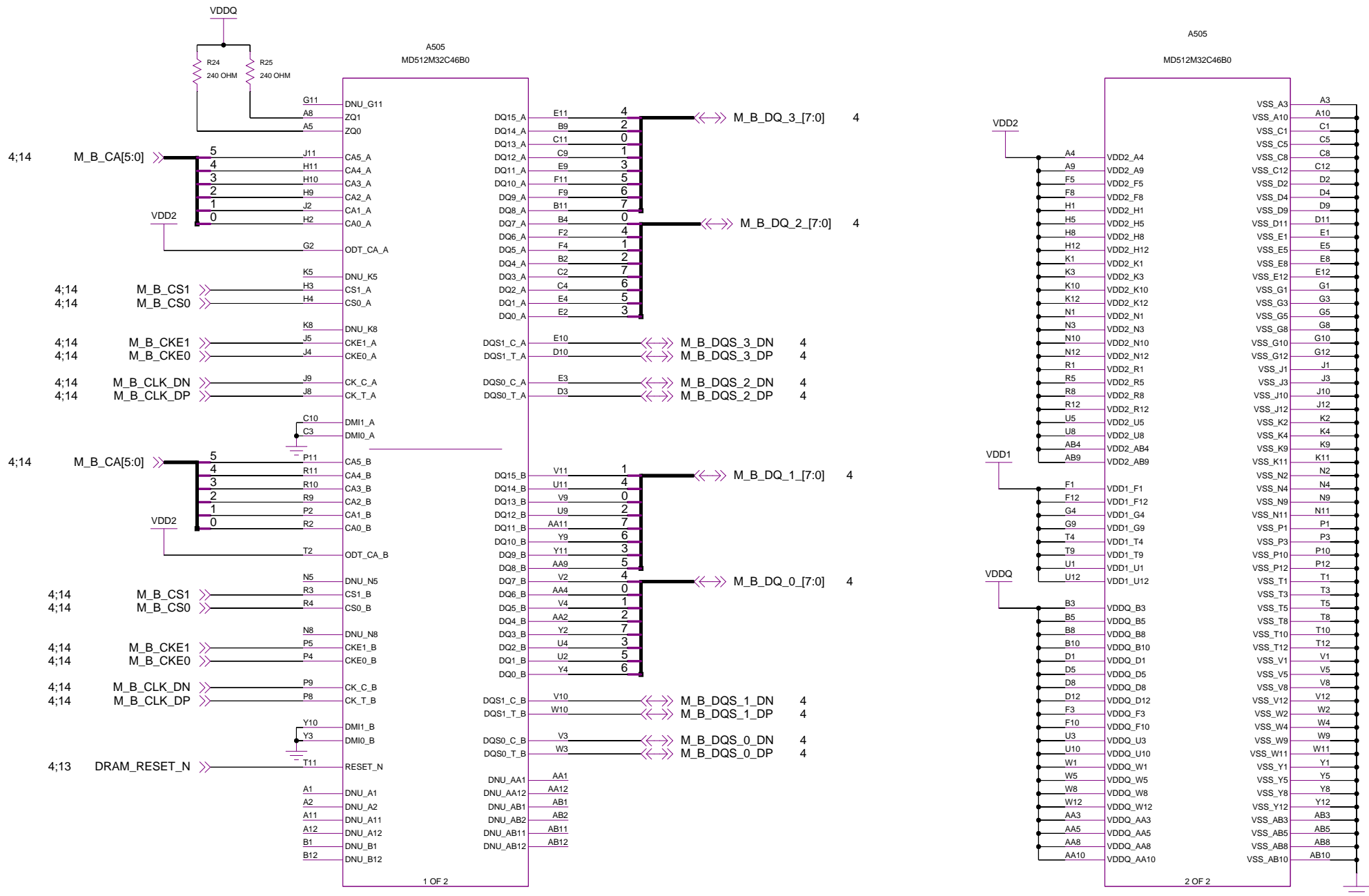
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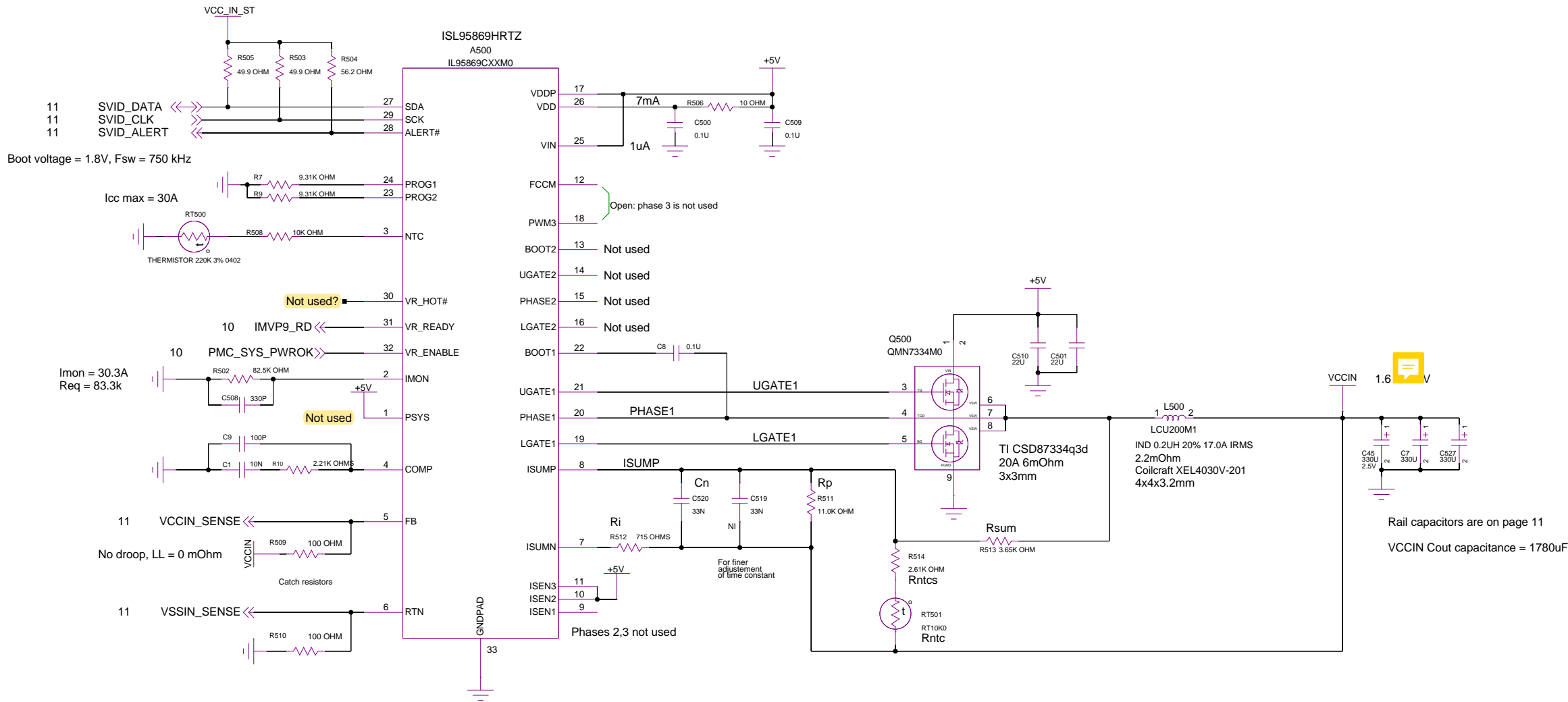
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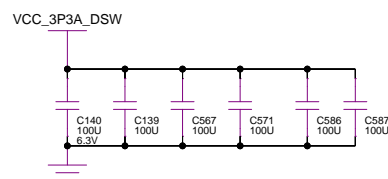
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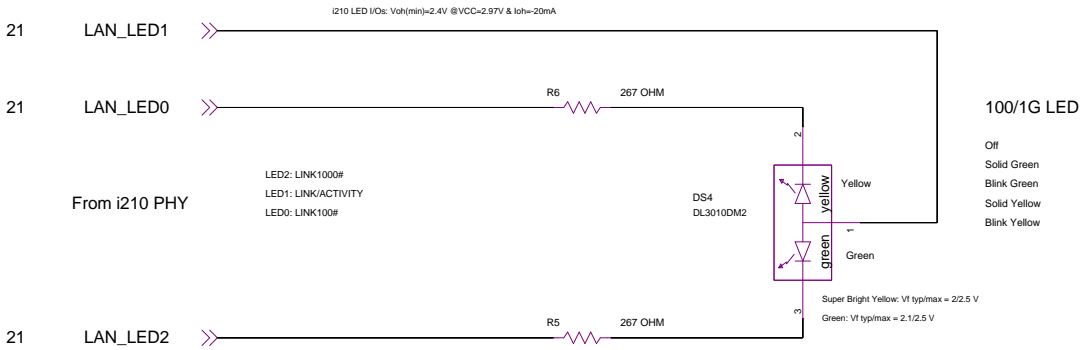
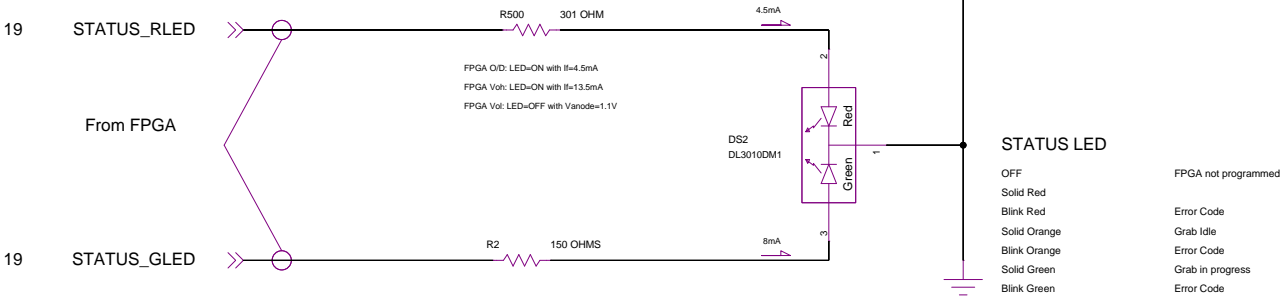
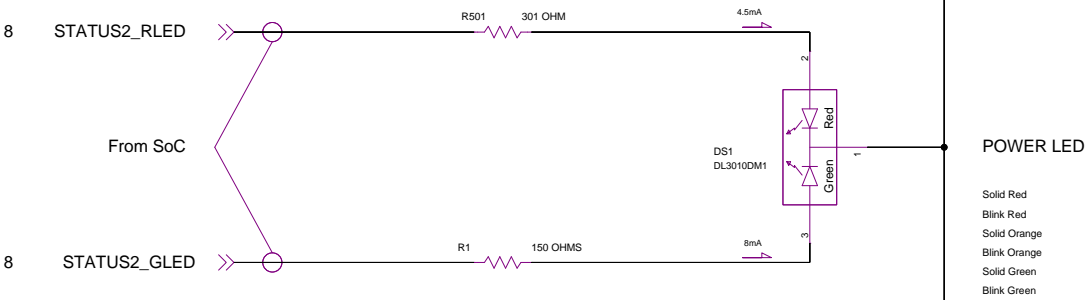
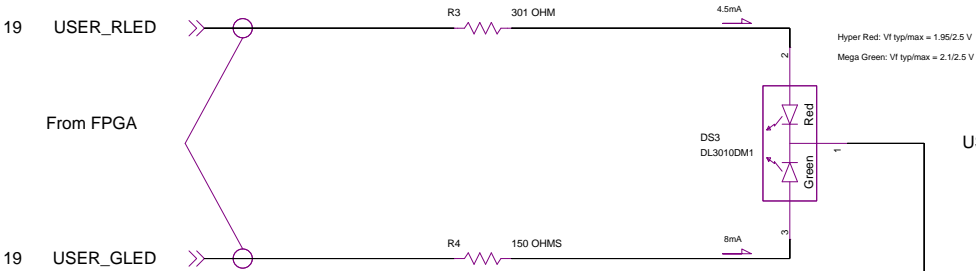
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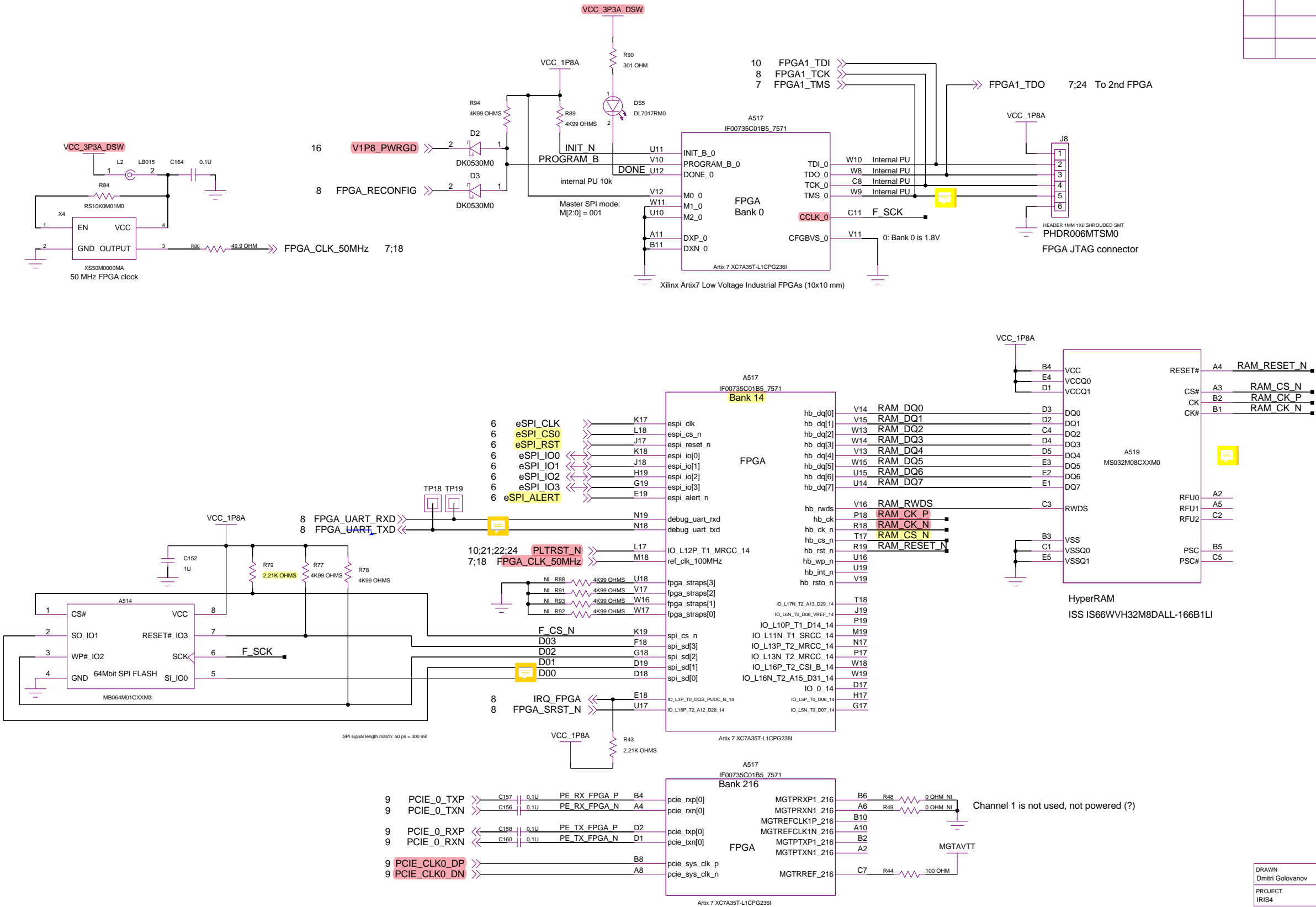
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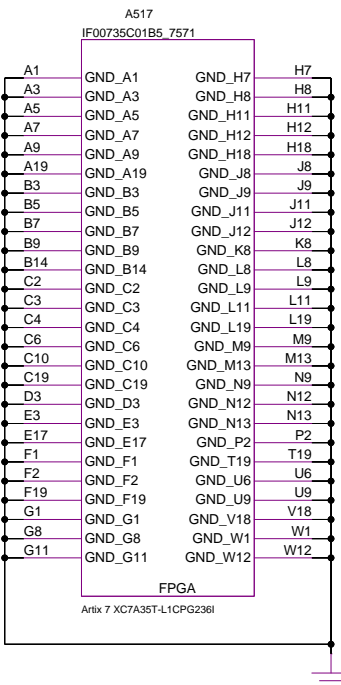
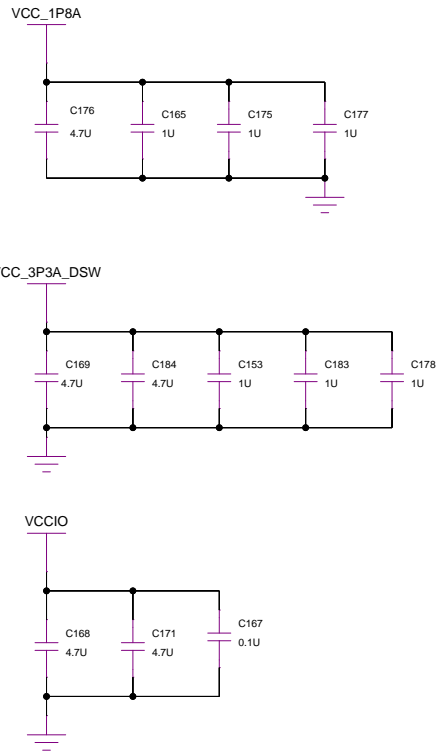
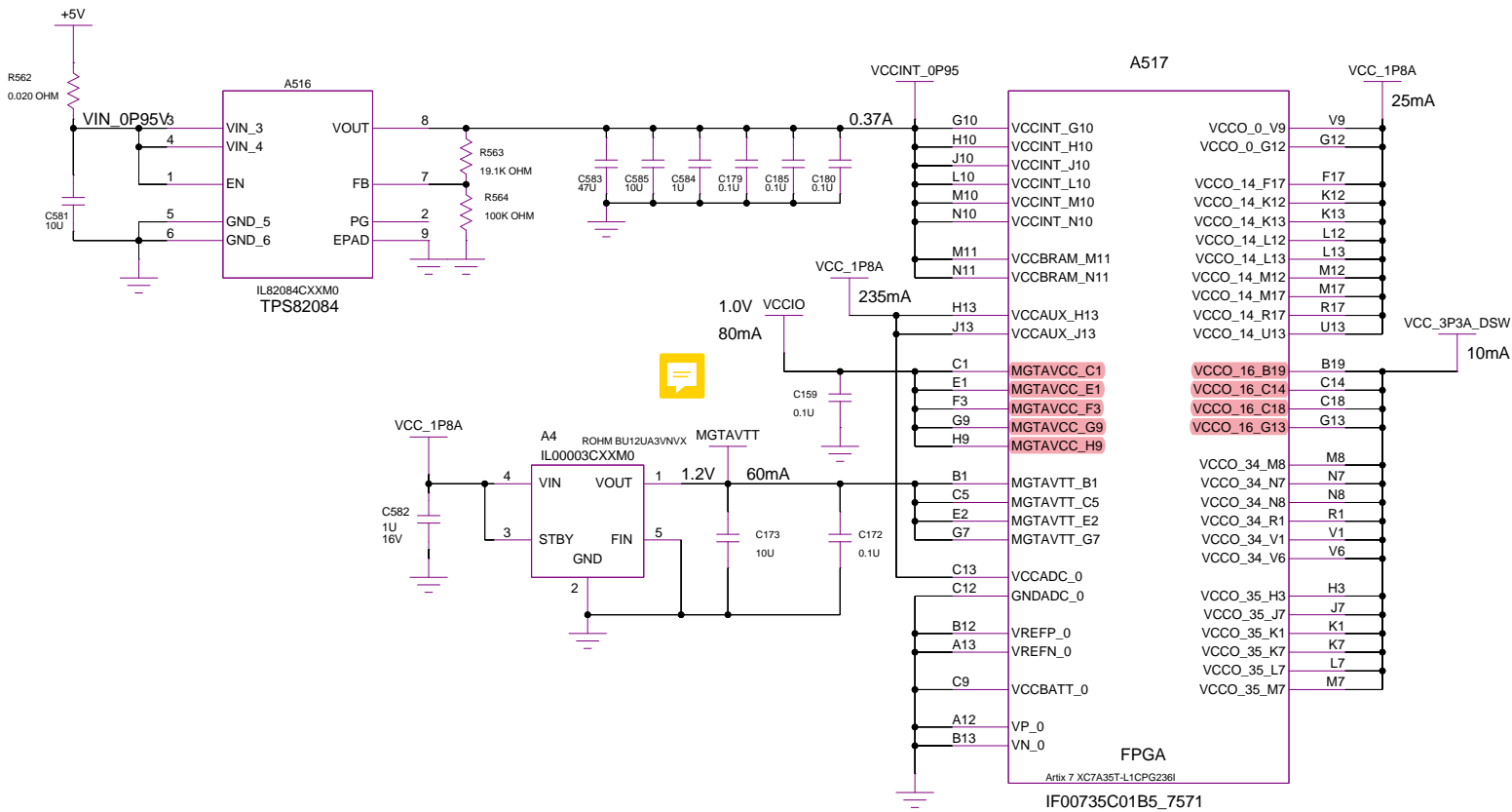
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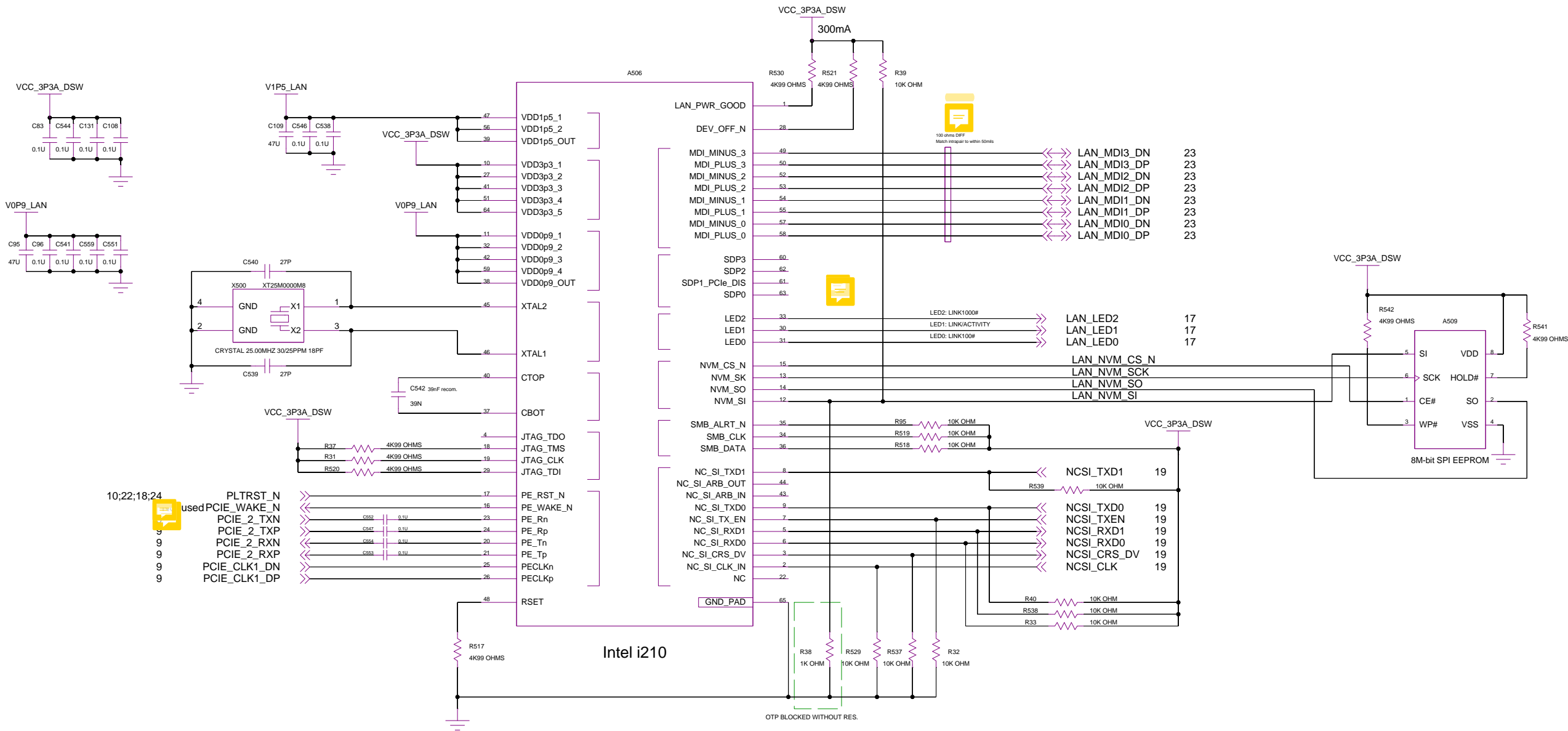
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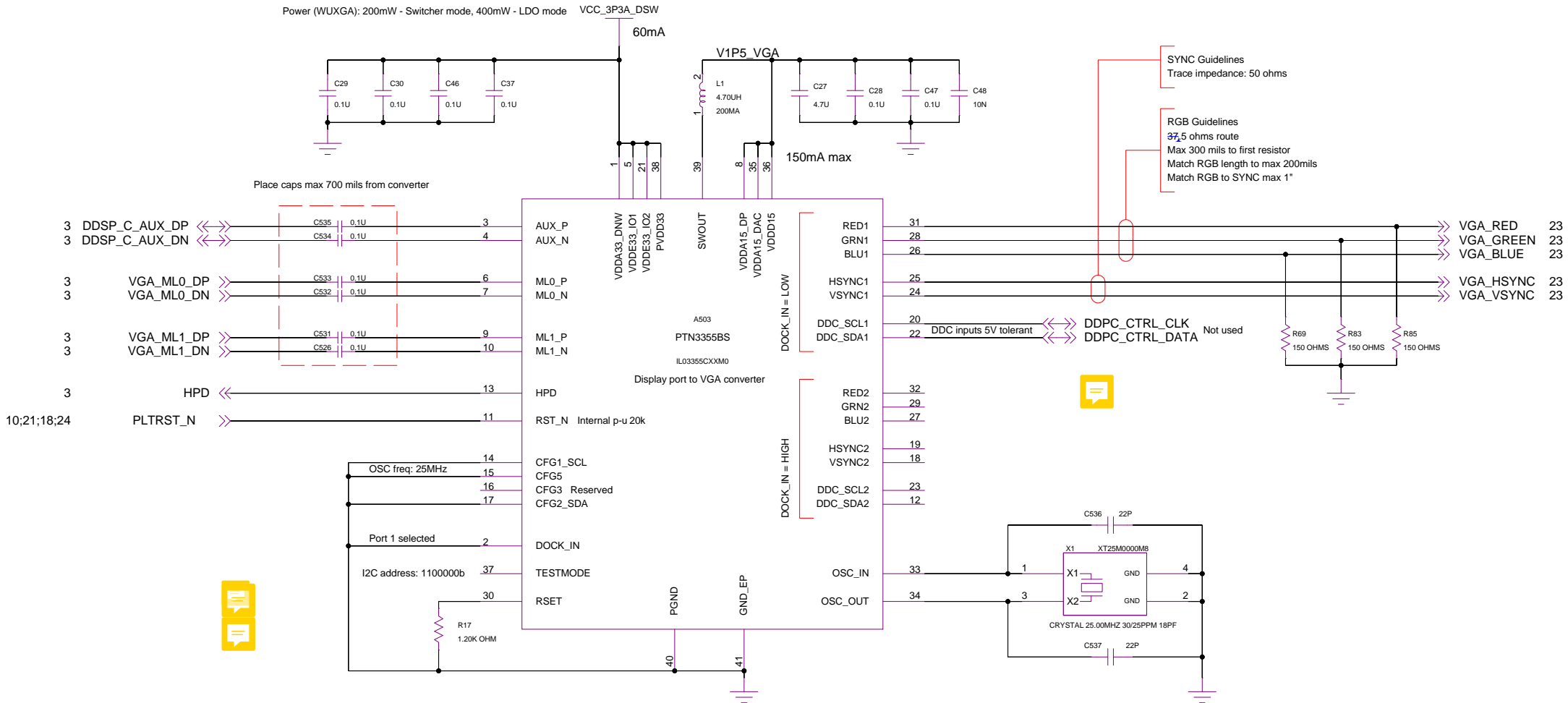
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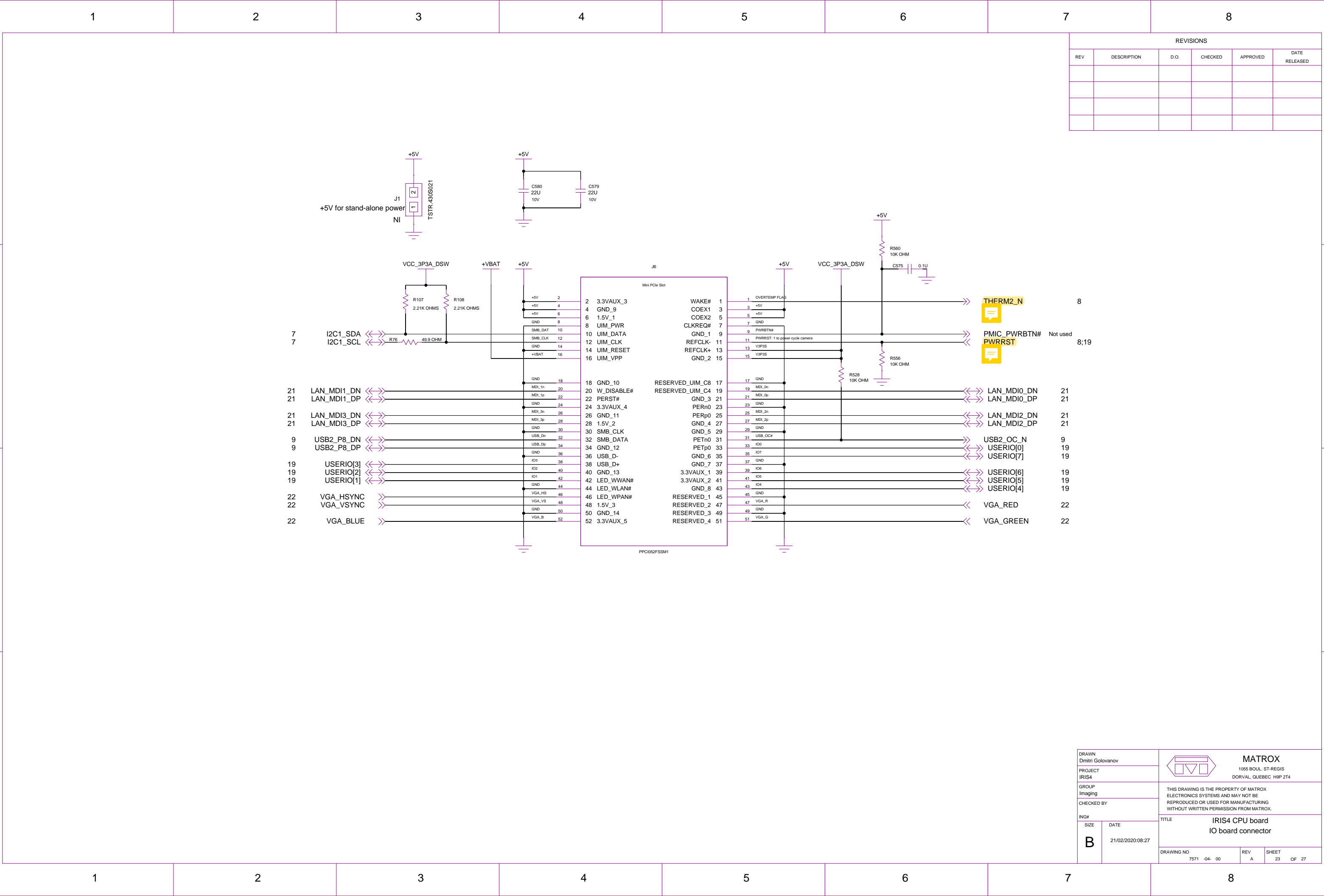
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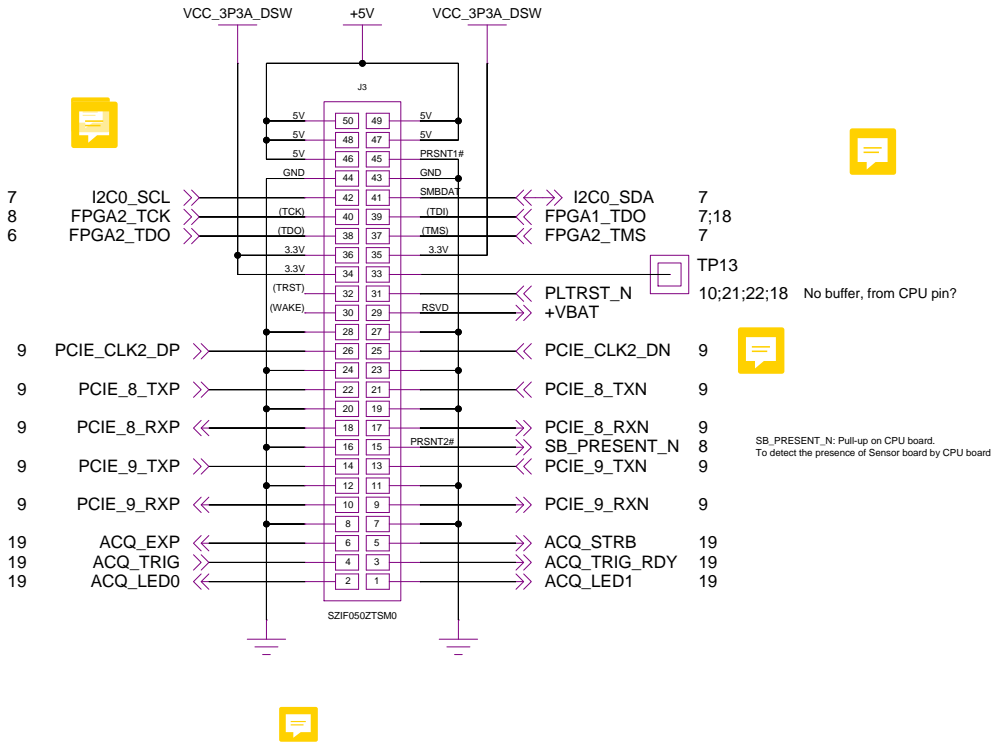
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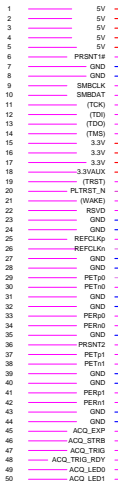
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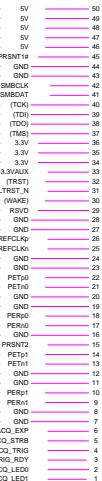
CPU Board ZIF pinout is inverted
Sensor board pos 1 aligned with CPU board pos 50
Connectors are head-to-head with latch on same side




Sensor board connector



CPU board connector



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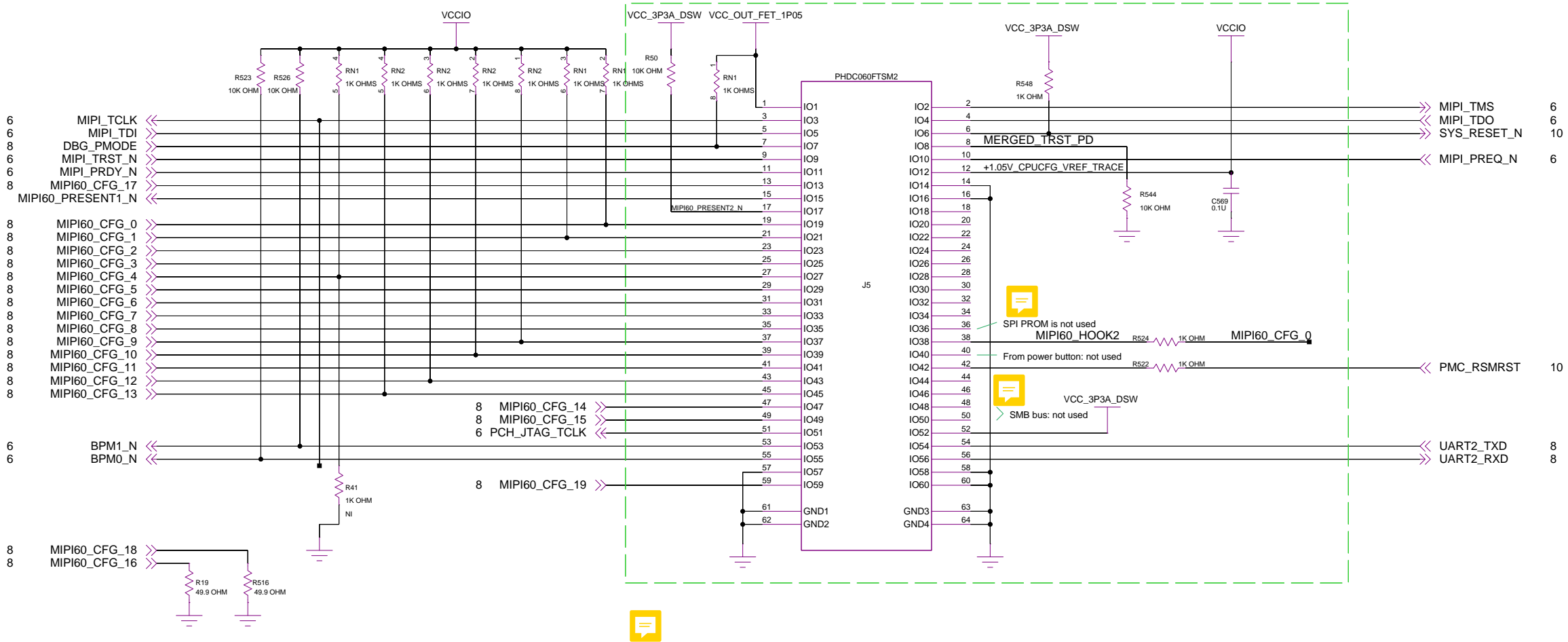
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The MIPI 60 debug connector could be implemented on a break-away extension of the PCB, on prototype version only.
In this case, all components inside this outline will be disconnected from EHL SoC pins on production revision



SUB=XDP

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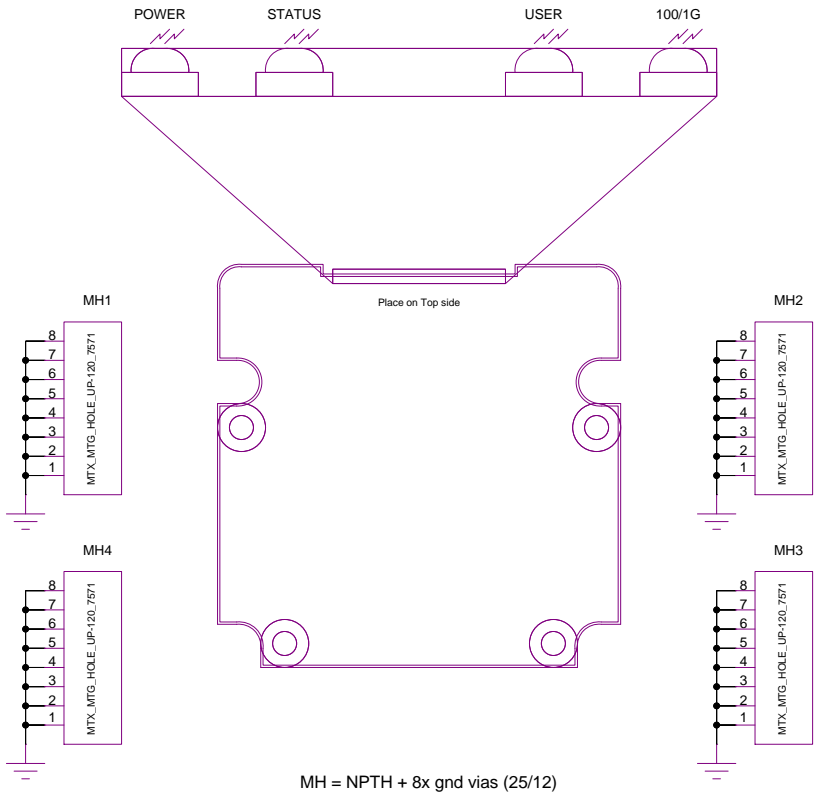
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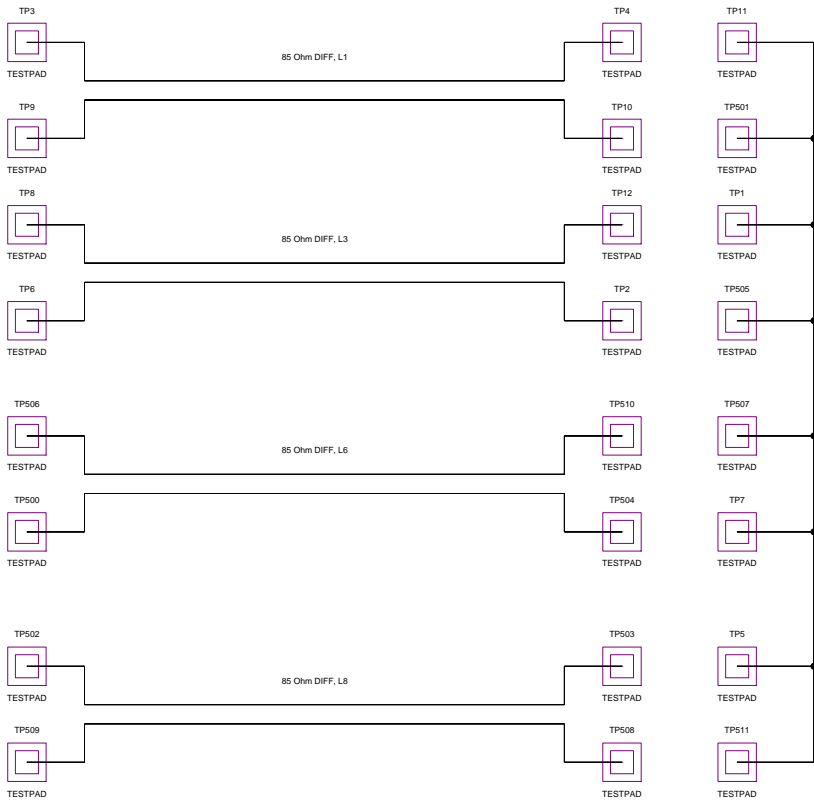
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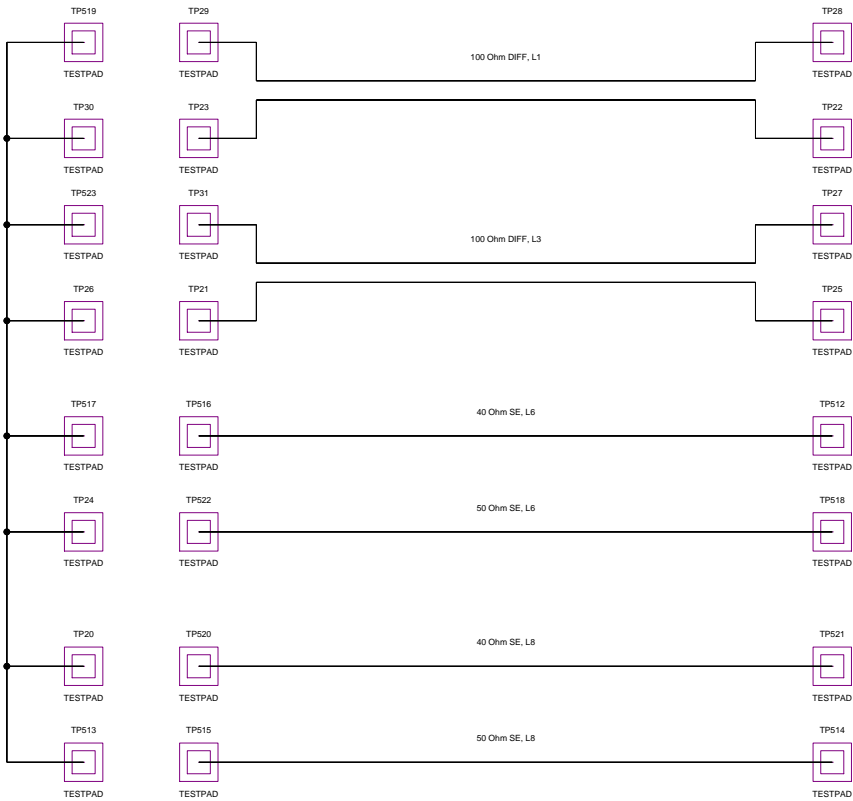
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Test coupons on panel upper cracker section
Route straight on full cracker length



Test coupons on panel lower cracker section
Route straight on full cracker length



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