

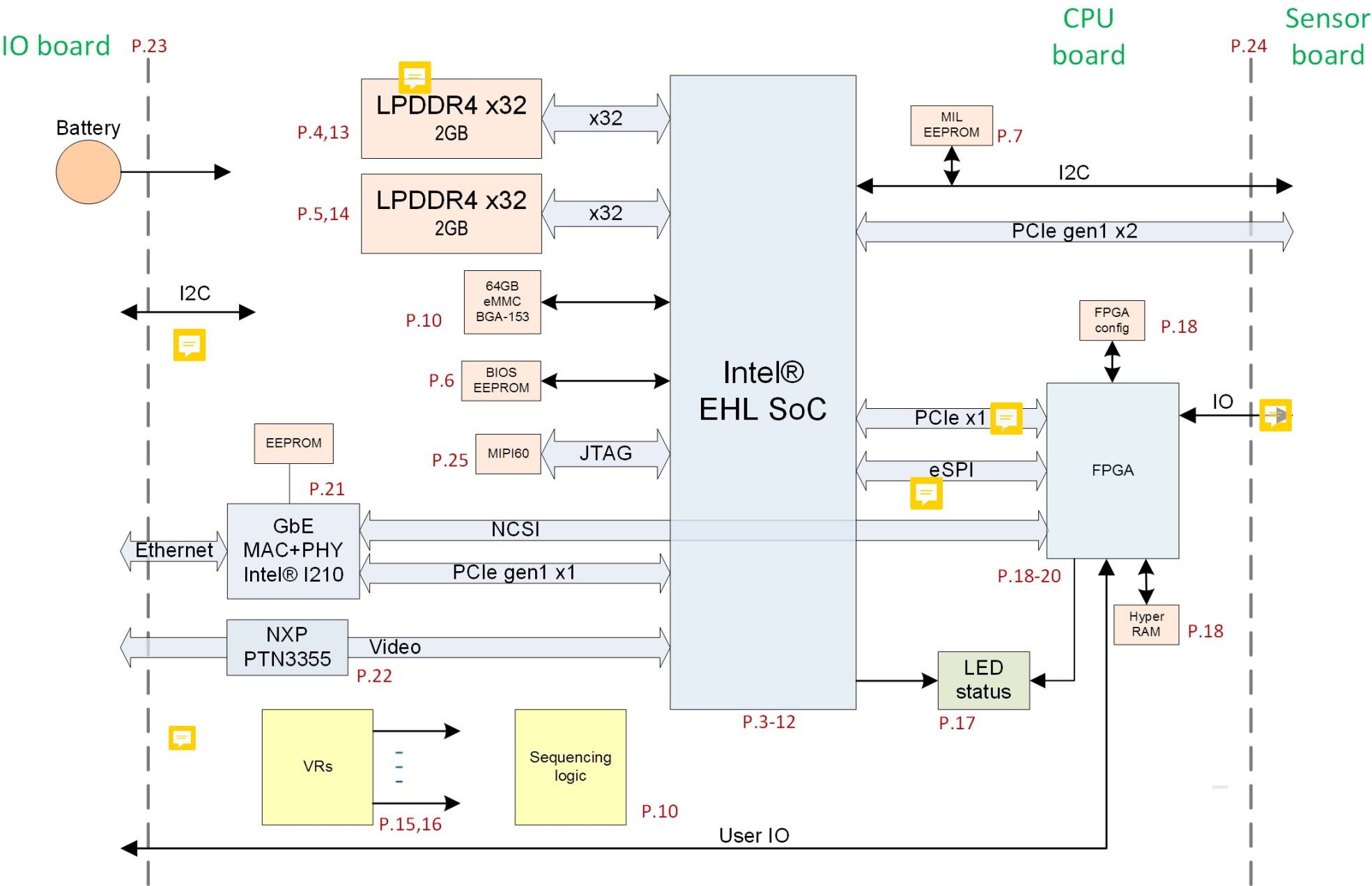
IRIS4 CPU Board


REVISIONS					
REV	DESCRIPTION	D.O.	CHECKED	APPROVED	DATE RELEASED

MATROX CONFIDENTIAL

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ING#		DRAWING NO	
SIZE B	DATE 21/01/2020:07:53	7571 -04- 00	REV A
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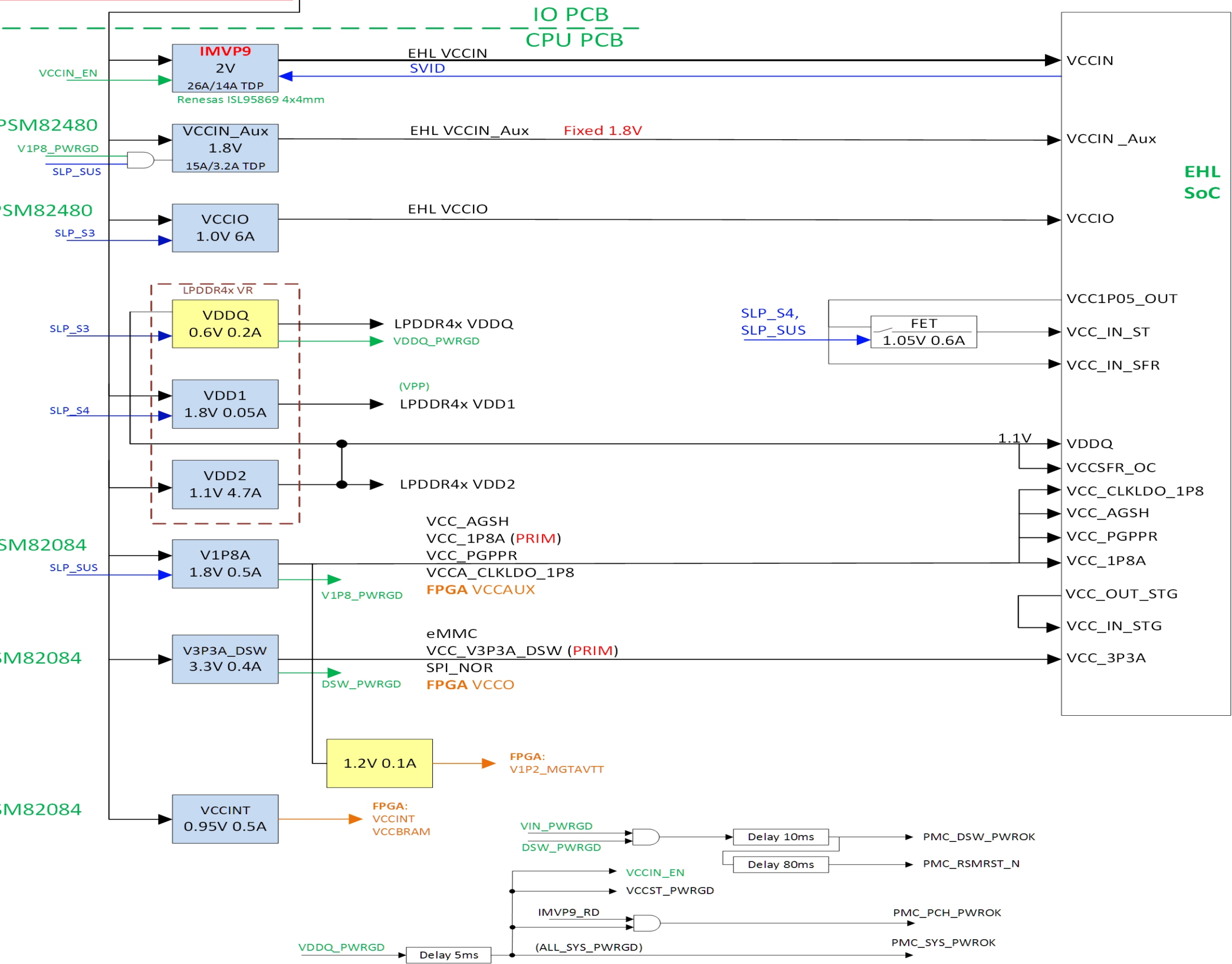
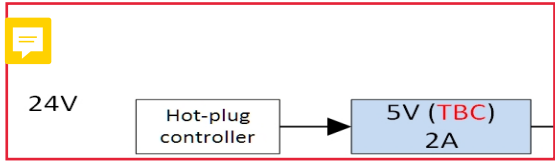
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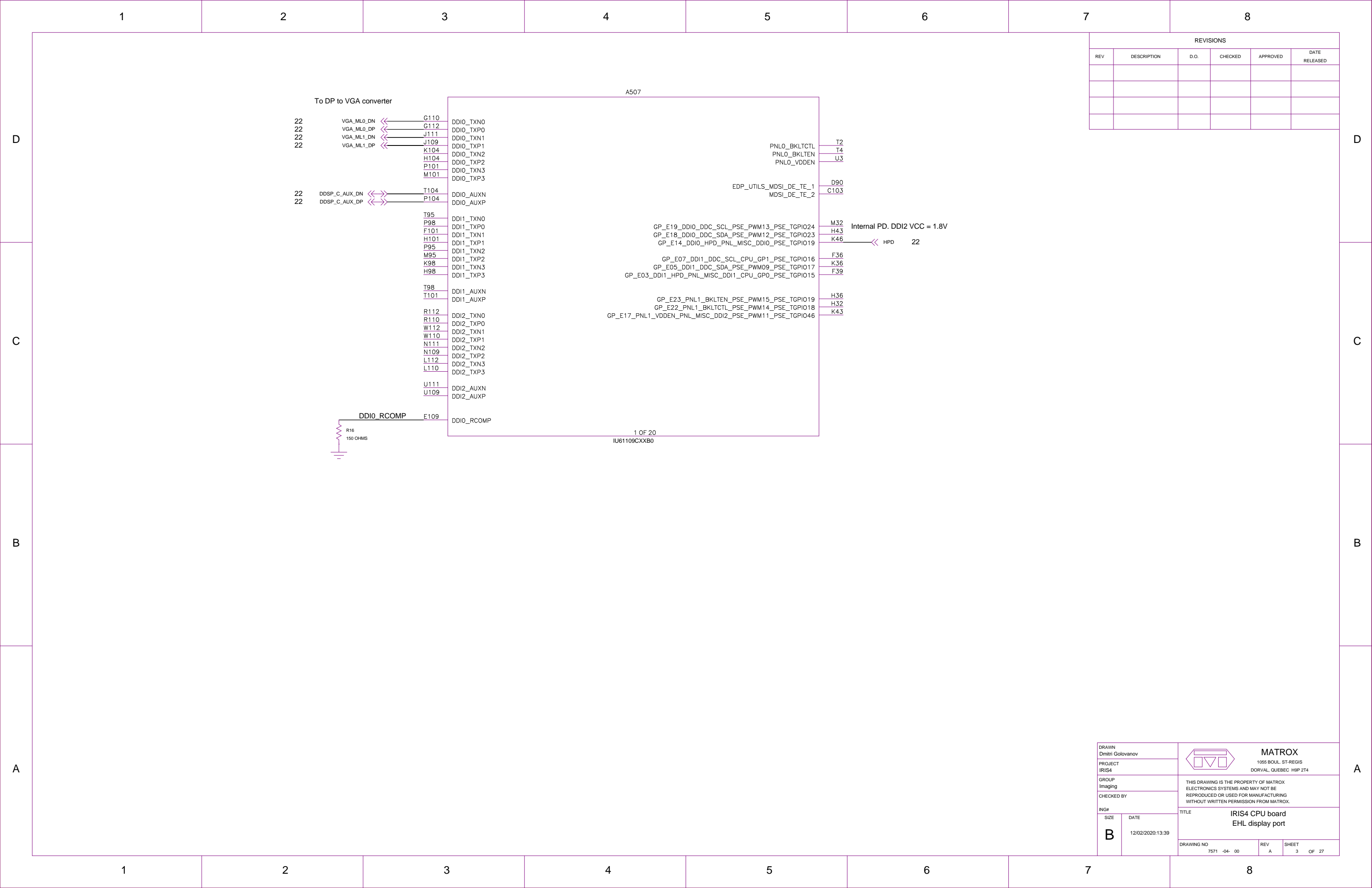
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SIZE B	DATE 17/01/2020:15:45	REV A	SHEET 2 OF 27



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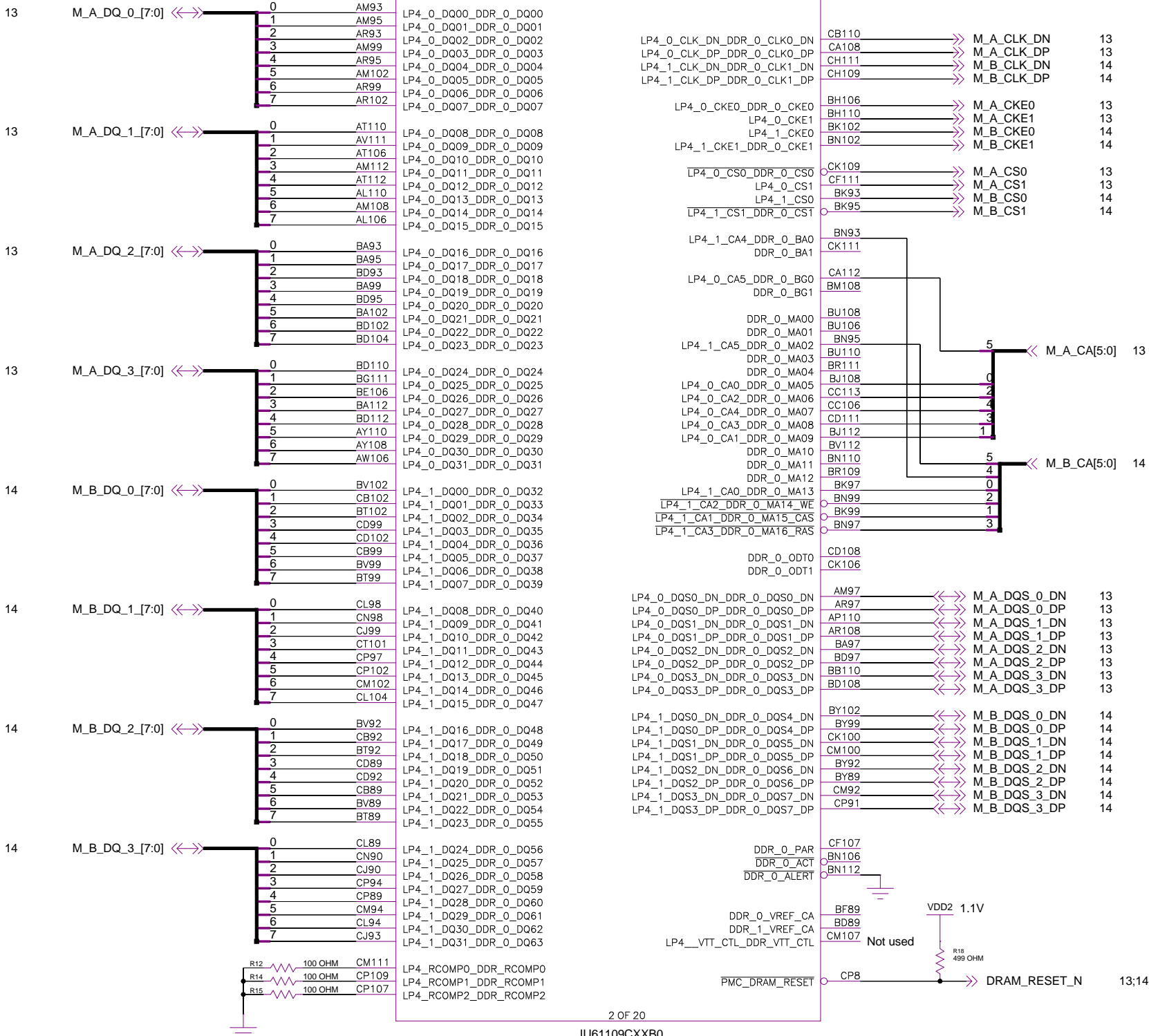
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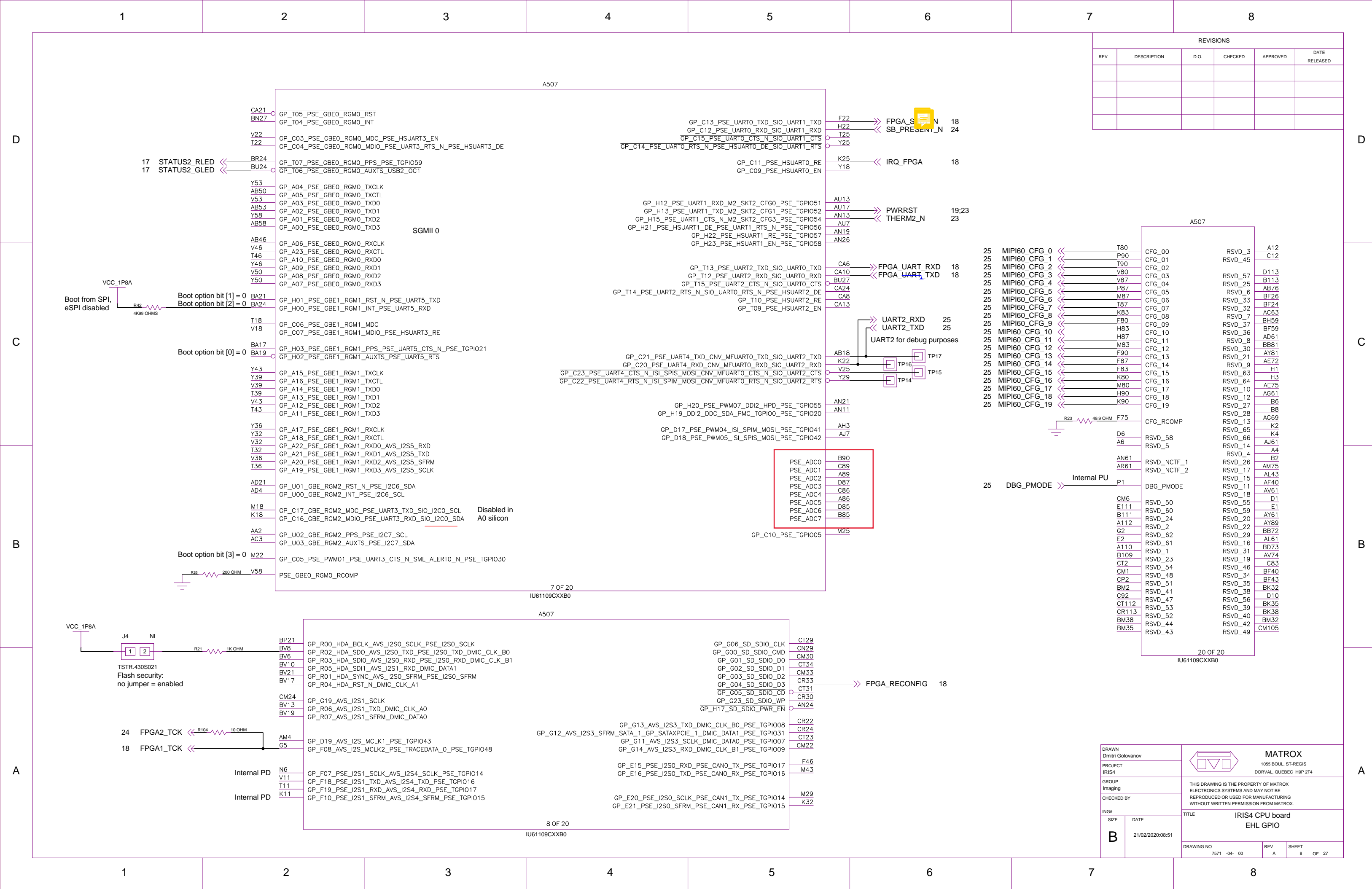
DDR sub-channels 0 and 1

A507

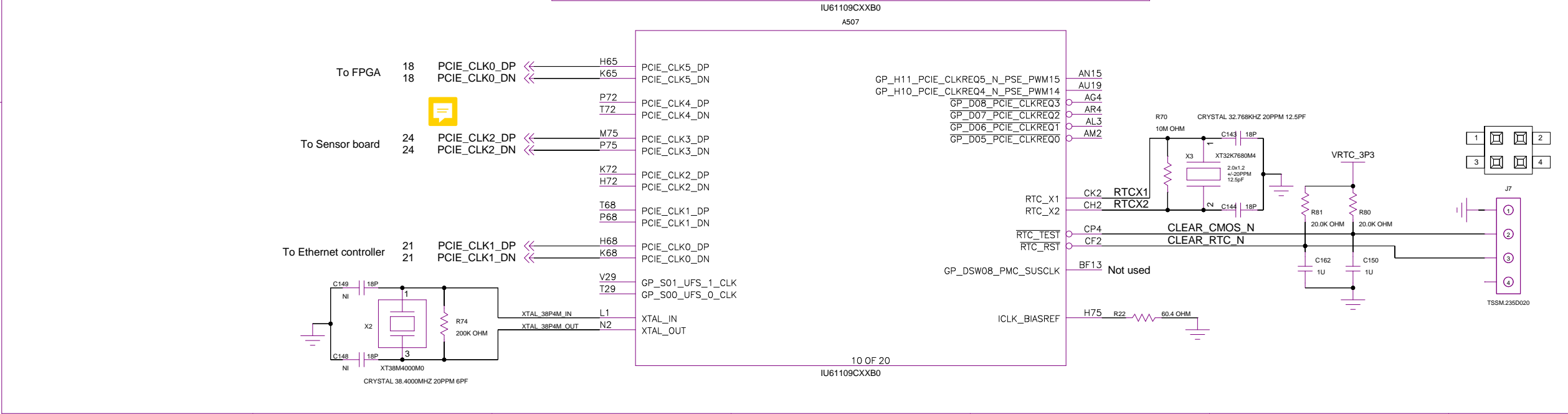
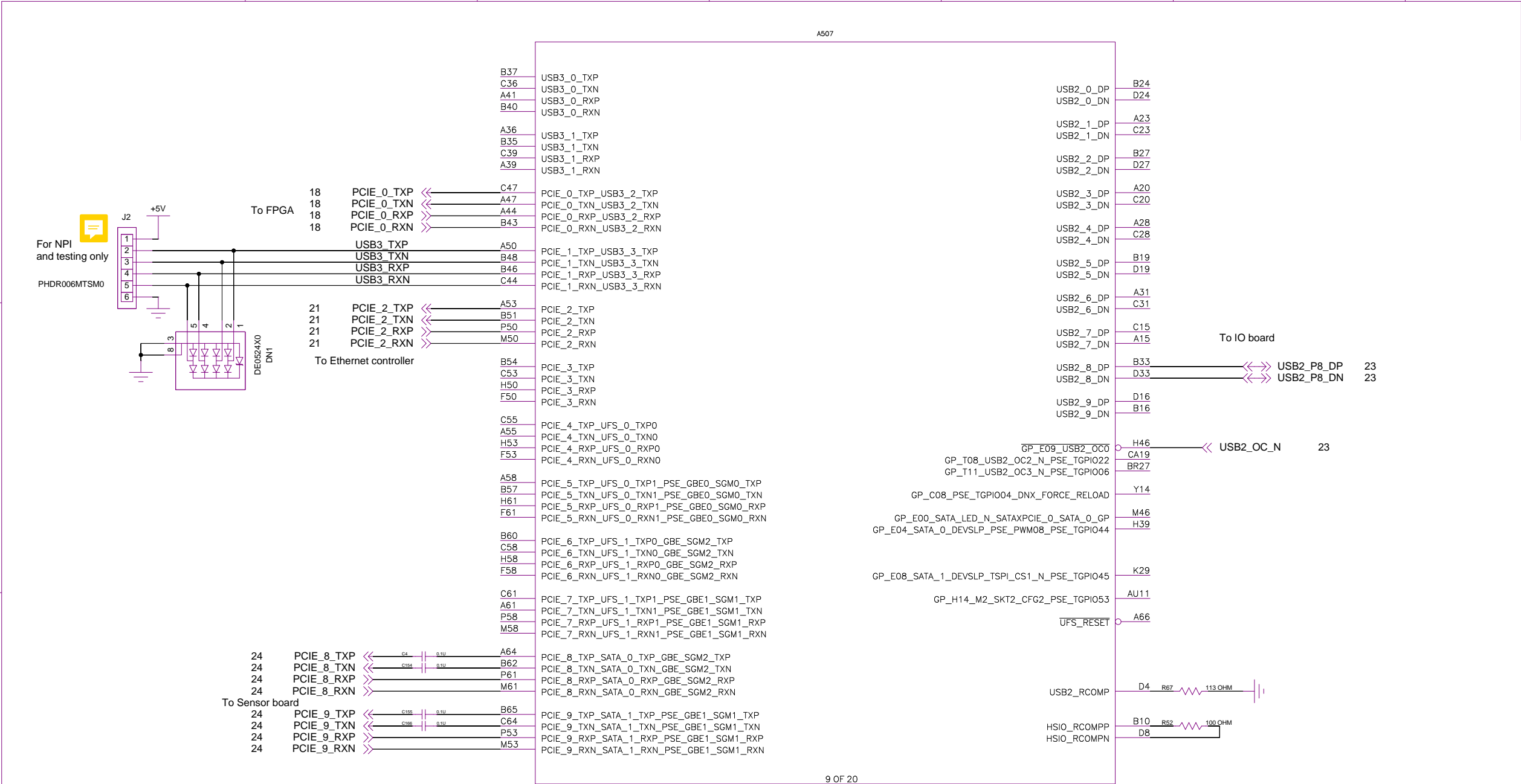



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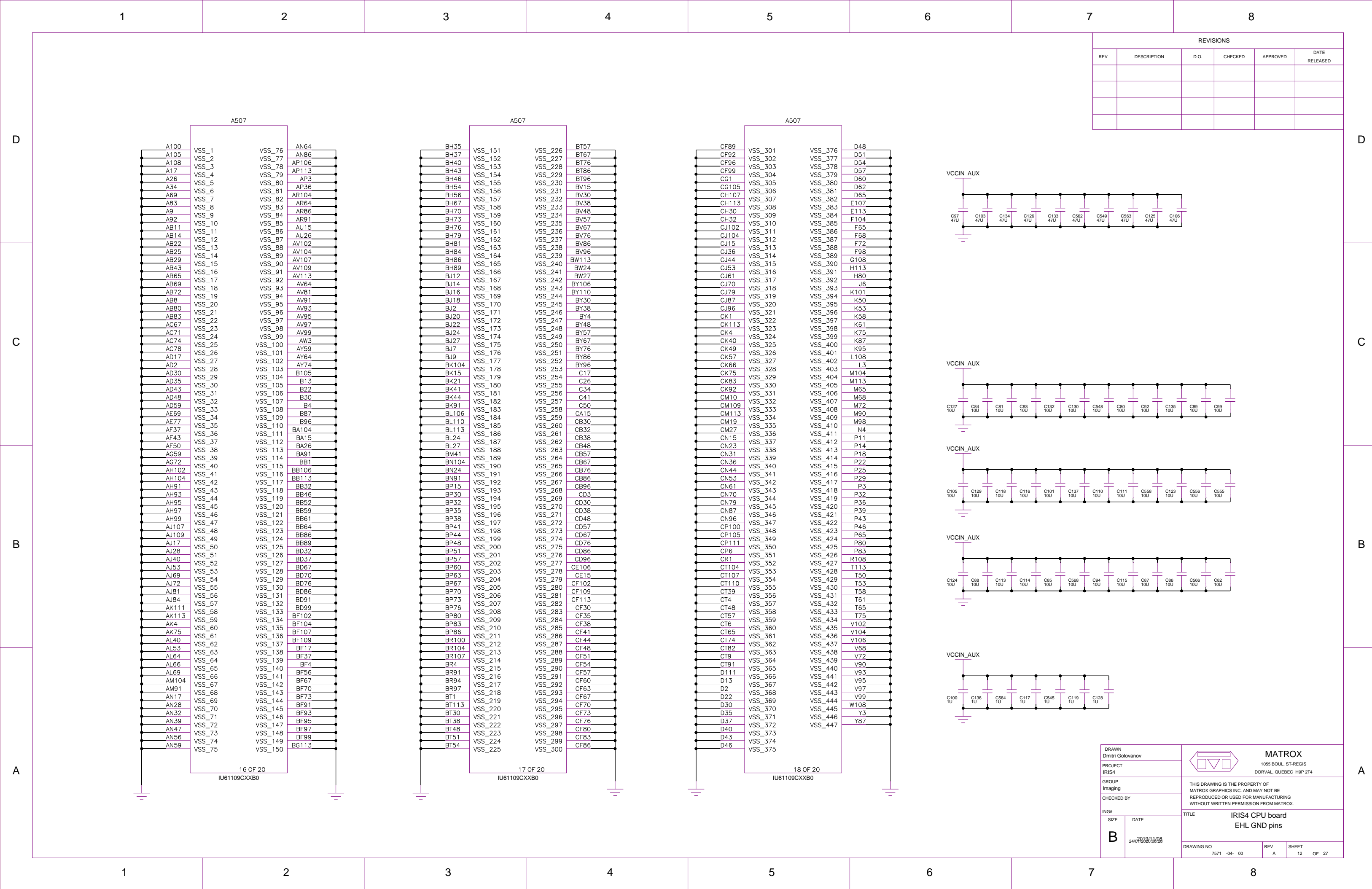
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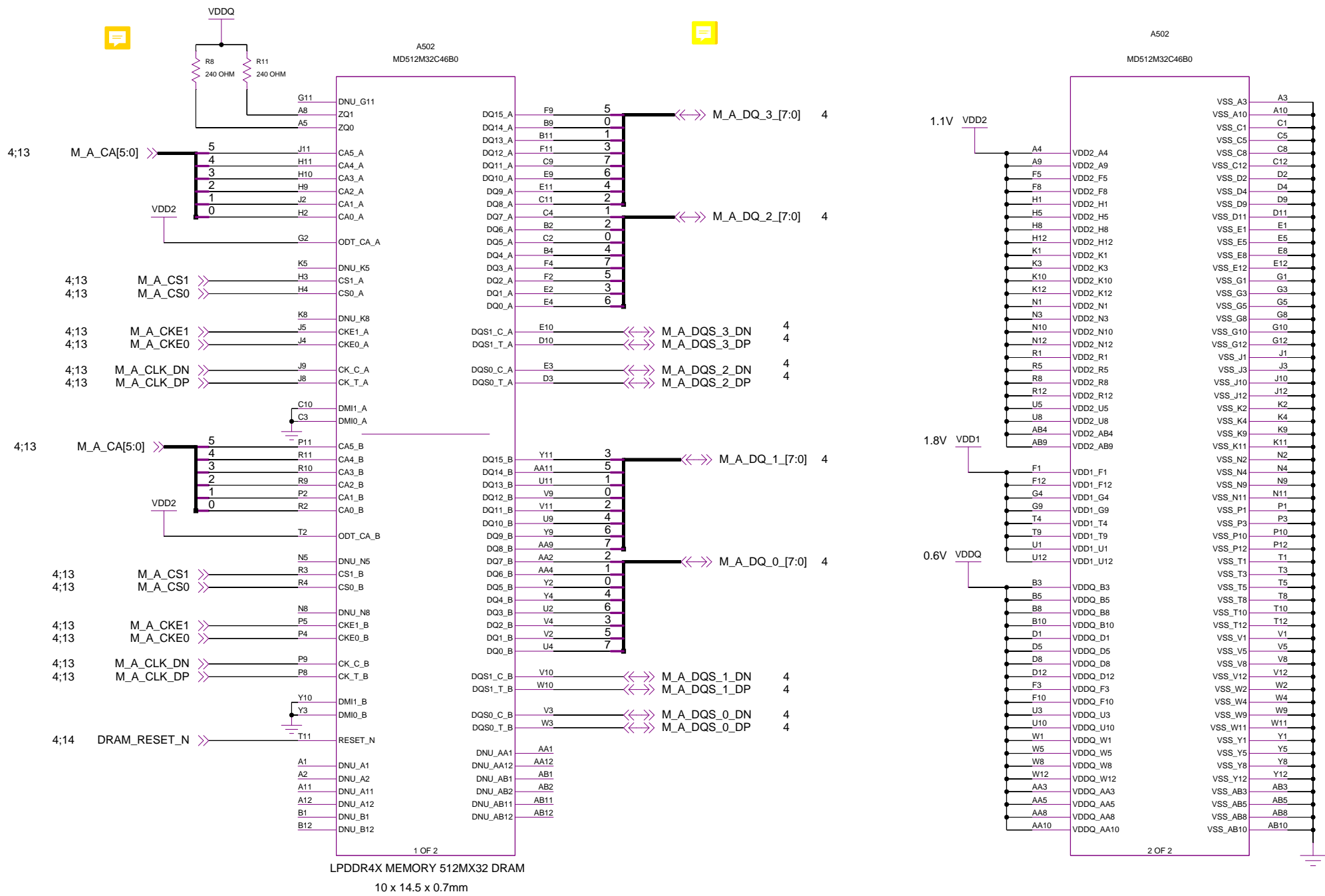
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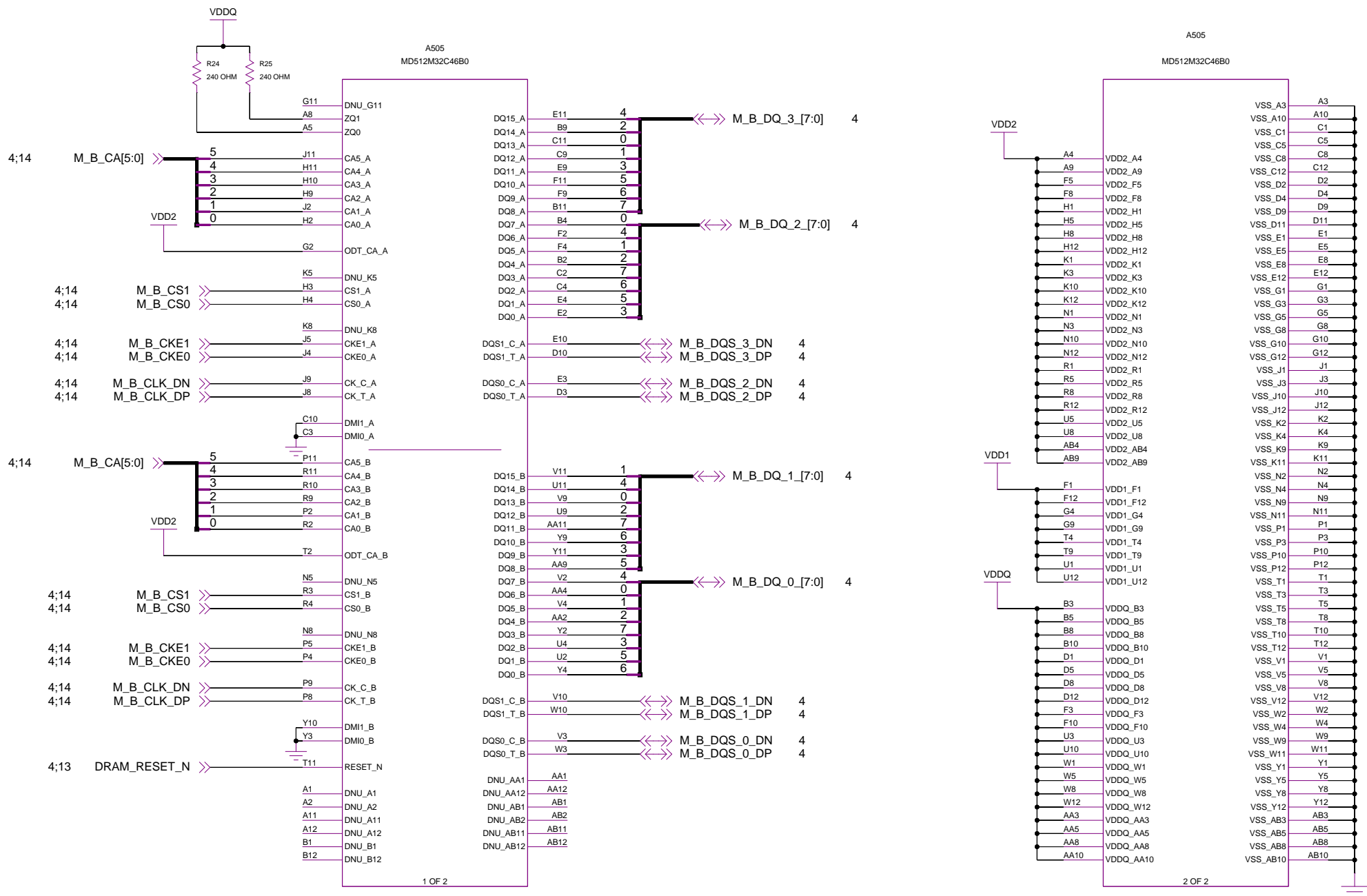



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Rail capacitors are on page 12

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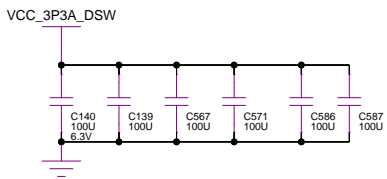
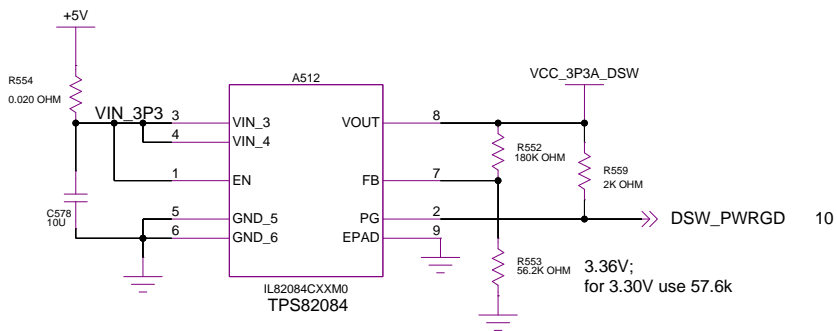
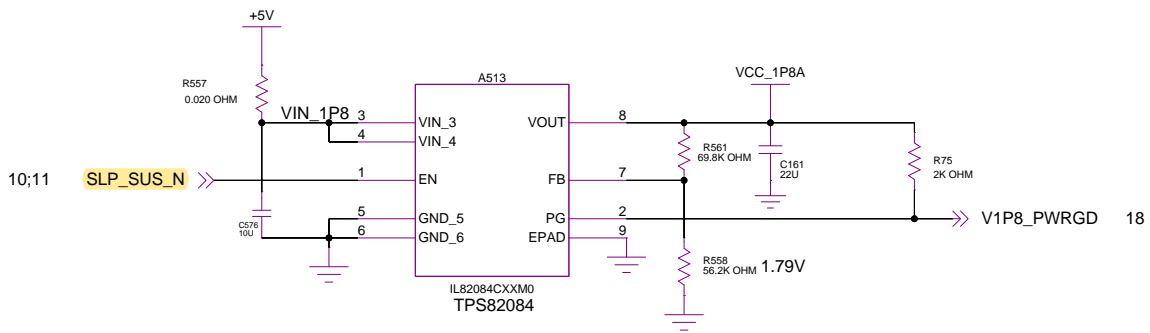
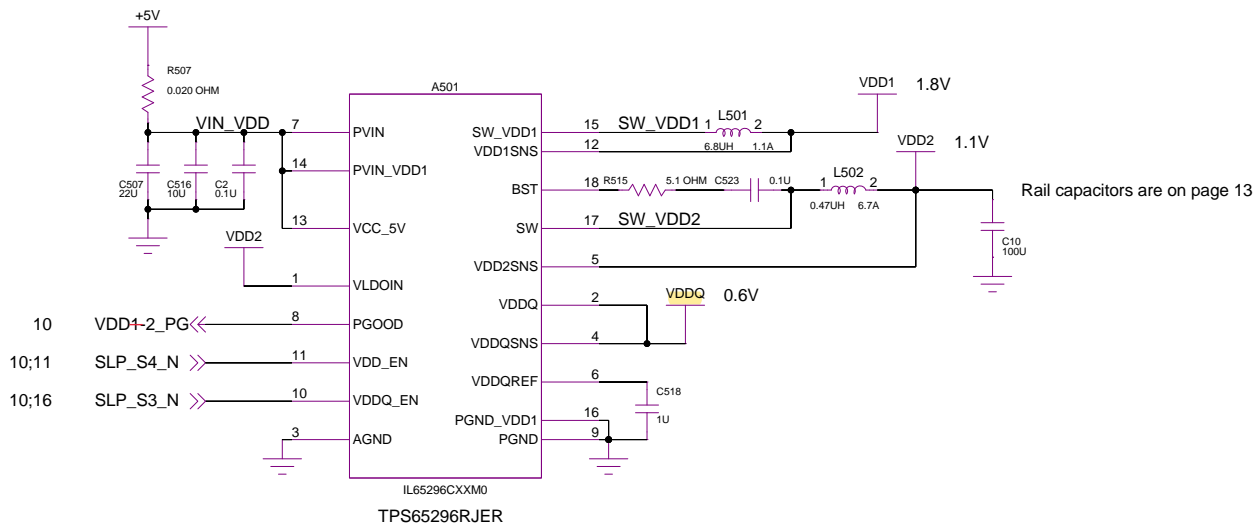
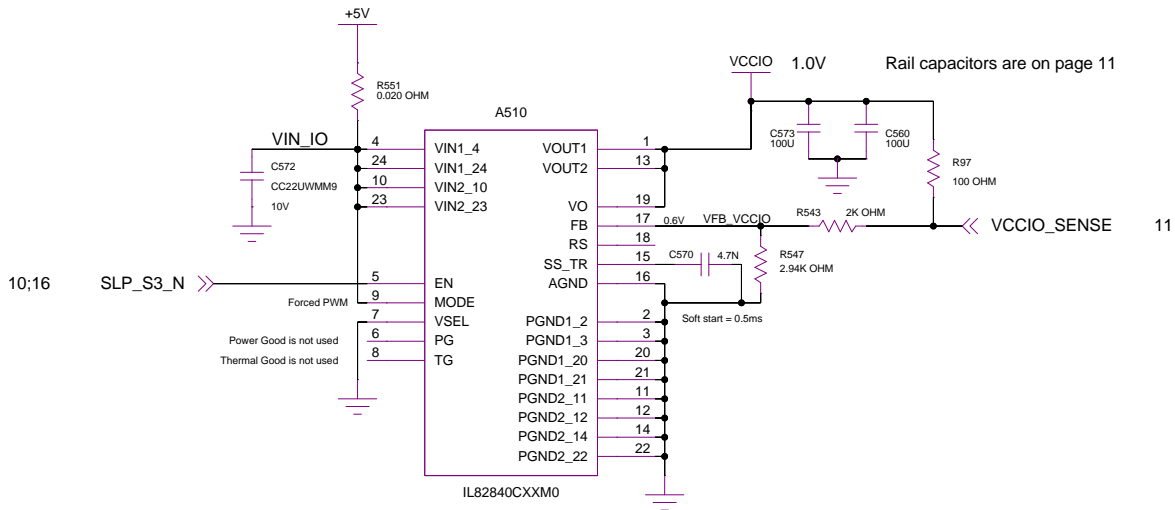
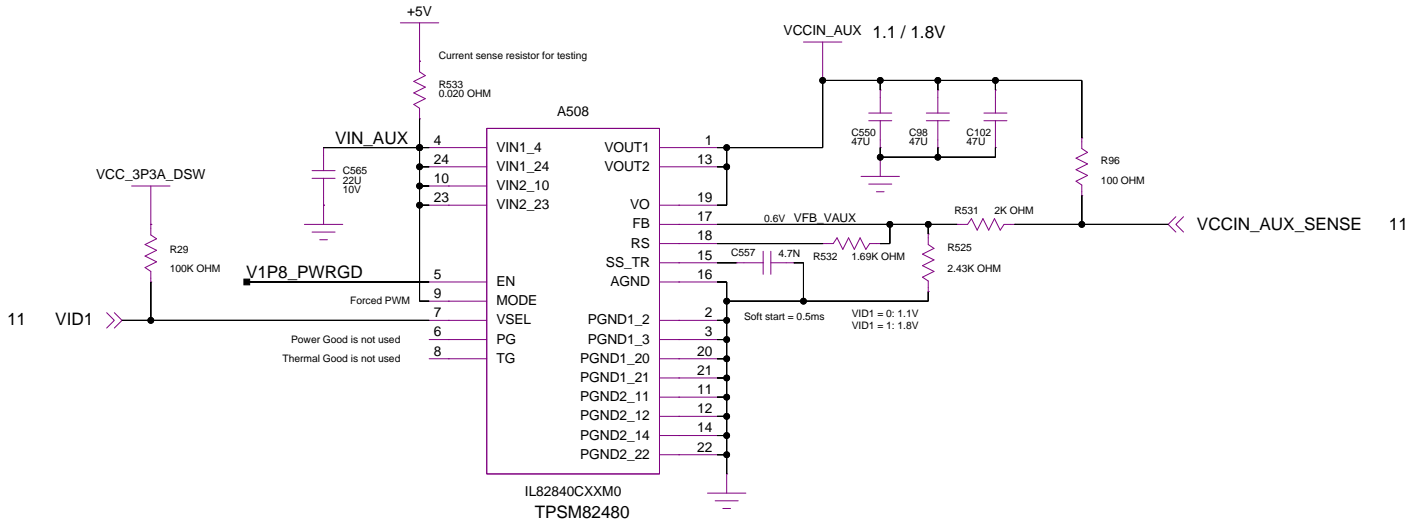
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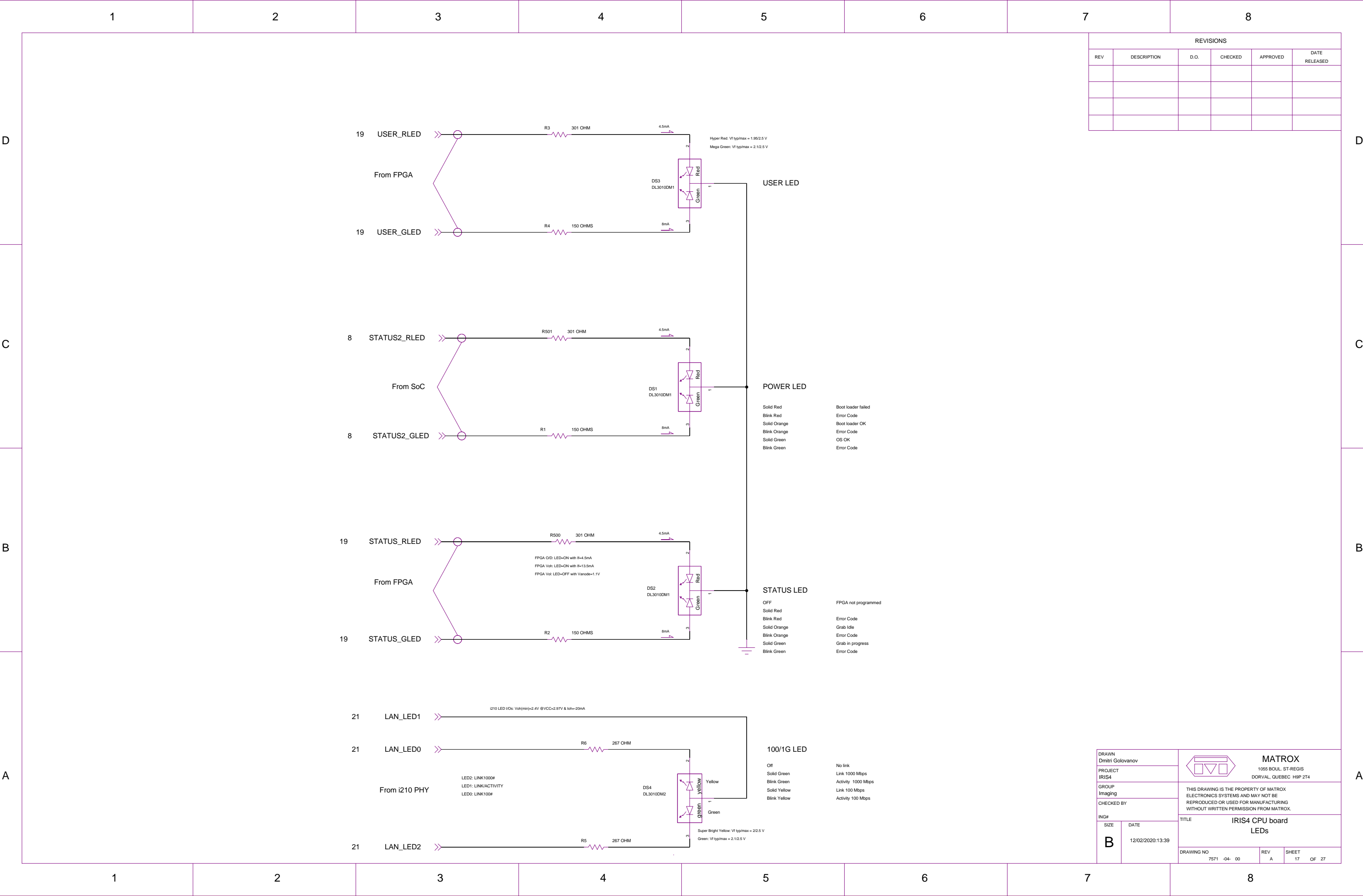
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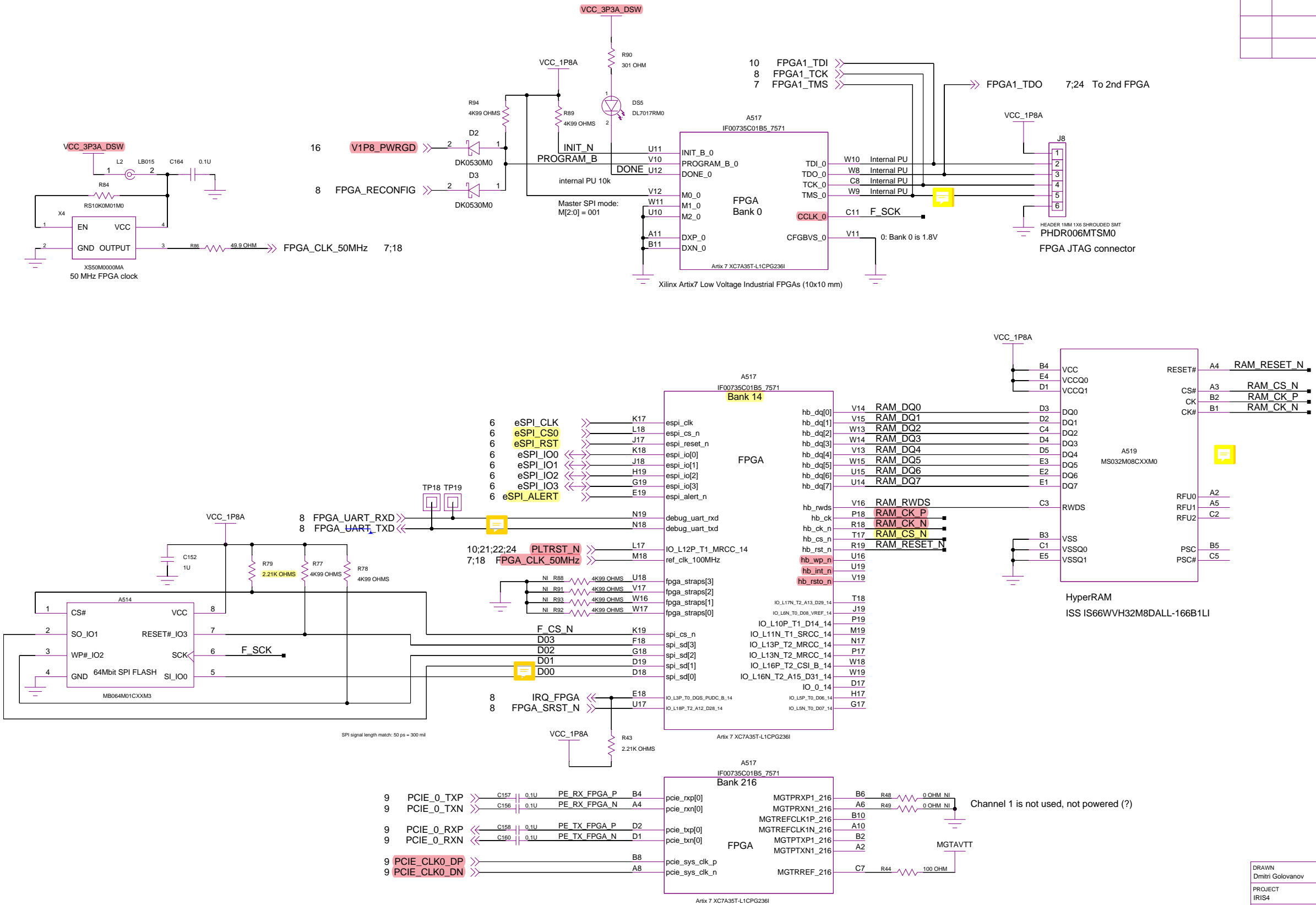
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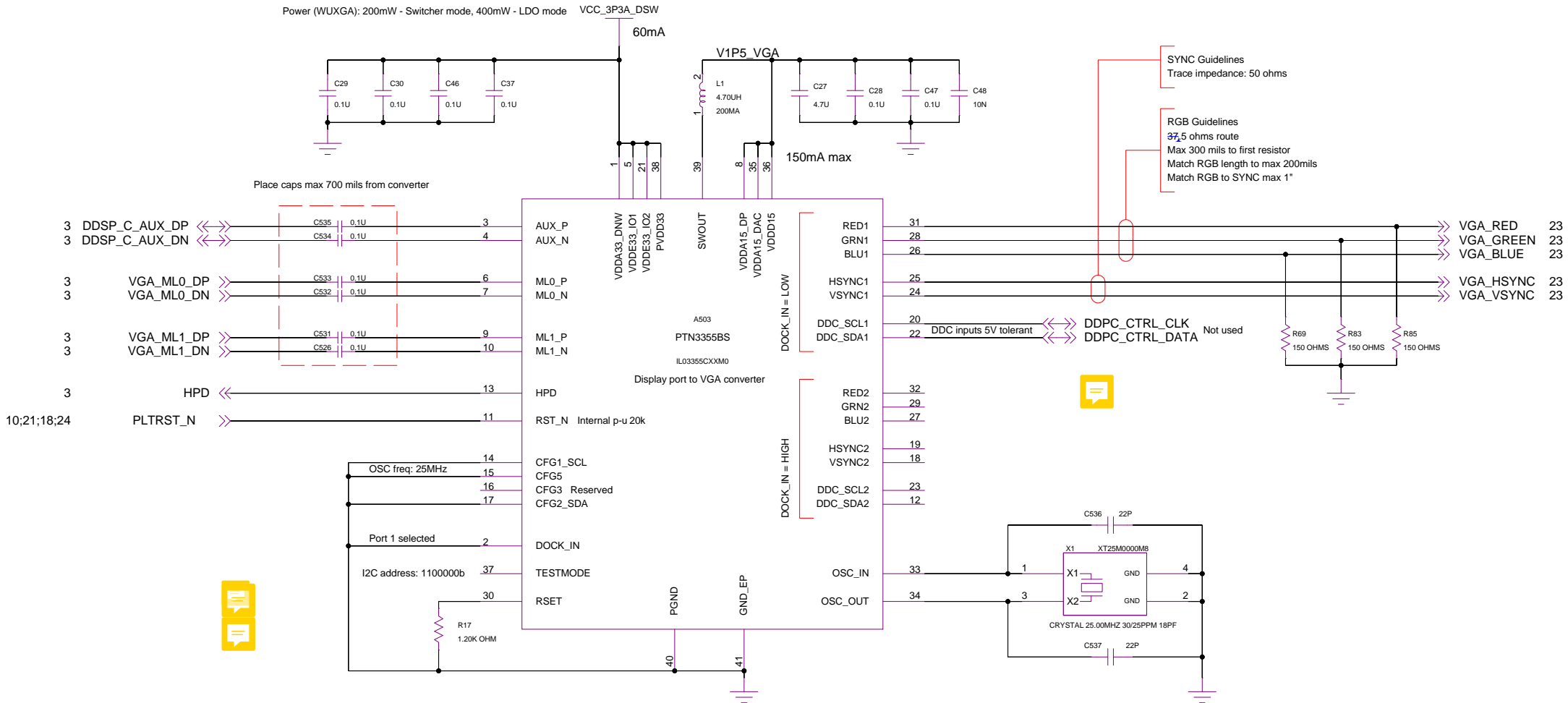
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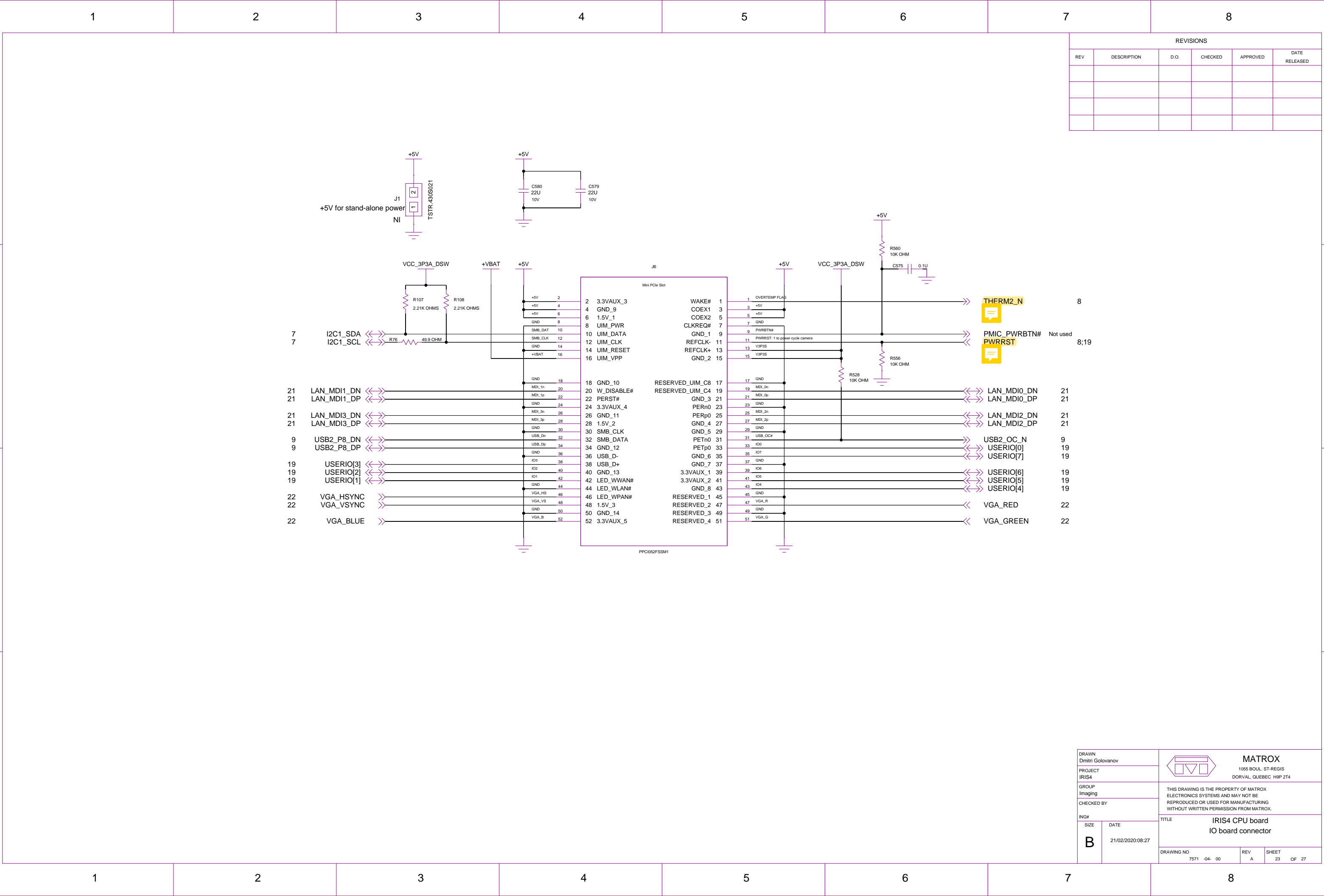
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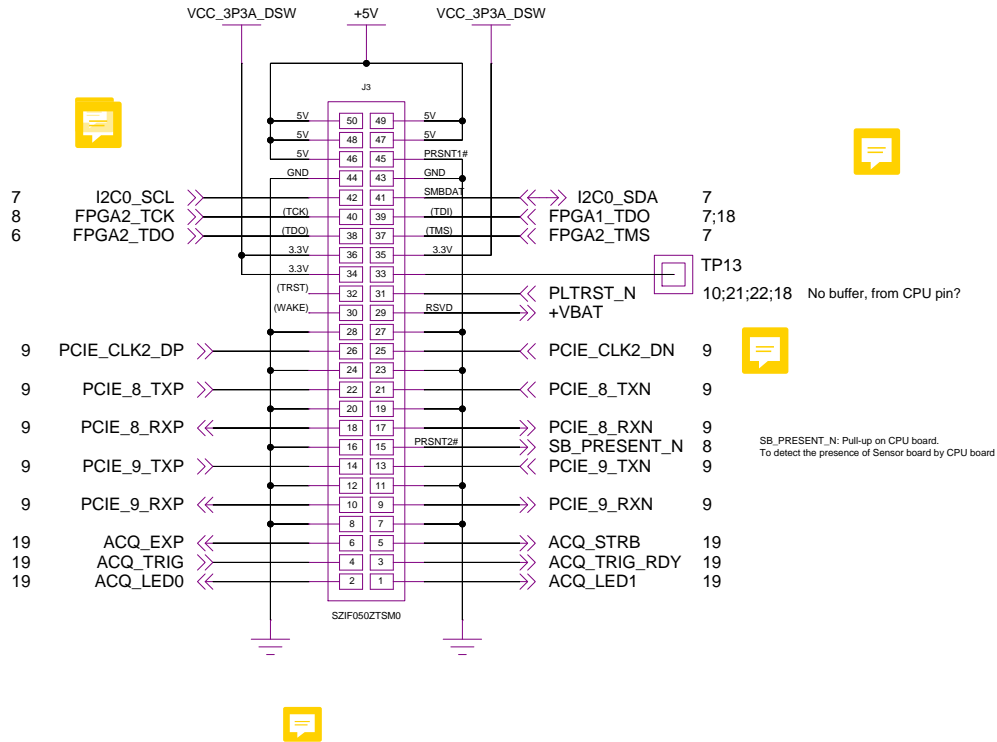
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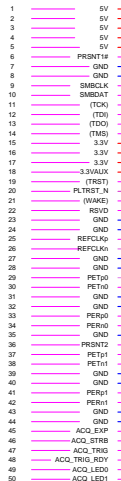
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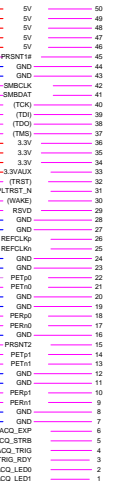
CPU Board ZIF pinout is inverted
Sensor board pos 1 aligned with CPU board pos 50
Connectors are head-to-head with latch on same side




Sensor board connector



CPU board connector



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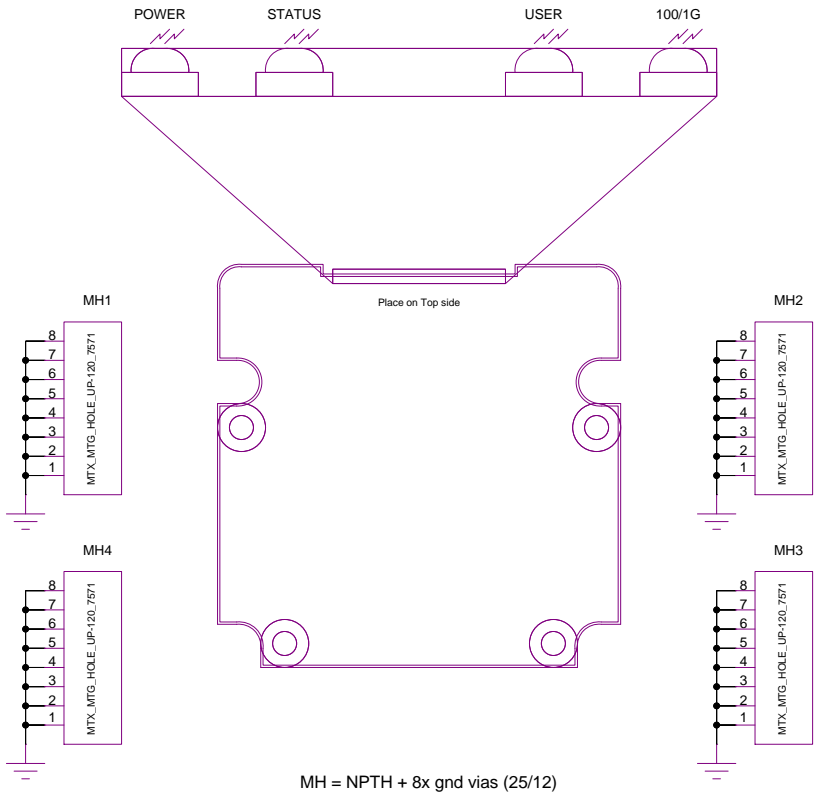
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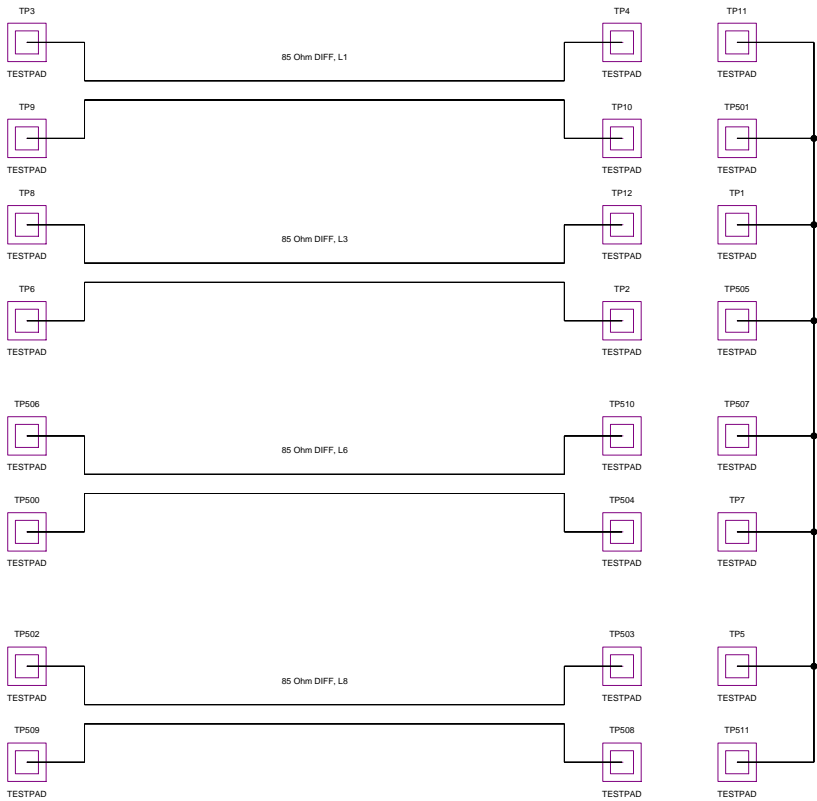
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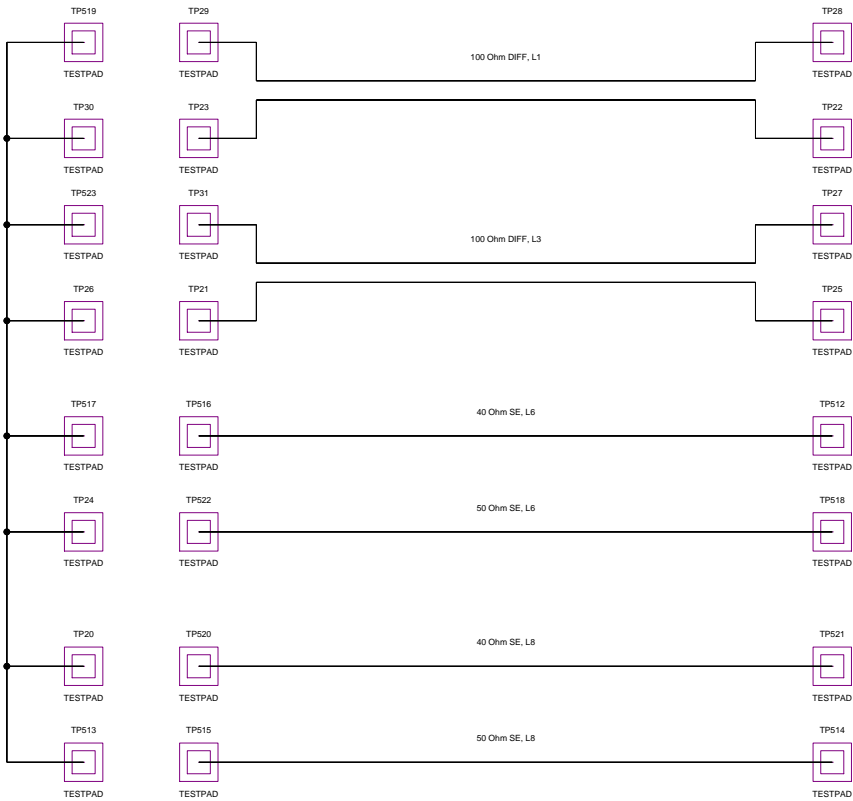
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Test coupons on panel upper cracker section
Route straight on full cracker length



Test coupons on panel lower cracker section
Route straight on full cracker length



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Revision History
Y7571-00 Rev.A: R1.00: First Release R1.10: Bring-up changes

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