

ZC706 EVALUATION PLATFORM HW-Z7-ZC706

(XC7Z045-FFG900)

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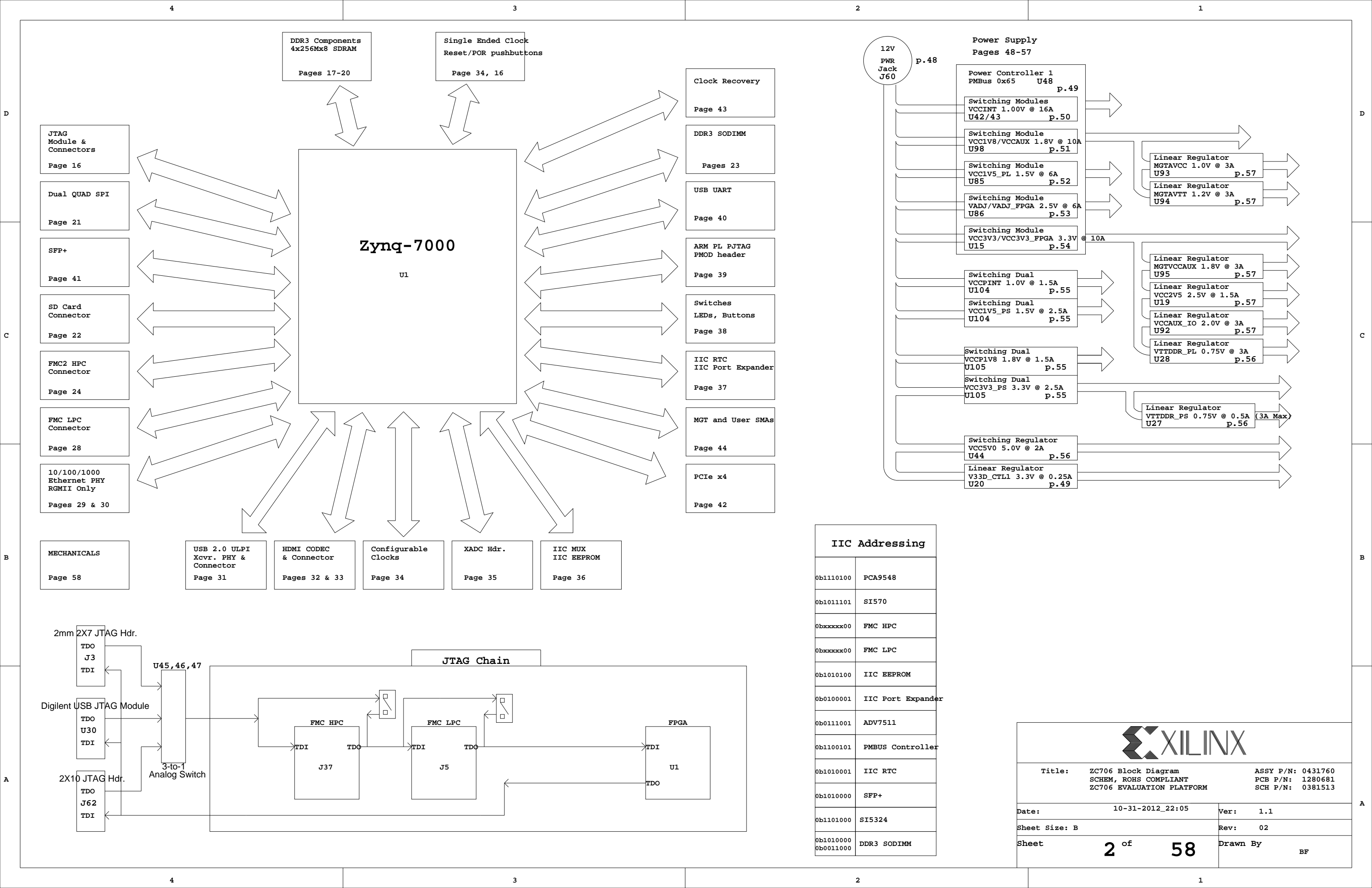
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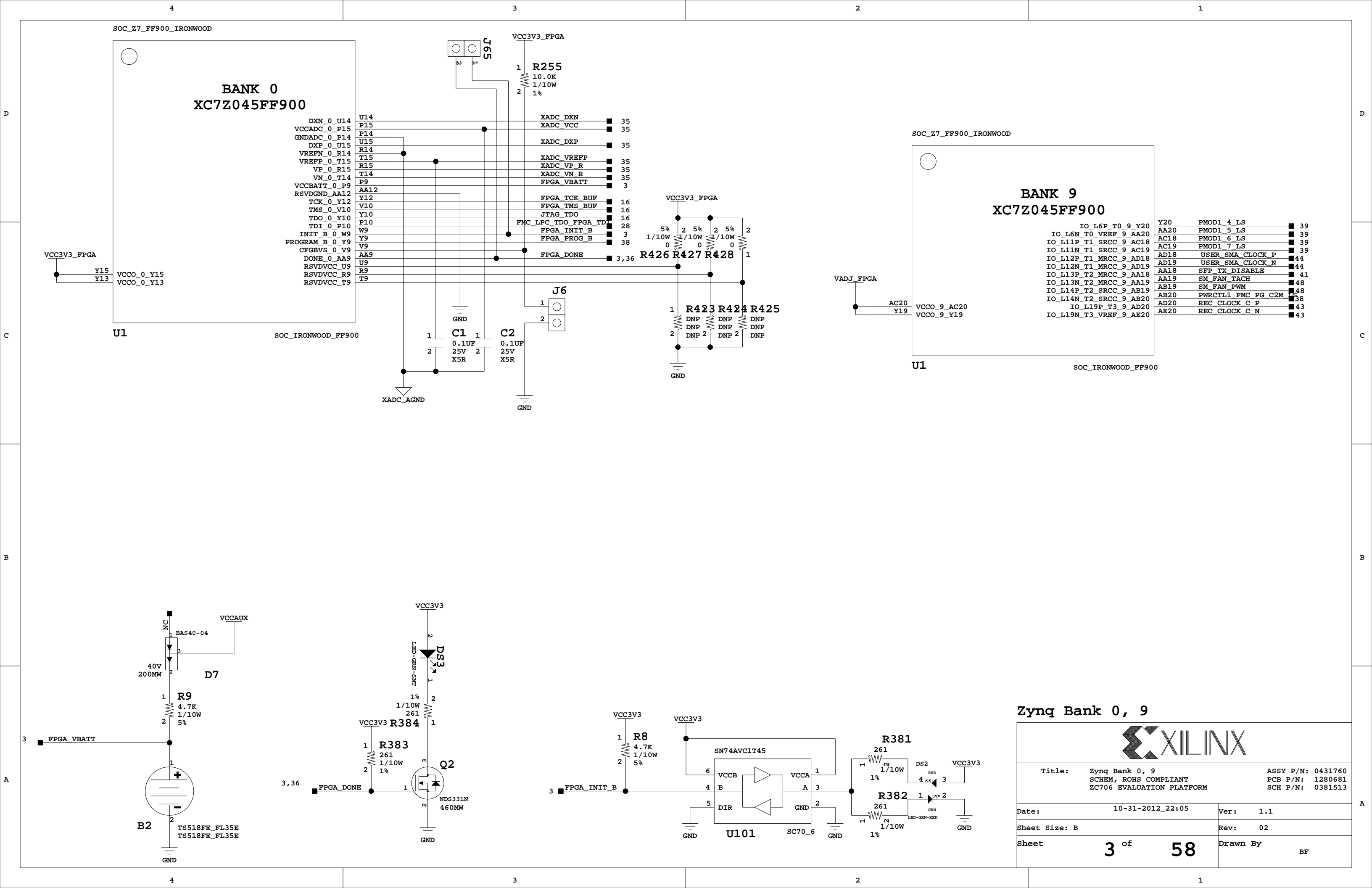
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Title:		ASSY P/N: 0431760	
		PCB P/N: 1280681	
		SCH P/N: 0381513	
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SOC_Z7_FF900_IRONWOOD

BANK 10
XC7Z045FF900

IO_0_10_AA13
IO_L1P_T0_10_AK13
IO_L1N_T0_10_AK12
IO_L2P_T0_10_AH18
IO_L2N_T0_10_AJ18
IO_L3P_T0_DQS_10_AJ14
IO_L3N_T0_DQS_10_AJ13
IO_L4P_T0_10_AJ16
IO_L4N_T0_10_AK16
IO_L5P_T0_10_AJ15
IO_L5N_T0_10_AK15
IO_L6P_T0_10_AH17
IO_L6N_T0_VREF_10_AH16
IO_L7P_T1_10_AE12
IO_L7N_T1_10_AF12
IO_L8P_T1_10_AH14
IO_L8N_T1_10_AH13
IO_L9P_T1_DQS_10_AD14
IO_L9N_T1_DQS_10_AD13
IO_L10P_T1_10_AG12
IO_L10N_T1_10_AH12
IO_L11P_T1_SRCC_10_AE13
IO_L11N_T1_SRCC_10_AF13
IO_L12P_T1_MRCC_10_AF14
IO_L12N_T1_MRCC_10_AG14
IO_L13P_T2_MRCC_10_AG17
IO_L13N_T2_MRCC_10_AG16
IO_L14P_T2_SRCC_10_AF15
IO_L14N_T2_SRCC_10_AG15
IO_L15P_T2_DQS_10_AF18
IO_L15N_T2_DQS_10_AF17
IO_L16P_T2_10_AE16
IO_L16N_T2_10_AE15
IO_L17P_T2_10_AE18
IO_L17N_T2_10_AE17
IO_L18P_T2_10_AD16
IO_L18N_T2_10_AD15
IO_L19P_T3_10_AC14
IO_L19N_T3_VREF_10_AC13
IO_L20P_T3_10_AA15
IO_L20N_T3_10_AA14
IO_L21P_T3_DQS_10_AB12
IO_L21N_T3_DQS_10_AC12
IO_L22P_T3_10_AB15
IO_L22N_T3_10_AB14
IO_L23P_T3_10_AC17
IO_L23N_T3_10_AC16
IO_L24P_T3_10_AB17
IO_L24N_T3_10_AB16
IO_25_10_AA17

AA13
AK13
AK12
AH18
AJ18
AJ14
AJ13
AJ16
AK16
AJ15
AK15
AH17
AH16
AE12
AF12
AH14
AH13
AD14
AD13
AG12
AH12
AE13
AF13
AF14
AG14
AG17
AG16
AF15
AG15
AF18
AF17
AE16
AE15
AE18
AE17
AD16
AD15
AC14
AC13
AA15
AA14
AB12
AC12
AB15
AB14
AC17
AC16
AB17
AB16
AA17

PL PJTAG TCK
PL PJTAG TMS
PL PJTAG TDI
IIC SDA MAIN LS
IIC SCL MAIN LS
GPIO DIP SW3
FMC LPC LA11 P
FMC LPC LA11 N
FMC LPC LA04 P
FMC LPC LA04 N
FMC LPC LA13 P
FMC LPC LA13 N
FMC LPC LA02 P
FMC LPC LA02 N
FMC LPC LA09 P
FMC LPC LA09 N
FMC LPC LA08 P
FMC LPC LA08 N
FMC LPC LA03 P
FMC LPC LA03 N
FMC LPC LA00 CC P
FMC LPC LA00 CC N
USRCLK P
USRCLK N
FMC LPC CLK0 M2C P
FMC LPC CLK0 M2C N
FMC LPC LA01 CC P
FMC LPC LA01 CC N
FMC LPC LA14 P
FMC LPC LA14 N
FMC LPC LA05 P
FMC LPC LA05 N
FMC LPC LA16 P
FMC LPC LA16 N
FMC LPC LA12 P
FMC LPC LA12 N
FMC LPC LA10 P
FMC LPC LA10 N
FMC LPC LA07 P
FMC LPC LA07 N
FMC LPC LA06 P
FMC LPC LA06 N
FMC LPC LA15 P
FMC LPC LA15 N
GPIO DIP SW2
GPIO DIP SW1
GPIO DIP SW0
FMOD1_3_LS
IIC RTC IRQ_1_B

R154
22
1/10W
1%

PL PJTAG TDO

VADJ_FPGA

AA16
AB13
AD17
AE14
AG18
AH15
AJ12

VCCO_10_AA16
VCCO_10_AB13
VCCO_10_AD17
VCCO_10_AE14
VCCO_10_AG18
VCCO_10_AH15
VCCO_10_AJ12

U1

SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK 11
XC7Z045FF900

IO_0_11_W23
IO_L1P_T0_11_AJ25
IO_L1N_T0_11_AK25
IO_L2P_T0_11_AK22
IO_L2N_T0_11_AK23
IO_L3P_T0_DQS_11_AJ21
IO_L3N_T0_DQS_11_AK21
IO_L4P_T0_11_AJ23
IO_L4N_T0_11_AJ24
IO_L5P_T0_11_AH23
IO_L5N_T0_11_AH24
IO_L6P_T0_11_AG22
IO_L6N_T0_VREF_11_AH22
IO_L7P_T1_11_AC24
IO_L7N_T1_11_AD24
IO_L8P_T1_11_AG24
IO_L8N_T1_11_AG25
IO_L9P_T1_DQS_11_AF23
IO_L9N_T1_DQS_11_AF24
IO_L10P_T1_11_AD21
IO_L10N_T1_11_AE21
IO_L11P_T1_SRCC_11_AD23
IO_L11N_T1_SRCC_11_AE23
IO_L12P_T1_MRCC_11_AE22
IO_L12N_T1_MRCC_11_AF22
IO_L13P_T2_MRCC_11_AG21
IO_L13N_T2_MRCC_11_AH21
IO_L14P_T2_SRCC_11_AF20
IO_L14N_T2_SRCC_11_AG20
IO_L15P_T2_DQS_11_AJ20
IO_L15N_T2_DQS_11_AK20
IO_L16P_T2_11_AK17
IO_L16N_T2_11_AK18
IO_L17P_T2_11_AH19
IO_L17N_T2_11_AJ19
IO_L18P_T2_11_AF19
IO_L18N_T2_11_AG19
IO_L19P_T3_11_AB21
IO_L19N_T3_VREF_11_AB22
IO_L20P_T3_11_W21
IO_L20N_T3_11_Y21
IO_L21P_T3_DQS_11_Y22
IO_L21N_T3_DQS_11_Y23
IO_L22P_T3_11_AA24
IO_L22N_T3_11_AB24
IO_L23P_T3_11_AA22
IO_L23N_T3_11_AA23
IO_L24P_T3_11_AC22
IO_L24N_T3_11_AC23
IO_25_11_AC21

W23
AJ25
AK25
AK22
AK23
AJ21
AK21
AJ23
AJ24
AH23
AH24
AG22
AH22
AC24
AD24
AG24
AG25
AF23
AF24
AD21
AE21
AD23
AE23
AE22
AF22
AG21
AH21
AF20
AG20
AJ20
AK20
AK17
AK18
AH19
AJ19
AF19
AG19
AB21
AB22
W21
Y21
Y22
Y23
AA24
AB24
AA22
AA23
AC22
AC23
AC21

SI5324 RST_LS
SI5324 INT_ALM_LS
GPIO_SW_LEFT
PCIE_WAKE_B_LS
PCIE_PERST_LS
FMOD1_0_LS
FMOD1_1_LS
FMC_HPC_LA07_P
FMC_HPC_LA07_N
FMC_HPC_LA05_P
FMC_HPC_LA05_N
FMC_HPC_LA06_P
FMC_HPC_LA06_N
FMC_HPC_LA14_P
FMC_HPC_LA14_N
FMC_HPC_LA10_P
FMC_HPC_LA10_N
FMC_HPC_LA12_P
FMC_HPC_LA12_N
FMC_HPC_LA09_P
FMC_HPC_LA09_N
FMC_HPC_LA11_P
FMC_HPC_LA11_N
FMC_HPC_CLK0_M2C_P
FMC_HPC_CLK0_M2C_N
FMC_HPC_LA01_CC_P
FMC_HPC_LA01_CC_N
FMC_HPC_LA00_CC_P
FMC_HPC_LA00_CC_N
FMC_HPC_LA04_P
FMC_HPC_LA04_N
FMC_HPC_LA02_P
FMC_HPC_LA02_N
FMC_HPC_LA03_P
FMC_HPC_LA03_N
FMC_HPC_LA08_P
FMC_HPC_LA08_N
FMC_HPC_LA08_N
FMOD1_2_LS
HDMI_SPDIF_OUT_LS
GPIO_LED_RIGHT
GPIO_LED_LEFT
FMC_HPC_LA15_P
FMC_HPC_LA15_N
FMC_HPC_LA16_P
FMC_HPC_LA16_N
FMC_HPC_LA13_P
FMC_HPC_LA13_N
HDMI_R_D35
HDMI_INT
HDMI_R_SPDIF

VADJ_FPGA

AB23
AE24
AF21
AH25
AJ22
AK19
W22

VCCO_11_AB23
VCCO_11_AE24
VCCO_11_AF21
VCCO_11_AH25
VCCO_11_AJ22
VCCO_11_AK19
VCCO_11_W22

U1

SOC_IRONWOOD_FF900

Zynq Bank 10, 11



Title: Zynq Bank 10, 11
SCHEM, ROHS COMPLIANT
ZC706 EVALUATION PLATFORM

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SOC_Z7_FF900_IRONWOOD

BANK 12
XC7Z045FF900

IO_0_12_Y25
IO_L1P_T0_12_Y30
IO_L1N_T0_12_AA30
IO_L2P_T0_12_AB29
IO_L2N_T0_12_AB30
IO_L3P_T0_DQS_12_Y26
IO_L3N_T0_DQS_12_Y27
IO_L4P_T0_12_Y28
IO_L4N_T0_12_AA29
IO_L5P_T0_12_AA27
IO_L5N_T0_12_AA28
IO_L6P_T0_12_AB25
IO_L6N_T0_VREF_12_AB26
IO_L7P_T1_12_AC26
IO_L7N_T1_12_AD26
IO_L8P_T1_12_AD30
IO_L8N_T1_12_AE30
IO_L9P_T1_DQS_12_AC29
IO_L9N_T1_DQS_12_AD29
IO_L10P_T1_12_AD25
IO_L10N_T1_12_AE26
IO_L11P_T1_SRCC_12_AB27
IO_L11N_T1_SRCC_12_AC27
IO_L12P_T1_MRCC_12_AC28
IO_L12N_T1_MRCC_12_AD28
IO_L13P_T2_MRCC_12_AE28
IO_L13N_T2_MRCC_12_AF28
IO_L14P_T2_SRCC_12_AE27
IO_L14N_T2_SRCC_12_AF27
IO_L15P_T2_DQS_12_AF29
IO_L15N_T2_DQS_12_AG29
IO_L16P_T2_12_AF30
IO_L16N_T2_12_AG30
IO_L17P_T2_12_AG26
IO_L17N_T2_12_AG27
IO_L18P_T2_12_AE25
IO_L18N_T2_12_AF25
IO_L19P_T3_12_AH28
IO_L19N_T3_VREF_12_AH29
IO_L20P_T3_12_AJ30
IO_L20N_T3_12_AK30
IO_L21P_T3_DQS_12_AJ28
IO_L21N_T3_DQS_12_AJ29
IO_L22P_T3_12_AK27
IO_L22N_T3_12_AK28
IO_L23P_T3_12_AH26
IO_L23N_T3_12_AH27
IO_L24P_T3_12_AJ26
IO_L24N_T3_12_AK26
IO_25_12_AA25

Y25 HDMI_R_D21 33
Y30 FMC LPC LA33 P 28
AA30 FMC LPC LA33 N 28
AB29 FMC LPC LA30 P 28
AB30 FMC LPC LA30 N 28
Y26 FMC LPC LA32 P 28
Y27 FMC LPC LA32 N 28
Y28 HDMI_R_D28 33
AA29 HDMI_R_D22 33
AA27 HDMI_R_D31 33
AA28 HDMI_R_D18 33
AB25 HDMI_R_D10 33
AB26 HDMI_R_D17 33
AC26 HDMI_R_D19 33
AD26 HDMI_R_D16 33
AD30 HDMI_R_D23 33
AE30 HDMI_R_D20 33
AC29 FMC LPC LA31 P 28
AD29 FMC LPC LA31 N 28
AD25 FMC LPC LA28 P 28
AE26 FMC LPC LA28 N 28
AB27 FMC LPC LA17 CC P 28
AC27 FMC LPC LA17 CC N 28
AC28 FMC LPC CLK1 M2C P 28
AD28 FMC LPC CLK1 M2C N 28
AE28 HDMI_R_D8 33
AF28 HDMI_R_D29 33
AE27 FMC LPC LA18 CC P 28
AF27 FMC LPC LA18 CC N 28
AF29 FMC LPC LA25 P 28
AG29 FMC LPC LA25 N 28
AF30 FMC LPC LA24 P 28
AG30 FMC LPC LA24 N 28
AG26 FMC LPC LA20 P 28
AG27 FMC LPC LA20 N 28
AE25 FMC LPC LA29 P 28
AF25 FMC LPC LA29 N 28
AH28 FMC LPC LA21 P 28
AH29 FMC LPC LA21 N 28
AJ30 FMC LPC LA26 P 28
AK30 FMC LPC LA26 N 28
AJ28 FMC LPC LA27 P 28
AJ29 FMC LPC LA27 N 28
AK27 FMC LPC LA22 P 28
AK28 FMC LPC LA22 N 28
AH26 FMC LPC LA19 P 28
AH27 FMC LPC LA19 N 28
AJ26 FMC LPC LA23 P 28
AK26 FMC LPC LA23 N 28
AA25 HDMI_R_D7 33

VADJ_FPGA

AA26 VCCO_12_AA26
AC30 VCCO_12_AC30
AD27 VCCO_12_AD27
AG28 VCCO_12_AG28
AK29 VCCO_12_AK29
Y29 VCCO_12_Y29

U1

SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK 13
XC7Z045FF900

IO_0_13_U21
IO_L1P_T0_13_P30
IO_L1N_T0_13_R30
IO_L2P_T0_13_T30
IO_L2N_T0_13_U30
IO_L3P_T0_DQS_13_N28
IO_L3N_T0_DQS_13_P28
IO_L4P_T0_13_N29
IO_L4N_T0_13_P29
IO_L5P_T0_13_T29
IO_L5N_T0_13_U29
IO_L6P_T0_13_R28
IO_L6N_T0_VREF_13_T28
IO_L7P_T1_13_V28
IO_L7N_T1_13_V29
IO_L8P_T1_13_W29
IO_L8N_T1_13_W30
IO_L9P_T1_DQS_13_V27
IO_L9N_T1_DQS_13_W28
IO_L10P_T1_13_W25
IO_L10N_T1_13_W26
IO_L11P_T1_SRCC_13_U25
IO_L11N_T1_SRCC_13_V26
IO_L12P_T1_MRCC_13_U26
IO_L12N_T1_MRCC_13_U27
IO_L13P_T2_MRCC_13_R25
IO_L13N_T2_MRCC_13_R26
IO_L14P_T2_SRCC_13_R27
IO_L14N_T2_SRCC_13_T27
IO_L15P_T2_DQS_13_N26
IO_L15N_T2_DQS_13_N27
IO_L16P_T2_13_P25
IO_L16N_T2_13_P26
IO_L17P_T2_13_T24
IO_L17N_T2_13_T25
IO_L18P_T2_13_P23
IO_L18N_T2_13_P24
IO_L19P_T3_13_P21
IO_L19N_T3_VREF_13_R21
IO_L20P_T3_13_T22
IO_L20N_T3_13_T23
IO_L21P_T3_DQS_13_R22
IO_L21N_T3_DQS_13_R23
IO_L22P_T3_13_U22
IO_L22N_T3_13_V22
IO_L23P_T3_13_U24
IO_L23N_T3_13_V24
IO_L24P_T3_13_V23
IO_L24N_T3_13_W24
IO_25_13_V21

U21 HDMI_R_VSYNC 33
P30 FMC HPC LA28 P 26
R30 FMC HPC LA28 N 26
T30 FMC HPC LA24 P 26
U30 FMC HPC LA24 N 26
N28 HDMI_R_D33 33
P28 HDMI_R_CLK 33
N29 FMC HPC LA31 P 25
P29 FMC HPC LA31 N 25
T29 FMC HPC LA25 P 25
U29 FMC HPC LA25 N 25
R28 FMC HPC LA26 P 24
T28 FMC HPC LA26 N 24
V28 FMC HPC LA27 P 24
V29 FMC HPC LA27 N 24
W29 FMC HPC LA21 P 24
W30 FMC HPC LA21 N 26
V27 FMC HPC LA22 P 25
W28 FMC HPC LA22 N 25
W25 FMC HPC LA18 CC P 24
W26 FMC HPC LA18 CC N 24
U25 FMC HPC LA20 P 25
V26 FMC HPC LA20 N 25
U26 FMC HPC CLK1 M2C P 25
U27 FMC HPC CLK1 M2C N 25
R25 FMC HPC LA29 P 25
R26 FMC HPC LA29 N 25
R27 GPIO_SW_RIGHT 38
T27 HDMI_R_D11 3
N26 FMC HPC LA33 P 25
N27 FMC HPC LA33 N 25
P25 FMC HPC LA23 P 24
P26 FMC HPC LA23 N 24
T24 FMC HPC LA19 P 26
T25 FMC HPC LA19 N 26
P23 FMC HPC LA30 P 26
P24 FMC HPC LA30 N 26
P21 FMC HPC LA32 P 26
R21 FMC HPC LA32 N 26
T22 HDMI_R_D5 33
T23 HDMI_R_D9 33
R22 HDMI_R_HSYNC 33
R23 HDMI_R_D6 33
U22 HDMI_R_D32 33
V22 HDMI_R_D30 33
U24 HDMI_R_D4 33
V24 HDMI_R_DE 33
V23 FMC HPC LA17 CC P 33
W24 FMC HPC LA17 CC N 24
V21 HDMI_R_D34 33

VADJ_FPGA

N30 VCCO_13_N30
P27 VCCO_13_P27
R24 VCCO_13_R24
T21 VCCO_13_T21
U28 VCCO_13_U28
V25 VCCO_13_V25

U1

SOC_IRONWOOD_FF900

Zynq Bank 12, 13



Title: Zynq Bank 12, 13 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
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D

C

B

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D

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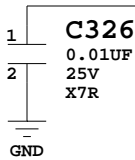
SOC_Z7_FF900_IRONWOOD

BANK 33
XC7Z045FF900

IO_0_VRN_33_L5	L5	VRN_33	6
IO_L1P_T0_33_J4	J4	PL_DDR3_D3	23
IO_L1N_T0_33_J3	J3	PL_DDR3_DM0	23
IO_L2P_T0_33_L1	L1	PL_DDR3_D0	23
IO_L2N_T0_33_K1	K1	PL_DDR3_D4	23
IO_L3P_T0_DQS_33_K3	K3	PL_DDR3_DQS0_P	23
IO_L3N_T0_DQS_33_K2	K2	PL_DDR3_DQS0_N	23
IO_L4P_T0_33_L3	L3	PL_DDR3_D5	23
IO_L4N_T0_33_L2	L2	PL_DDR3_D1	23
IO_L5P_T0_33_K5	K5	PL_DDR3_D2	23
IO_L5N_T0_33_J5	J5	PL_DDR3_D6	23
IO_L6P_T0_33_K6	K6	PL_DDR3_D7	23
IO_L6N_T0_VREF_33_J6	J6		
IO_L7P_T1_33_G2	G2	GPIO_LED_CENTER	38
IO_L7N_T1_33_F2	F2	PL_DDR3_DM1	23
IO_L8P_T1_33_H6	H6	PL_DDR3_D10	23
IO_L8N_T1_33_G6	G6	PL_DDR3_D8	23
IO_L9P_T1_DQS_33_J1	J1	PL_DDR3_DQS1_P	23
IO_L9N_T1_DQS_33_H1	H1	PL_DDR3_DQS1_N	23
IO_L10P_T1_33_H2	H2	PL_DDR3_D13	23
IO_L10N_T1_33_G1	G1	PL_DDR3_D12	23
IO_L11P_T1_SRCC_33_H4	H4	PL_DDR3_D9	23
IO_L11N_T1_SRCC_33_H3	H3	PL_DDR3_D11	23
IO_L12P_T1_MRCC_33_G5	G5	PL_DDR3_D14	23
IO_L12N_T1_MRCC_33_G4	G4	PL_DDR3_D15	23
IO_L13P_T2_MRCC_33_F5	F5	NC	
IO_L13N_T2_MRCC_33_E5	E5	PL_DDR3_D19	23
IO_L14P_T2_SRCC_33_F4	F4	PL_DDR3_D20	23
IO_L14N_T2_SRCC_33_F3	F3	PL_DDR3_D21	23
IO_L15P_T2_DQS_33_E6	E6	PL_DDR3_DQS2_P	23
IO_L15N_T2_DQS_33_D5	D5	PL_DDR3_DQS2_N	23
IO_L16P_T2_33_D4	D4	PL_DDR3_D18	23
IO_L16N_T2_33_D3	D3	PL_DDR3_D23	23
IO_L17P_T2_33_E3	E3	PL_DDR3_D17	23
IO_L17N_T2_33_E2	E2	PL_DDR3_D16	23
IO_L18P_T2_33_E1	E1	PL_DDR3_DM2	23
IO_L18N_T2_33_D1	D1	PL_DDR3_D22	23
IO_L19P_T3_33_C4	C4	PL_DDR3_D31	23
IO_L19N_T3_VREF_33_C3	C3		
IO_L20P_T3_33_B5	B5	PL_DDR3_D27	23
IO_L20N_T3_33_B4	B4	PL_DDR3_D26	23
IO_L21P_T3_DQS_33_A5	A5	PL_DDR3_DQS3_P	23
IO_L21N_T3_DQS_33_A4	A4	PL_DDR3_DQS3_N	23
IO_L22P_T3_33_C2	C2	PL_DDR3_DM3	23
IO_L22N_T3_33_C1	C1	PL_DDR3_D30	23
IO_L23P_T3_33_B2	B2	PL_DDR3_D25	23
IO_L23N_T3_33_B1	B1	PL_DDR3_D29	23
IO_L24P_T3_33_A3	A3	PL_DDR3_D28	23
IO_L24N_T3_33_A2	A2	PL_DDR3_D24	23
IO_25_VRP_33_L4	L4	VRP_33	6

VCC1V5_PL	B3	VCCO_33_B3
	E4	VCCO_33_E4
	F1	VCCO_33_F1
	H5	VCCO_33_H5
	J2	VCCO_33_J2
	L6	VCCO_33_L6

VTTVREF_SODIMM

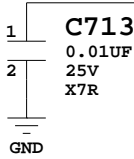


SOC_Z7_FF900_IRONWOOD

BANK 34
XC7Z045FF900

IO_0_VRN_34_M12	M12	NC	
IO_L1P_T0_34_B10	B10	PL_DDR3_A8	23
IO_L1N_T0_34_A10	A10	PL_DDR3_A13	23
IO_L2P_T0_34_B9	B9	PL_DDR3_A1	23
IO_L2N_T0_34_A9	A9	PL_DDR3_A3	23
IO_L3P_T0_DQS_PUDC_B_34_A8	A8	PL_CPU_RESET	38
IO_L3N_T0_DQS_34_A7	A7	PL_DDR3_BA2	23
IO_L4P_T0_34_C7	C7	PL_DDR3_CKE1	23
IO_L4N_T0_34_B7	B7	PL_DDR3_A11	23
IO_L5P_T0_34_C6	C6	PL_DDR3_A15	23
IO_L5N_T0_34_B6	B6	PL_DDR3_A5	23
IO_L6P_T0_34_C9	C9	PL_DDR3_ODT1	23
IO_L6N_T0_VREF_34_C8	C8		
IO_L7P_T1_34_J11	J11	PL_DDR3_S0_B	23
IO_L7N_T1_34_H11	H11	PL_DDR3_RAS_B	23
IO_L8P_T1_34_E11	E11	PL_DDR3_A2	23
IO_L8N_T1_34_D11	D11	PL_DDR3_A4	23
IO_L9P_T1_DQS_34_H12	H12	PL_DDR3_A12	23
IO_L9N_T1_DQS_34_G11	G11	PL_DDR3_A14	23
IO_L10P_T1_34_E10	E10	PL_DDR3_A0	23
IO_L10N_T1_34_D10	D10	PL_DDR3_CKE0	23
IO_L11P_T1_SRCC_34_G10	G10	PL_DDR3_CLK0_P	23
IO_L11N_T1_SRCC_34_F10	F10	PL_DDR3_CLK0_N	23
IO_L12P_T1_MRCC_34_D9	D9	PL_DDR3_CLK1_P	23
IO_L12N_T1_MRCC_34_D8	D8	PL_DDR3_CLK1_N	23
IO_L13P_T2_MRCC_34_H9	H9	SYSCLK_P	34
IO_L13N_T2_MRCC_34_G9	G9	SYSCLK_N	34
IO_L14P_T2_SRCC_34_F9	F9	PL_DDR3_A6	23
IO_L14N_T2_SRCC_34_E8	E8	PL_DDR3_A7	23
IO_L15P_T2_DQS_34_J8	J8	PL_DDR3_A9	23
IO_L15N_T2_DQS_34_H8	H8	PL_DDR3_S1_B	23
IO_L16P_T2_34_F8	F8	PL_DDR3_BA0	23
IO_L16N_T2_34_F7	F7	PL_DDR3_WE_B	23
IO_L17P_T2_34_E7	E7	PL_DDR3_CAS_B	23
IO_L17N_T2_34_D6	D6	PL_DDR3_A10	23
IO_L18P_T2_34_H7	H7	PL_DDR3_BA1	23
IO_L18N_T2_34_G7	G7	PL_DDR3_ODT0	23
IO_L19P_T3_34_L7	L7	PL_DDR3_D39	23
IO_L19N_T3_VREF_34_K7	K7		
IO_L20P_T3_34_J10	J10	PL_DDR3_D38	23
IO_L20N_T3_34_J9	J9	PL_DDR3_D35	23
IO_L21P_T3_DQS_34_L8	L8	PL_DDR3_DQS4_P	23
IO_L21N_T3_DQS_34_K8	K8	PL_DDR3_DQS4_N	23
IO_L22P_T3_34_K11	K11	PL_DDR3_D36	23
IO_L22N_T3_34_K10	K10	PL_DDR3_D32	23
IO_L23P_T3_34_L10	L10	PL_DDR3_D37	23
IO_L23N_T3_34_L9	L9	PL_DDR3_D33	23
IO_L24P_T3_34_L12	L12	PL_DDR3_DM4	23
IO_L24N_T3_34_K12	K12	PL_DDR3_D34	23
IO_25_VRP_34_M10	M10	PL_DDR3_TEMP_EVENT	23

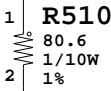
VTTVREF_SODIMM



VCC1V5_PL

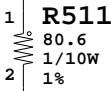
A6	VCCO_34_A6
C10	VCCO_34_C10
D7	VCCO_34_D7
F11	VCCO_34_F11
G8	VCCO_34_G8
J12	VCCO_34_J12
K9	VCCO_34_K9

VCC1V5_PL



VRN_33

VRP_33



Zynq Bank 33, 34



Title: Zynq Bank 33, 34 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 6 of 58	Drawn By BF	

SOC_Z7_FF900_IRONWOOD

BANK 35
XC7Z045FF900

IO_0_VRN_35_K16
IO_L1P_T0_AD0P_35_L15
IO_L1N_T0_AD0N_35_L14
IO_L2P_T0_AD8P_35_J13
IO_L2N_T0_AD8N_35_H13
IO_L3P_T0_DQS_AD1P_35_L13
IO_L3N_T0_DQS_AD1N_35_K13
IO_L4P_T0_35_J14
IO_L4N_T0_35_H14
IO_L5P_T0_AD9P_35_K15
IO_L5N_T0_AD9N_35_J15
IO_L6P_T0_35_J16
IO_L6N_T0_VREF_35_H16
IO_L7P_T1_AD2P_35_G17
IO_L7N_T1_AD2N_35_G16
IO_L8P_T1_AD10P_35_G15
IO_L8N_T1_AD10N_35_G14
IO_L9P_T1_DQS_AD3P_35_G12
IO_L9N_T1_DQS_AD3N_35_F12
IO_L10P_T1_AD11P_35_F13
IO_L10N_T1_AD11N_35_E12
IO_L11P_T1_SRCC_35_E13
IO_L11N_T1_SRCC_35_D13
IO_L12P_T1_MRCC_35_F15
IO_L12N_T1_MRCC_35_F14
IO_L13P_T2_MRCC_35_E16
IO_L13N_T2_MRCC_35_E15
IO_L14P_T2_AD4P_SRCC_35_D15
IO_L14N_T2_AD4N_SRCC_35_D14
IO_L15P_T2_DQS_AD12P_35_F17
IO_L15N_T2_DQS_AD12N_35_E17
IO_L16P_T2_35_D16
IO_L16N_T2_35_C16
IO_L17P_T2_AD5P_35_C17
IO_L17N_T2_AD5N_35_B16
IO_L18P_T2_AD13P_35_B17
IO_L18N_T2_AD13N_35_A17
IO_L19P_T3_35_C14
IO_L19N_T3_VREF_35_C13
IO_L20P_T3_AD6P_35_C12
IO_L20N_T3_AD6N_35_B12
IO_L21P_T3_DQS_AD14P_35_B15
IO_L21N_T3_DQS_AD14N_35_A15
IO_L22P_T3_AD7P_35_C11
IO_L22N_T3_AD7N_35_B11
IO_L23P_T3_35_B14
IO_L23N_T3_35_A14
IO_L24P_T3_AD15P_35_A13
IO_L24N_T3_AD15N_35_A12
IO_25_VRP_35_M16

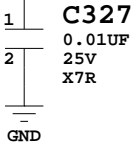
VCC1V5_PL

VCCO_35_A16
VCCO_35_B13
VCCO_35_D17
VCCO_35_E14
VCCO_35_H15
VCCO_35_L16

U1

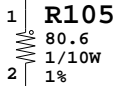
SOC_IRONWOOD_FF900

VTTVREF_SODIMM

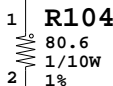


K16 VRN_35
L15 XADC_VAUX0P_R
L14 XADC_VAUX0N_R
J13 XADC_VAUX8P_R
H13 XADC_VAUX8N_R
L13 XADC_AD1_R_P
K13 XADC_AD1_R_N
J14 XADC_GPIO_3
H14 XADC_GPIO_0
K15 GPIO_SW_CENTER
J15 XADC_GPIO_1
J16 XADC_GPIO_2
H16
G17 PL_DDR3_RESET_B
G16 PL_DDR3_D43
G15 PL_DDR3_D44
G14 PL_DDR3_DM5
G12 PL_DDR3_DQS5_P
F12 PL_DDR3_DQS5_N
F13 PL_DDR3_D42
E12 PL_DDR3_D45
E13 PL_DDR3_D47
D13 PL_DDR3_D46
F15 PL_DDR3_D41
F14 PL_DDR3_D40
E16 PL_DDR3_D51
E15 PL_DDR3_D49
D15 PL_DDR3_D48
D14 PL_DDR3_D54
F17 PL_DDR3_DQS6_P
E17 PL_DDR3_DQS6_N
D16 PL_DDR3_D50
C16 PL_DDR3_DM6
C17 PL_DDR3_D52
B16 PL_DDR3_D53
B17 PL_DDR3_D55
A17 GPIO_LED_0
C14 PL_DDR3_D62
C13
C12 PL_DDR3_D57
B12 PL_DDR3_D56
B15 PL_DDR3_DQS7_P
A15 PL_DDR3_DQS7_N
C11 PL_DDR3_DM7
B11 PL_DDR3_D61
B14 PL_DDR3_D63
A14 PL_DDR3_D59
A13 PL_DDR3_D60
A12 PL_DDR3_D58
M16 VRP_35

VCC1V5_PL



VRN_35



VRP_35

GND

Zynq Bank 35



Title: Zynq Bank 35 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 7 of 58	Drawn By BF	

SOC_Z7_FF900_IRONWOOD

BANK 109
XC7Z045FF900

MGTXTXP0_109_AK10	
MGTXTXN0_109_AK9	
MGTXRXN0_109_AH10	
MGTXRXN0_109_AH9	
MGTXTXP1_109_AK6	
MGTXTXN1_109_AK5	
MGTXRXN1_109_AJ8	
MGTXRXN1_109_AJ7	
MGTXTXP2_109_AJ4	
MGTXTXN2_109_AJ3	
MGTXRXN2_109_AJ2	
MGTXTXP3_109_AK2	
MGTXTXN3_109_AK1	
MGTXRXN3_109_AE8	
MGTXRXN3_109_AE7	
MGTREFCLK0P_109_AD10	
MGTREFCLK0N_109_AD9	
MGTREFCLK1P_109_AF10	
MGTREFCLK1N_109_AF9	

AK10	FMC HPC DP0 C2M P	24
AK9	FMC HPC DP0 C2M N	24
AH10	FMC HPC DP0 M2C P	24
AH9	FMC HPC DP0 M2C N	24
AK6	FMC HPC DP1 C2M P	24
AK5	FMC HPC DP1 C2M N	24
AJ8	FMC HPC DP1 M2C P	24
AJ7	FMC HPC DP1 M2C N	24
AJ4	FMC HPC DP2 C2M P	24
AJ3	FMC HPC DP2 C2M N	24
AG8	FMC HPC DP2 M2C P	24
AG7	FMC HPC DP2 M2C N	24
AK2	FMC HPC DP3 C2M P	24
AK1	FMC HPC DP3 C2M N	24
AE8	FMC HPC DP3 M2C P	24
AE7	FMC HPC DP3 M2C N	24
AD10	FMC HPC GBTCLK0 M2C P	24
AD9	FMC HPC GBTCLK0 M2C N	24
AF10	NC	
AF9	NC	

U1

SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

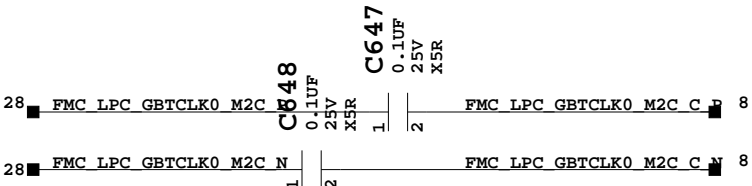
BANK 110
XC7Z045FF900

MGTXTXP0_110_AH2	
MGTXTXN0_110_AH1	
MGTXRXN0_110_AH6	
MGTXRXN0_110_AH5	
MGTXTXP1_110_AF2	
MGTXTXN1_110_AF1	
MGTXRXN1_110_AG4	
MGTXRXN1_110_AG3	
MGTXTXP2_110_AE4	
MGTXTXN2_110_AE3	
MGTXRXN2_110_AF6	
MGTXRXN2_110_AF5	
MGTXTXP3_110_AD2	
MGTXTXN3_110_AD1	
MGTXRXN3_110_AD6	
MGTXRXN3_110_AD5	
MGTREFCLK0P_110_AA8	
MGTREFCLK0N_110_AA7	
MGTREFCLK1P_110_AC8	
MGTREFCLK1N_110_AC7	

AH2	FMC HPC DP4 C2M P	24
AH1	FMC HPC DP4 C2M N	24
AH6	FMC HPC DP4 M2C P	24
AH5	FMC HPC DP4 M2C N	24
AF2	FMC HPC DP5 C2M P	24
AF1	FMC HPC DP5 C2M N	24
AG4	FMC HPC DP5 M2C P	24
AG3	FMC HPC DP5 M2C N	24
AE4	FMC HPC DP6 C2M P	24
AE3	FMC HPC DP6 C2M N	24
AF6	FMC HPC DP6 M2C P	24
AF5	FMC HPC DP6 M2C N	24
AD2	FMC HPC DP7 C2M P	24
AD1	FMC HPC DP7 C2M N	24
AD6	FMC HPC DP7 M2C P	24
AD5	FMC HPC DP7 M2C N	24
AA8	FMC HPC GBTCLK1 M2C P	24
AA7	FMC HPC GBTCLK1 M2C N	24
AC8	SI5324_OUT_C_P	43
AC7	SI5324_OUT_C_N	43

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SOC_IRONWOOD_FF900

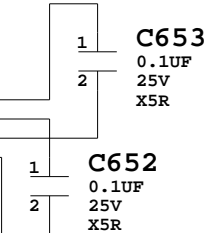


SOC_Z7_FF900_IRONWOOD

BANK 111
XC7Z045FF900

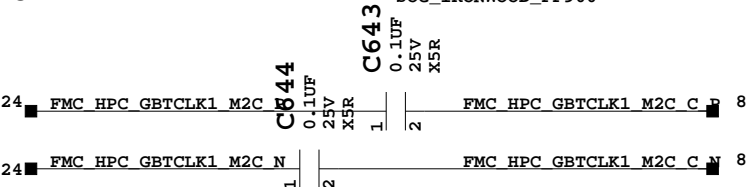
MGTXTXP0_111_AB2	
MGTXTXN0_111_AB1	
MGTXRXN0_111_AC4	
MGTXRXN0_111_AC3	
MGTXTXP1_111_Y2	
MGTXTXN1_111_Y1	
MGTXRXN1_111_AB6	
MGTXRXN1_111_AB5	
MGTXTXP2_111_W4	
MGTXTXN2_111_W3	
MGTXRXN2_111_Y6	
MGTXRXN2_111_Y5	
MGTXTXP3_111_V2	
MGTXTXN3_111_V1	
MGTXRXN3_111_AA4	
MGTXRXN3_111_AA3	
MGTREFCLK0P_111_U8	
MGTREFCLK0N_111_U7	
MGTREFCLK1P_111_W8	
MGTREFCLK1N_111_W7	

AB2	FMC LPC DP0 C2M P	28
AB1	FMC LPC DP0 C2M N	28
AC4	FMC LPC DP0 M2C P	28
AC3	FMC LPC DP0 M2C N	28
Y2	SMA MGT TX P	
Y1	SMA MGT TX N	
AB6	SMA MGT RX P	
AB5	SMA MGT RX N	
W4	SFP TX P	
W3	SFP TX N	
Y6	SFP RX P	
Y5	SFP RX N	
V2		
V1		
AA4		
AA3		
U8	FMC LPC GBTCLK0 M2C C_P	8
U7	FMC LPC GBTCLK0 M2C C_N	8
W8	SMA MGT REFCLK P	
W7	SMA MGT REFCLK N	



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SOC_IRONWOOD_FF900

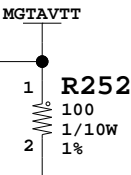


SOC_Z7_FF900_IRONWOOD

BANK 112
XC7Z045FF900

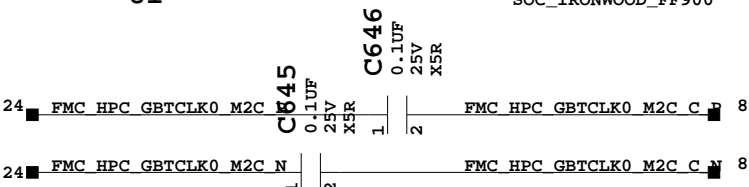
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MGTXTXN0_112_T1	
MGTXRXN0_112_V6	
MGTXRXN0_112_V5	
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MGTXTXN1_112_R3	
MGTXRXN1_112_U4	
MGTXRXN1_112_U3	
MGTXTXP2_112_P2	
MGTXTXN2_112_P1	
MGTXRXN2_112_T6	
MGTXRXN2_112_T5	
MGTXTXP3_112_N4	
MGTXTXN3_112_N3	
MGTXRXN3_112_P6	
MGTXRXN3_112_P5	
MGTREFCLK0P_112_N8	
MGTREFCLK0N_112_N7	
MGTREFCLK1P_112_R8	
MGTREFCLK1N_112_R7	
MGTAVTTRCAL_112_AB10	
MGTTRREF_112_AB9	

T2	PCIE TX3 P	42
T1	PCIE TX3 N	42
V6	PCIE RX3 P	42
V5	PCIE RX3 N	42
R4	PCIE TX2 P	42
R3	PCIE TX2 N	42
U4	PCIE RX2 P	42
U3	PCIE RX2 N	42
P2	PCIE TX1 P	42
P1	PCIE TX1 N	42
T6	PCIE RX1 P	42
T5	PCIE RX1 N	42
N4	PCIE TX0 P	42
N3	PCIE TX0 N	42
P6	PCIE RX0 P	42
P5	PCIE RX0 N	42
N8	PCIE CLK_Q0_P	42
N7	PCIE_CLK_Q0_N	42
R8	NC	
R7	NC	
AB10		
AB9		



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SOC_IRONWOOD_FF900



Zynq MGT Banks



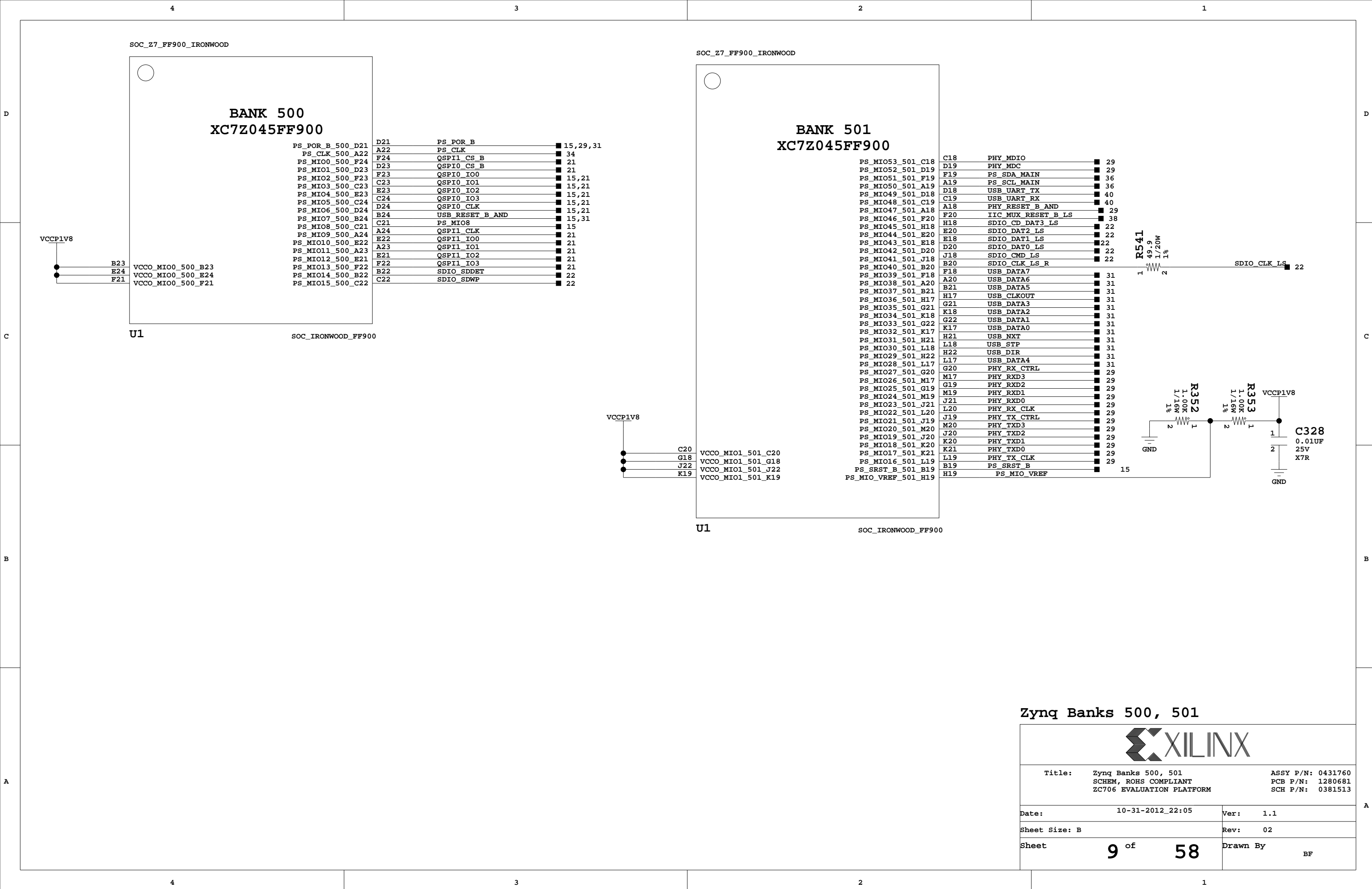
Title: Zynq MGT Banks
SCHEM, ROHS COMPLIANT
ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

Date: 10-31-2012_22:05 Ver: 1.1

Sheet Size: B Rev: 02

Sheet 8 of 58 Drawn By BF



SOC_Z7_FF900_IRONWOOD

BANK 502
XC7Z045FF900

PS_DDR_DRST_B_502_F25	F25	PS_DDR3_RESET_B		17,18,19,20
PS_DDR_DQ1_502_E25	E25	PS_DDR3_DQ3		17
PS_DDR_DQ0_502_A25	A25	PS_DDR3_DQ1		17
PS_DDR_DQ3_502_D25	D25	PS_DDR3_DQ6		17
PS_DDR_DQ2_502_B27	B27	PS_DDR3_DQ7		17
PS_DDR_DM0_502_C27	C27	PS_DDR3_DM0		17
PS_DDR_DQS_N0_502_B26	B26	PS_DDR3_DQS0_N		17
PS_DDR_DQS_P0_502_C26	C26	PS_DDR3_DQS0_P		17
PS_DDR_DQ5_502_E26	E26	PS_DDR3_DQ0		17
PS_DDR_DQ4_502_B25	B25	PS_DDR3_DQ5		17
PS_DDR_DQ7_502_E27	E27	PS_DDR3_DQ2		17
PS_DDR_DQ6_502_D26	D26	PS_DDR3_DQ4		17
PS_DDR_DQ9_502_A27	A27	PS_DDR3_DQ8		18
PS_DDR_DQ8_502_A29	A29	PS_DDR3_DQ10		18
PS_DDR_DQ11_502_A28	A28	PS_DDR3_DQ9		18
PS_DDR_DQ10_502_A30	A30	PS_DDR3_DQ13		18
PS_DDR_DM1_502_B30	B30	PS_DDR3_DM1		18
PS_DDR_DQS_N1_502_B29	B29	PS_DDR3_DQS1_N		18
PS_DDR_DQS_P1_502_C29	C29	PS_DDR3_DQS1_P		18
PS_DDR_DQ13_502_D30	D30	PS_DDR3_DQ12		18
PS_DDR_DQ12_502_C28	C28	PS_DDR3_DQ11		18
PS_DDR_DQ15_502_D29	D29	PS_DDR3_DQ14		18
PS_DDR_DQ14_502_D28	D28	PS_DDR3_DQ15		18
PS_DDR_A13_502_H23	H23	PS_DDR3_A13		17,18,19,20
PS_DDR_A14_502_J24	J24	PS_DDR3_A14		17,18,19,20
PS_DDR_A11_502_H24	H24	PS_DDR3_A11		17,18,19,20
PS_DDR_A12_502_K23	K23	PS_DDR3_A12		17,18,19,20
PS_DDR_A9_502_J23	J23	PS_DDR3_A9		17,18,19,20
PS_DDR_A10_502_G26	G26	PS_DDR3_A10		17,18,19,20
PS_DDR_A7_502_K22	K22	PS_DDR3_A7		17,18,19,20
PS_DDR_A8_502_F27	F27	PS_DDR3_A8		17,18,19,20
PS_DDR_A5_502_G24	G24	PS_DDR3_A5		17,18,19,20
PS_DDR_A6_502_H26	H26	PS_DDR3_A6		17,18,19,20
PS_DDR_A3_502_G25	G25	PS_DDR3_A3		17,18,19,20
PS_DDR_A4_502_J26	J26	PS_DDR3_A4		17,18,19,20
PS_DDR_VRP_502_M21	M21	PS_VRP	10	
PS_DDR_VRN_502_N21	N21	PS_VRN	10	
PS_DDR_CKP_502_K25	K25	PS_DDR3_CLK_P		17,18,19,20
PS_DDR_CKN_502_J25	J25	PS_DDR3_CLK_N		17,18,19,20
PS_DDR_A2_502_L27	L27	PS_DDR3_A2		17,18,19,20
PS_DDR_A1_502_K26	K26	PS_DDR3_A1		17,18,19,20
PS_DDR_A0_502_L25	L25	PS_DDR3_A0		17,18,19,20
PS_DDR_BA2_502_M25	M25	PS_DDR3_BA2		17,18,19,20
PS_DDR_BA1_502_M26	M26	PS_DDR3_BA1		17,18,19,20
PS_DDR_BA0_502_M27	M27	PS_DDR3_BA0		17,18,19,20
PS_DDR_ODT_502_L23	L23	PS_DDR3_ODT		17,18,19,20
PS_DDR_CS_B_502_N22	N22	PS_DDR3_CS_B		17,18,19,20
PS_DDR_CKE_502_M22	M22	PS_DDR3_CKE		17,18,19,20
PS_DDR_WE_B_502_N23	N23	PS_DDR3_WE_B		17,18,19,20
PS_DDR_CAS_B_502_M24	M24	PS_DDR3_CAS_B		17,18,19,20
PS_DDR_RAS_B_502_N24	N24	PS_DDR3_RAS_B		17,18,19,20
PS_DDR_DQ16_502_H27	H27	PS_DDR3_DQ16		19
PS_DDR_DQ17_502_G27	G27	PS_DDR3_DQ17		19
PS_DDR_DQ18_502_H28	H28	PS_DDR3_DQ18		19
PS_DDR_DQ19_502_E28	E28	PS_DDR3_DQ19		19
PS_DDR_DM2_502_H29	H29	PS_DDR3_DM2		19
PS_DDR_DQS_P2_502_G29	G29	PS_DDR3_DQS2_P		19
PS_DDR_DQS_N2_502_F29	F29	PS_DDR3_DQS2_N		19
PS_DDR_DQ20_502_E30	E30	PS_DDR3_DQ20		19
PS_DDR_DQ21_502_F28	F28	PS_DDR3_DQ21		19
PS_DDR_DQ22_502_G30	G30	PS_DDR3_DQ22		19
PS_DDR_DQ23_502_F30	F30	PS_DDR3_DQ23		19
PS_DDR_DQ24_502_J29	J29	PS_DDR3_DQ27		20
PS_DDR_DQ25_502_K27	K27	PS_DDR3_DQ24		20
PS_DDR_DQ26_502_J30	J30	PS_DDR3_DQ25		20
PS_DDR_DQ27_502_J28	J28	PS_DDR3_DQ26		20
PS_DDR_DM3_502_K28	K28	PS_DDR3_DM3		20
PS_DDR_DQS_P3_502_L28	L28	PS_DDR3_DQS3_P		20
PS_DDR_DQS_N3_502_L29	L29	PS_DDR3_DQS3_N		20
PS_DDR_DQ28_502_K30	K30	PS_DDR3_DQ28		20
PS_DDR_DQ29_502_M29	M29	PS_DDR3_DQ29		20
PS_DDR_DQ30_502_L30	L30	PS_DDR3_DQ30		20
PS_DDR_DQ31_502_M30	M30	PS_DDR3_DQ31		20
PS_DDR_VREF0_502_L22	L22			
PS_DDR_VREF1_502_L24	L24			

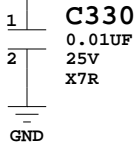
VCC1V5_PS

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C30	VCCO_DDR_502_C30
D27	VCCO_DDR_502_D27
G28	VCCO_DDR_502_G28
H25	VCCO_DDR_502_H25
K29	VCCO_DDR_502_K29
L26	VCCO_DDR_502_L26
M23	VCCO_DDR_502_M23

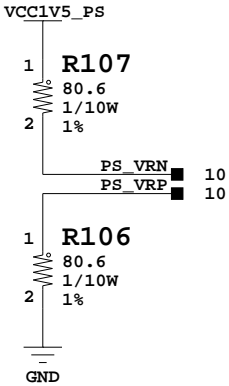
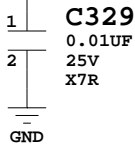
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SOC_IRONWOOD_FF900

VTTVREF_PS



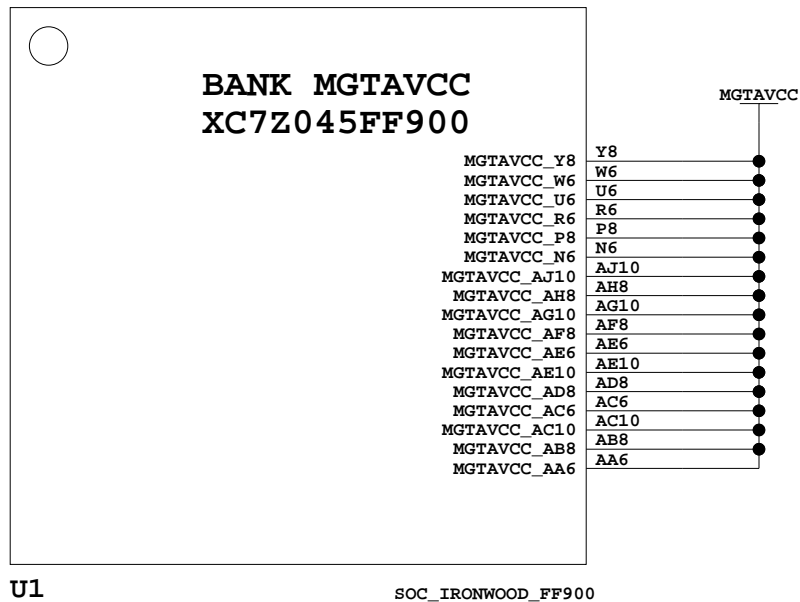
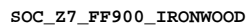
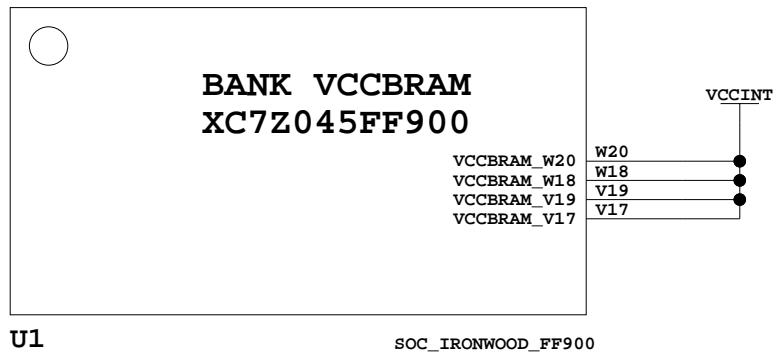
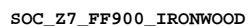
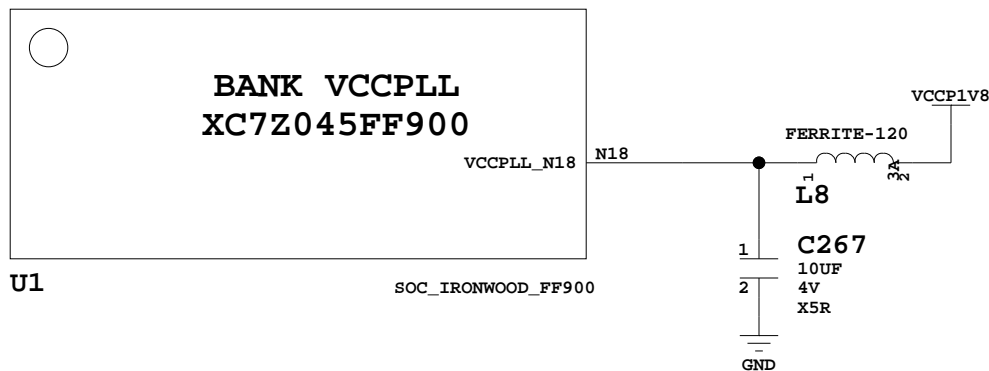
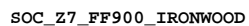
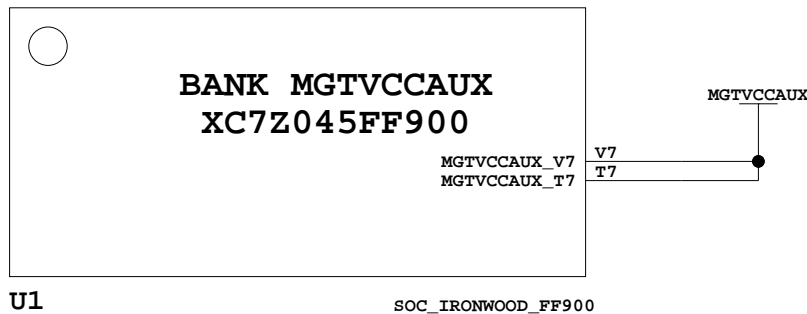
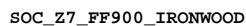
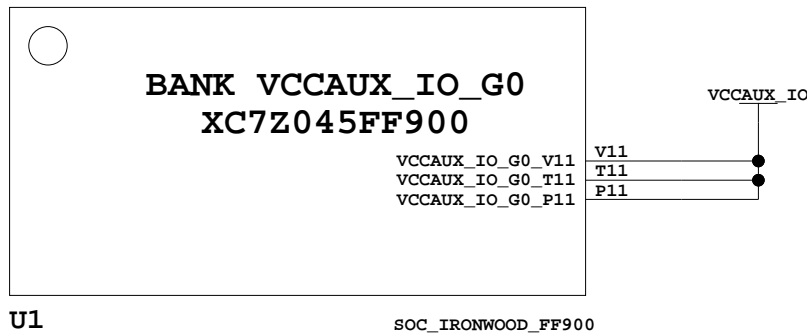
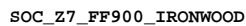
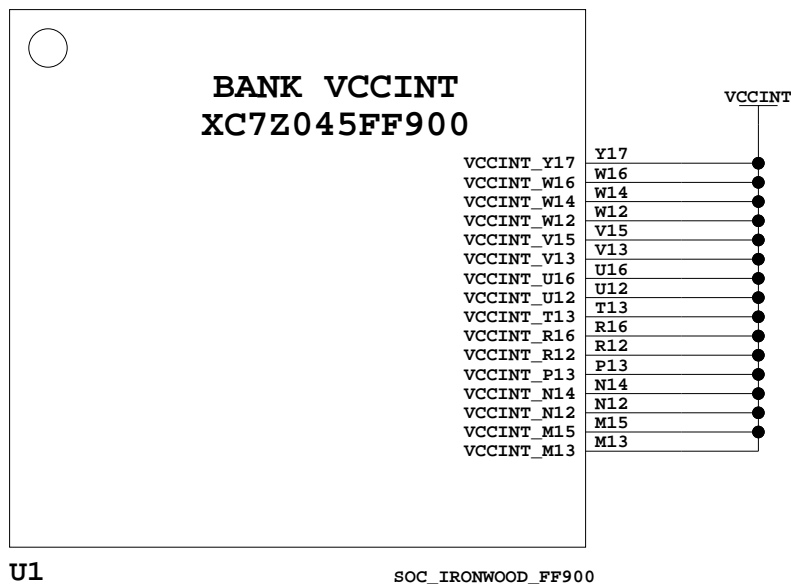
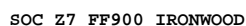
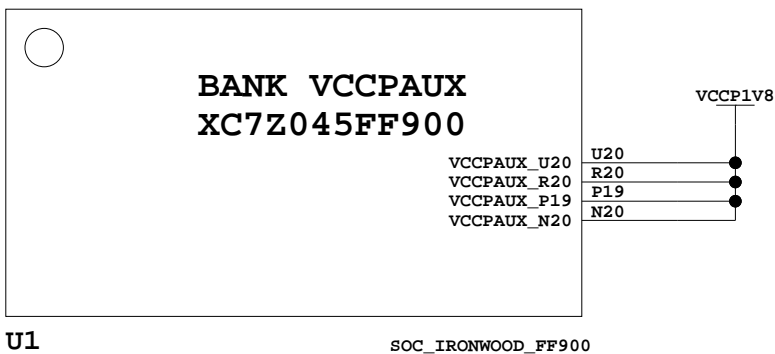
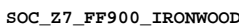
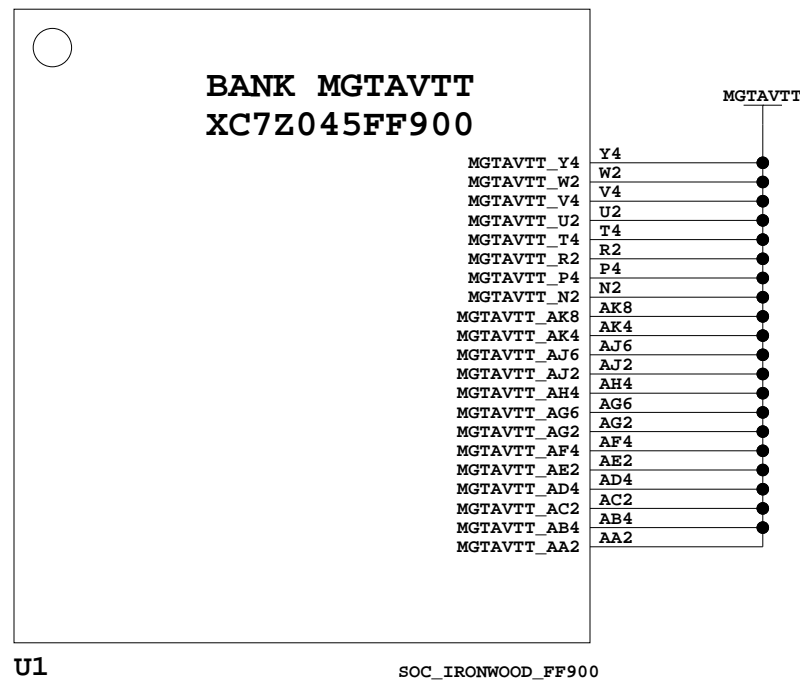
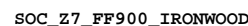
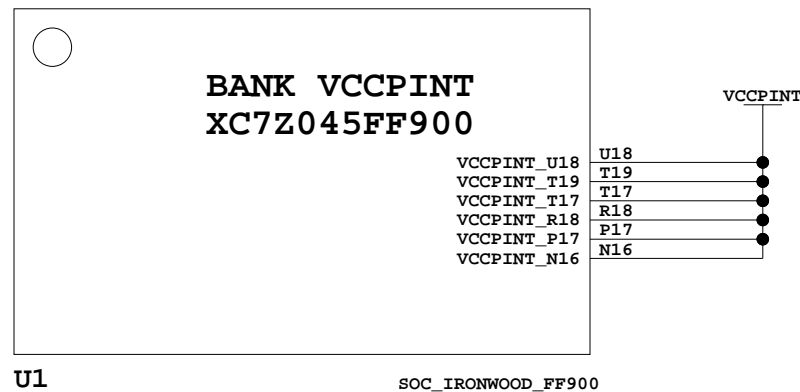
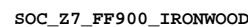
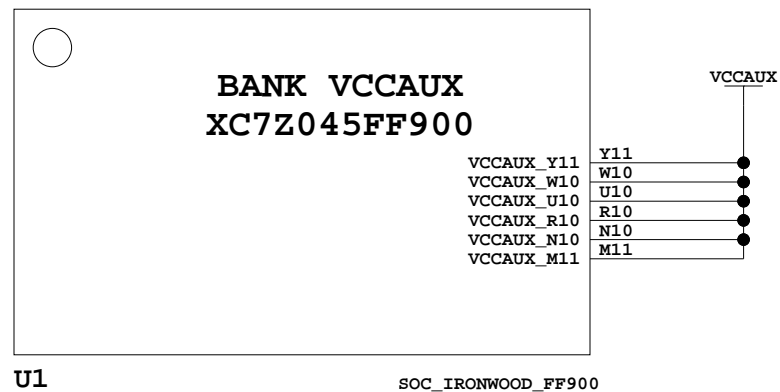
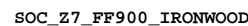
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Zynq Bank 502



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Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 10 of 58	Drawn By BF	



Zynq Power Pins



Title:		Zynq Power Pins SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date:	10-31-2012_22:05		Ver: 1.1
Sheet Size:	B		Rev: 02
Sheet	11 of 58	Drawn By BF	



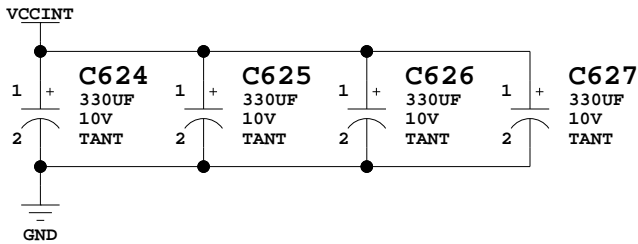
Zynq GND



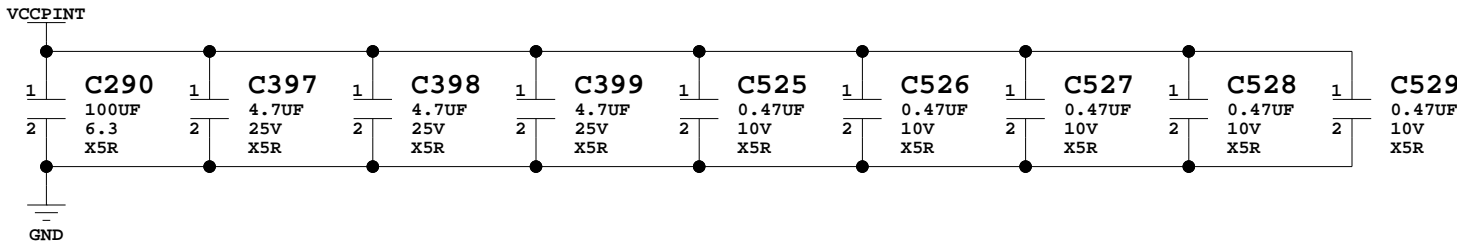
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Date: 10-31-2012_22:05		Ver: 1.1	
Sheet Size: B		Rev: 02	
Sheet 12 of 58		Drawn By BF	

BYPASS CAPACITORS

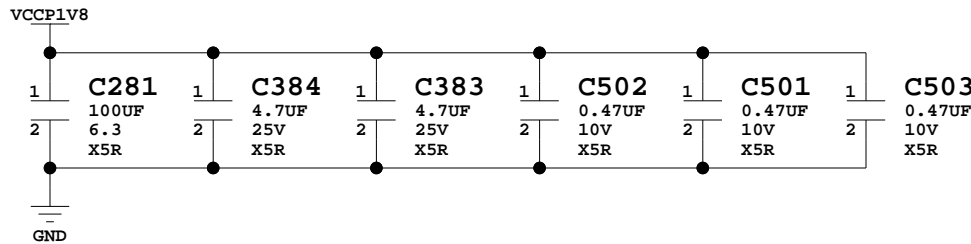
VCCINT 330uF (4)



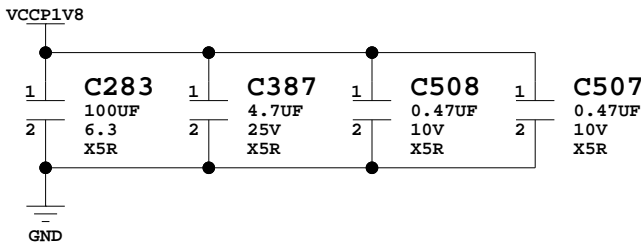
VCCPINT 100uF (1), 4.7uF (3), 0.47uF (5)



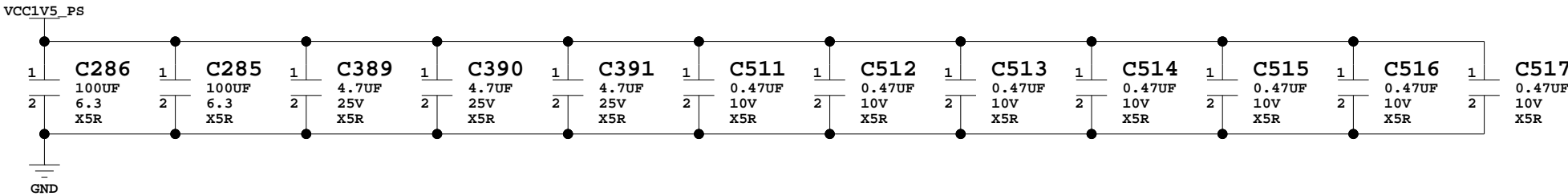
VCCPAUX 100uF (1), 4.7uF (2), 0.47uF (3)



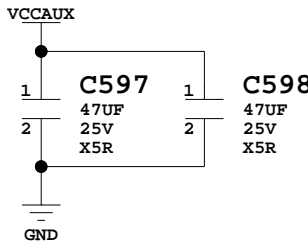
VCC0 PS 100uF (1), 4.7uF (1), 0.47uF (2)



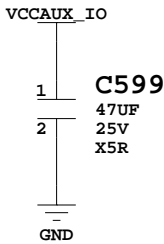
VCC1V5_PS 100uF (2), 4.7uF (3), 0.47uF (7)



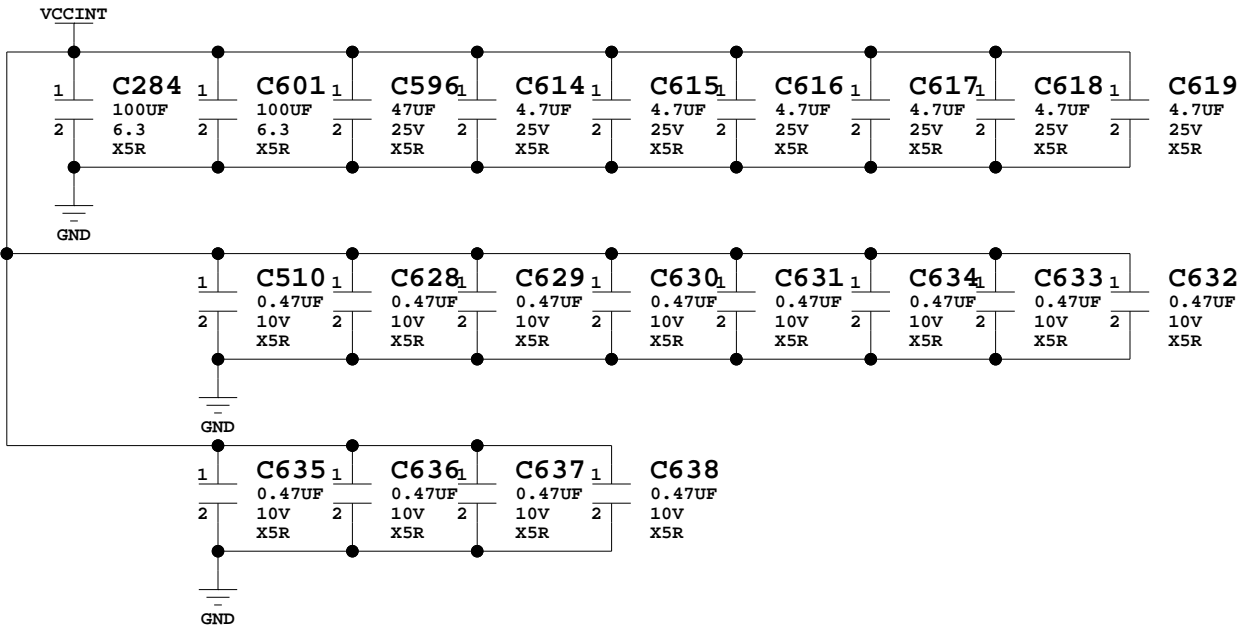
VCCAUX 47uF (2)



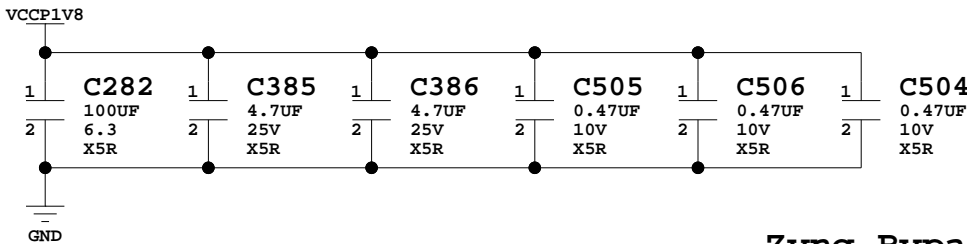
VCCAUX_IO 47uF (1)



VCCBRAM 100uF (2), 47uF (1), 4.7uF (6), 0.47uF (12)



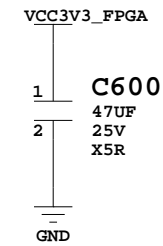
VCCO P1 100uF (1), 4.7uF (2), 0.47uF (3)



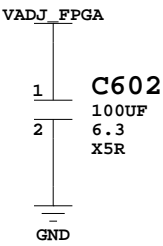
Zynq Bypass Capacitors Page 1

Title: Zynq Bypass Capacitors Page 1 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	13 of 58	Drawn By	BF

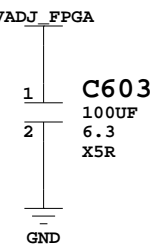
Bank 0 VCC3V3 100uF (1)



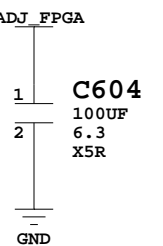
Bank 9 VADJ_FPGA 100uF (1)



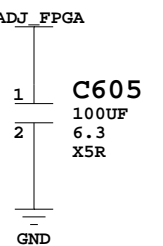
Bank 10 VADJ_FPGA 100uF (1)



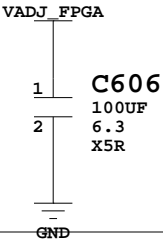
Bank 11 VADJ_FPGA 100uF (1)



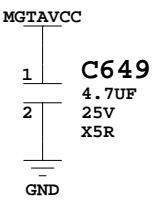
Bank 12 VADJ_FPGA 100uF (1)



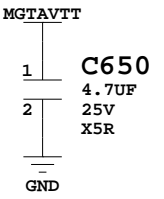
Bank 13 VADJ_FPGA 100uF (1)



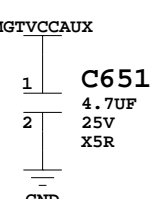
MGTAVCC 4.7uF (1)



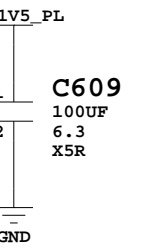
MGTAVTT 4.7uF (1)



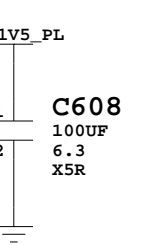
MGTVCCAUX 4.7uF (1)



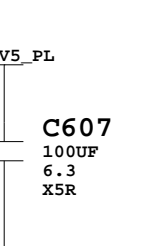
Bank 33 VCC1V5_PL 100uF (1)




Bank 34 VCC1V5_PL 100uF (1)

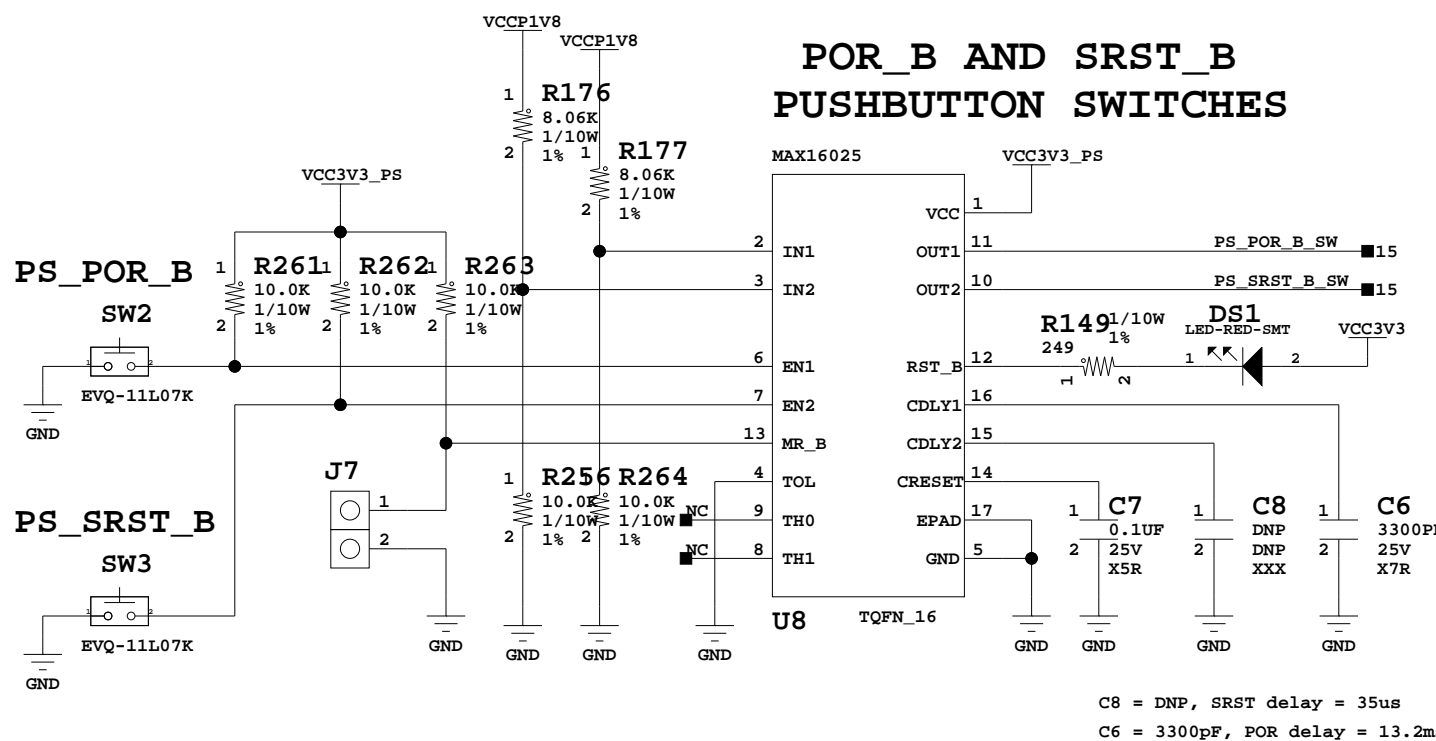


Bank 35 VCC1V5_PL 100uF (1)



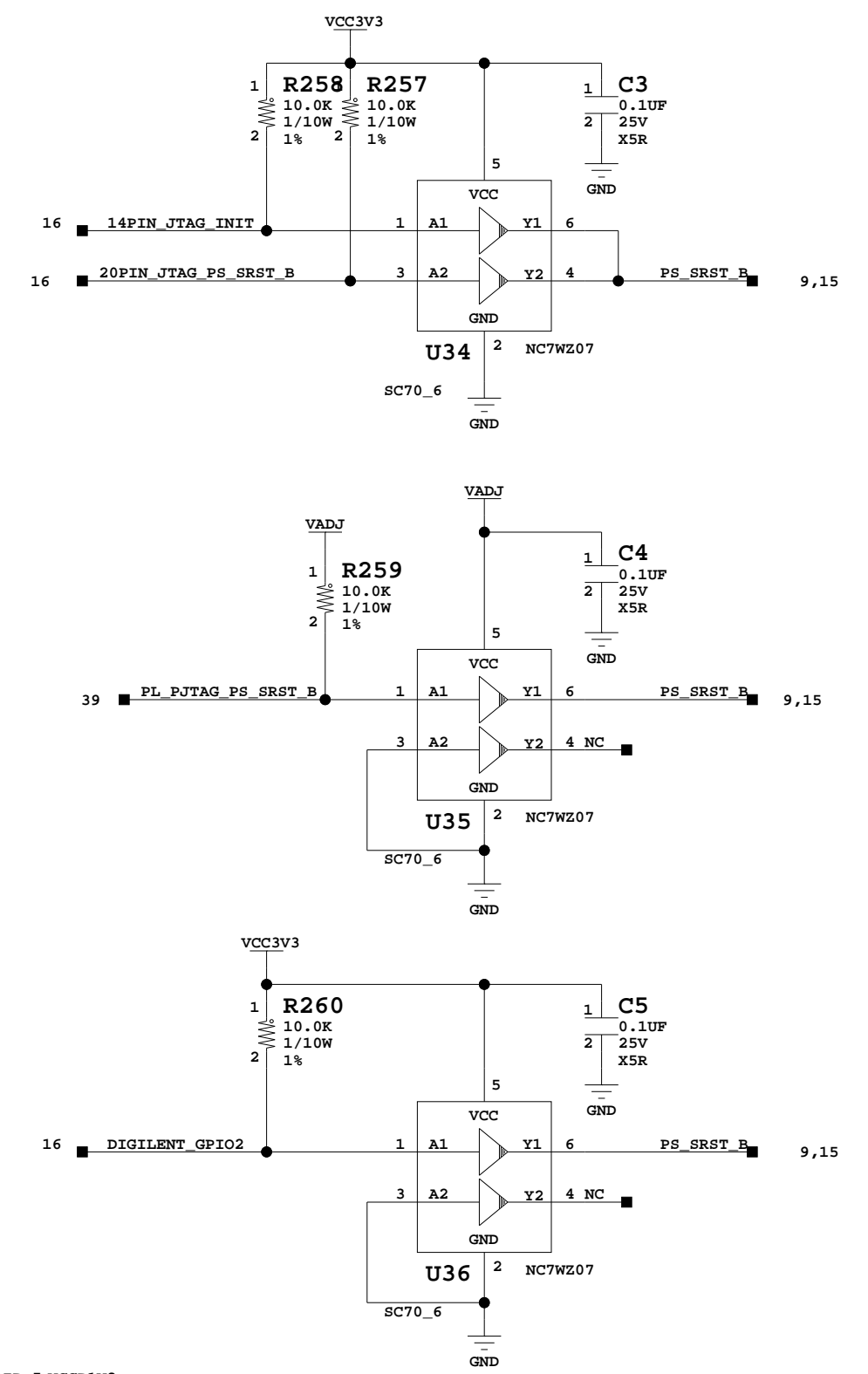
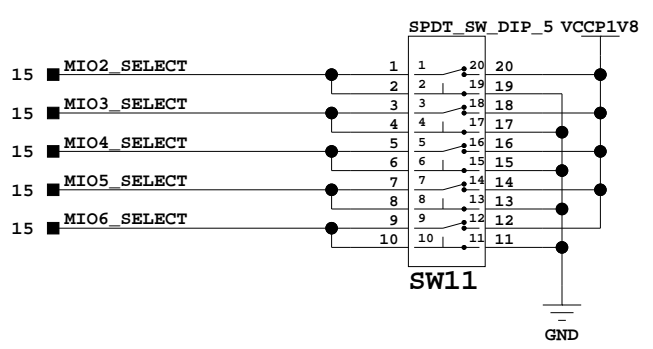
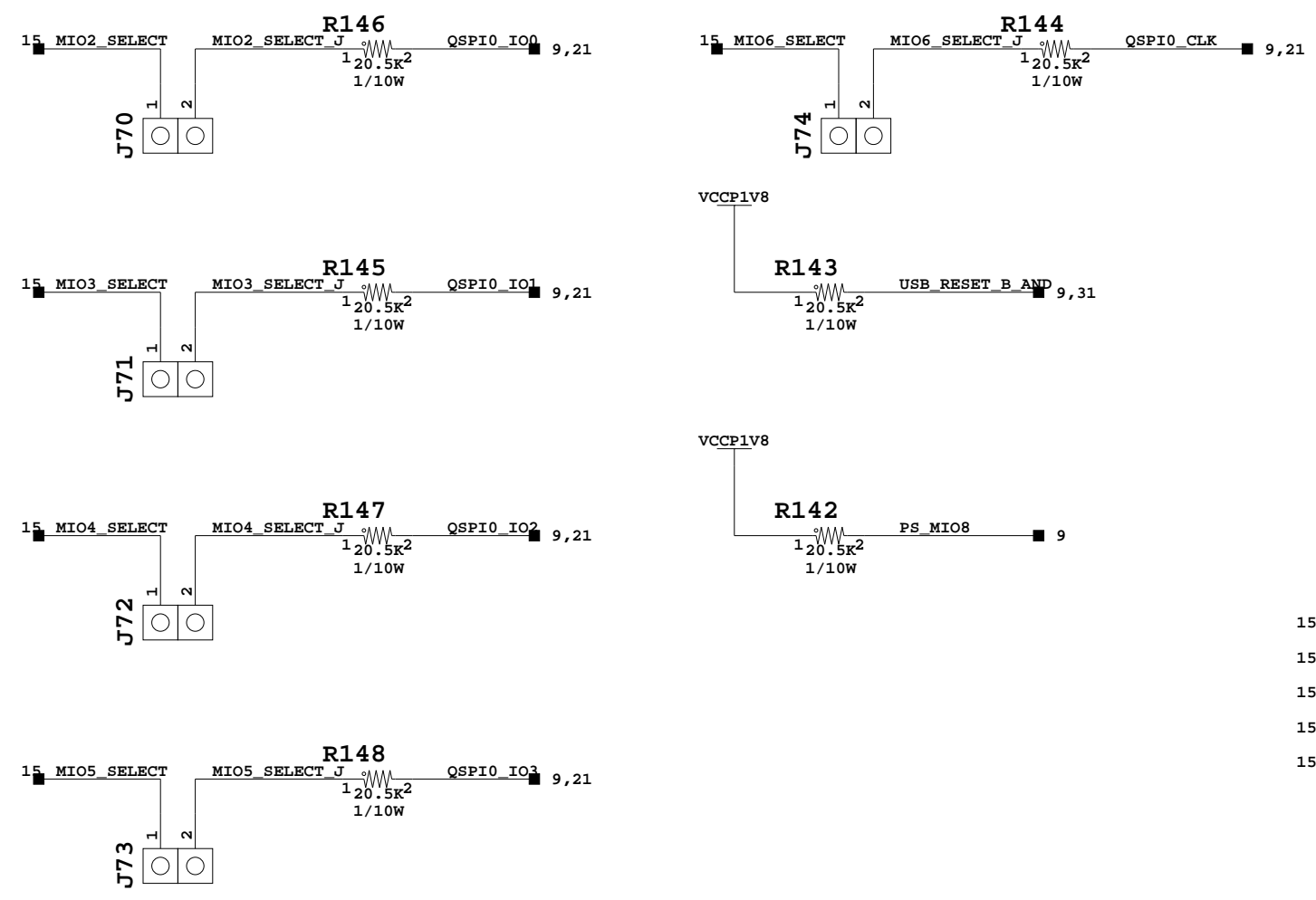
Zynq Bypass Capacitors Page 2

			
Title:		Zynq Bypass Capacitors Page 2	
		SCHEM, ROHS COMPLIANT	
		ZC706 EVALUATION PLATFORM	
		ASSY P/N: 0431760	
		PCB P/N: 1280681	
		SCH P/N: 0381513	
Date:		10-31-2012_22:05	
		Ver: 1.1	
Sheet Size: B		Rev: 02	
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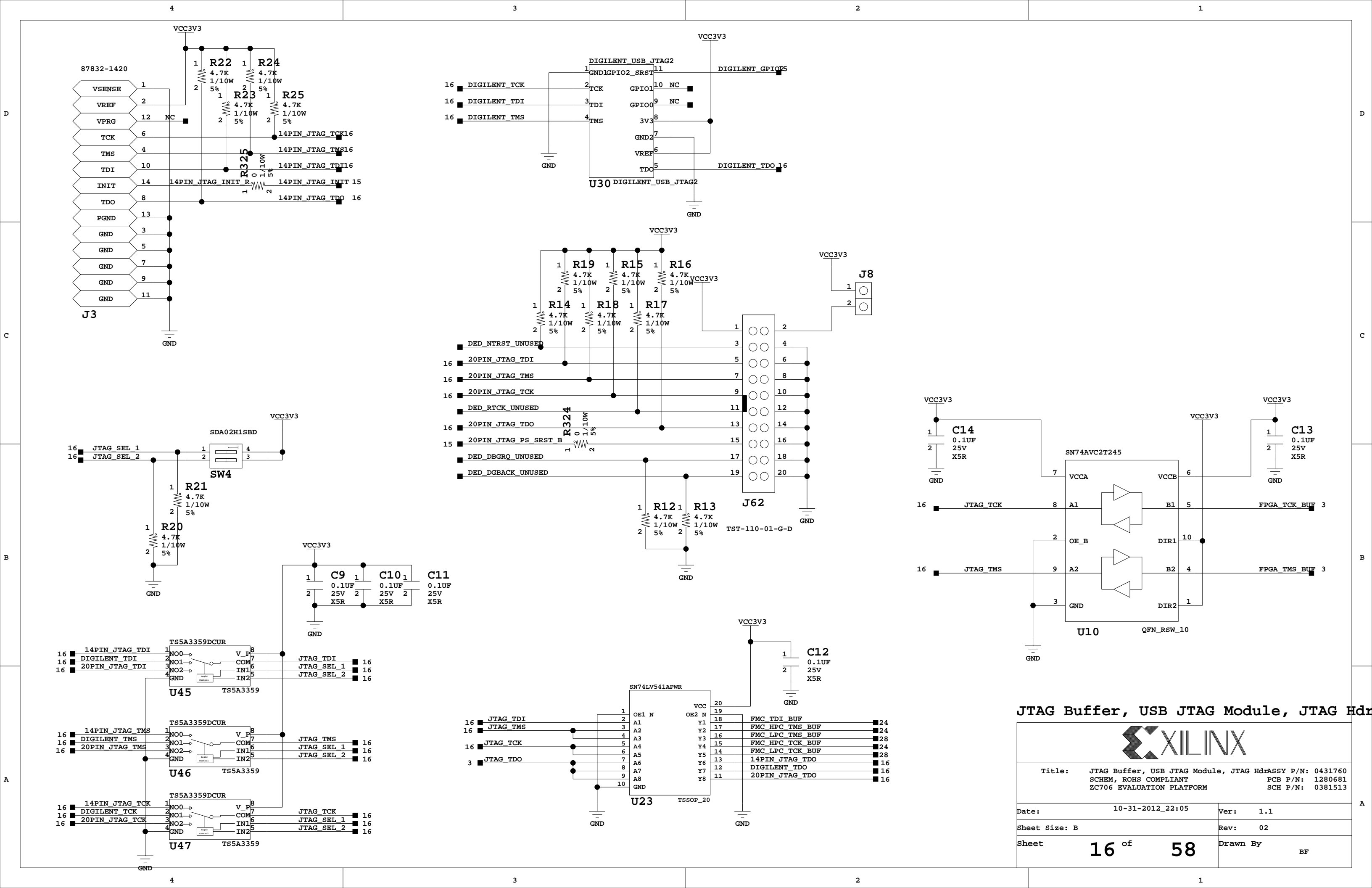
MIO[8:2] SELECTION HEADERS

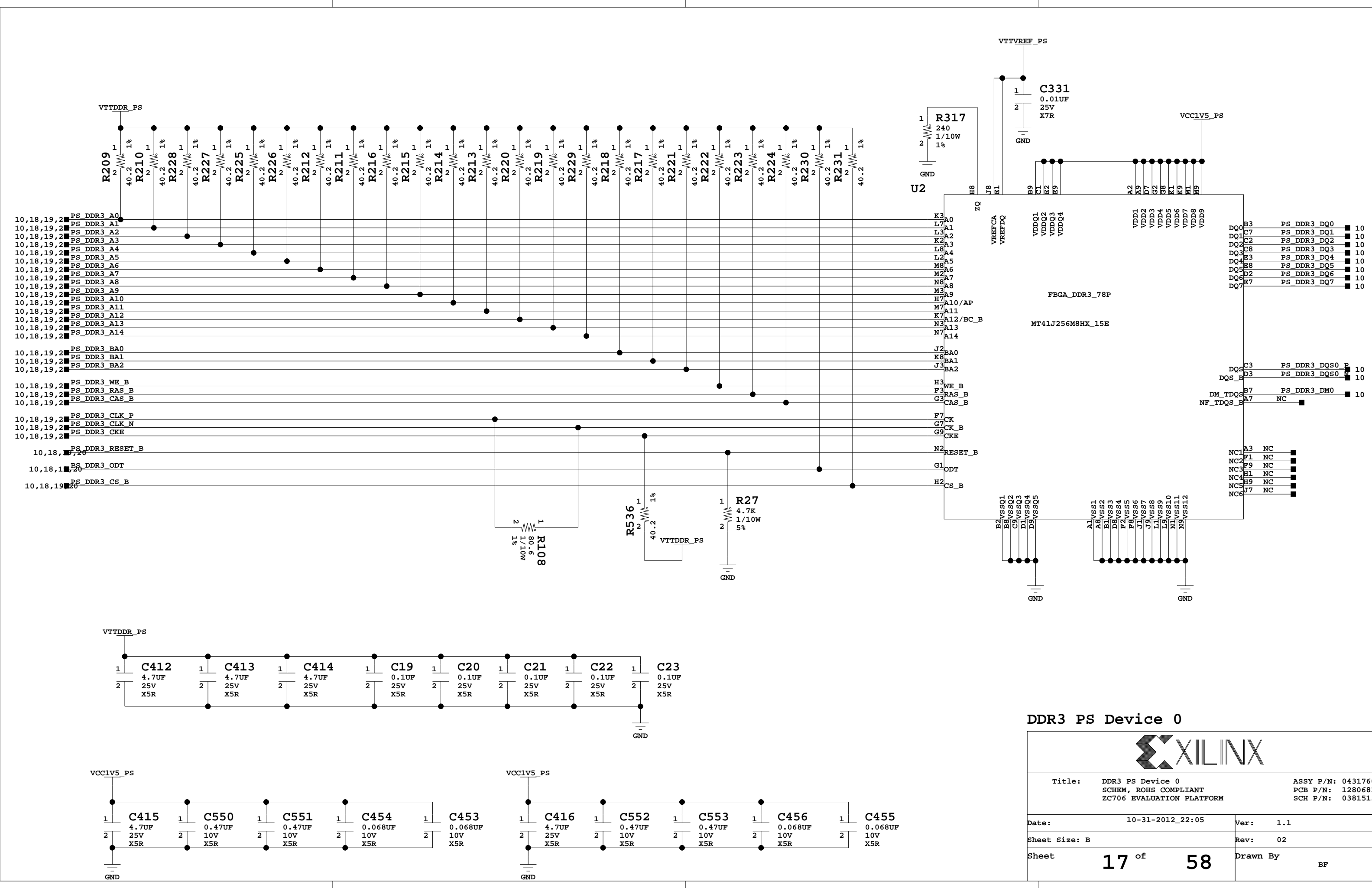
20.5K resistors must be placed near middle of QSPI traces



Power Supervisor, Zynq Config Pins, ResetASSY

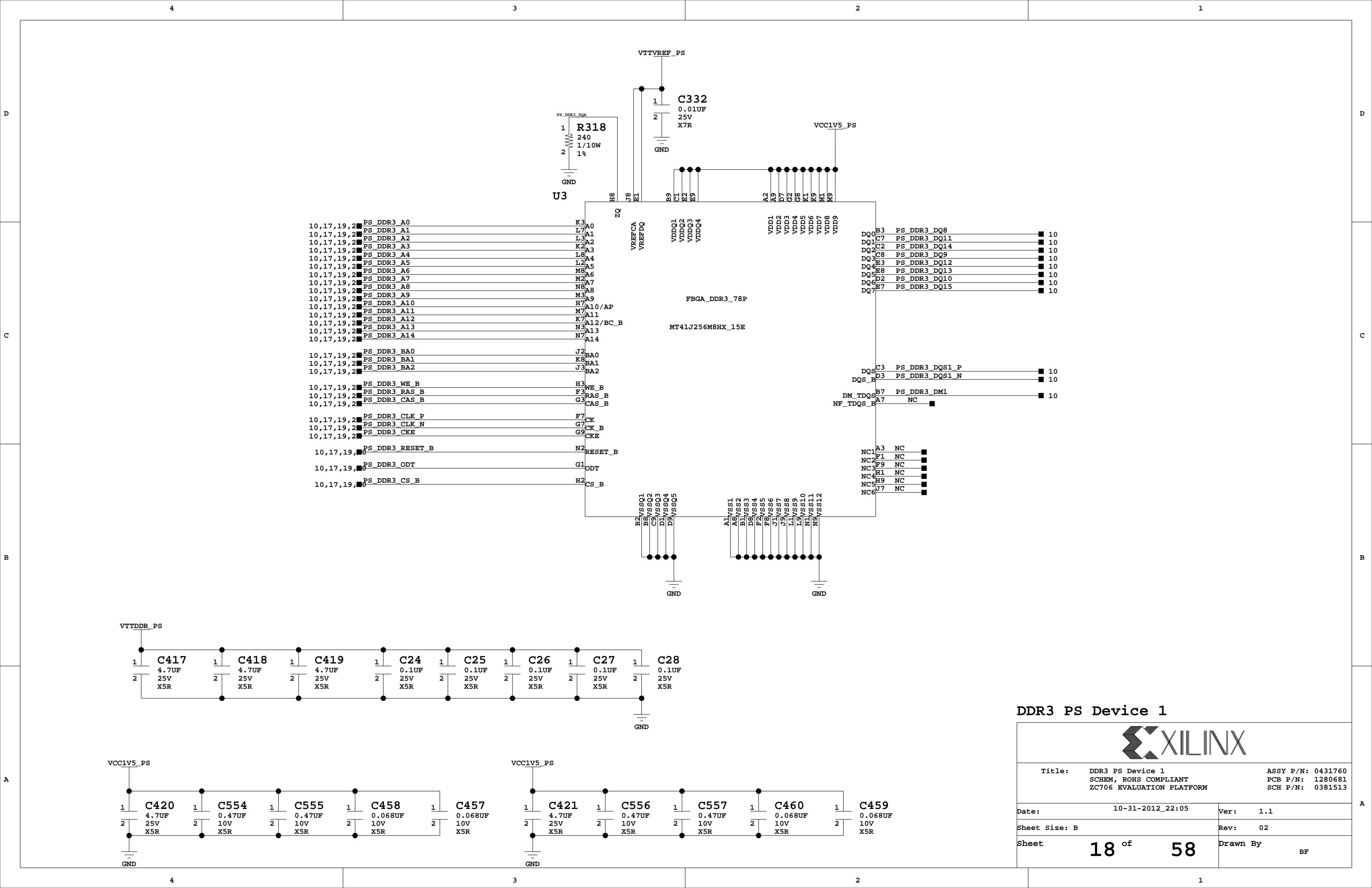
Title: Power Supervisor, Zynq Config Pins, ResetASSY P/N: 0431760 SCHEM, ROHS COMPLIANT PCB P/N: 1280681 ZC706 EVALUATION PLATFORM SCH P/N: 0381513	
Date: 11-1-2012_18:19	Ver: 1.1
Sheet Size: B	Rev: 02
Sheet 15 of 58	Drawn By BF

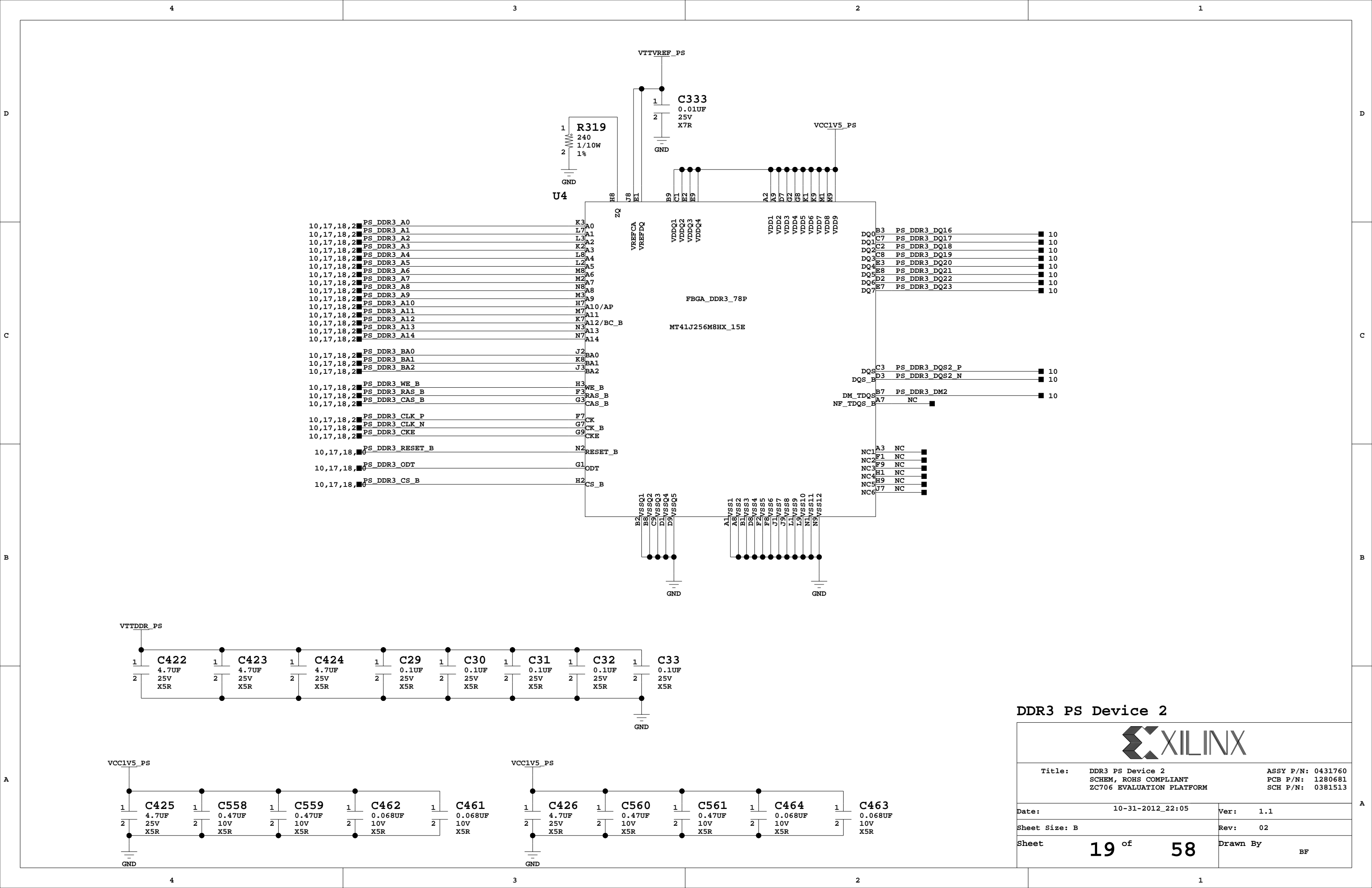


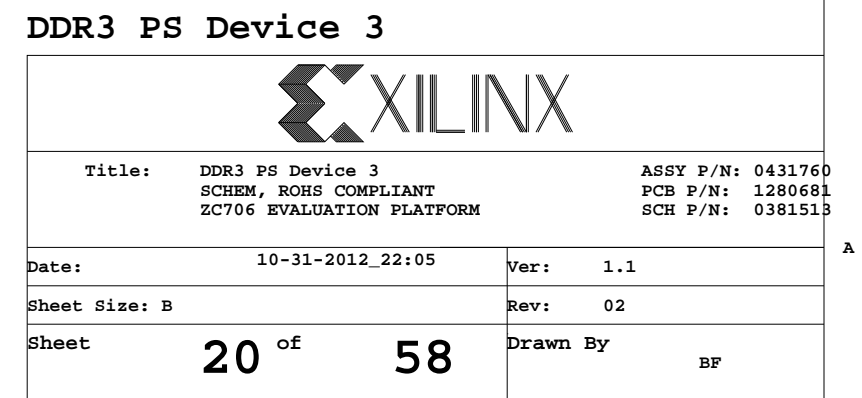


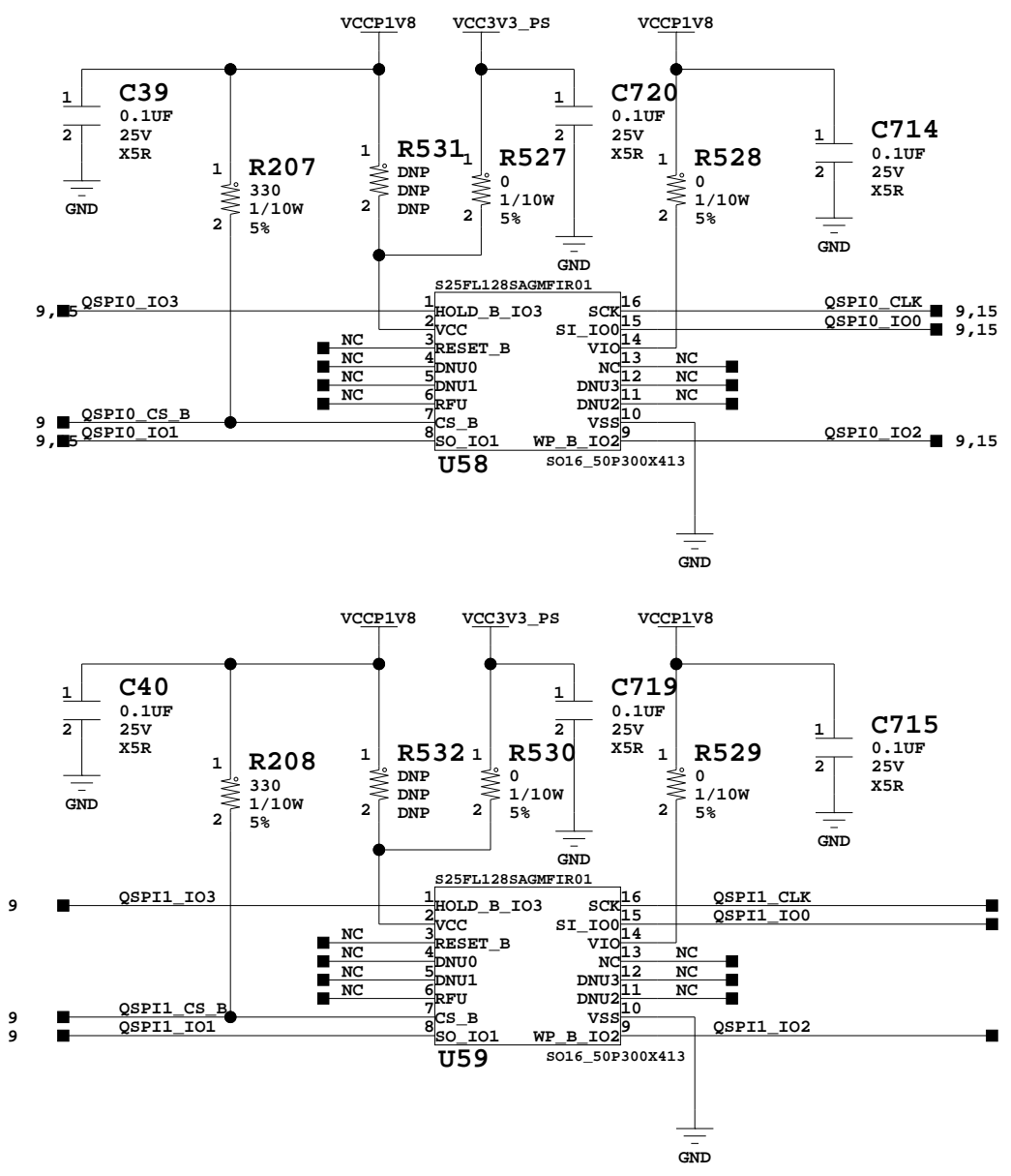
DDR3 PS Device 0

Title:		DDR3 PS Device 0	
SCHEM, ROHS COMPLIANT		ASSY P/N: 0431760	
ZC706 EVALUATION PLATFORM		PCB P/N: 1280681	
		SCH P/N: 0381513	
Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	17 of 58	Drawn By	BF



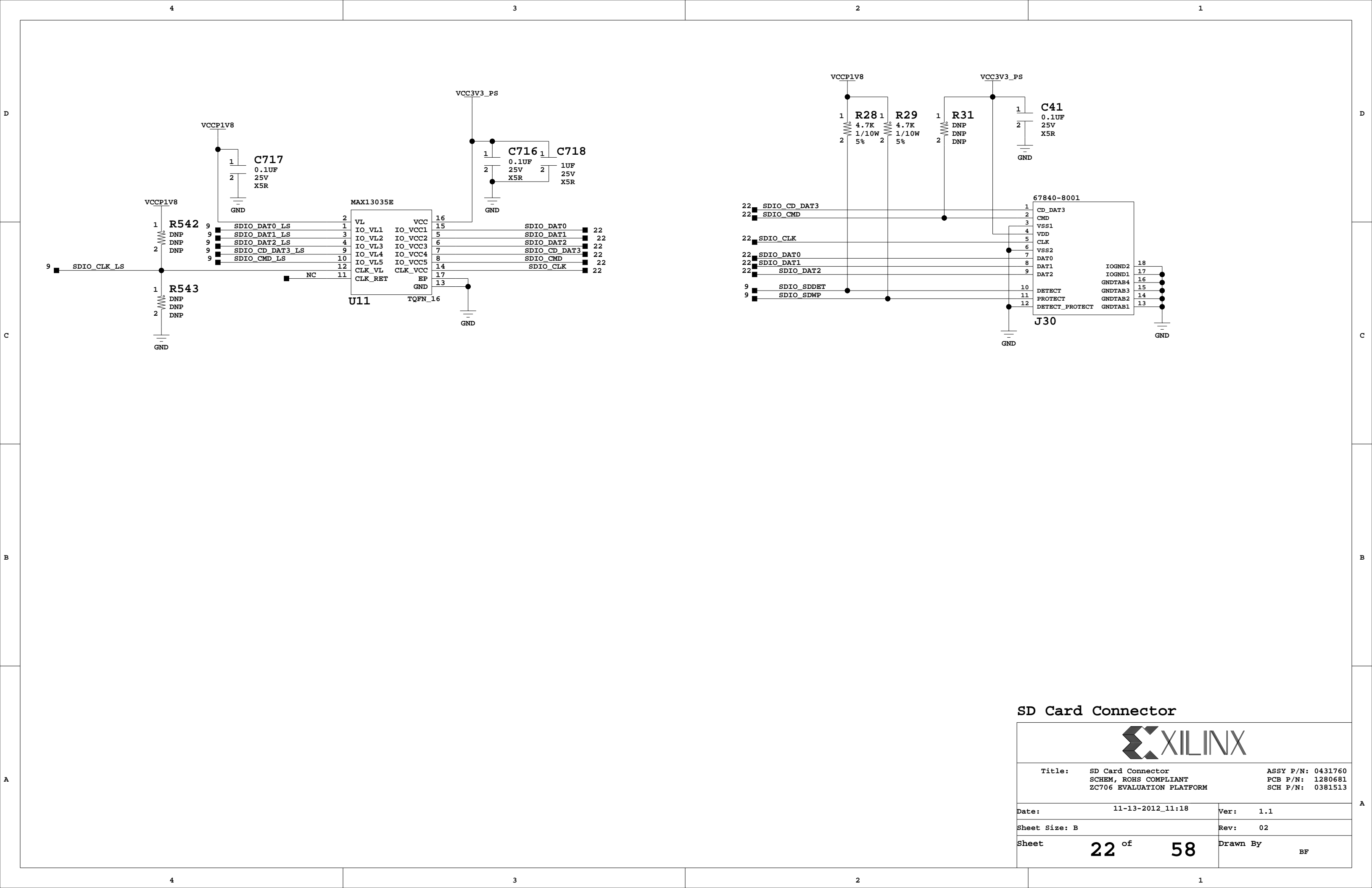







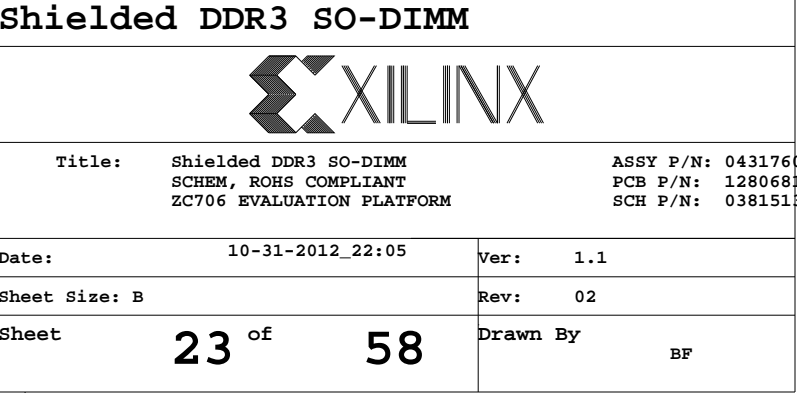
Dual Quad SPIs

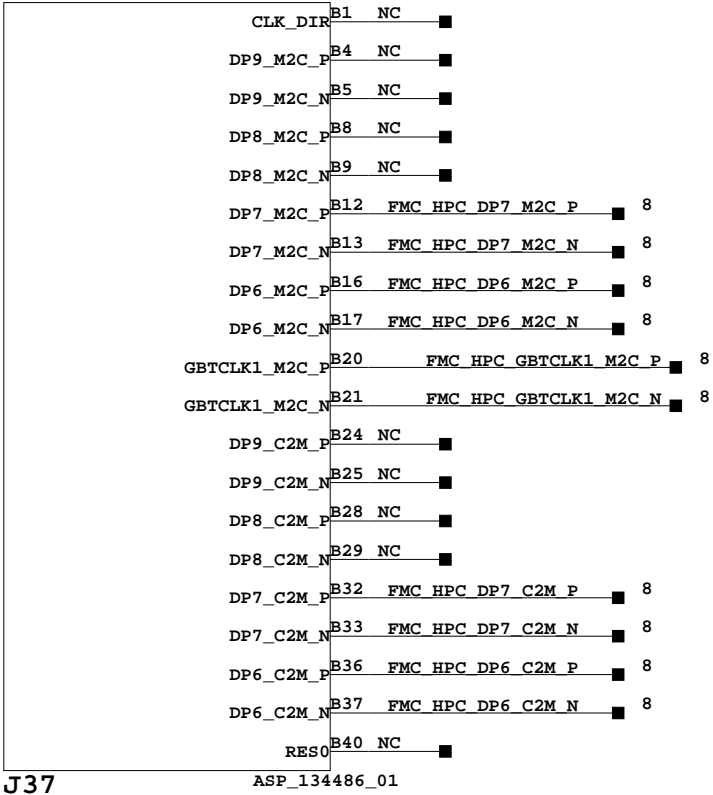
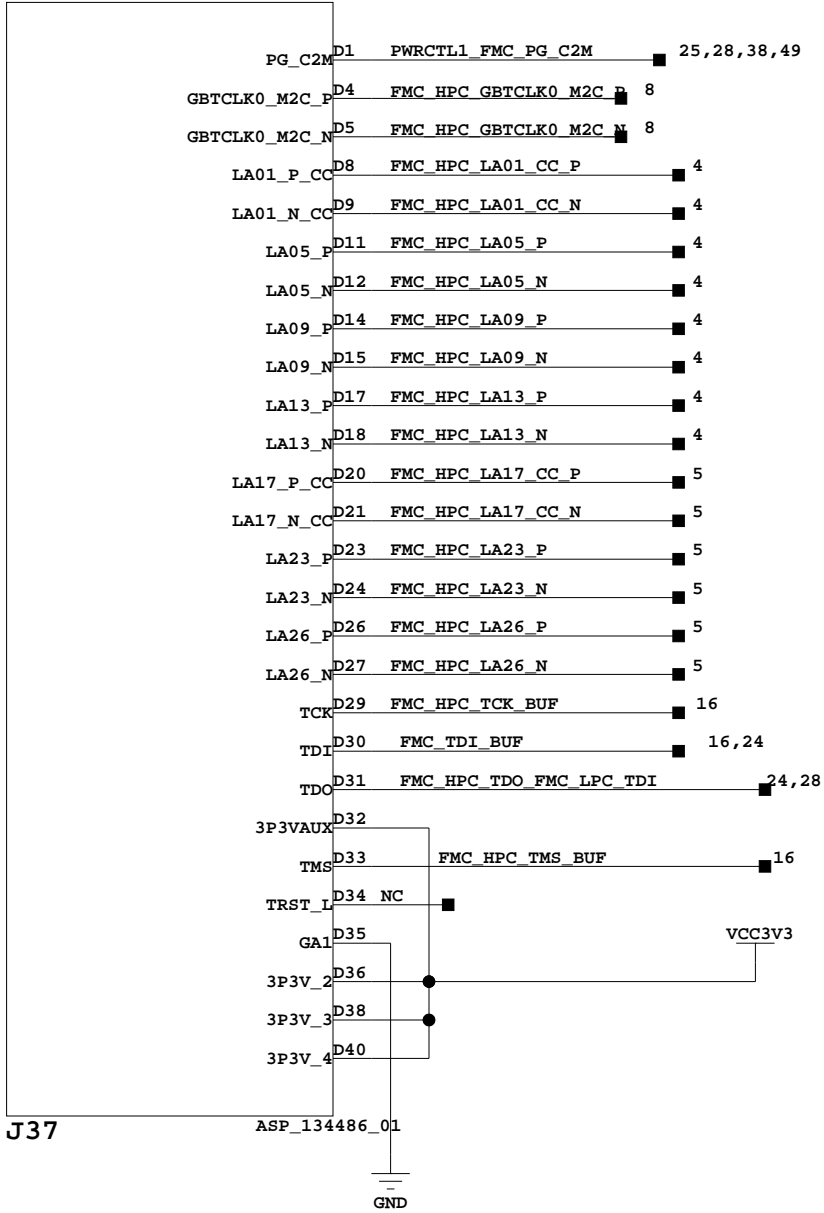
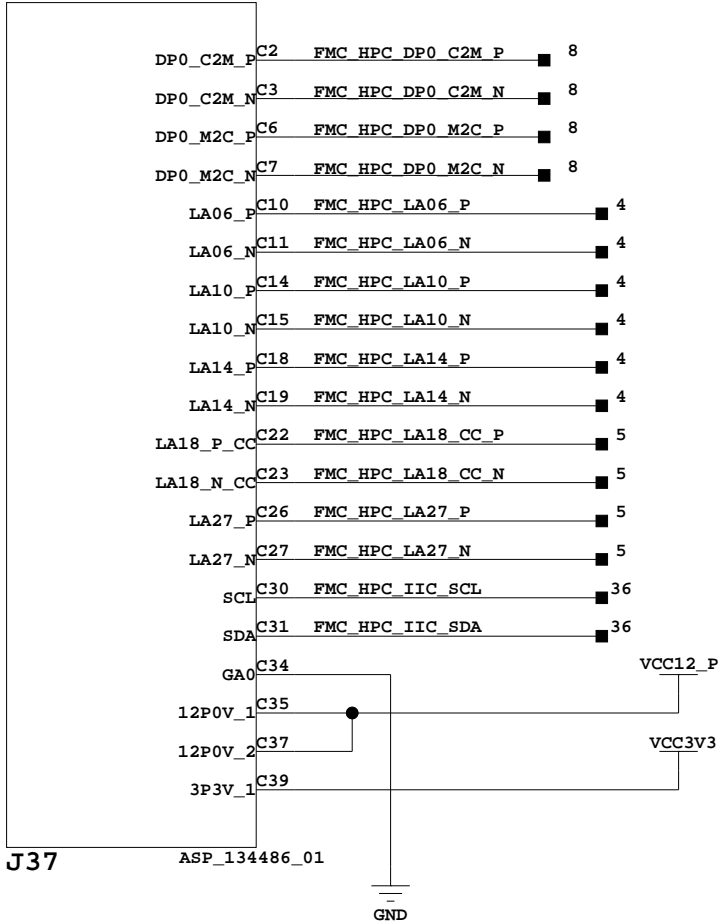
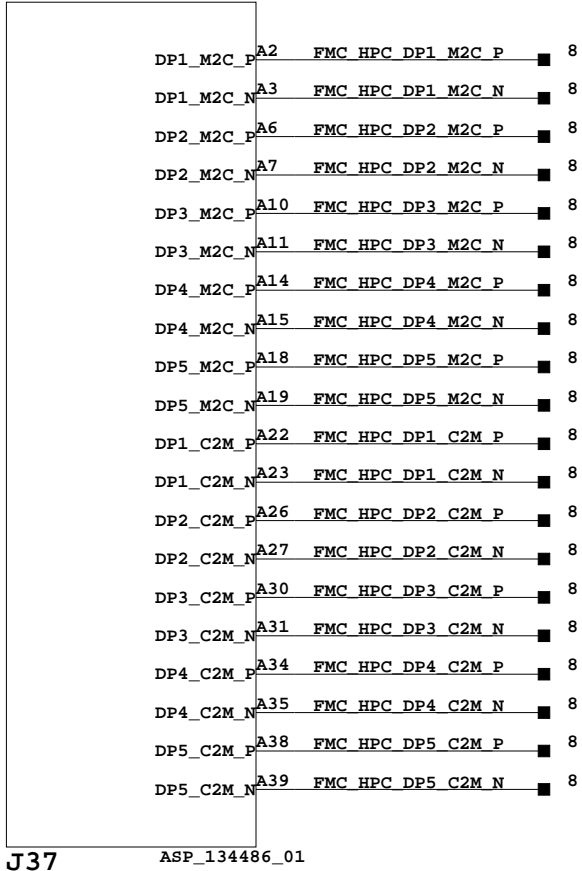
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SCHEM, ROHS COMPLIANT		PCB P/N: 1280681	
ZC706 EVALUATION PLATFORM		SCH P/N: 0381513	
Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size: B		Rev:	02
Sheet	21 of 58	Drawn By	BF



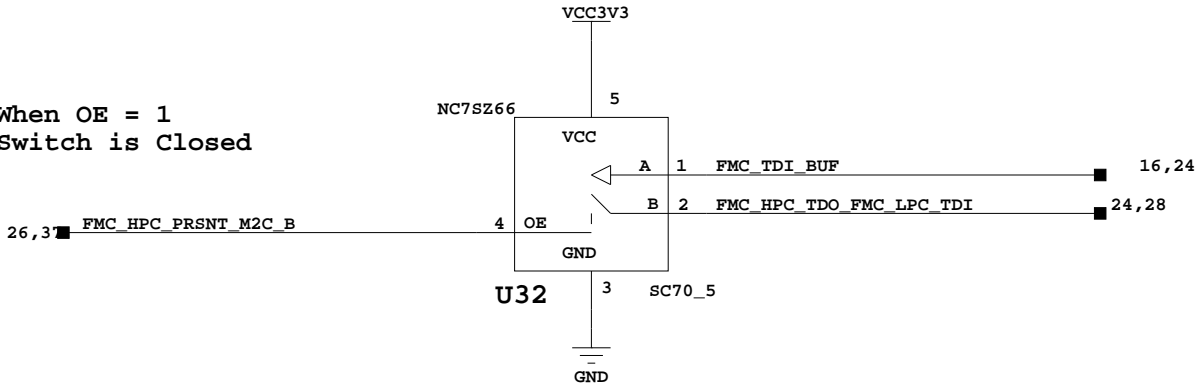
SD Card Connector

			
Title:		SD Card Connector	
		SCHEM, ROHS COMPLIANT	
		ZC706 EVALUATION PLATFORM	
Date:		11-13-2012_11:18	Ver: 1.1
Sheet Size:		B	Rev: 02
Sheet		22 of 58	Drawn By BF





When OE = 1
Switch is Closed



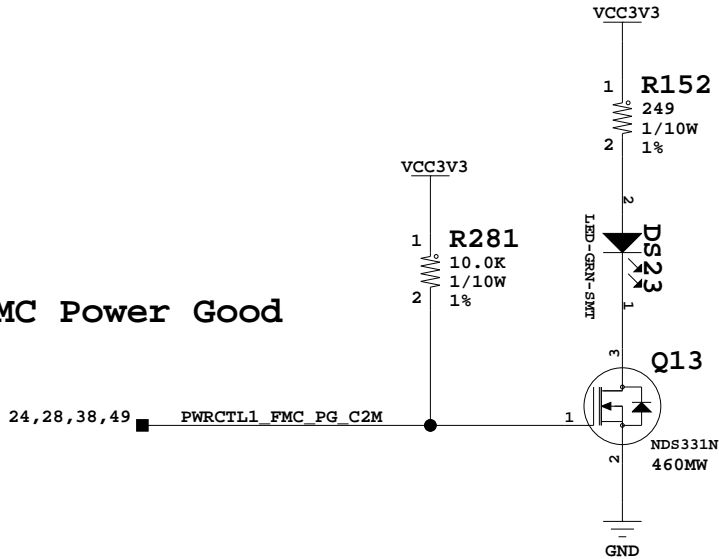
ANSI/VITA 57.1 - Revised 2010 FMC HPC Header, Rows A, B, C, D



Title: FMC HPC Header, Rows A, B, C, D SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM
ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	24 of 58	Drawn By	BF

FMC Power Good



ANSI/VITA 57.1 - Revised 2010
FMC HPC Header, Rows E, F, G



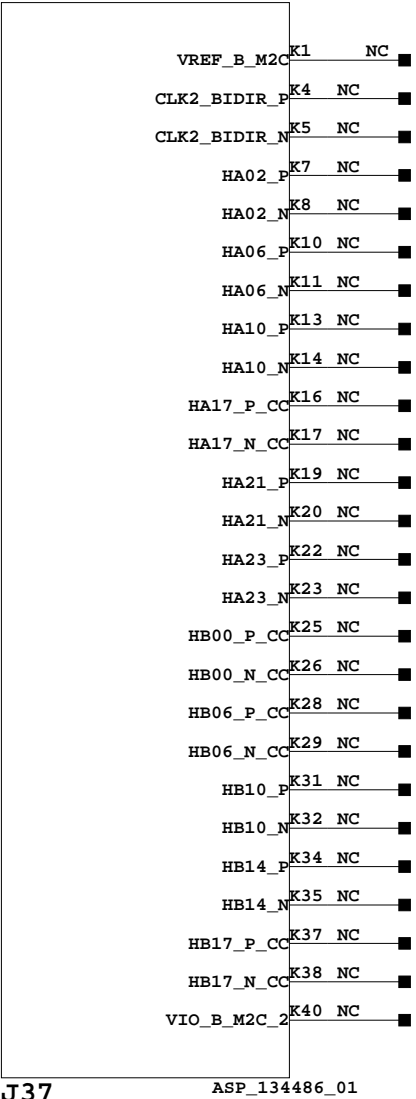
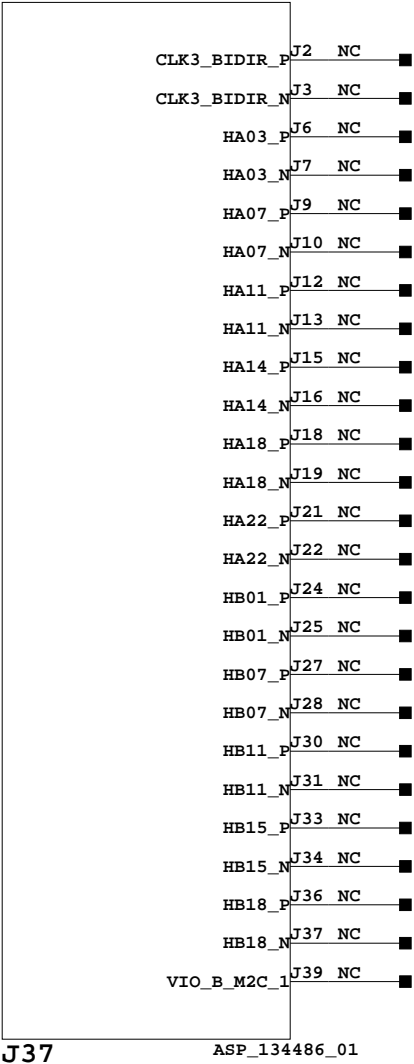
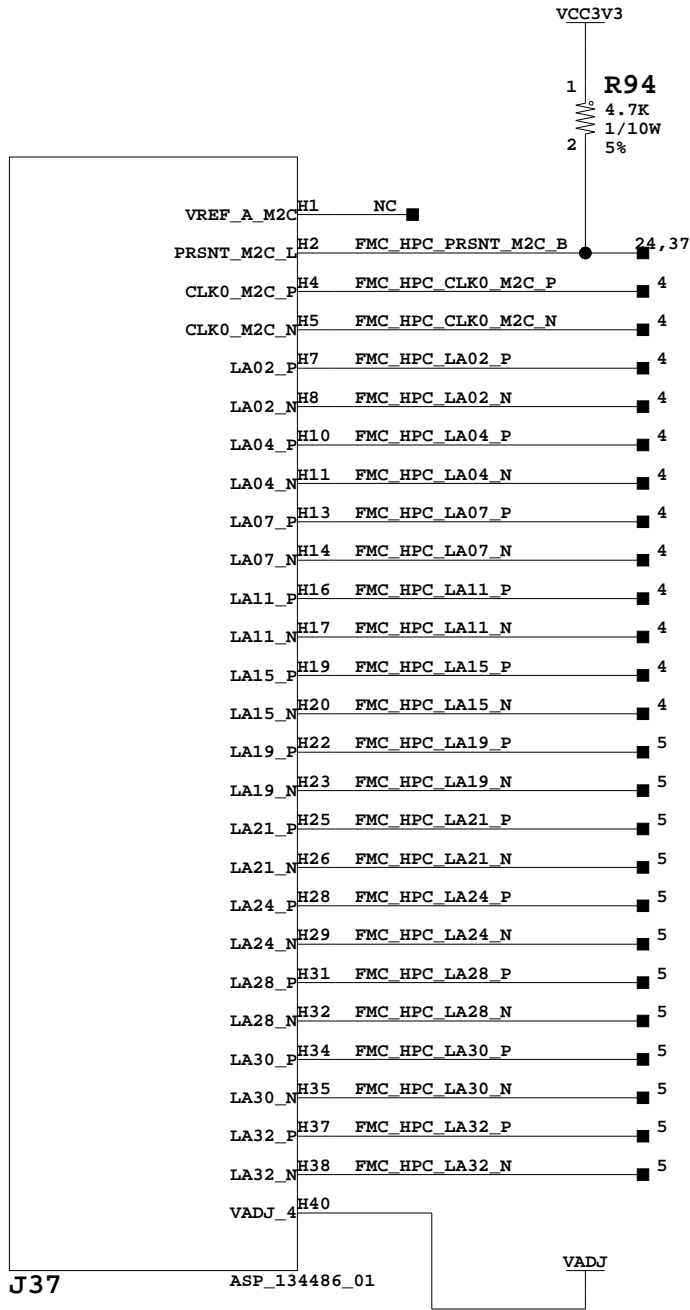
Title: FMC HPC Header, Rows E, F, G
SCHEM, ROHS COMPLIANT
ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

Date: 10-31-2012_22:05 Ver: 1.1


Sheet Size: B Rev: 02

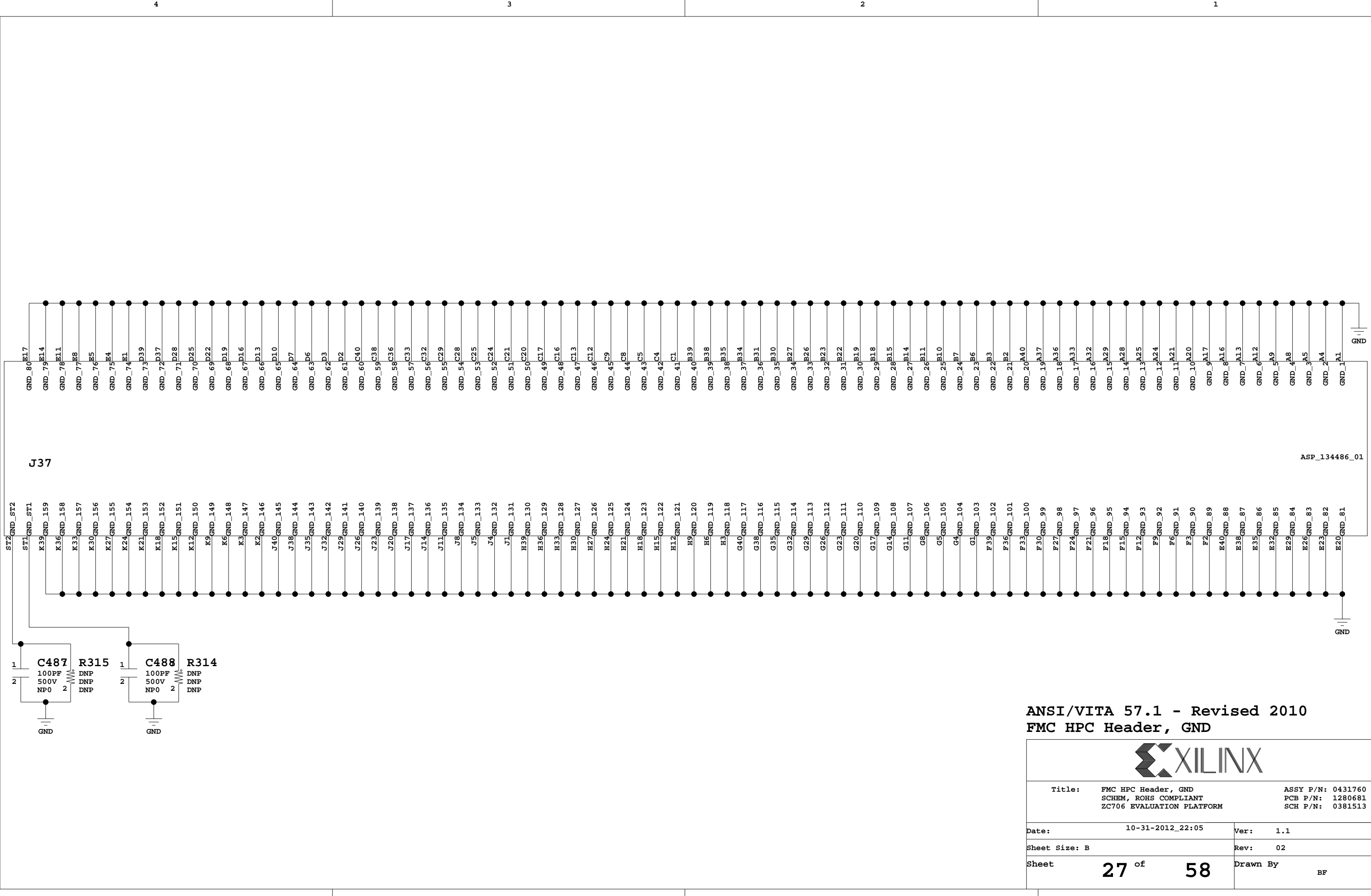
Sheet 25 of 58 Drawn By BF



1

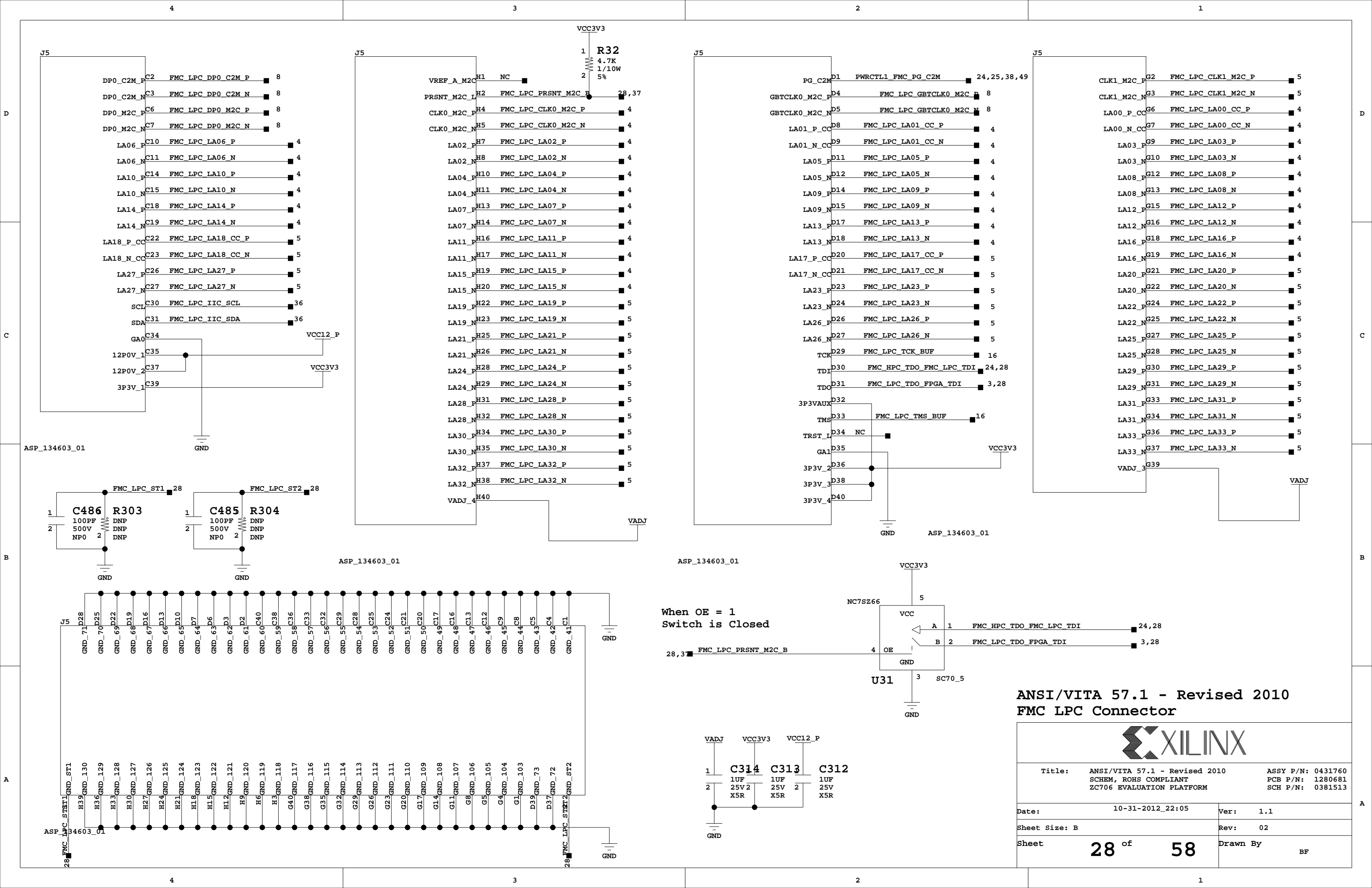
ANSI/VITA 57.1 - Revised 2010
FMC HPC Header, Rows H, J, K

		
Title: FMC HPC Header, Rows H, J, K SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
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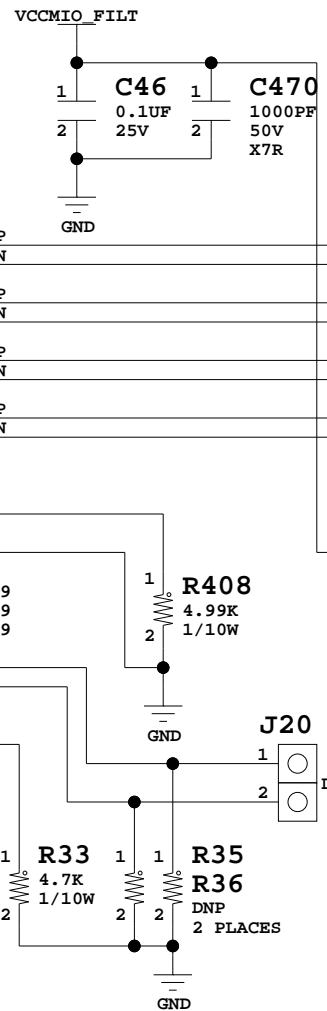
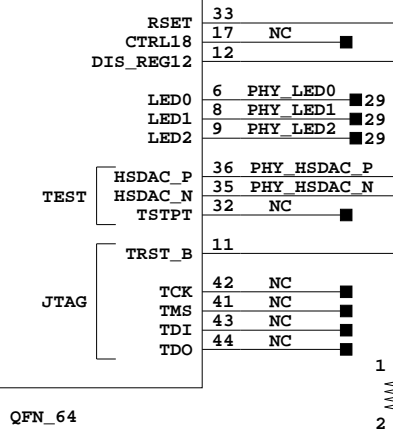
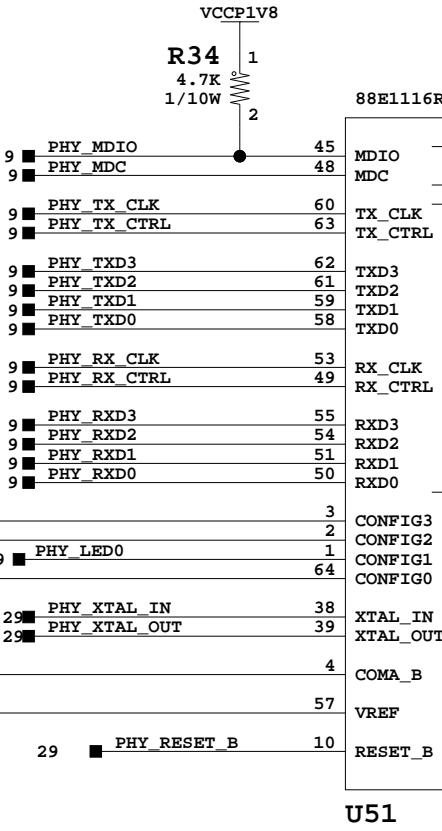
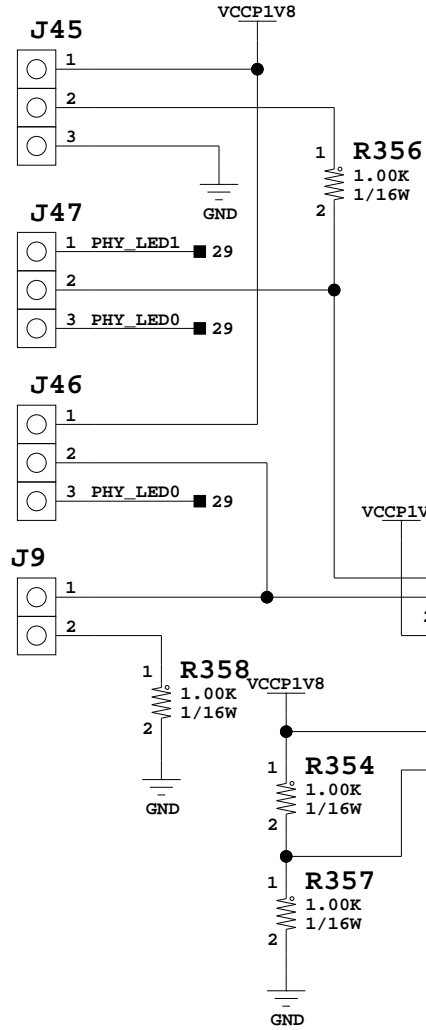
ANSI/VITA 57.1 - Revised 2010
FMC HPC Header, GND

Title:		FMC HPC Header, GND SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	
		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
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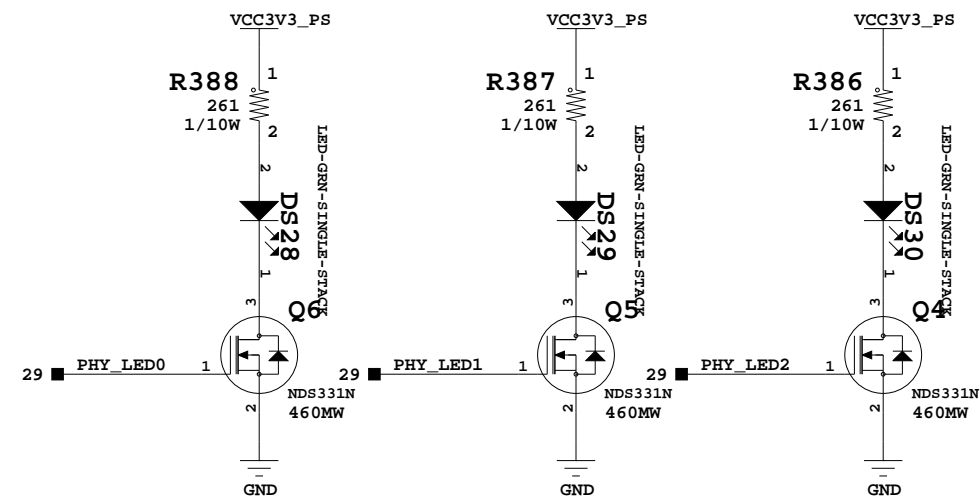
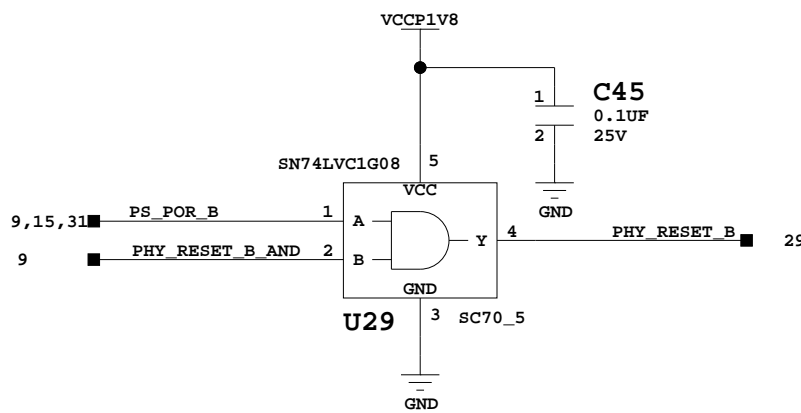
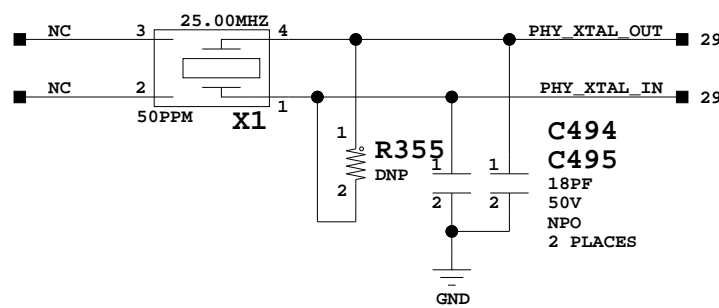
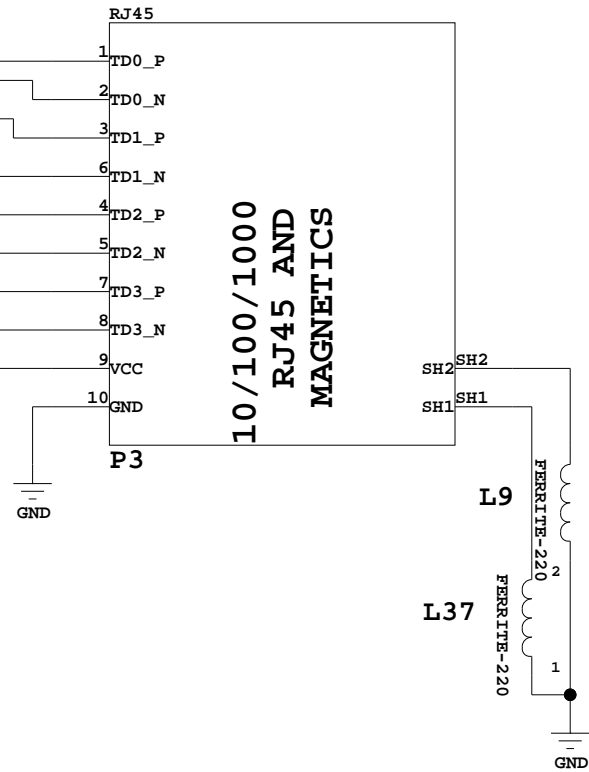


CONFIGURATION MAPPING			
PIN	SETTING	CONFIGURATION	
CONFIG0	VCCO_MIO1	PHYAD[1]=1	PHYAD[0]=1
CONFIG1	EPHY_LED0	PHYAD[3]=0	PHYAD[2]=1
CONFIG2	GND	ENA_XC=0	PHYAD[4]=0
	EPHY_LED0	ENA_XC=0	PHYAD[4]=1
	VCCO_MIO1	ENA_XC=1	PHYAD[4]=1
CONFIG3	GND	RGMII_TX=0	RGMII_RX=0
	EPHY_LED0	RGMII_TX=0	RGMII_RX=1
	EPHY_LED1	RGMII_TX=1	RGMII_RX=0
	VCCO_MIO1	RGMII_TX=1	RGMII_RX=1

2



1



GEM / MDIO

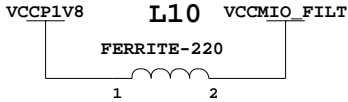


Title: GEM / MDIO SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
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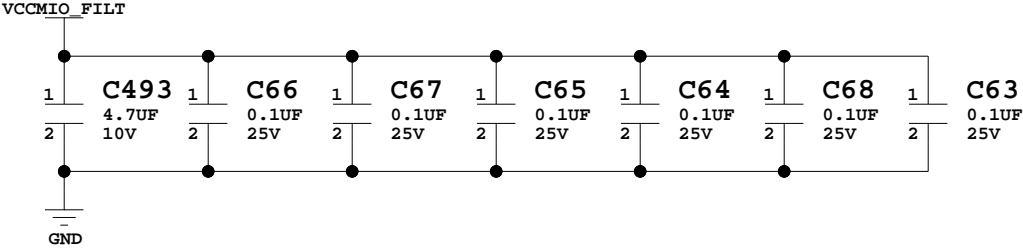
2 SEE CONFIGURATION MAPPING TABLE FOR JUMPER SETTINGS

1 TEST PORT: IF USING THE TEST PORT INSTALL 49.9 OHM PULLDOWN RESISTORS ON HSDAC_P AND HSDAC_N.

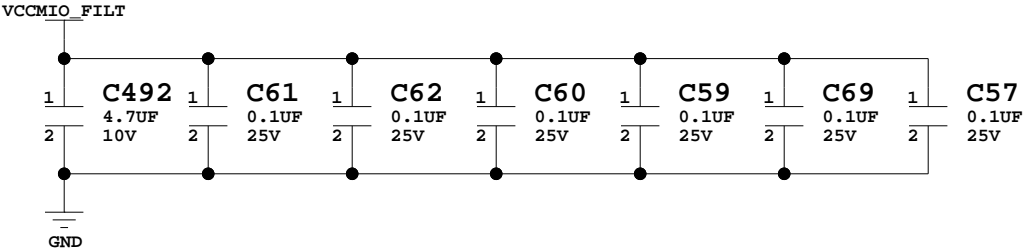
GEM / MDIO - POWER & DECOUPLING



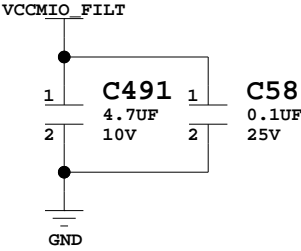
AVDDX, AVDDR, AVDDC



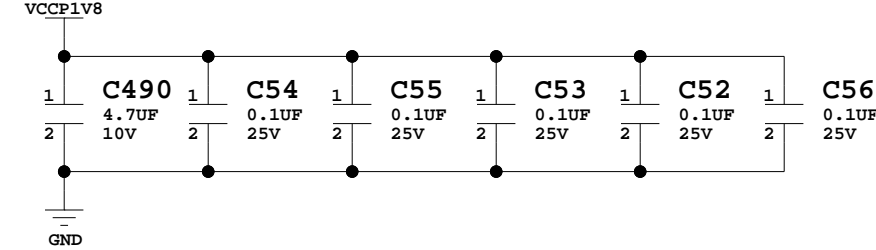
AVDD



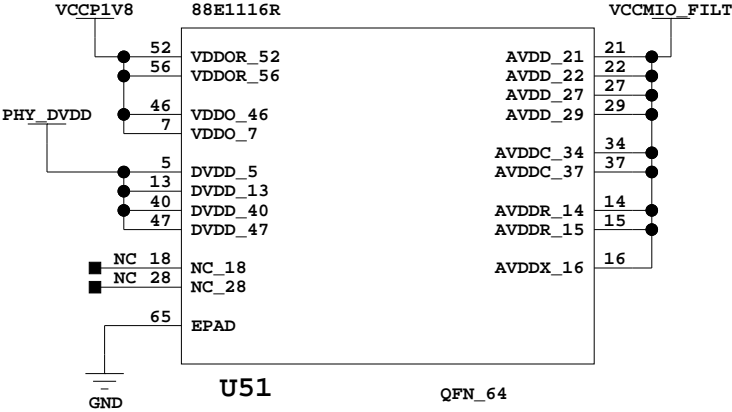
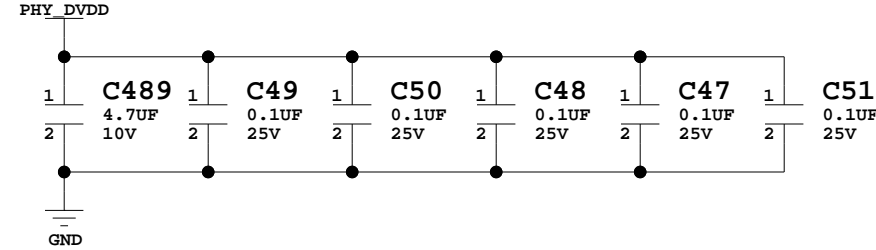
MAGNETICS / RJ45



VDDO, VDDOR



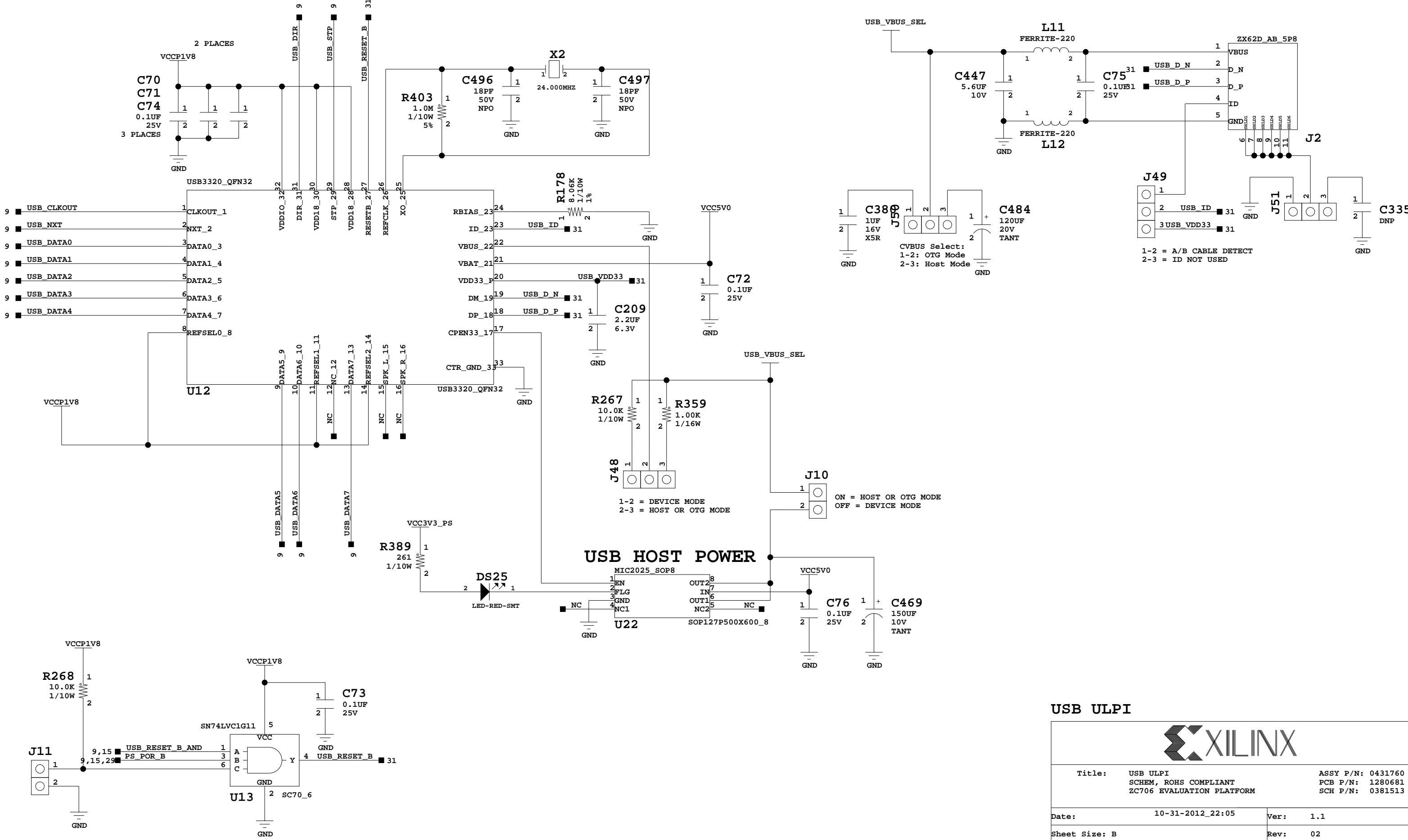
DVDD



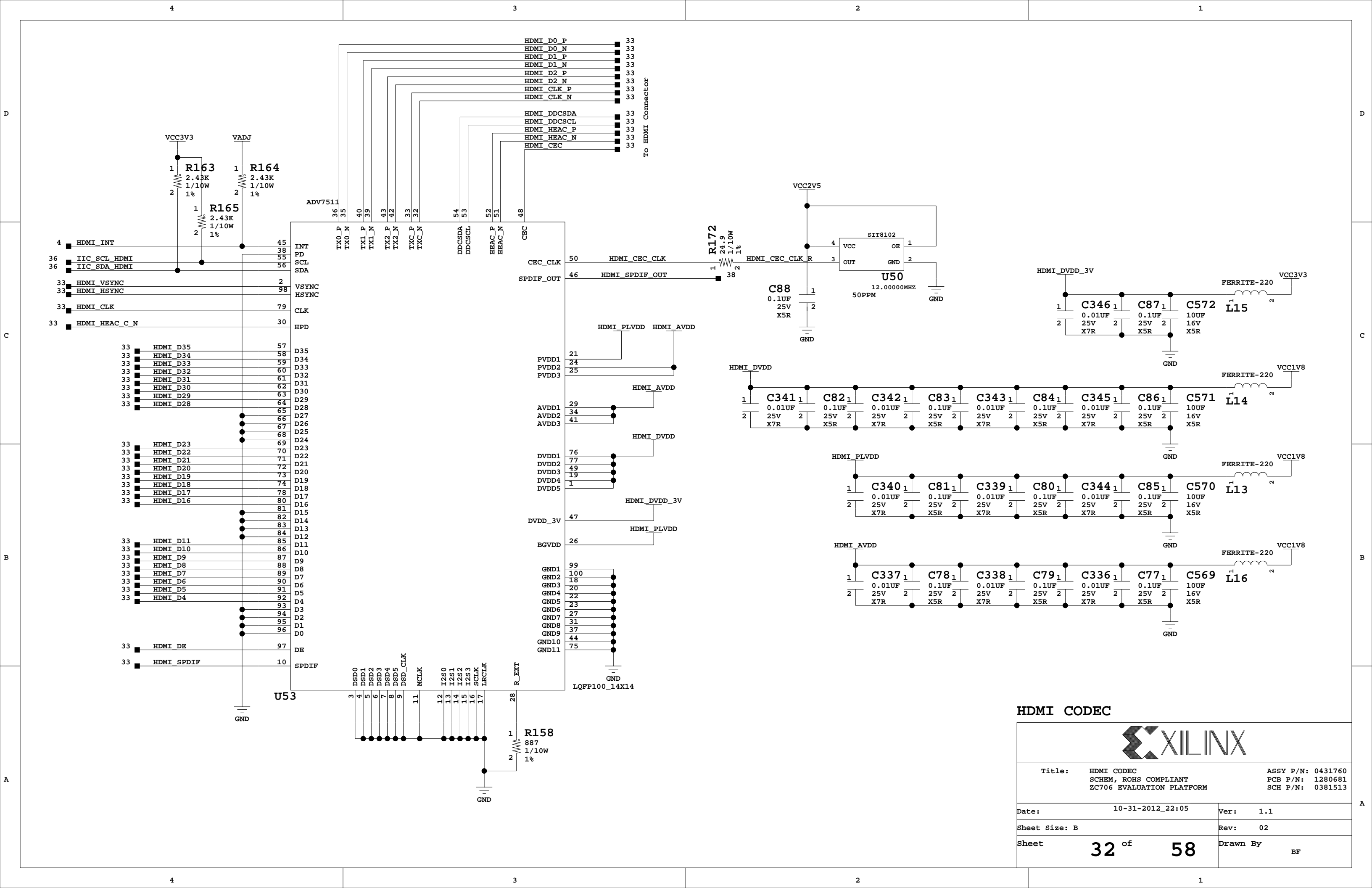
GEM / MDIO

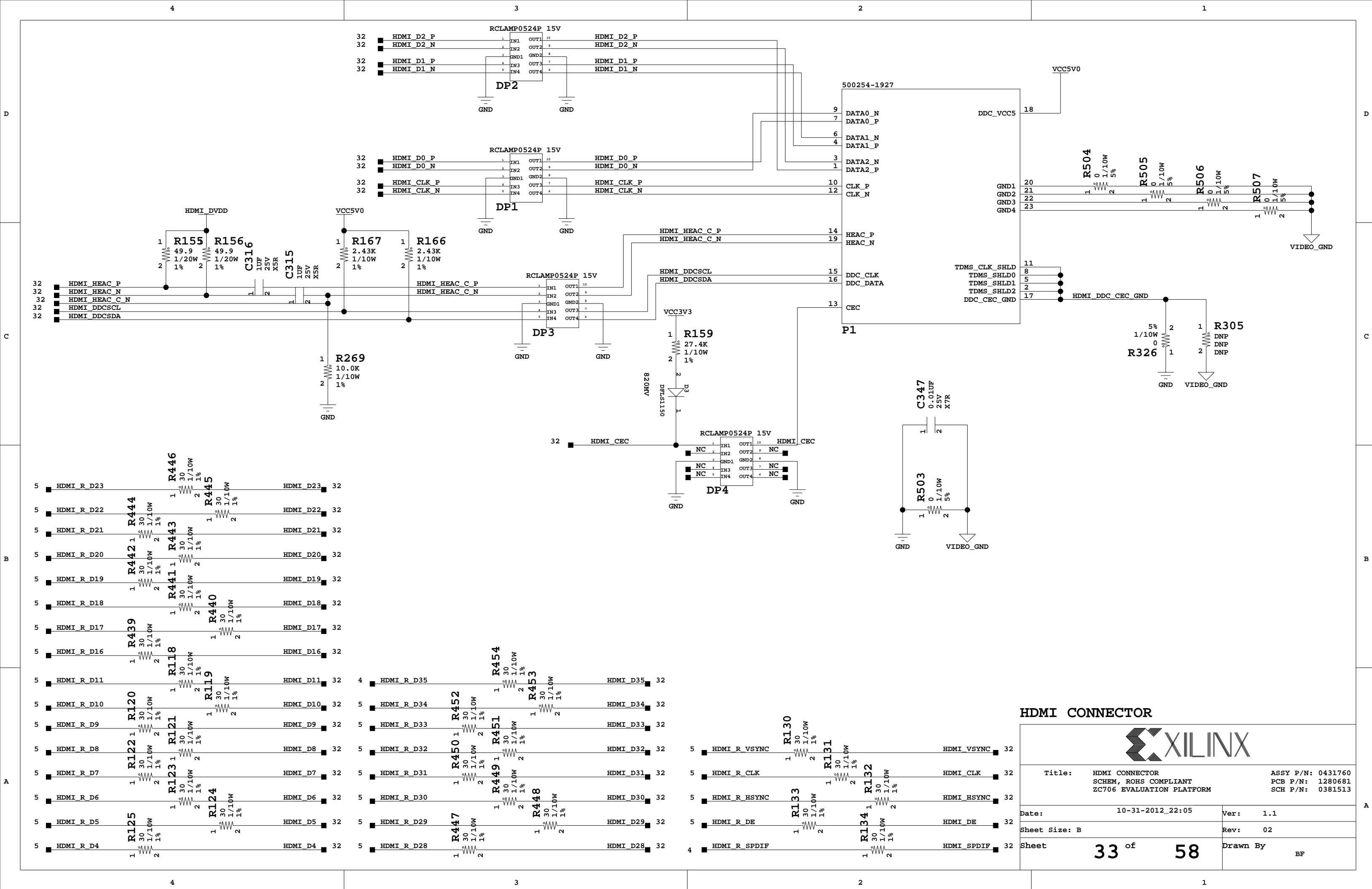
Title: GEM / MDIO SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
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USB 2.0 ULPI TRANSCEIVER AND CONNECTOR

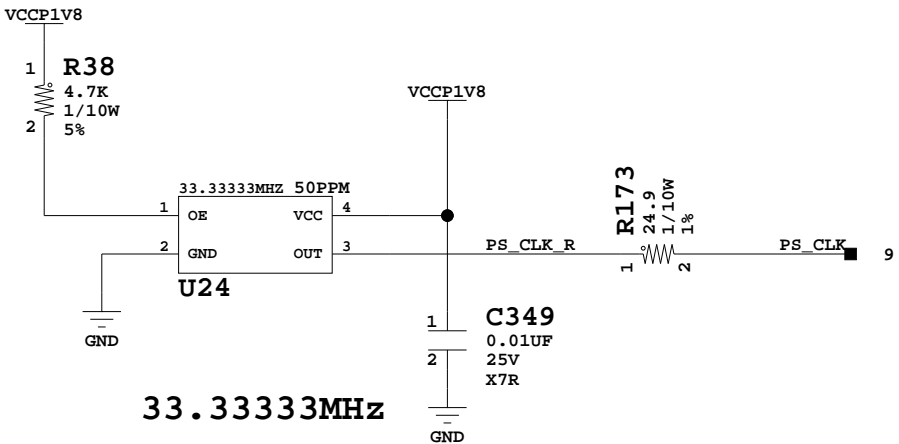
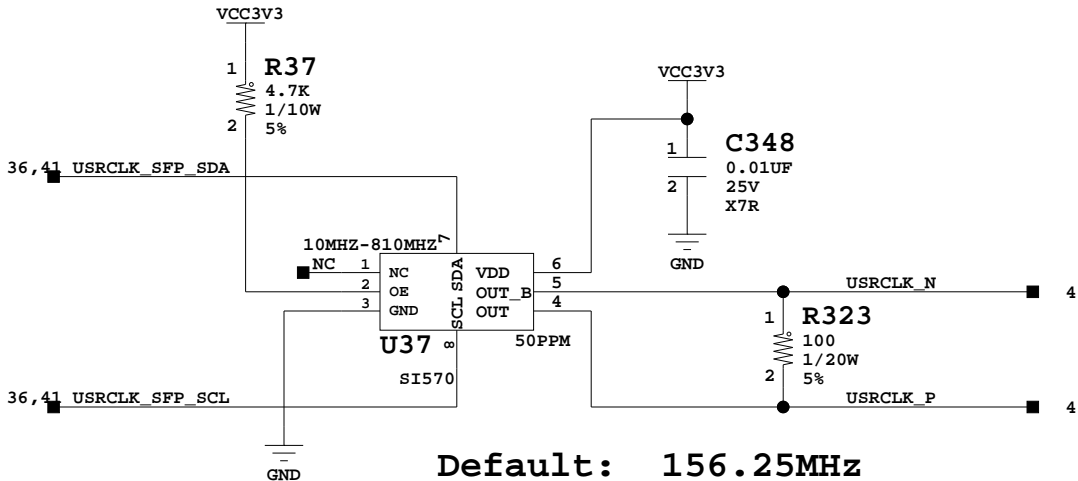
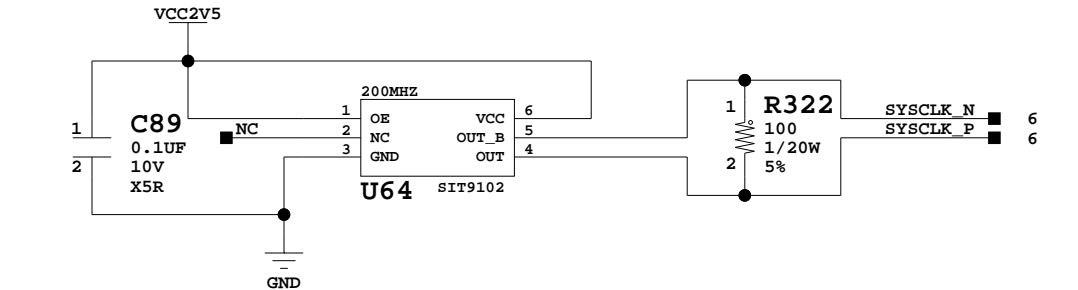


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ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513		
Date:	10-31-2012_22:05	Ver: 1.1
Sheet Size:	B	Rev: 02
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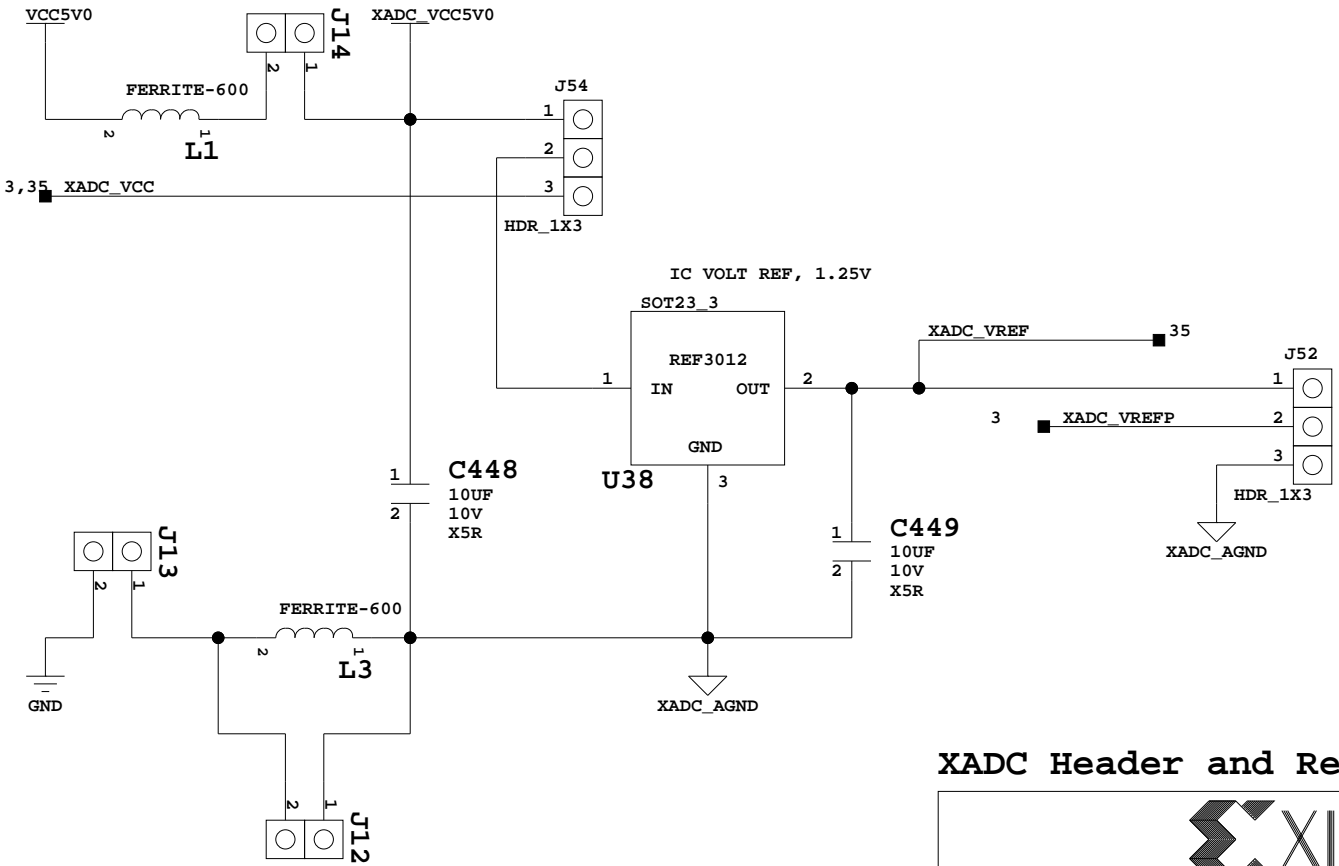
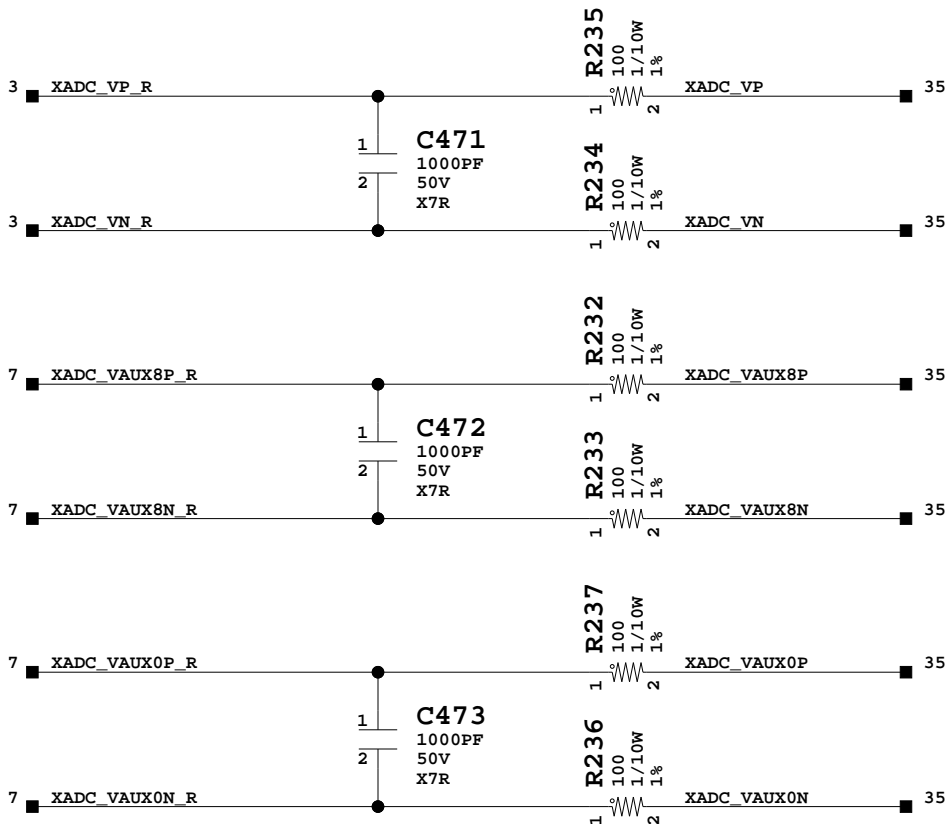
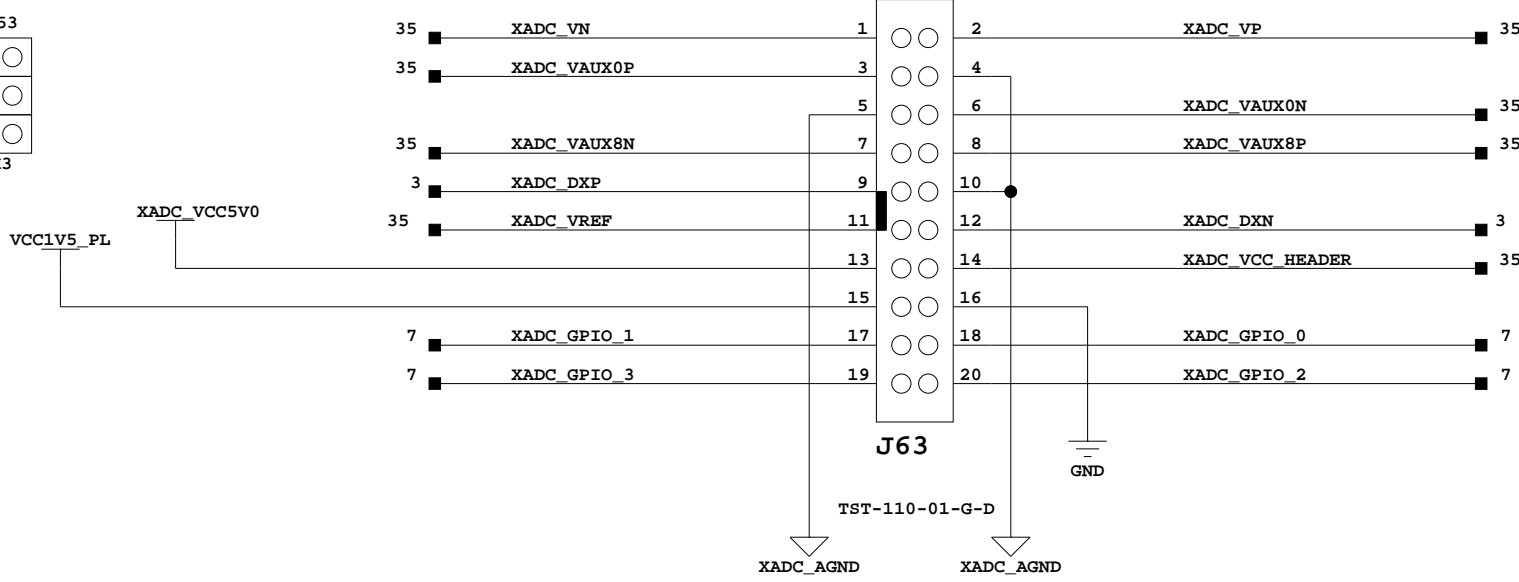
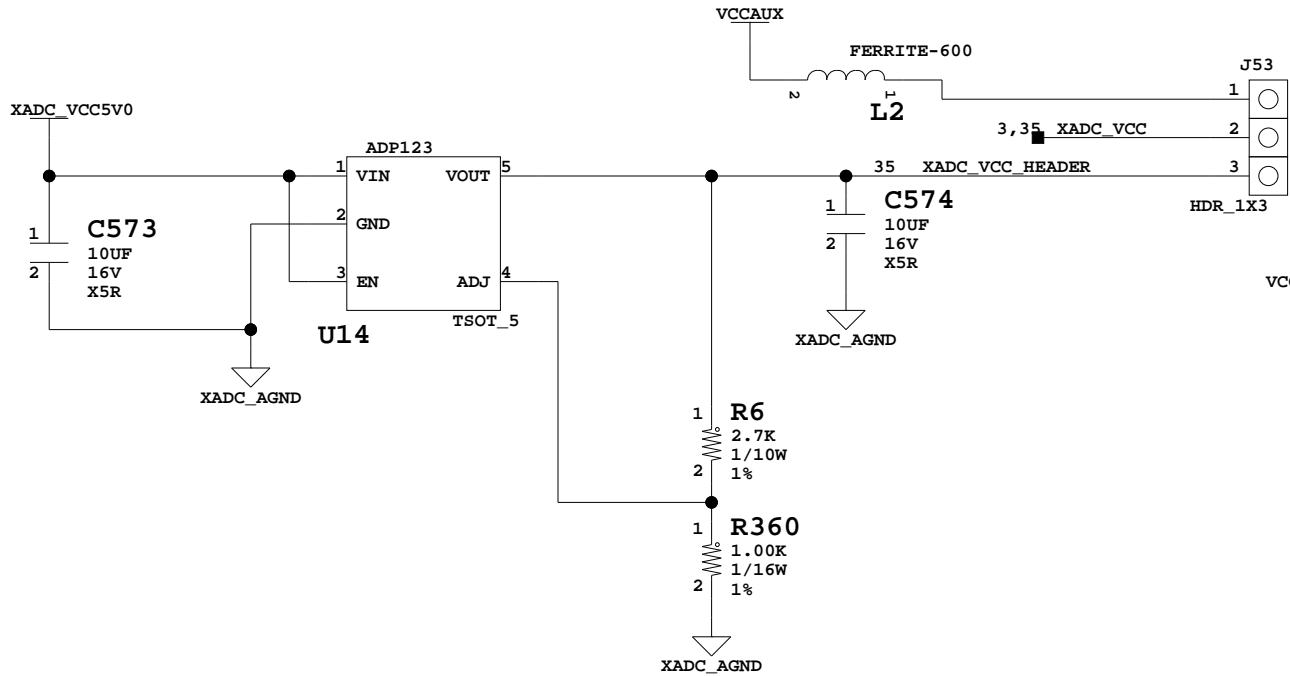


SIT9102AI-243N25E200.0000



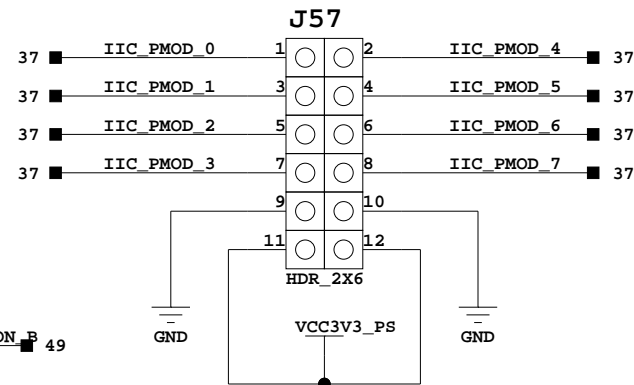
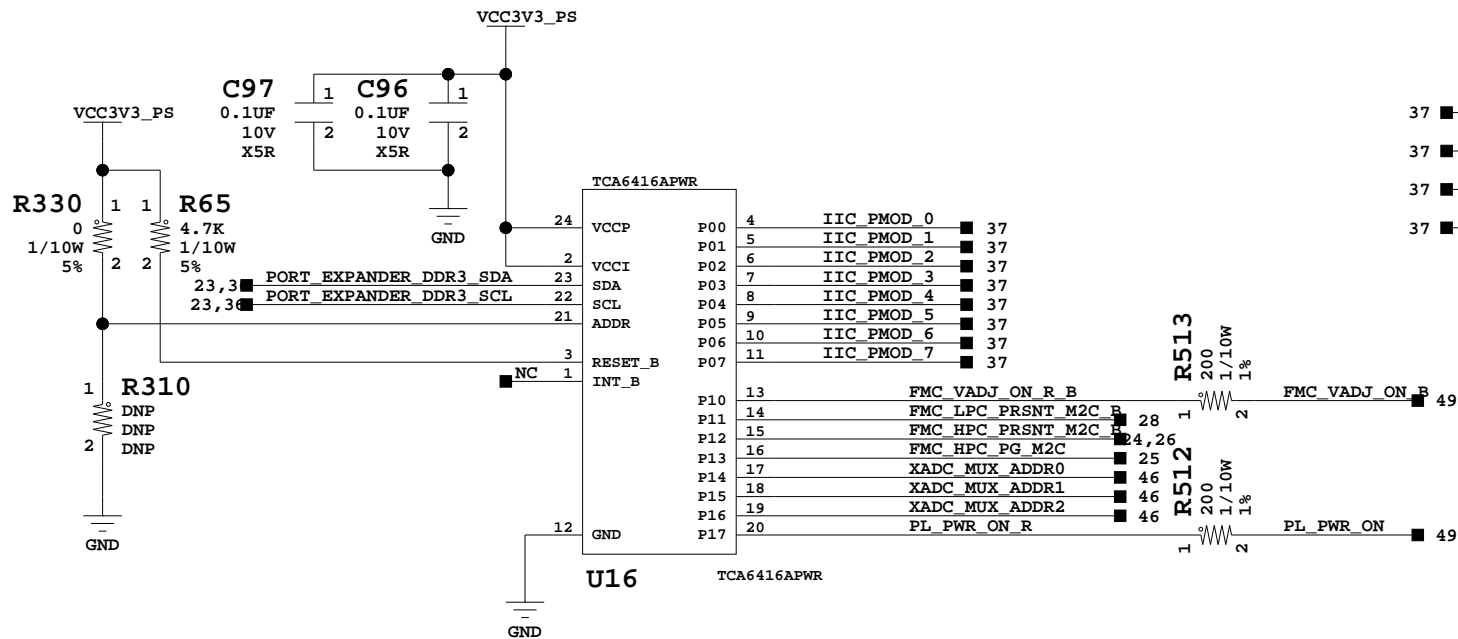
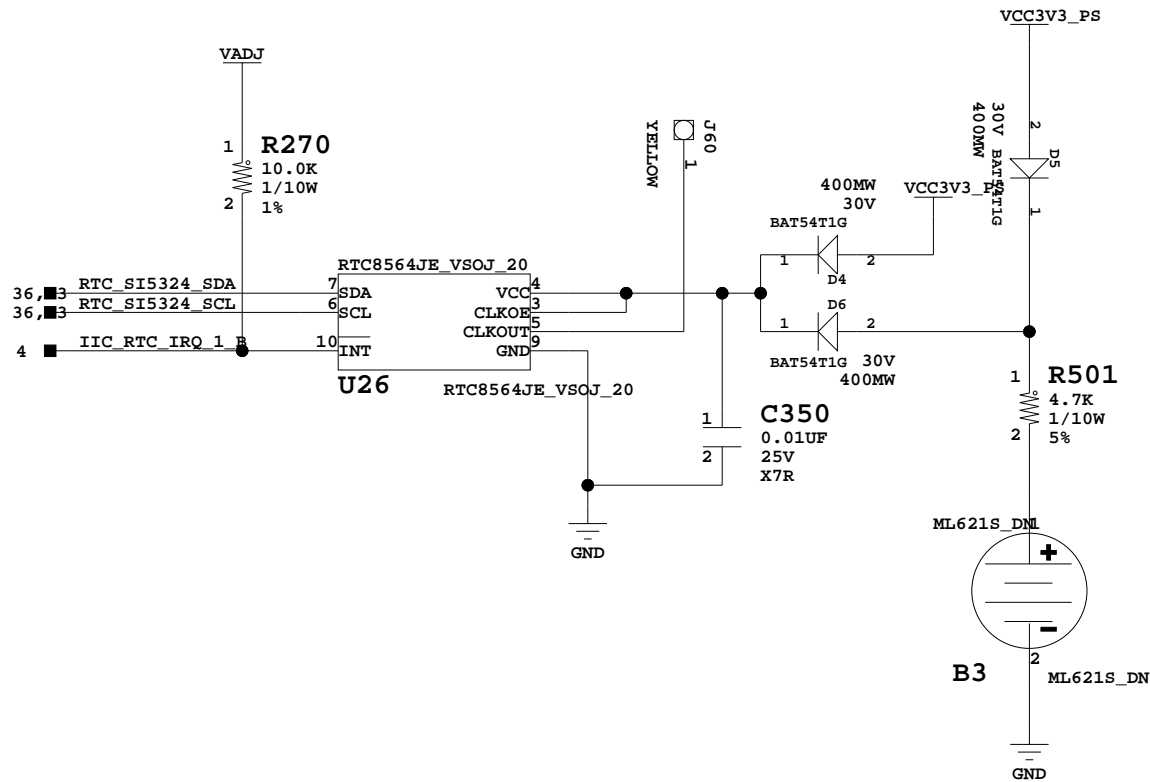
Clocks

Title:		ASSY P/N: 0431760	
SCHEM, ROHS COMPLIANT		PCB P/N: 1280681	
ZC706 EVALUATION PLATFORM		SCH P/N: 0381513	
Date:	10-31-2012_22:05	Ver:	1.1
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XADC Header and Reference

Title: XADC Header and Reference SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
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IIC Real Time Clock, Port Expander



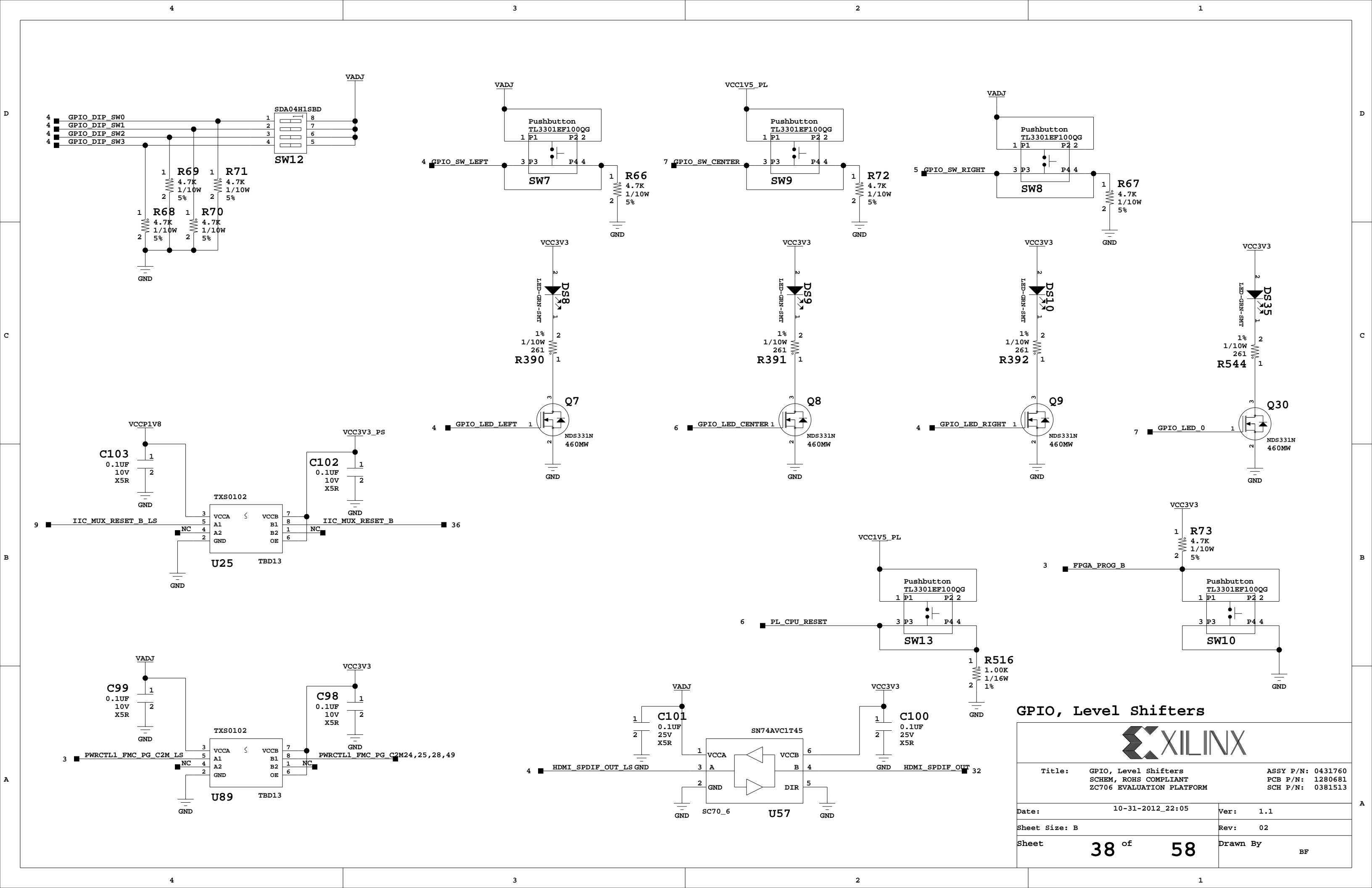
Title: IIC Real Time Clock, Port Expander SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM

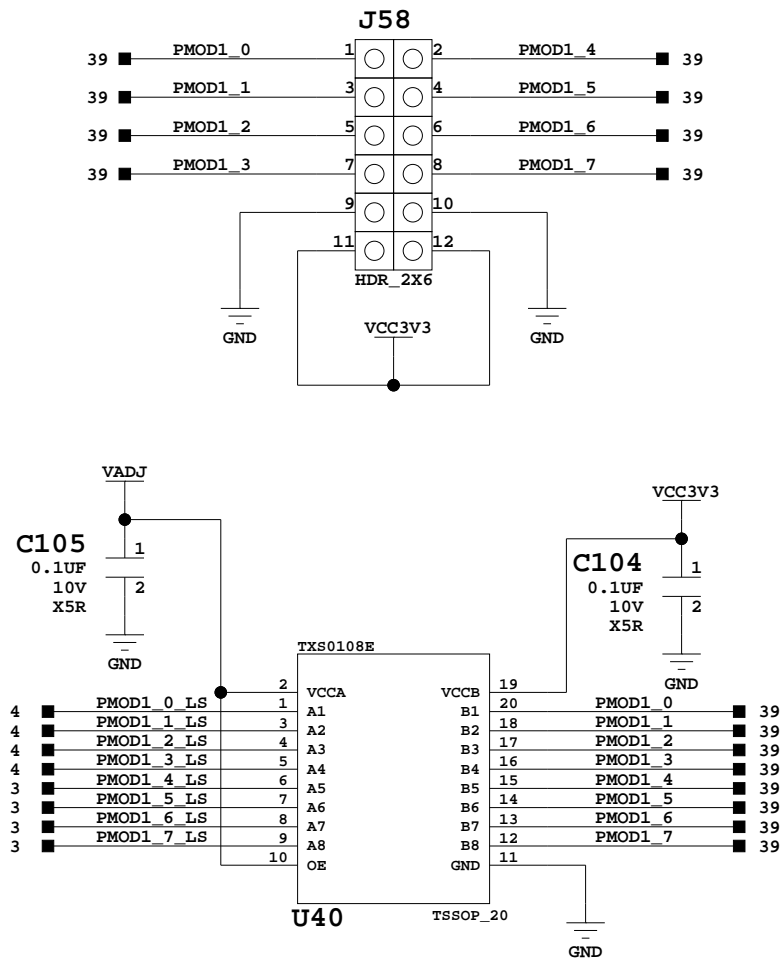
ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513

Date: 10-31-2012_22:05 Ver: 1.1

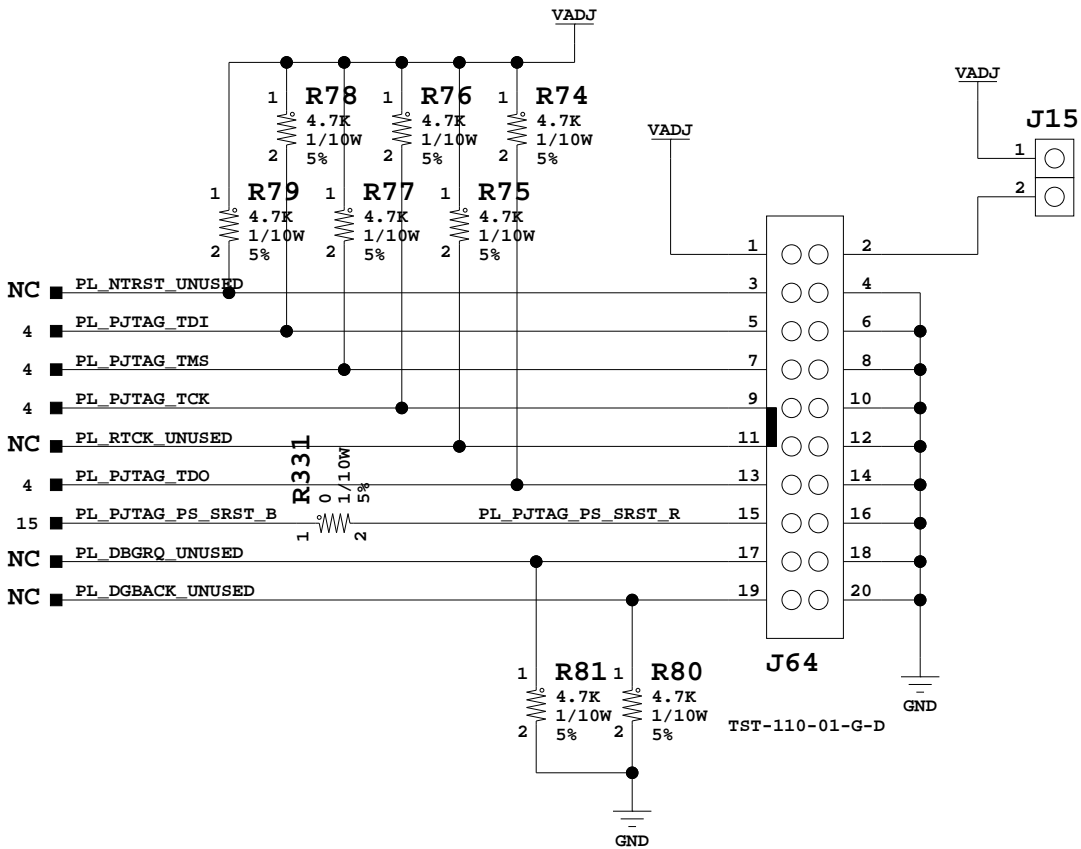
Sheet Size: B Rev: 02

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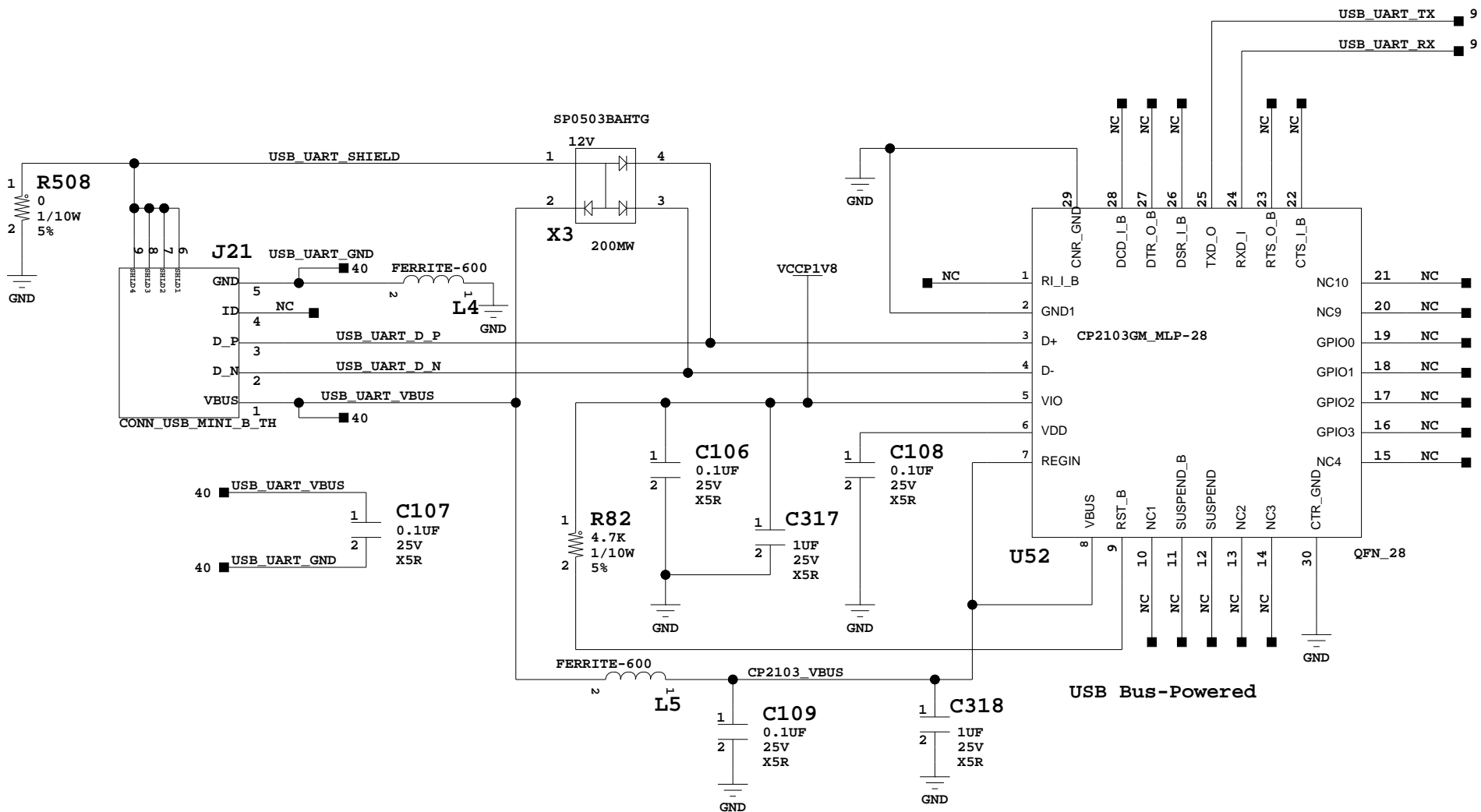
ARM PJTAG Header



ARM PJTAG Header, PMOD1

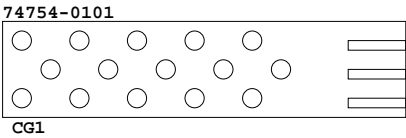
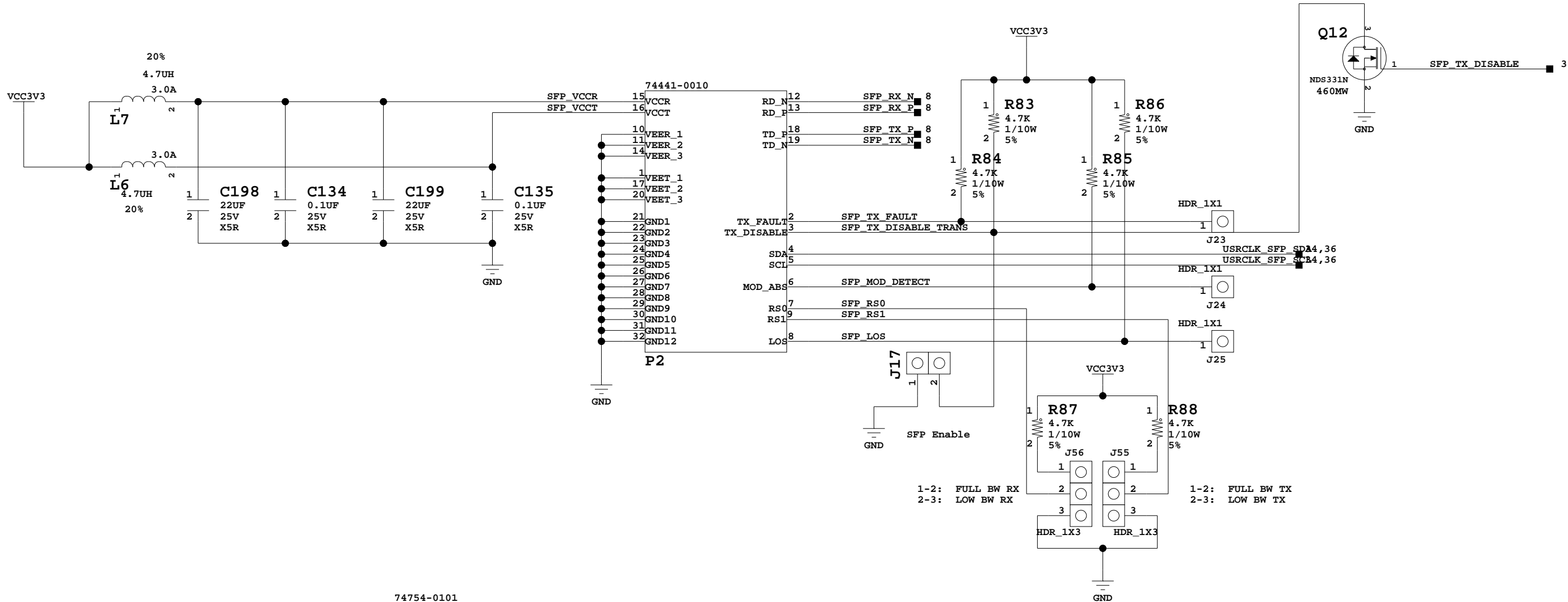


Title: ARM PJTAG Header, PMOD1 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
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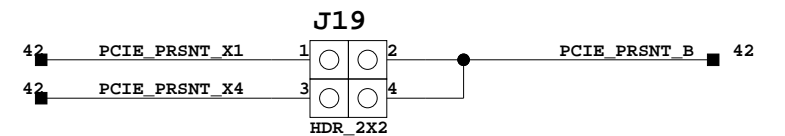
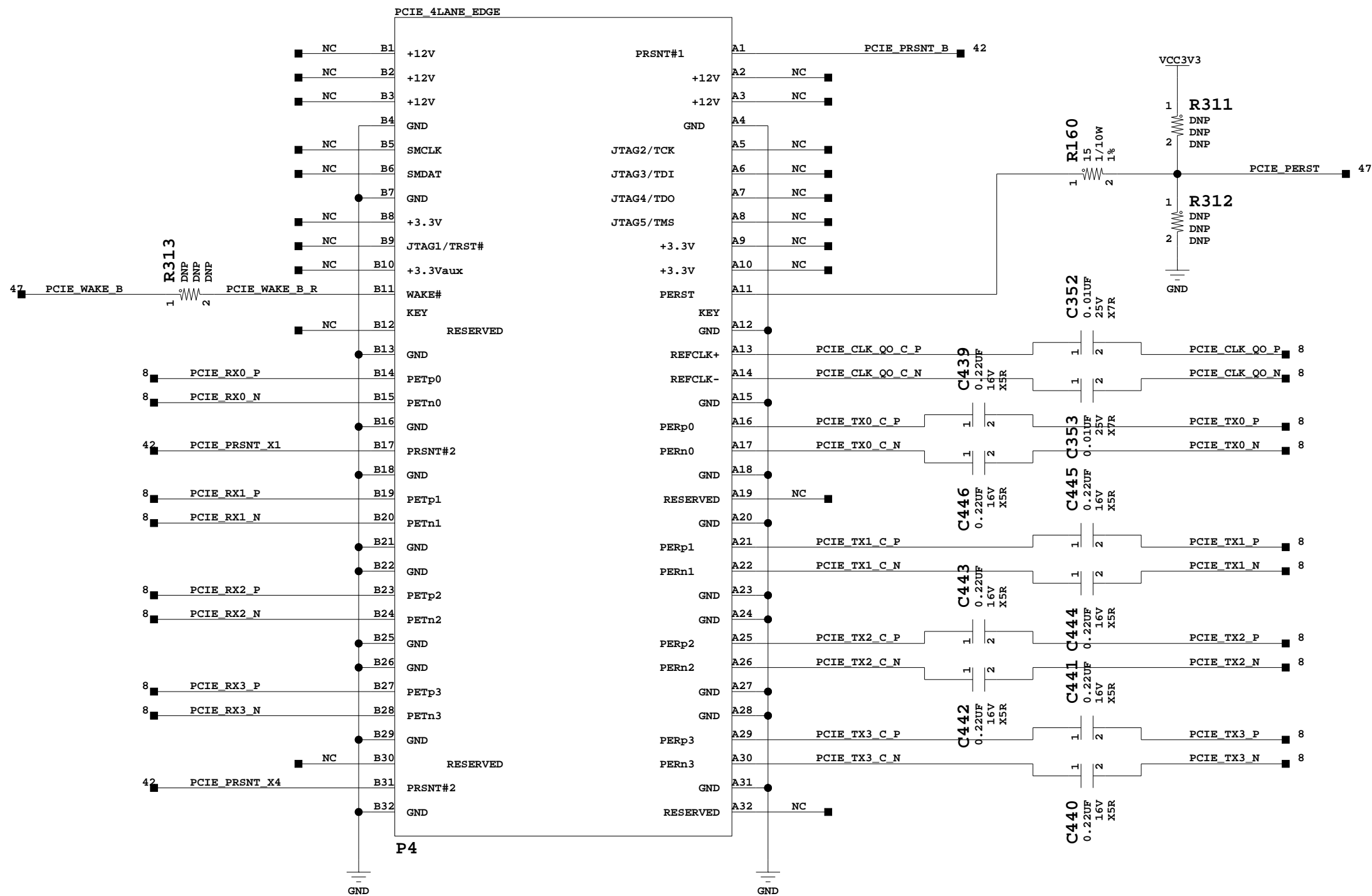
USB UART

Title:		ASSY P/N: 0431760	
SCHEM, ROHS COMPLIANT		PCB P/N: 1280681	
ZC706 EVALUATION PLATFORM		SCH P/N: 0381513	
Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
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SFP+ Connector and Cage

Title:		ASSY P/N: 0431760	
SCHEM, ROHS COMPLIANT		PCB P/N: 1280681	
ZC706 EVALUATION PLATFORM		SCH P/N: 0381513	
Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
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PCIE x4 Card edge

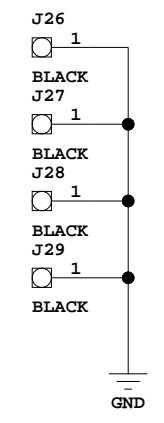
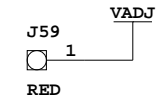
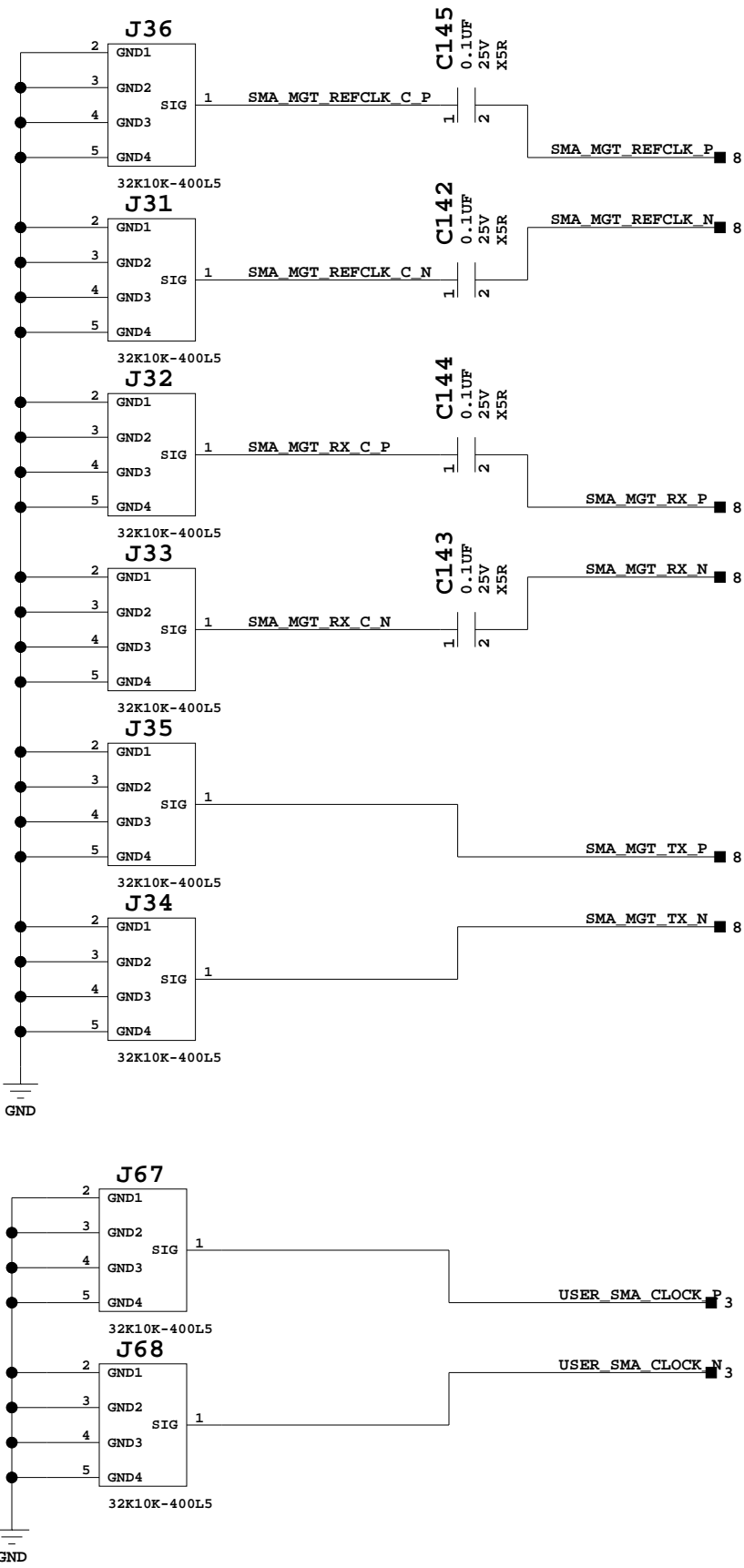


Title:	PCIe x8 Card edge	ASSY P/N: 0431760
	SCHEM, ROHS COMPLIANT	PCB P/N: 1280681
	ZC706 EVALUATION PLATFORM	SCH P/N: 0381513

Date:	10-31-2012_22:05	Ver:	1.1
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Sheet Size: B	Rev: 02
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Sheet	42	of	58	Drawn By	BF
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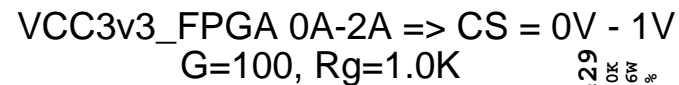
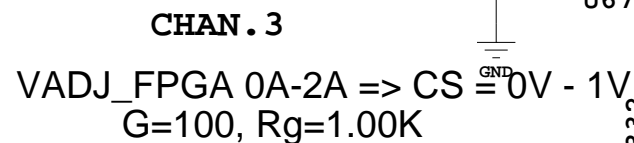
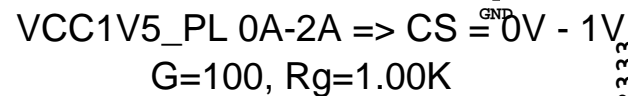
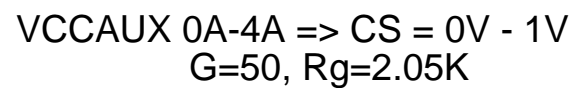


Place near FMC connectors

SMA and Testpoints

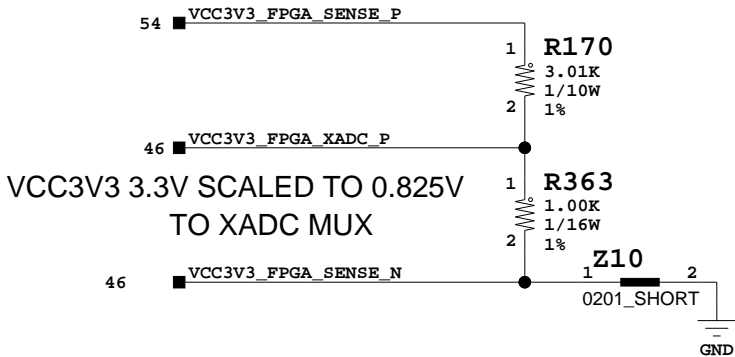
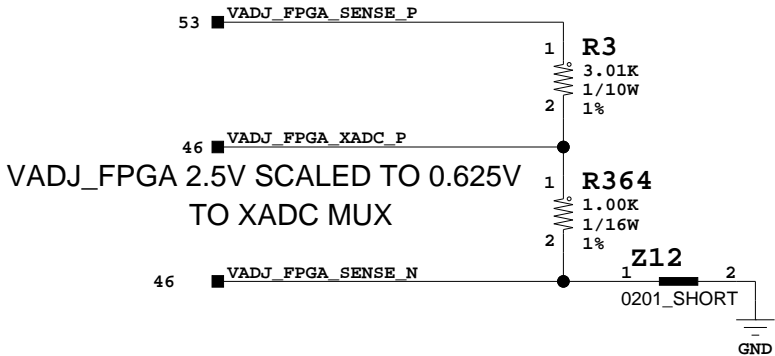
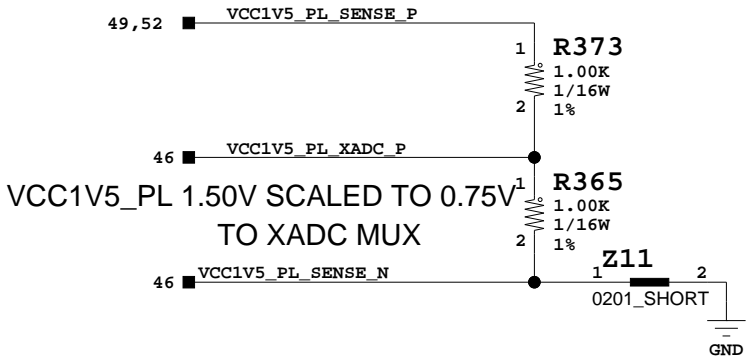
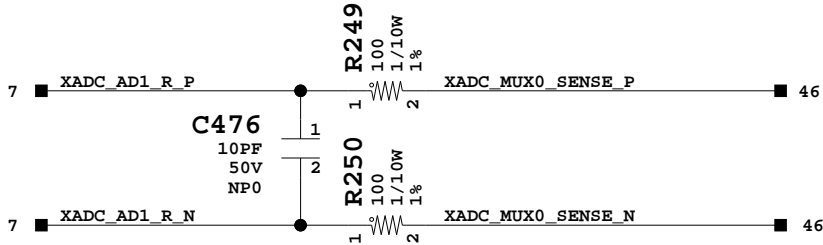
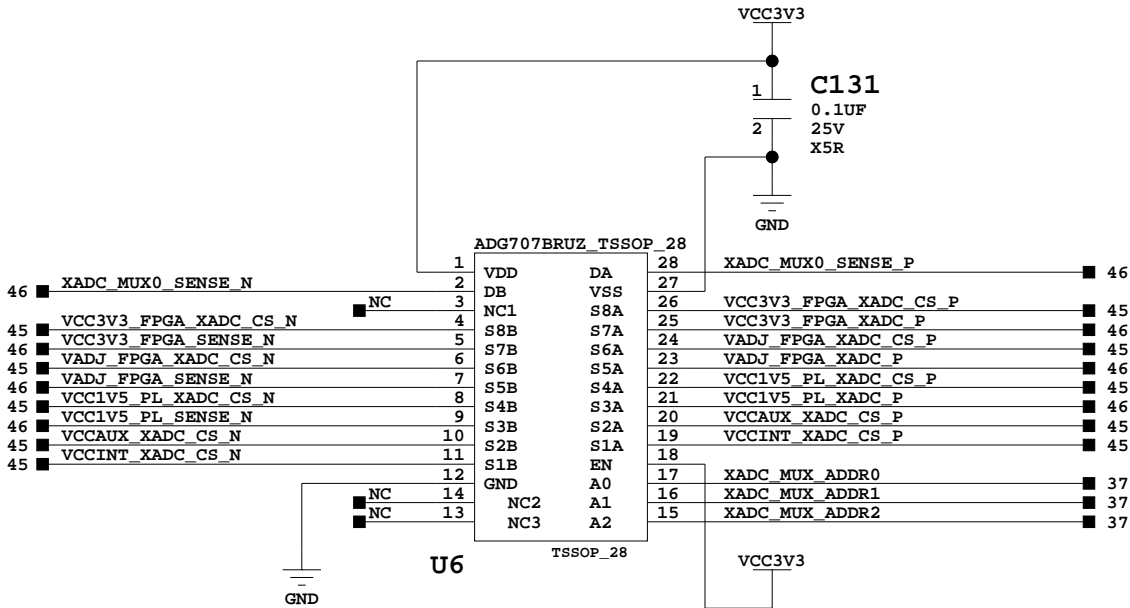
Title: SMA and Testpoints SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
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VCCINT 0A-16A => CS = 0V - 0.8V G=10, Rg=11K
VCCINT 0A-8A => CS = 0V - 0.8V G=20, Rg=5.23K



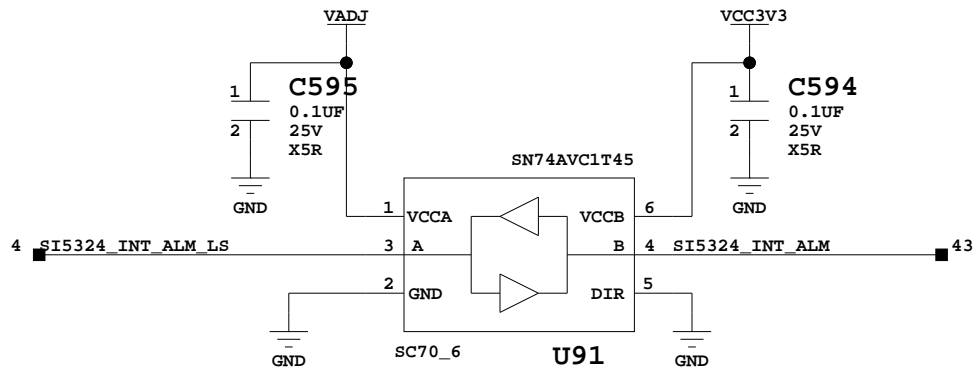
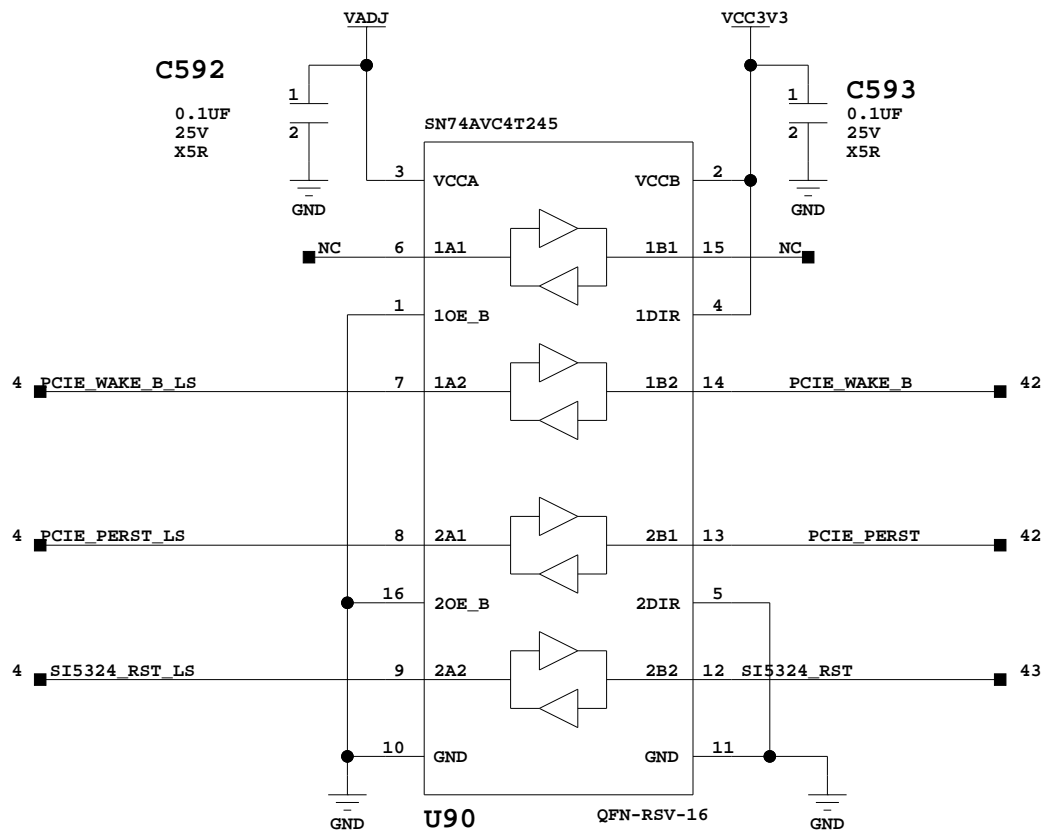
Title: XADC I/F Monitoring Page 1 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date: 10-31-2012_22:05		Ver: 1.1	
Sheet Size: B		Rev: 02	
Sheet 45 of 58		Drawn By BF	

XADC I/F MONITORING CIRCUIT PAGE 2



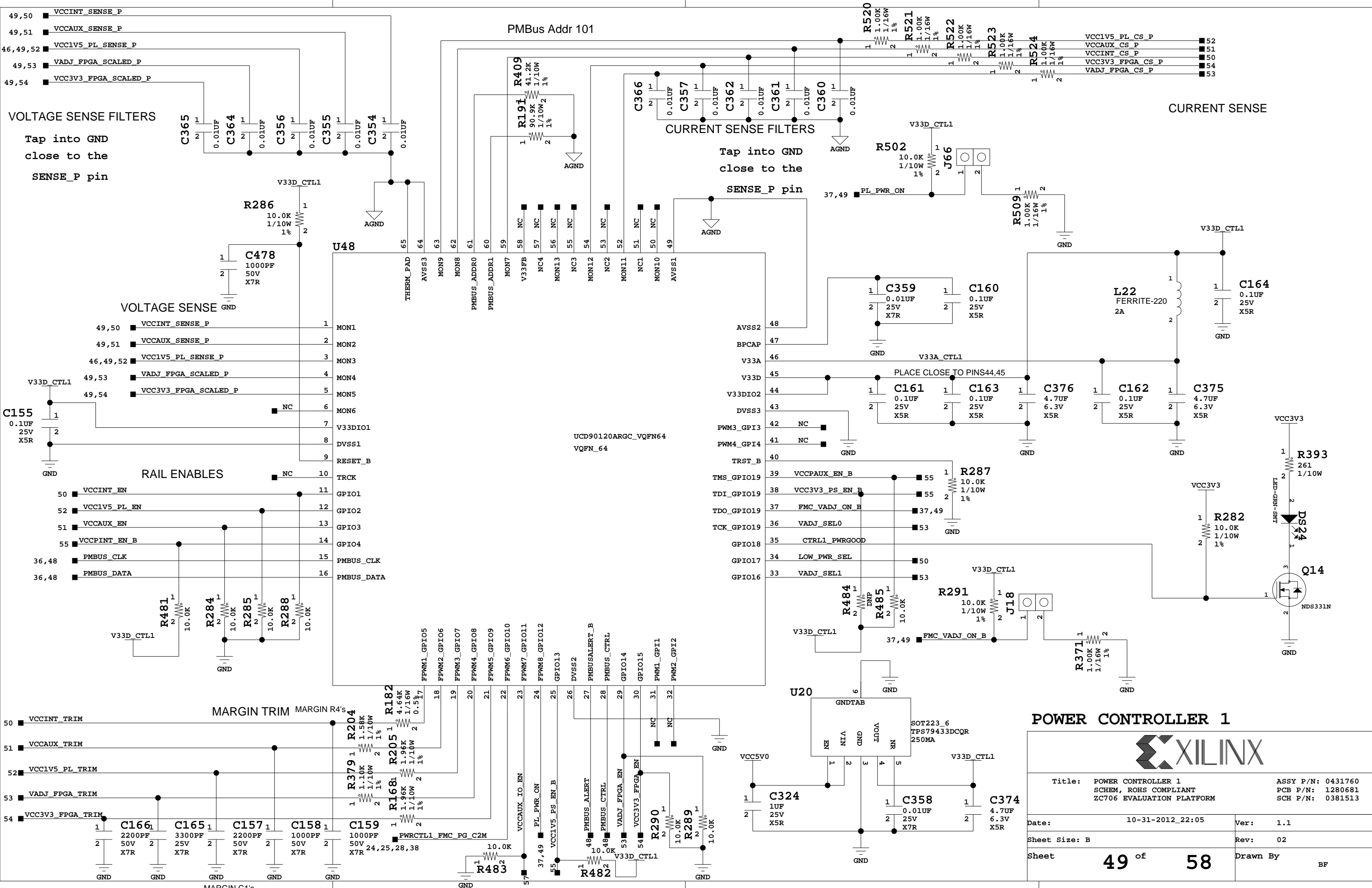
XADC I/F Monitoring Page 2

Title: XADC I/F Monitoring Page 3 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	46 of 58	Drawn By	BF

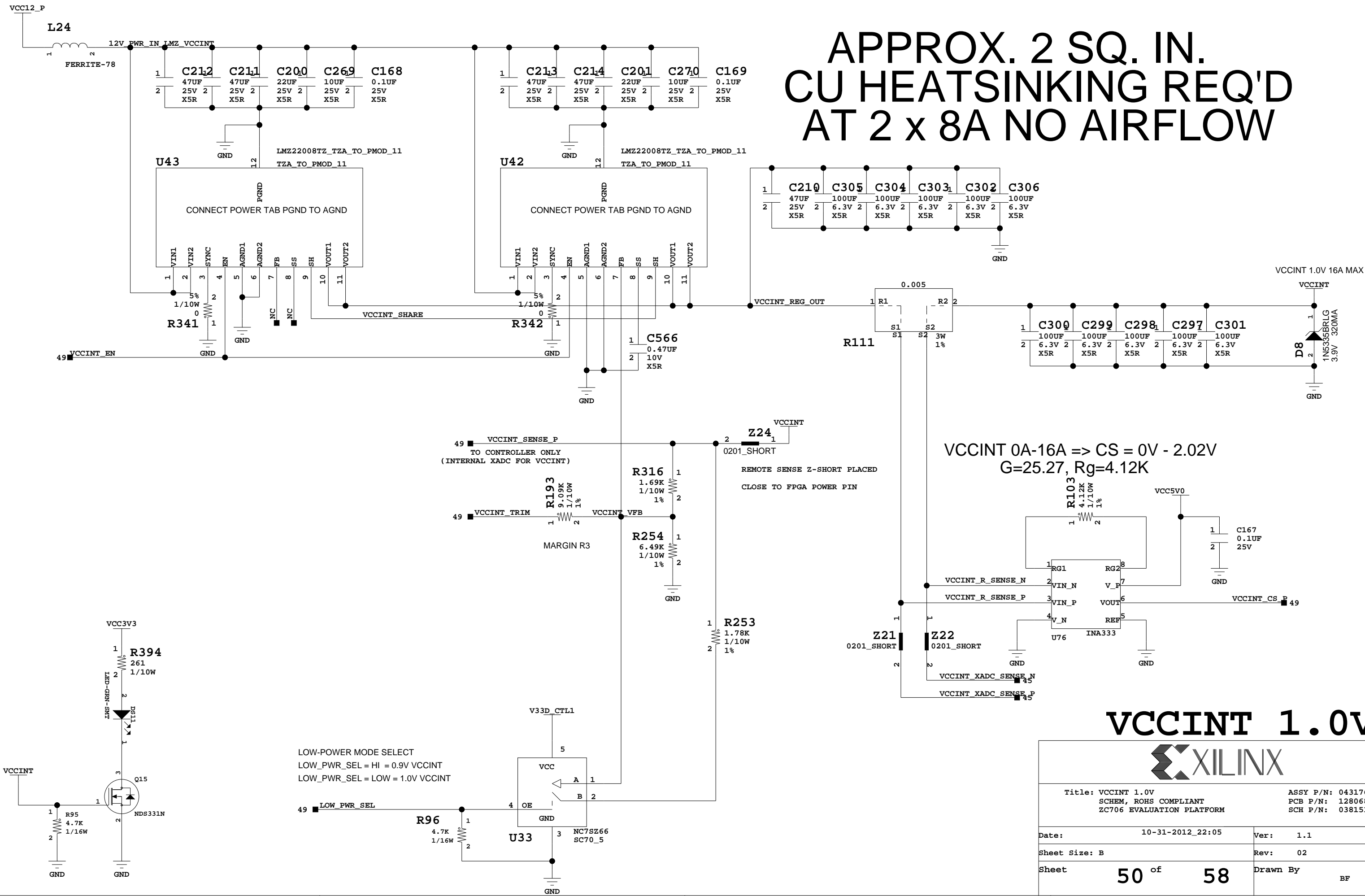


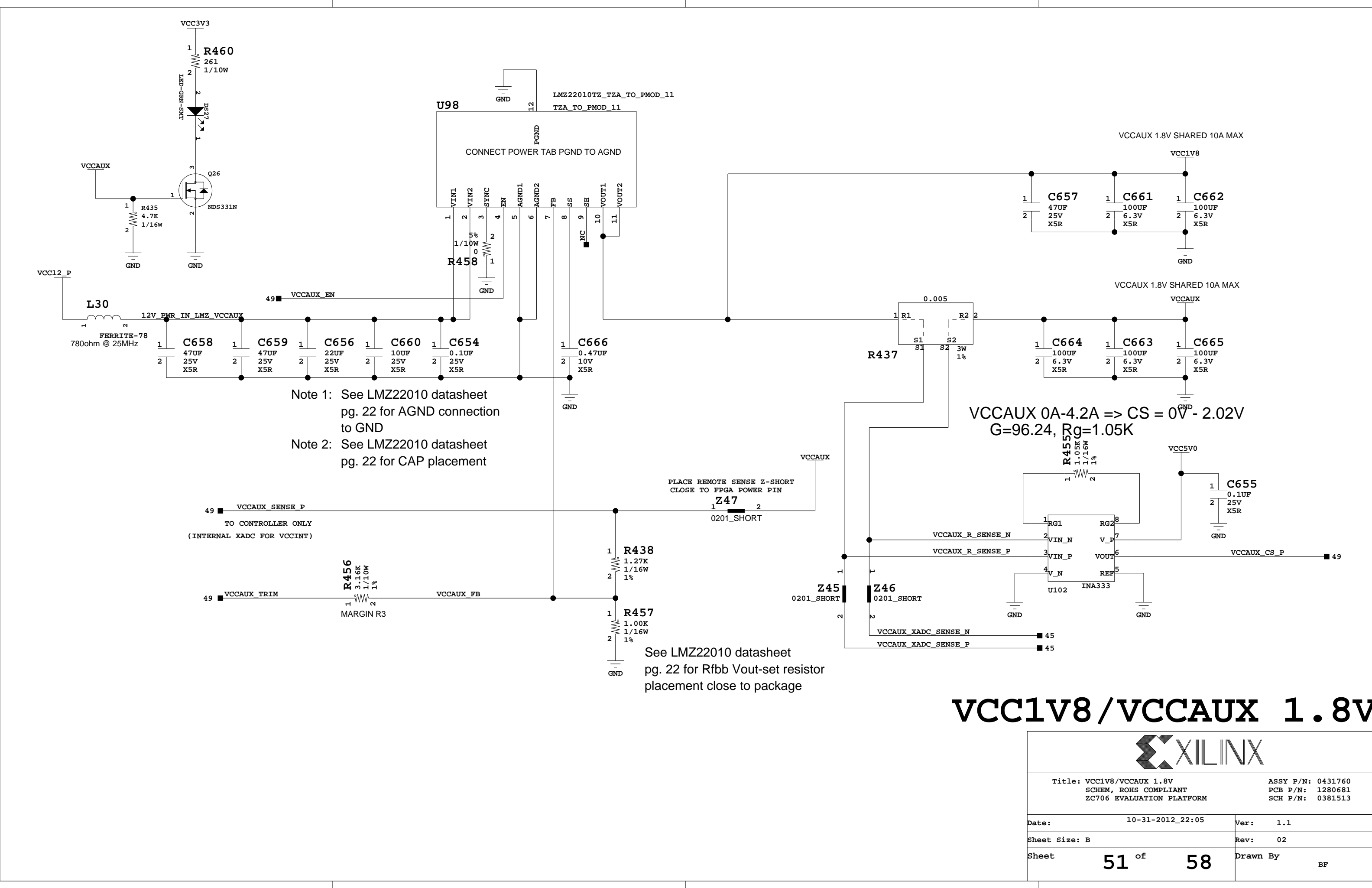
Level Shifters

Title:		ASSY P/N: 0431760	
SCHEM, ROHS COMPLIANT		PCB P/N: 1280681	
ZC706 EVALUATION PLATFORM		SCH P/N: 0381513	
Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
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APPROX. 2 SQ. IN.
CU HEATSINKING REQ'D
AT 2 x 8A NO AIRFLOW





Note 1: See LMZ22010 datasheet
pg. 22 for AGND connection
to GND

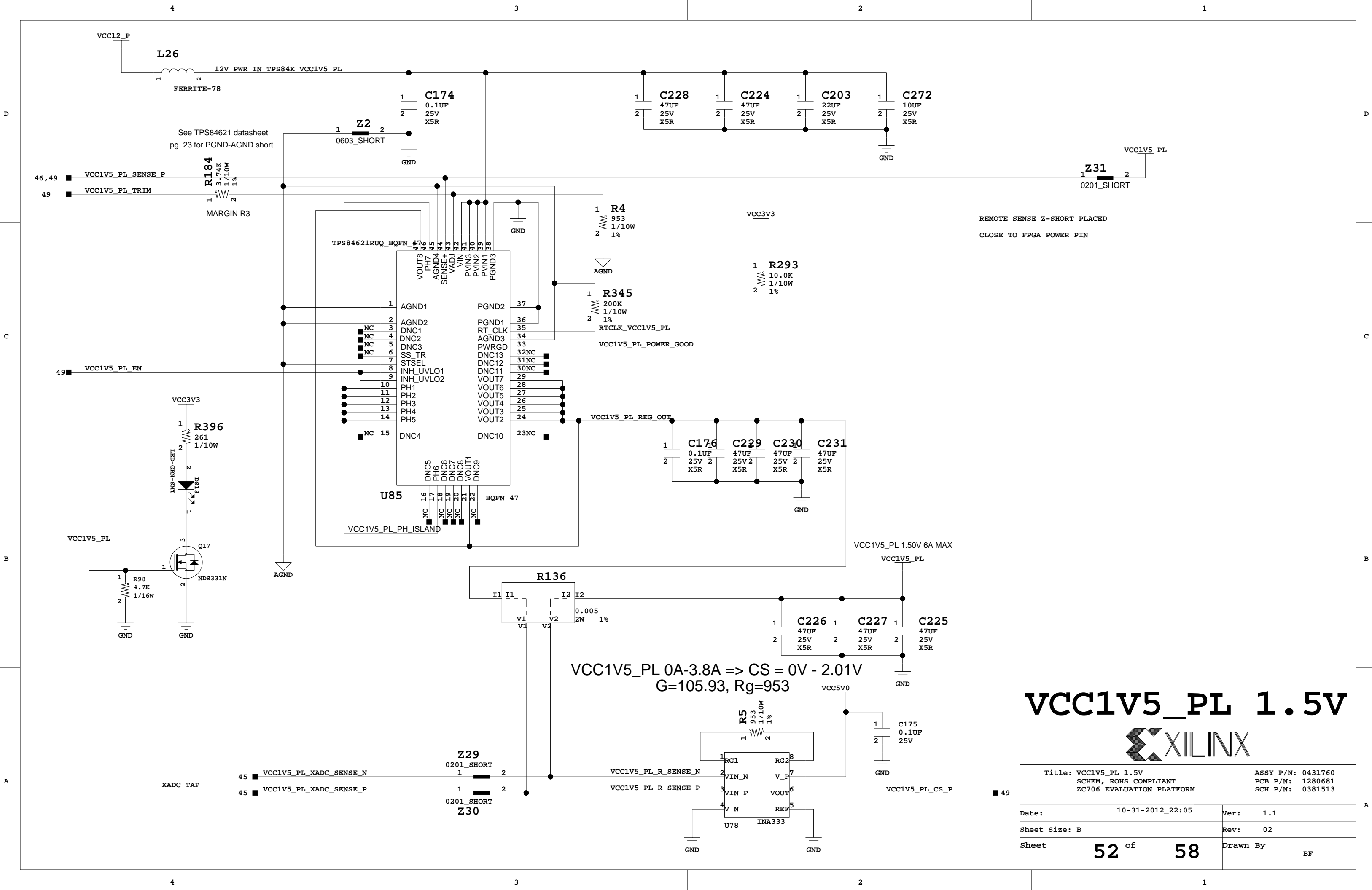
Note 2: See LMZ22010 datasheet
pg. 22 for CAP placement

See LMZ22010 datasheet
pg. 22 for Rfbb Vout-set resistor
placement close to package

VCCAUX 0A-4.2A => CS = 0V - 2.02V
G=96.24, Rg=1.05K

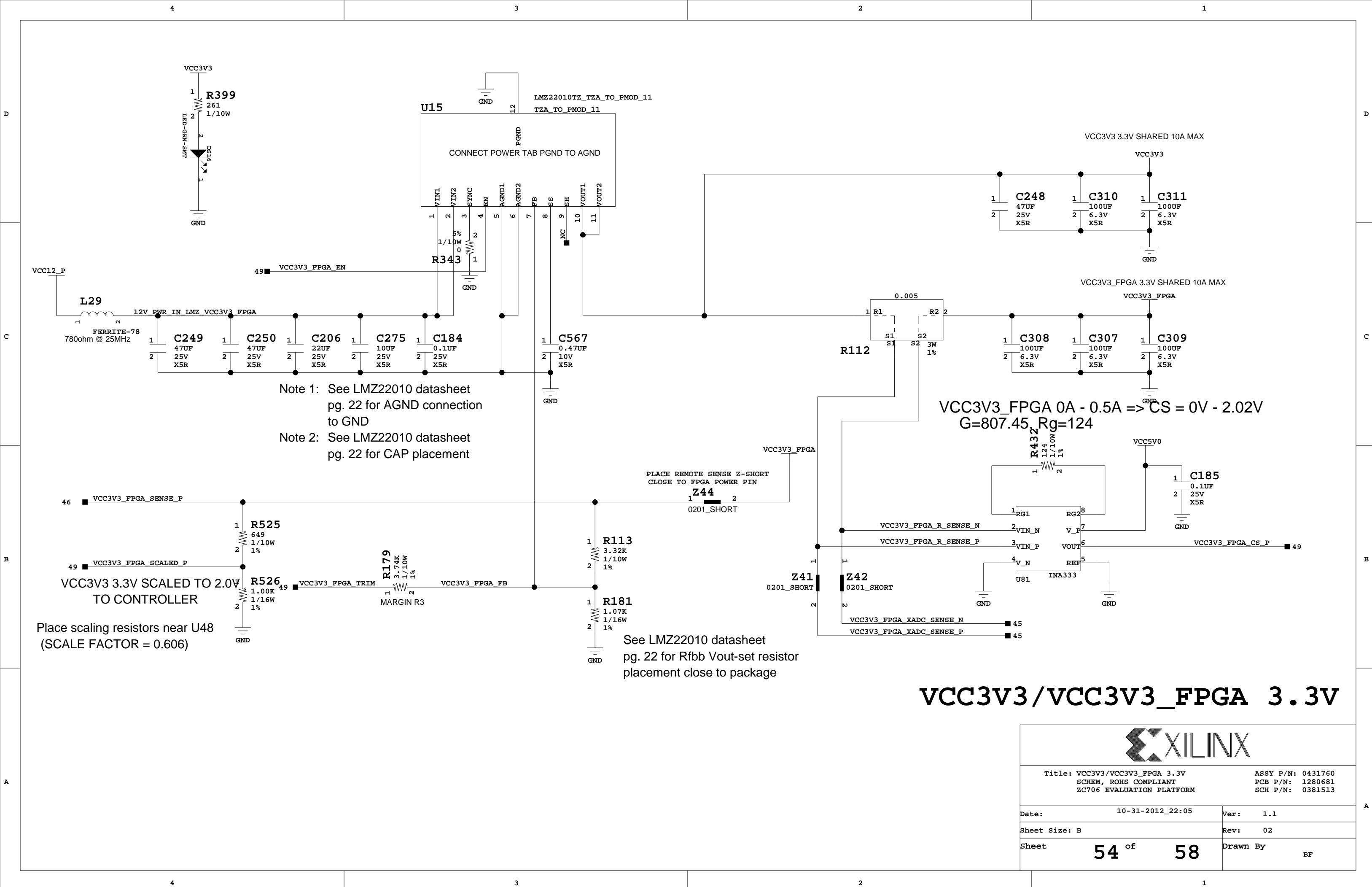
VCC1V8 / VCCAUX 1.8V

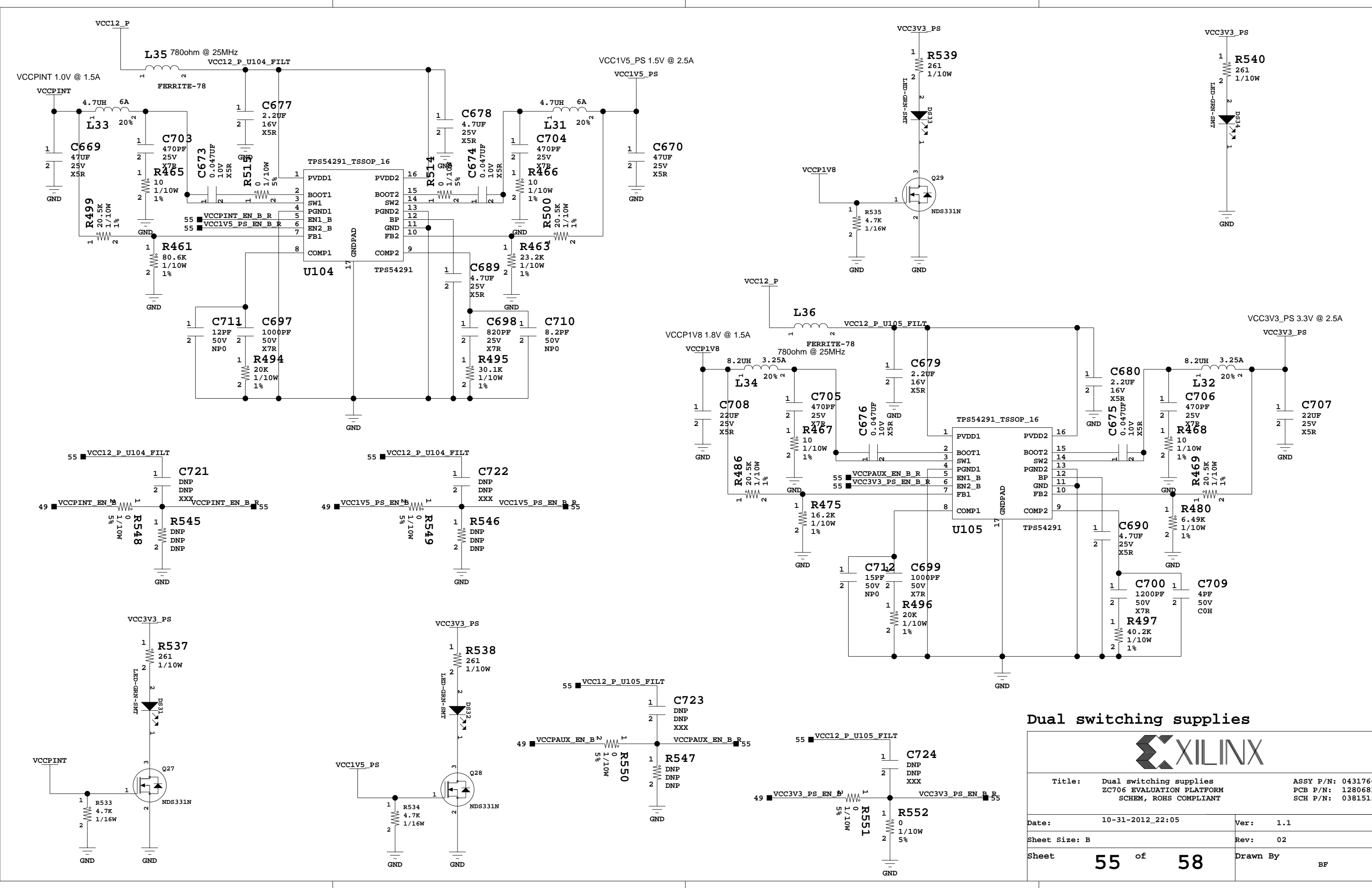
Title: VCC1V8/VCCAUX 1.8V SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	
ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date: 10-31-2012_22:05	Ver: 1.1
Sheet Size: B	Rev: 02
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Title: VADJ (Default 2.5V) SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 53 of 58	Drawn By BF	

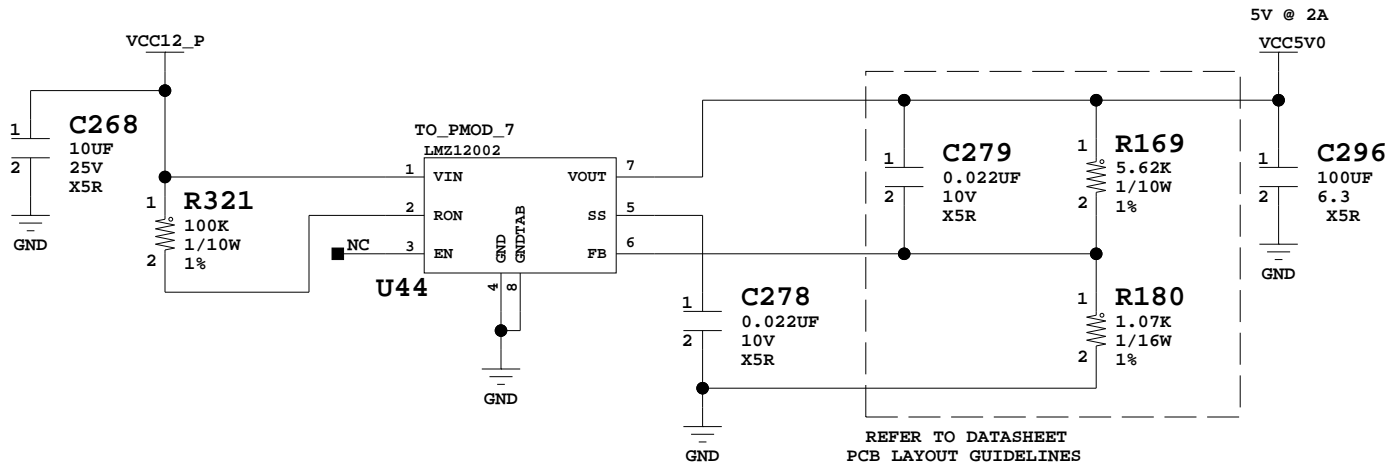
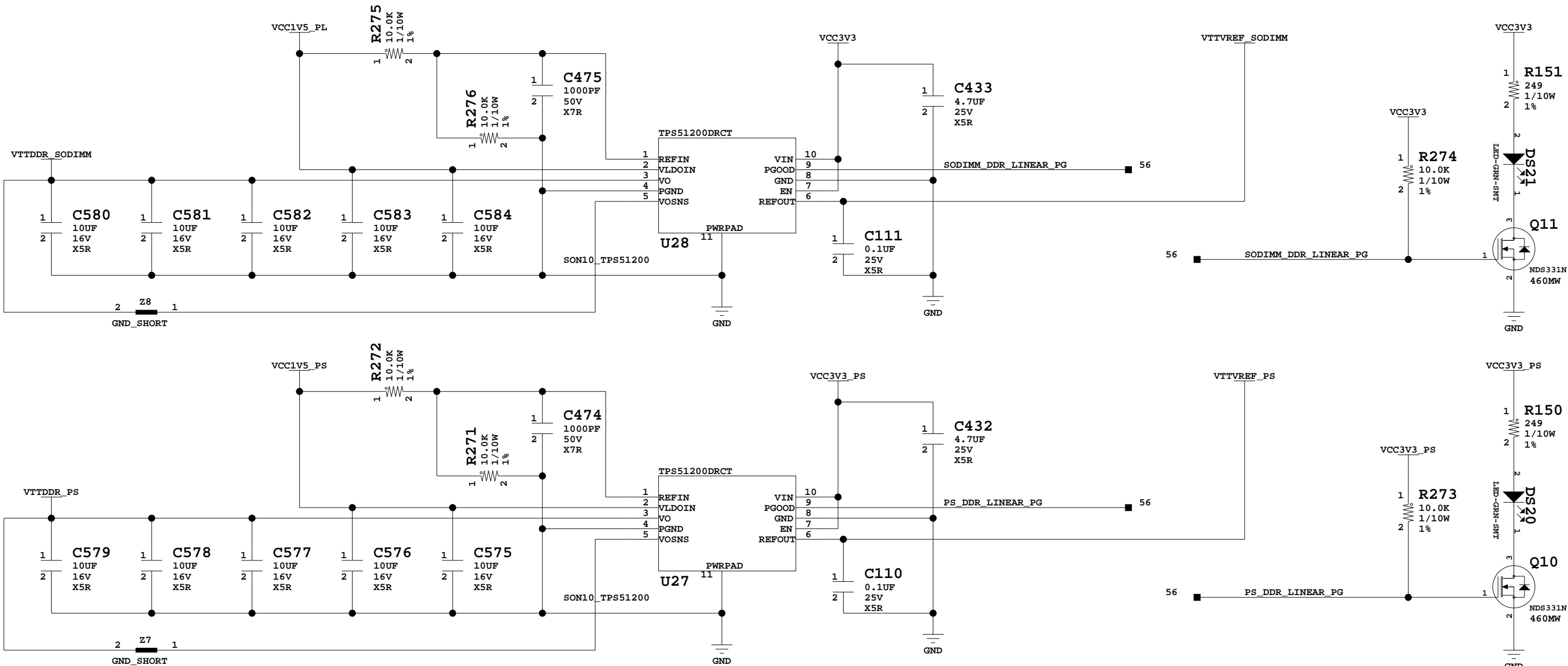




Dual switching supplies



Title: Dual switching supplies ZC706 EVALUATION PLATFORM SCHEM, ROHS COMPLIANT		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 55 of 58	Drawn By BF	



Linear Power Supplies Page 1



Title: Linear Power Supplies Page 1 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 56 of 58	Drawn By BF	

D

C

B

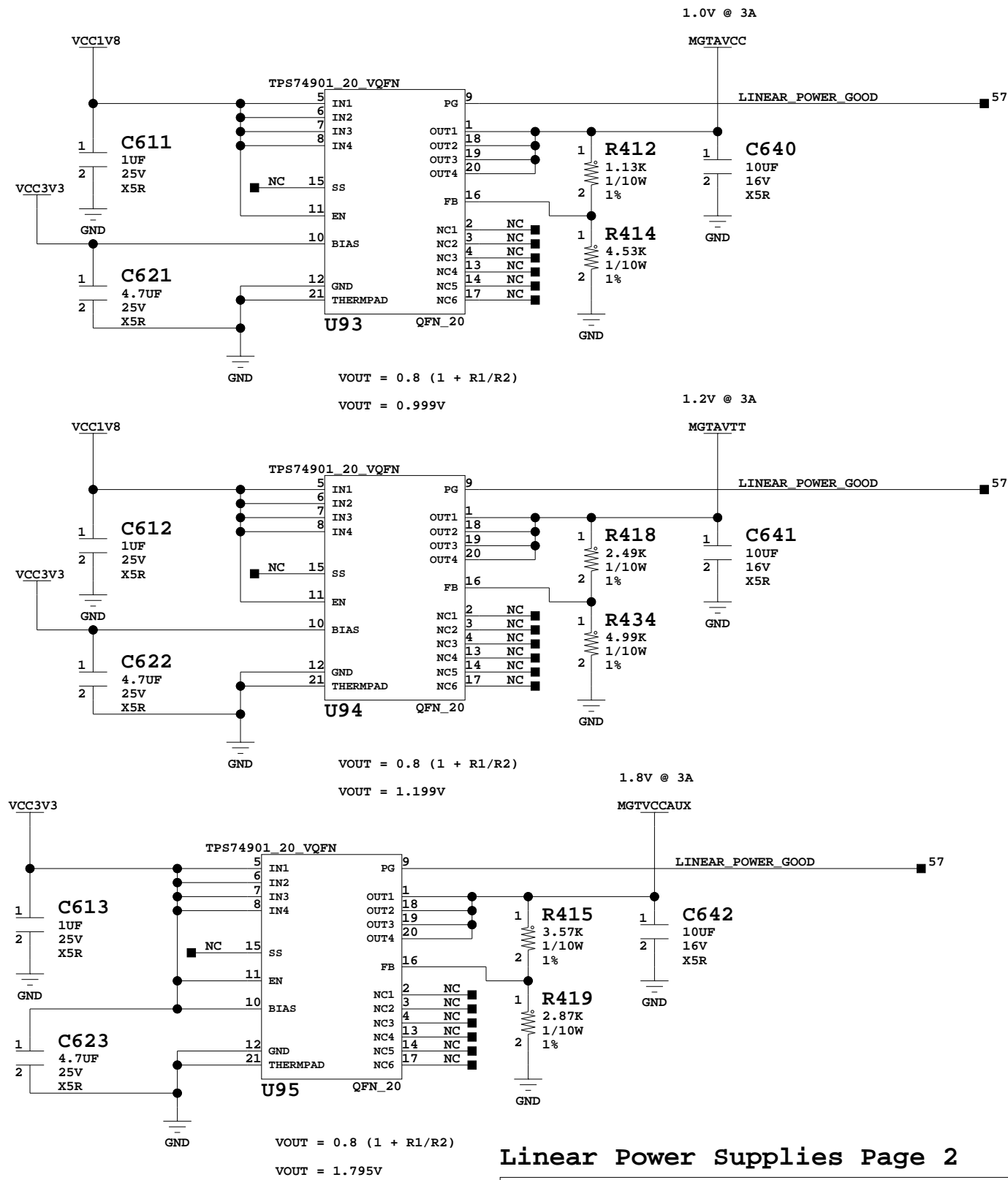
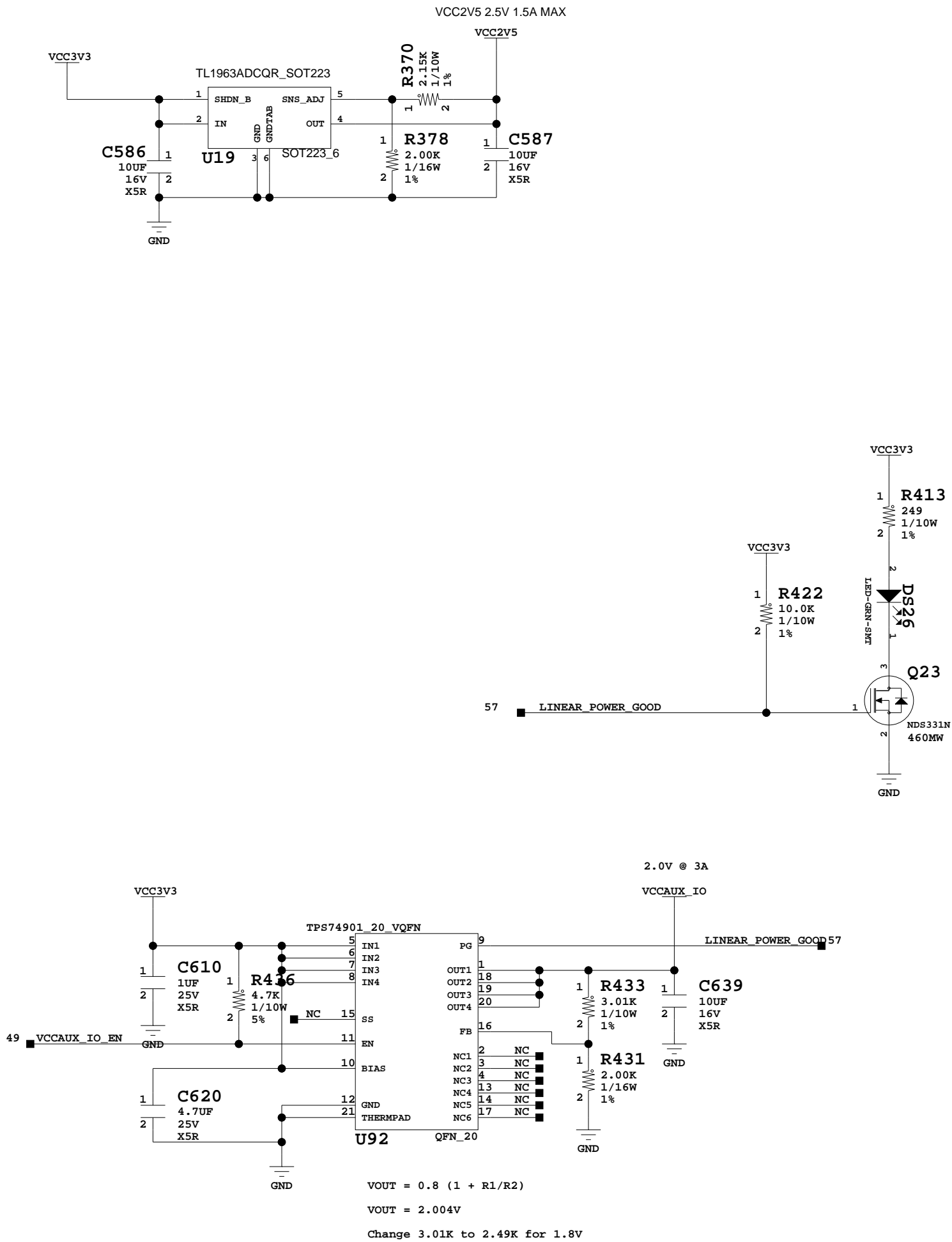
A

D

C

B

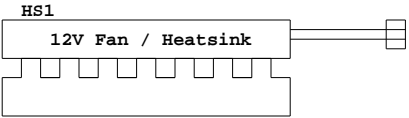
A



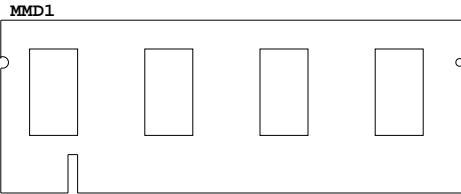
Linear Power Supplies Page 2



Title: Linear Power Supplies Page 2 ZC706 EVALUATION PLATFORM SCHEM, ROHS COMPLIANT		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
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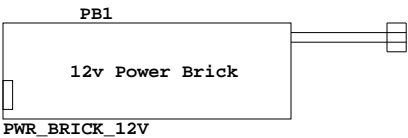
12VDC



DDR3_SODIMM



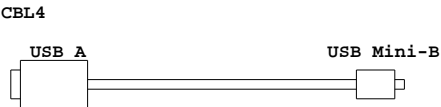
PC_POWER_CABLE
Power Cord



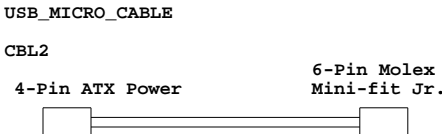
PWR_BRICK_12V



USB Mini-B Cable
USB_MINIB_CABLE

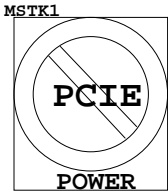


USB Micro-B Cable

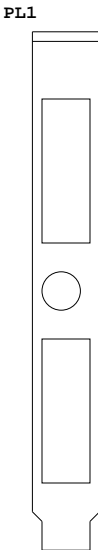


PCIe Adapter Cable

PCIe_ADAPTER_CABLE



PCIE_POWER_STICKER



ZC706_PCIE_PLATE

MJB1



JUMPER_BLOCK_2-PIN

MJB2



JUMPER_BLOCK_2-PIN

MJB3



JUMPER_BLOCK_2-PIN

MJB4



JUMPER_BLOCK_2-PIN

MJB5



JUMPER_BLOCK_2-PIN

MJB6



JUMPER_BLOCK_2-PIN

MJB7



JUMPER_BLOCK_2-PIN

MJB8



JUMPER_BLOCK_2-PIN

MJB9



JUMPER_BLOCK_2-PIN

MJB10



JUMPER_BLOCK_2-PIN

MJB11



JUMPER_BLOCK_2-PIN

MJB12



JUMPER_BLOCK_2-PIN

MJB13



JUMPER_BLOCK_2-PIN

MJB14



JUMPER_BLOCK_2-PIN

MJB15



JUMPER_BLOCK_2-PIN

MJB16



JUMPER_BLOCK_2-PIN

MJB17



JUMPER_BLOCK_2-PIN

MJB18



JUMPER_BLOCK_2-PIN

MJB19



JUMPER_BLOCK_2-PIN

MJB20



JUMPER_BLOCK_2-PIN

MJB21



JUMPER_BLOCK_2-PIN

MJB22



JUMPER_BLOCK_2-PIN

MSO1



STANDOFF_0P625

MW1



WASHER_FLAT_RUBBER BUMPER

MRB1



MS1

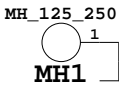


MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"

MS12



MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"

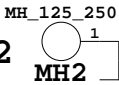


MH1



GND

NOTE: No standoff foot on MH2



MH2



GND

MSO3



STANDOFF_0P625

MW3



WASHER_FLAT_4 RUBBER BUMPER

MRB3



MS3

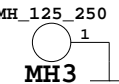


MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"

MS14



MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"



MH3



GND

MSO4



STANDOFF_0P500

MW4



WASHER_FLAT_4RUBBER BUMPER

MRB4



MS4

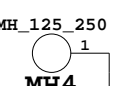


MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"

MS15



MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"



MH4



GND

MSO5



STANDOFF_0P500

MW5



WASHER_FLAT_4RUBBER BUMPER

MRB5



MS5

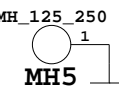


MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"

MS16



MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"



MH5



GND

MSO6



STANDOFF_0P625

MW6



WASHER_FLAT_4 RUBBER BUMPER

MRB6



MS6

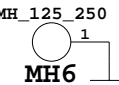


MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"

MS17



MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"



MH6



GND

NOTE: These two standoffs are shorter and must be connected to MH4 and MH5 to level the board properly

Mechanical Components



Title: Mechanical Components SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513

Date:	11-9-2012_11:18	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	58 of 58	Drawn By	BF