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**AXI XGS decoder core**

**User Guide**

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| Authors | Gert Rijckbosch |
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# Disclaimer

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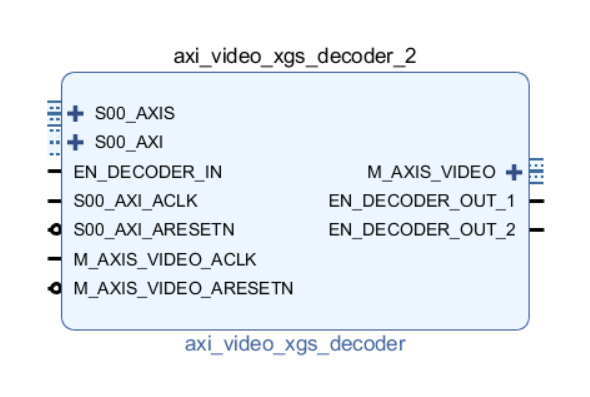
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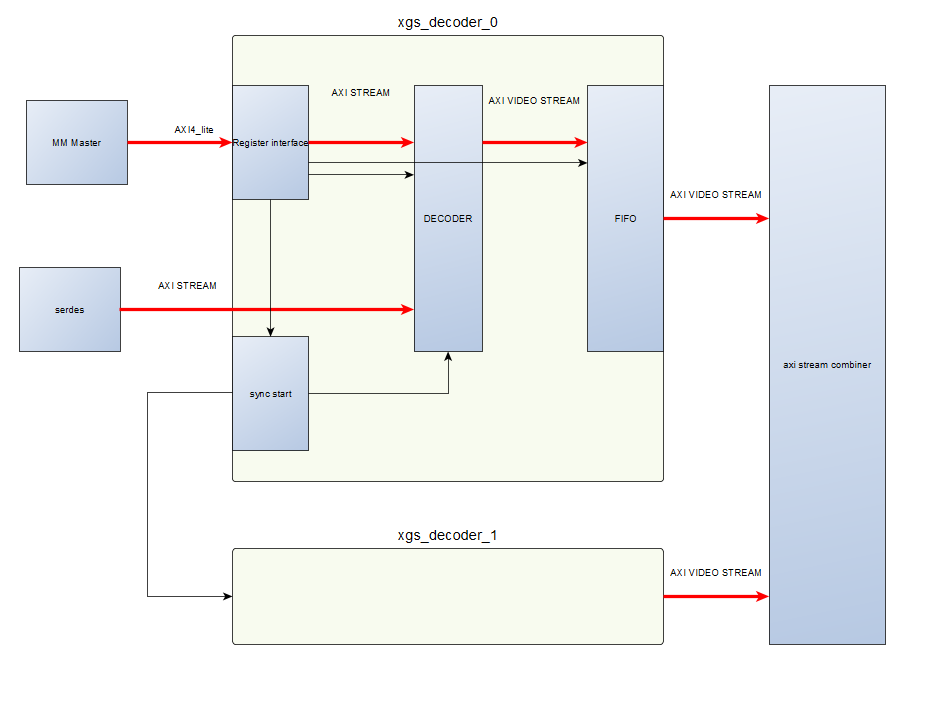
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# Description

AXI XGS decoder is an IP block that takes data of the xgs deser axi streaming and converts it to an axi video streaming, writing only selected raw data to the axi video streaming bus.



# Main Blocks



## Register interface

The register interface connects trough an AXI4\_LITE interface to the XGS\_DECODER IP.

Specific registers and their function are described in the section register map.

## Sync start

The sync start block drives an en\_decoder signal to the xgs\_decoder IP were it is initiated and all other xgs\_decoder IP’s. This allows all decode blocks to start synchronously. This is necessary to make sure all decoder blocks are decoding the same frame.

## Decoder

The decoder block decodes the data stream and creates SOF, EOL and valid signals according to the AXI4 Video streaming standard.

## FIFO

The FIFO is used as an interface to the AXI4 video stream. It’s a shallow FIFO allowing for some necessary backpressure from the combiner.

# Parameters

Following custom parameters control this block:

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Default value | Description | Editable |
| C\_FAMILY | kintexu | Family generic, hidden in customization interface. Not editable. | n |
| C\_NROF\_DATACONN | 12 | Total number of incoming HiSpi lanes | y |
| C\_INPUT\_DATAWIDTH | 12 | Number of bits per pixel of incoming data | n |
| C\_AXIS\_TDATA\_WIDTH | 12\*12 | Axi streaming data width | n |
| C\_AXIS\_TUSER\_WIDTH | 1 | Number of tuser bit per byte on axi streaming slave side (used for SOF) | n |
| C\_AXIS\_TDEST\_WIDTH | 1 | Number of tdest bit not used for now | n |
| C\_AXIS\_TID\_WIDTH | 1 | Number of tid bit not used for now | n |
| C\_S00\_AXI\_DATA\_WIDTH | 32 | Axi4 lite data width | n |
| C\_S00\_AXI\_ADDR\_WIDTH | 12 | Axi4 lite address width | n |
| C\_USEEXT\_EN | 1 | Enable for the use of the external decoder enable pin, should be used when more than one decoder IP is used. | y |
| NumberOffEnables | 2 | The number of decoder enable output pins that is visible (on the master decoder there should be 1 for each decoder , master and slaves(s)) | y |

# Port Description

Signals grouped as per clock domain.

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **Interface** | **Signal Type** | **Description** |
| **Clock Domain:** AXI\_MM\_CLOCK | | | |
| S00\_AXI\_ACLK | clock | input | Axi clock |
| S00\_AXI\_ARESETN | reset | input | Active low reset |
| S00\_AXI | AXI LITE | Slave | Axi MM bus interface with 32-bit register interface and 16 registers. |
| EN\_DECODER\_IN | synchro | input | synchronization signal input in order to start multiple decoder blocks at the same time |
| EN\_DECODER\_OUT\_n | synchro | output | synchronization signal output in order to start multiple decoder blocks at the same time |
| **Clock Domain:** AXI\_STREAM\_CLK | | | |
| S\_AXIS\_ACLK | clock | input | Axi Slave ST clock |
| S\_AXIS\_ARESETN | reset | input | Active low reset |
| S\_AXIS | AXI STREAM | Sink | Axi Slave ST bus interface |
| M\_AXIS\_VIDEO\_ACLK | clock | input | Axi Master ST clock |
| M\_AXIS\_VIDEO\_ARESETN | reset | input | Active low reset |
| M\_AXIS\_VIDEO | AXI VIDEO STREAM | Source | Axi Master ST bus interface |

# Register map

## Overview

The following registers are accessible through the AXI4 Lite Slave (S\_AXI) interface.

|  |  |  |  |
| --- | --- | --- | --- |
| **Address Offset** | **Register Name** | **R/W** | **Description** |
| 0x0000 | ENABLE | R/W | Bit 0 is used to synchronously enable all possible xgs\_decoder IP blocks |
| 0x0004 | SYNC\_WORD4 | R/W | Contains all word necessary for synchronization, See detailed description for more info. |
| 0x0008 | CHANNEL\_SETTINGS | R/W | Contains all channel related settings. See detailed description for more info |
| 0x000C | FRAMESCNT | R | Number of frames captured per stream |
| 0x0010 | IMGLINESCNT | R | Number of image lines captured per frame |
| 0x0014 | EMBLINESCNT | R | Number of embedded lines captured per frame |
| 0x0018 | IMGPIXELCNT | R | Number of pixels captured per lane per frame |
| 0x001C | CLOCKSCNT | R | Number of clocks counted per frame |
| 0x0020 | STARTLINECNT | R | Number of SOL decoded |
| 0x0024 | ENDLINECNT | R | Number of EOL decoded |
| 0x0028 | STATUSBITS | R | Debug feature. See detailed description for more info. |
| 0x002C | CRCSTATUS | R | CRC status bits per HiSpi data lane. A ‘1’ indicates CRC error occurred on that lane number. |
| 0x0030 | XSAMPLE | R/W | Configure on which pixel number the pixel trigger will be fired. |
| 0x0034 | YSAMPLE | R/W | Configure on which line number the line trigger will be fired. |
| 0x0038 | FRAMESAMPLE | R/W | Configure on which frame number the frame trigger will be fired. |
| 0x003C | RFU |  |  |

## Detailed description

### ENABLE: 0x0000

|  |  |  |
| --- | --- | --- |
| **Bit Offset** | **Field Name** | **Description** |
| [31:24] | RESERVED | Not used |
| [23:16] | TDEST | RFU |
| [15:12] | RESERVED | Not used |
| [11:8] | TID | RFU |
| [7:5] | RESERVED | Not used |
| 4 | reset\_fifo | 0: fifo decoder in operational mode  1: fifo decoder in reset mode |
| 3 | write\_crc | 0: crc data is not written to axi streaming bus  1: crc data is written to axi streaming bus |
| 2 | write\_emb | 0: embedded data is not written to axi streaming bus  1: embedded data is written to axi streaming bus |
| 1 | write\_img | 0: image data is not written to axi streaming bus  1: image data is written to axi streaming bus |
| 0 | ENABLE\_DECODER | 0: disable decoder: no HiSpi data is processed  1: enable decoder: HiSpi data is decoded and will be send to the axi streaming bus |

### SYNC\_WORD4: 0x0004

|  |  |  |
| --- | --- | --- |
| **Bit Offset** | **Field Name** | **Description** |
| 31 | RESERVED | Not used |
| [30:26] | eol\_value | EOL value to decode |
| [25:21] | sol\_img\_value | SOL image value to decode |
| [20:16] | sol\_emb\_value | SOL embedded value to decode |
| [15] | RESERVED | Not used |
| [14:10] | eof\_value | EOF value to decode |
| [9:5] | sof\_img\_value | SOF image value to decode |
| [4:0] | sof\_emb\_value | SOF embedded value to decode |

### CHANNEL\_SETTINGS: 0x0008

|  |  |  |
| --- | --- | --- |
| **Bit Offset** | **Field Name** | **Description** |
| [31:18] | RESERVED | Not used |
| [17:6] | CHANNELS\_ENABLE | One hot encoding for the channels being used. ‘1’ means channel is used |
| 5 | CRC\_LANE\_ENABLE | Must follow the same settings as the DUT (HiSpi) |
| 4 | FILL\_ENABLE | Must follow the same settings as the DUT (HiSpi) |
| [3:0] | DATAWIDTH | Number of bits per pixel the DUT is outputting (can be 10 or 12, default is 12). |

### STATUSBITS: 0x0028

|  |  |  |
| --- | --- | --- |
| **Bit Offset** | **Field Name** | **Description** |
| [31:19] | RESERVED | Not used |
| 18 | FRAME\_TRIGGER | Frame trigger flag |
| 17 | LINE\_TRIGGER | Line trigger flag |
| 16 | PIXEL\_TRIGGER | Pixel trigger flag |
| [15:9] | RESERVED | Not used |
| 8 | FIFO\_AFULL | FIFO almost full flag |
| 7 | FIFO\_FULL | FIFO full flag |
| 6 | FIFO\_AEMPTY | FIFO almost empty flag |
| 5 | FIFO\_EMPTY | FIFO empty flag |
| 4 | FIFO\_ERROR | FIFO error flag |
| 3 | FIFO\_RDEN | FIFO read operation ongoing |
| 2 | FIFO\_WR\_EN | FIFO write operation ongoing |
| 1 | TIMEOUT\_DEC | Decoder timeout flag |
| 0 | EN\_DECODER | Decoder active flag |

# Programming Sequence

* Program SYNC\_WORD4 and CHANNEL\_SETTINGS to the desired values.
* Follow all steps to program the deser block
* Enable decoder by putting bit 0 of ENABLE register(0x00) to ‘1’
* Enable the deser block to output data