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**AXI XGS Deserializer core**

**User Guide**

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# Disclaimer

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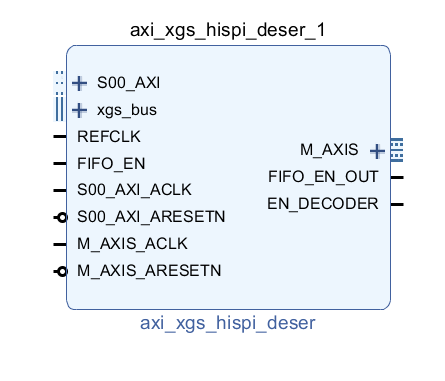
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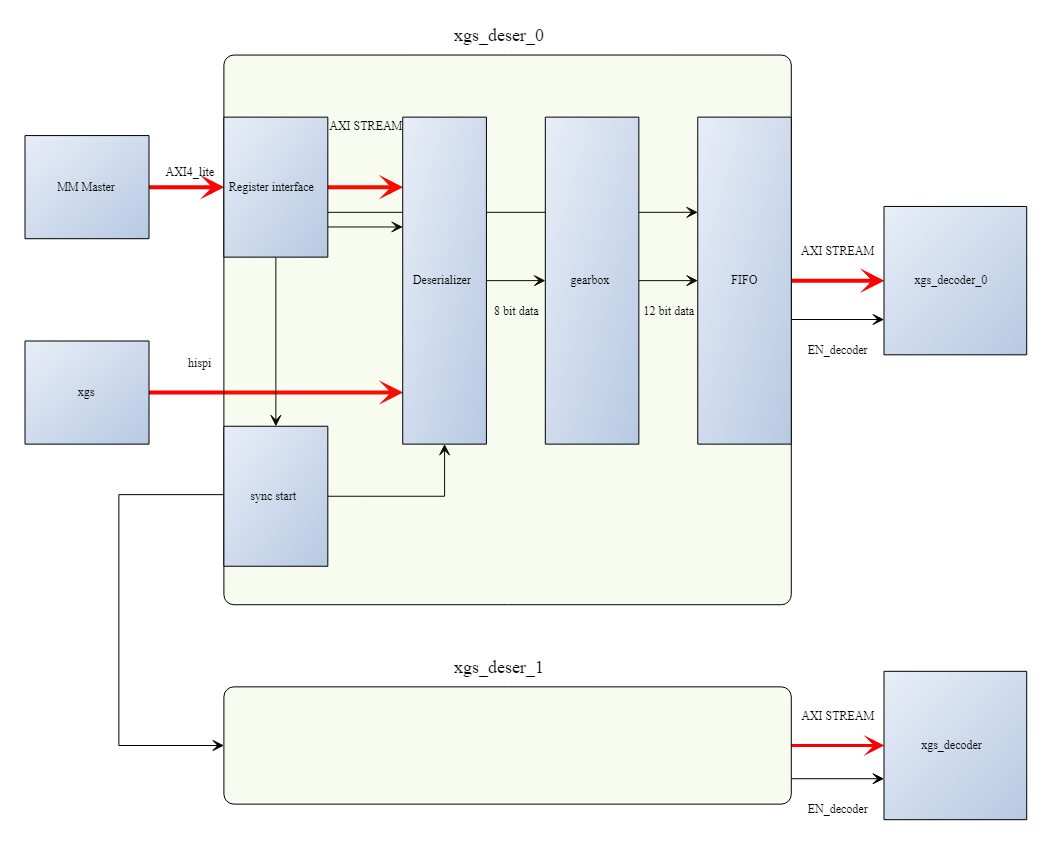
# Description

The axi\_xgs\_hispi\_deser is an IP block that takes data of the xgs family HiSpi lanes and converts it into an AXI streaming interface. This streaming interface can be connected to a decoder block to obtain the raw data content.

The IP performs bit and word alignment for Xilinx FPGA’s.



# Main Blocks



## Register interface

The register interface connects trough an AXI4\_LITE interface to the XGS deserializer IP.

Specific registers and their function are described in the section register map.

## Deserializer

Converts the serial incoming data stream to a parallel word of the native width of the FPGA.

## Gearbox

Converts the words in the FPGA’s native width into the DUT’s parallel word size.

## FIFO

FIFO used to convert the data stream into an AXI stream protocol.

# Parameters

Following custom parameters control this block

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Default value | Description | Editable |
| C\_SIM | 0 | Use simulation model | N |
| C\_NROF\_DATACONN | 12 | Number of HiSpi data input channels | Y |
| C\_INPUT\_DATAWIDTH | 12 | Number of bits per pixel of incoming data | N |
| C\_M\_AXIS\_TDATA\_WIDTH | 12\*12 | Master axi streaming bus data width | N |
| C\_M\_AXIS\_TUSER\_WIDTH | 1 | Master axi streaming number of Tuser bits | N |
| C\_S00\_AXI\_DATA\_WIDTH | 32 | Axi4 lite data width | N |
| C\_S00\_AXI\_ADDR\_WIDTH | 12 | Axi4 lite address width | N |
| C\_SERDES\_FAMILY | ULTRASCALE | FPGA family (only Xilinx Ultrascale supported) | N |
| C\_REFCLK\_F | 200 | Reference clock speed (MHz) | N |
| C\_SERDES\_DATAWIDTH | 8 | Depth of the FPGA device specific SERDES primitive | N |

# Port Description

Signals grouped as per clock domain.

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **Interface** | **Signal Type** | **Description** |
| **Clock Domain:** REF\_CLOCK | | | |
| REFCLK | clock | input | Reference clock for serdes delay taps |
| **Clock Domain:** XGS\_CLOCK | | | |
| DATA\_P | xgs\_bus | input | HiSpi differential data\_p input channels from the xgs device |
| DATA\_N | xgs\_bus | input | HiSpi differential data\_n input channels from the xgs device |
| D\_CLK\_P | xgs\_bus | clock | HiSpi differential clock\_p input channels from the xgs device |
| D\_CLK\_N | xgs\_bus | clock | HiSpi differential clock\_n input channels from the xgs device |
| **Clock Domain:** AXI\_MM\_CLOCK | | | |
| S00\_AXI\_ACLK | clock | input | Axi clock |
| S00\_AXI\_ARESETN | reset | input | Active low reset |
| S00\_AXI | AXI LITE | Slave | Axi MM bus interface with 32-bit register interface and 16 registers. |
| FIFO\_EN | synchro | input | synchronization signal input in order to start multiple axi\_xgs\_hispi\_deser IP blocks at the same time |
| FIFO\_EN\_OUT | synchro | output | synchronization signal output in order to start multiple axi\_xgs\_hispi\_deser IP blocks at the same time |
| EN\_DECODER | synchro | output | synchronization signal output in order to start multiple decoder blocks at the same time (legacy) |
| **Clock Domain:** AXI\_STREAM\_CLK | | | |
| M\_AXIS\_ACLK | clock | input | Axi Master ST clock |
| M\_AXIS\_ARESETN | reset | input | Active low reset |
| M\_AXIS | AXI STREAM | Source | Axi Master ST bus interface |

# Register map

## Overview

The following registers are accessible through the AXI4 Lite Slave (S00\_AXI) interface.

|  |  |  |  |
| --- | --- | --- | --- |
| **Address Offset** | **Register Name** | **R/W** | **Description** |
| 0x0000 | COMMAND | RW | Every bit can be used to send a command, the busy can be polled on the same bit |
| 0x0004 | TRAINING | W | Lowest bits represent the training/ idle word needed to do word alignment must be set to the same value as the DUT’s idle (blanking) word |
| 0x0008 | ENABLE\_TRAINING | W | One hot encoding to enable training per attached channel. Set to one for every active channel. |
| 0x000C | MANUAL\_TAP | W | Setting to change the delay tap on the data in order to get good bit to clock alignment |
| 0x0010 | ENABLE | W | Register used to enable and reset FIFO and DECODER  See detailed descripting for more details |
| 0x0014 | SERDES\_CLK\_STATUS | R | STATUS of the serdes clocks |
| 0x0018 | SERDES\_WORD\_ALIGN | R | STATUS of the word alignment |
| 0x001C | RFU |  |  |
| 0x0020 | SERDES\_SLIP\_COUNT\_0 | R |  |
| 0x0024 | SERDES\_SLIP\_COUNT\_1 | R |  |
| 0x0028 | SERDES\_SLIP\_COUNT\_2 | R |  |
| 0x002C | SERDES\_SHIFT\_STATUS\_0 | R | 6 bit per HiSpi lane: |
| 0x0030 | SERDES\_SHIFT\_STATUS\_1 | R |  |
| 0x0034 | SERDES\_SHIFT\_STATUS\_2 | R |  |
| 0x0038 | SERDES\_ERROR | R | Serdes error flag |
| 0x003C | RFU |  |  |

## Detailed register description

### COMMAND: 0x0000

|  |  |  |
| --- | --- | --- |
| **Bit Offset** | **Field Name** | **Description** |
| [31:1] | RESERVED | Not used |
| 0 | (W) START\_TRAINING  (R) BUSY\_TRAINING | Bit used to start the training algorithm and read back if the training is finished.  Once training is finished the software should check if all succeeded ( see other registers) |

### TRAINING: 0x0004

|  |  |  |
| --- | --- | --- |
| **Bit Offset** | **Field Name** | **Description** |
| [31:12] | RESERVED | Not used |
| [11:0] | TRAINING\_WORD | Configuration of serdes training word |

### ENABLE\_TRAINING: 0x0008

|  |  |  |
| --- | --- | --- |
| **Bit Offset** | **Field Name** | **Description** |
| [31:12] | RESERVED | Not used |
| [11:0] | ENABLE\_TRAINING | Set to one for every active HiSpi channel. |

### MANUAL\_TAP: 0x000C

|  |  |  |
| --- | --- | --- |
| **Bit Offset** | **Field Name** | **Description** |
| [31:16] | RESERVED | Not used |
| [15:0] | MANUAL\_TAP | Delay tap setting for serdes, range 0 to 1023. |

### ENABLE: 0x0010

|  |  |  |
| --- | --- | --- |
| **Bit Offset** | **Field Name** | **Description** |
| [31:2] | RESERVED | Not used |
| 3 | FILTER\_MODE | If set to 1, enable serdes filter mode |
| 2 | EN\_DECODER | Attached to en\_decoder output pin (not used anymore) |
| 1 | FIFO\_RESET | If set to 1, the axi stream fifo is in reset. |
| 0 | FIFO\_EN | If set to 1, the axi stream fifo gets filled. |

# Programming Sequence

* Enable FIFO reset ENABLE(0x10) bit 1 set to 1
* Disable FIFO reset ENABLE(0x10) bit 1 set to 0
* Set MANUAL\_TAP(0xC) to a desired value, default 0x0000
* Enable the used channels in the ENABLE\_TRAINING(0x08) default 0xFFF (12 channels enabled)
* Configure registers to enable word alignment: set TRAINING(0x04) to the same value as the idle word of the DUT.
* Configure the DUT to send out idle words
* Start the word alignment. Set bit 0 of the COMMAND register to 1. Poll bit 0 of the COMMAND register until it’s 0.
* ENABLE FIFO\_EN and EN\_DECODER by putting ENABLE(0x10) to 0x05
* Configure the DUT to capture images.