

***Matrox Pcie2AxiMaster***

***IP-Core specification***

**Project :**

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Revision history

**This section lists all revisions for the current document and explains the modifications made for each new revision**

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| --- | --- |
| **Revision** | **Description** |
| 0.01 | * Initial version |

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# Introduction

# IP-Core features

* Bridge between the PCIe Gen2x1 and the AXI4 Master Lite interface
* Based on the Xilinx PCIe Endpoint
* IP-Integrator ready
* Support up to 31 IRQ events
* Includes the Matrox SPI interface and the Xilinx Startup2 module

# Bloc diagram

# Pcie Xilinx end point

# Interrupts

## Legacy mode

Interrupts mappings :

Registre Status[0]: @BAR2 + 0x40

io[0]

reserved[7:1]

tick[9:8]

tick\_latch[11:10]

tick\_wrap[13:12]

tick\_wrap[13:12]

toe\_overrun[17:14]

toe\_frame\_sent[21:18]

toe\_list\_sent[25:22]

toe\_log\_available[26]

toe\_log\_overflow[27]

Registre Status[1]: @BAR2 + 0x44

timer\_start[15:0]

timer\_end[31:16]

## Interrupt queue mode

## Modelsim Validation framework

### Prerequisite

# FPGA implementation

# References