# VME\_INTF IP Block Timing Constraints

The K&S VME Bus Master interface implements basic data transfer and interrupt features of the VME Spec. So, overall timing requirements are based on the VME spec. In the FPGA design, the 125MHz system clock (8nsec) sets the timing granularity. So, the overall system timing is a function of a number of clock cycles and propagation delays. Timing constraints are written to bound the allowable propagation delays of the FPGA combinational paths.

Signals are grouped for convenience when writing timing constraints. The groupings below are based on signals with similar timing requirements.

VME Bus Master

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Group** | **Direction** | **Signals** | **Timing Reference** |
| Address & Control | output | vme\_a[31:0], vme\_am[5:0], vme\_lword\_n, vme\_write\_n, vme\_write, vme\_iack\_n, vme\_iackout\_n | CtrlA |
| Data | inout | vme\_db[31:0] | CtrlD, DTACK |
| CtrlA (address reference) | output | vme\_as |  |
| CtrlD (data reference) | output | vme\_ds0\_n, vme\_ds1\_n |  |
| DTACK (acknowledge ref) | input | vme\_dtack\_n |  |
|  | input | vme\_irq\_n[7:1] |  |

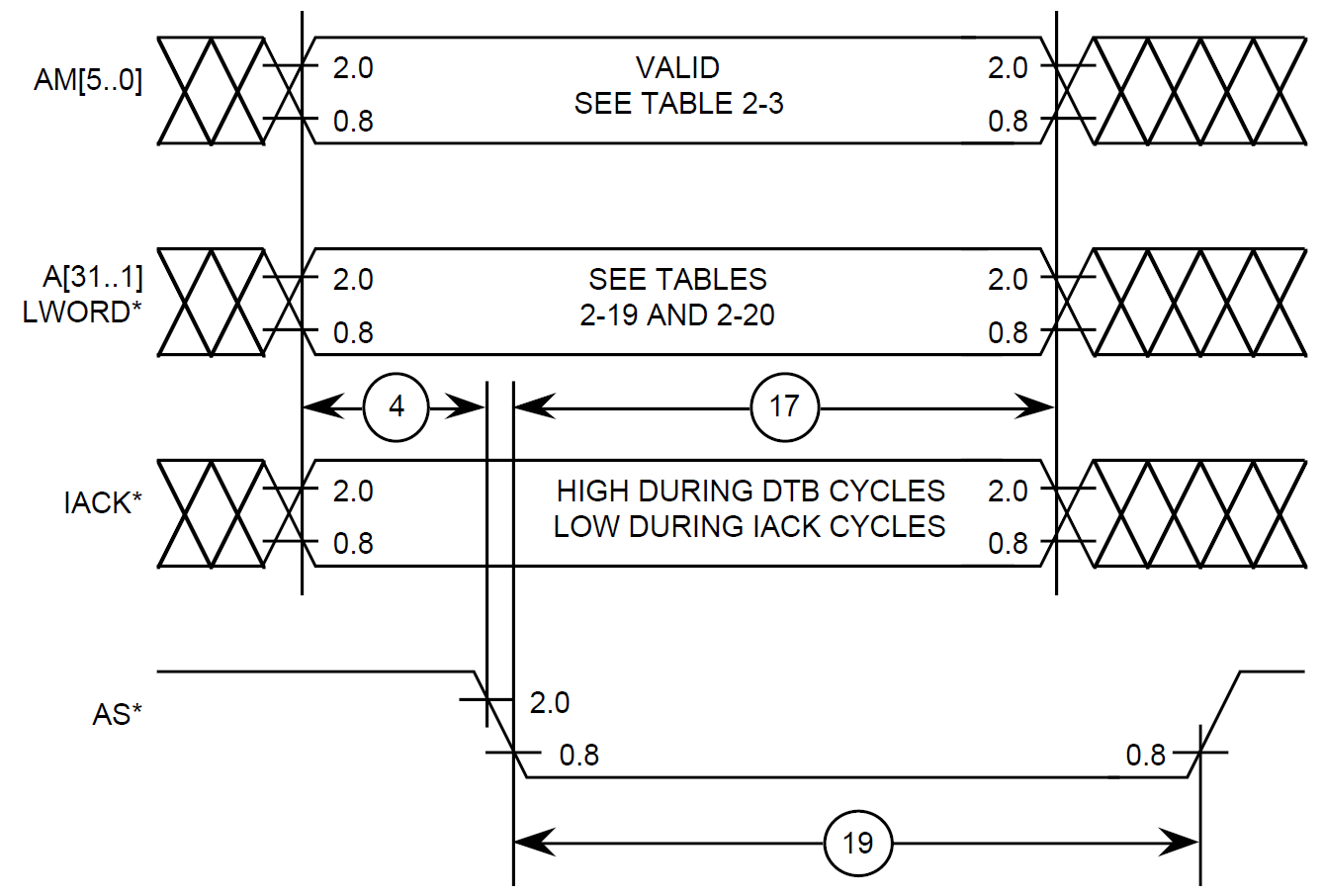


Figure 2-2: VME Address Broadcast Timing (all cycles)

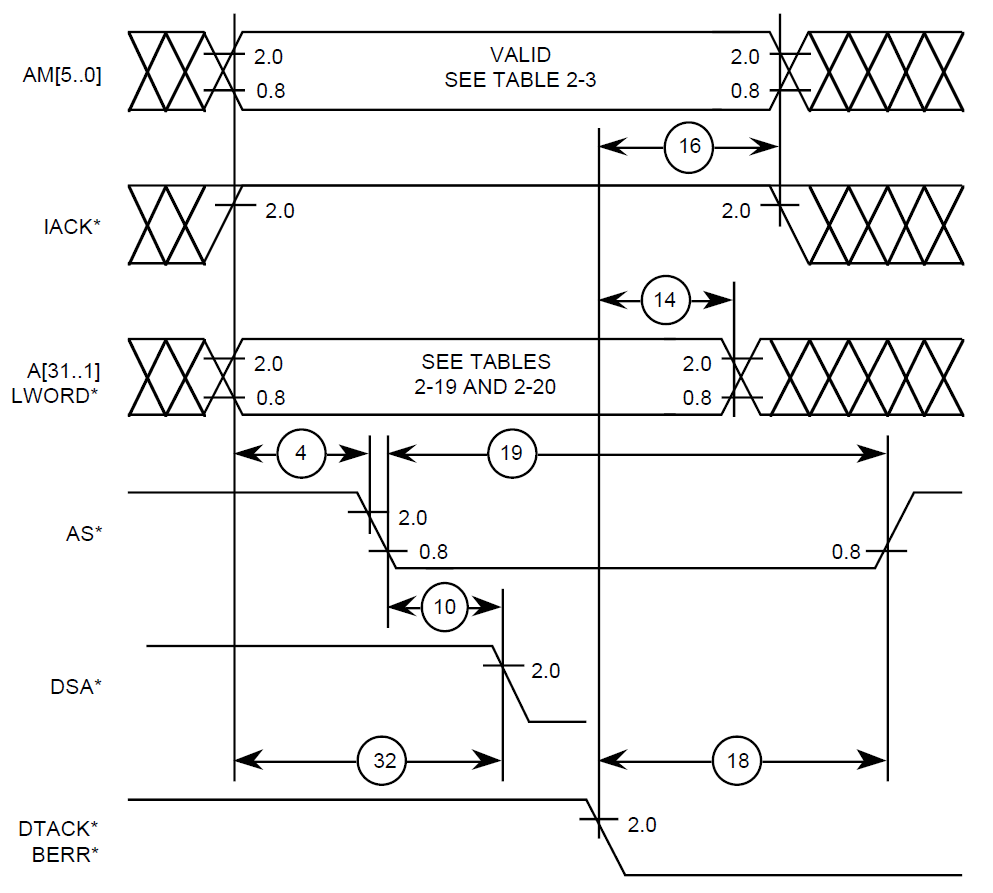


Figure -13: Data Transfer Timing

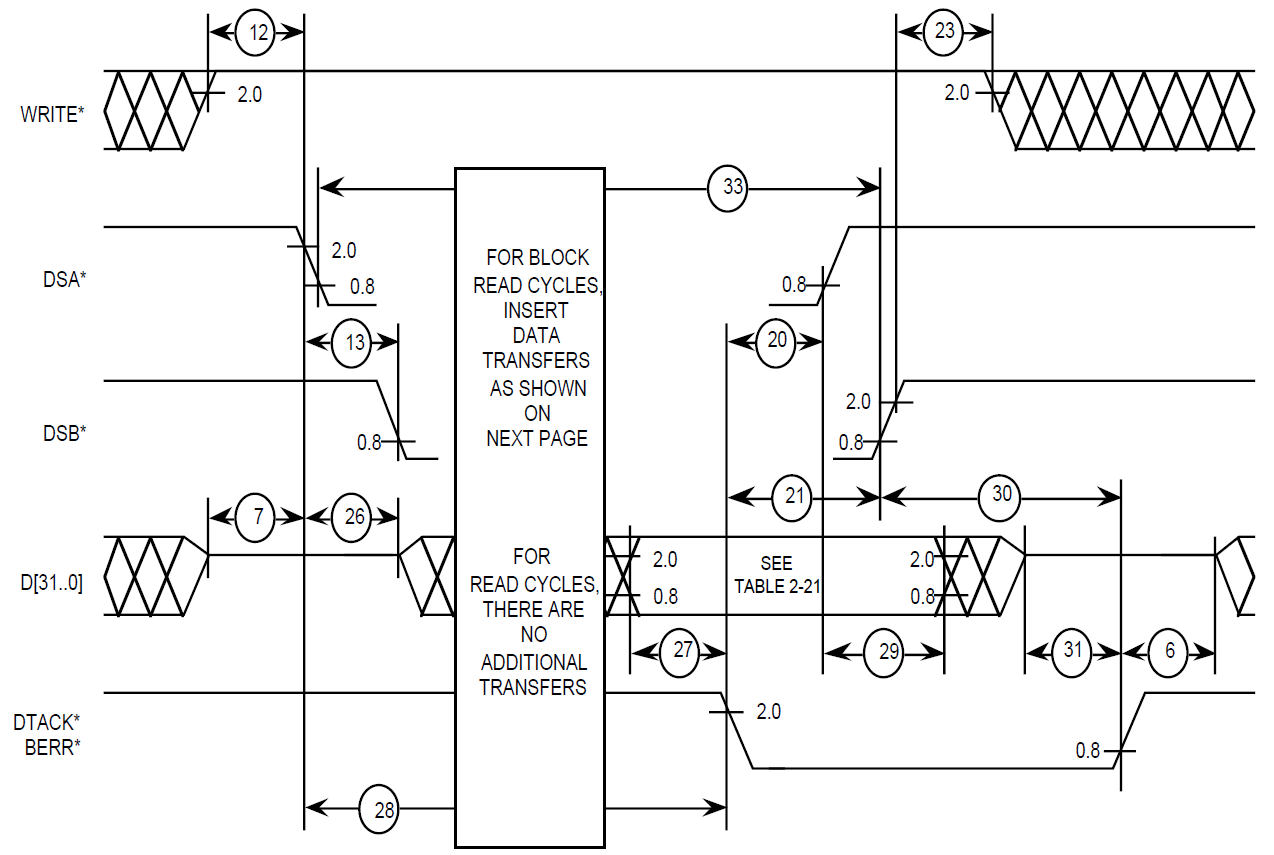


Figure -17: Data Read Transfer Cycle Timing

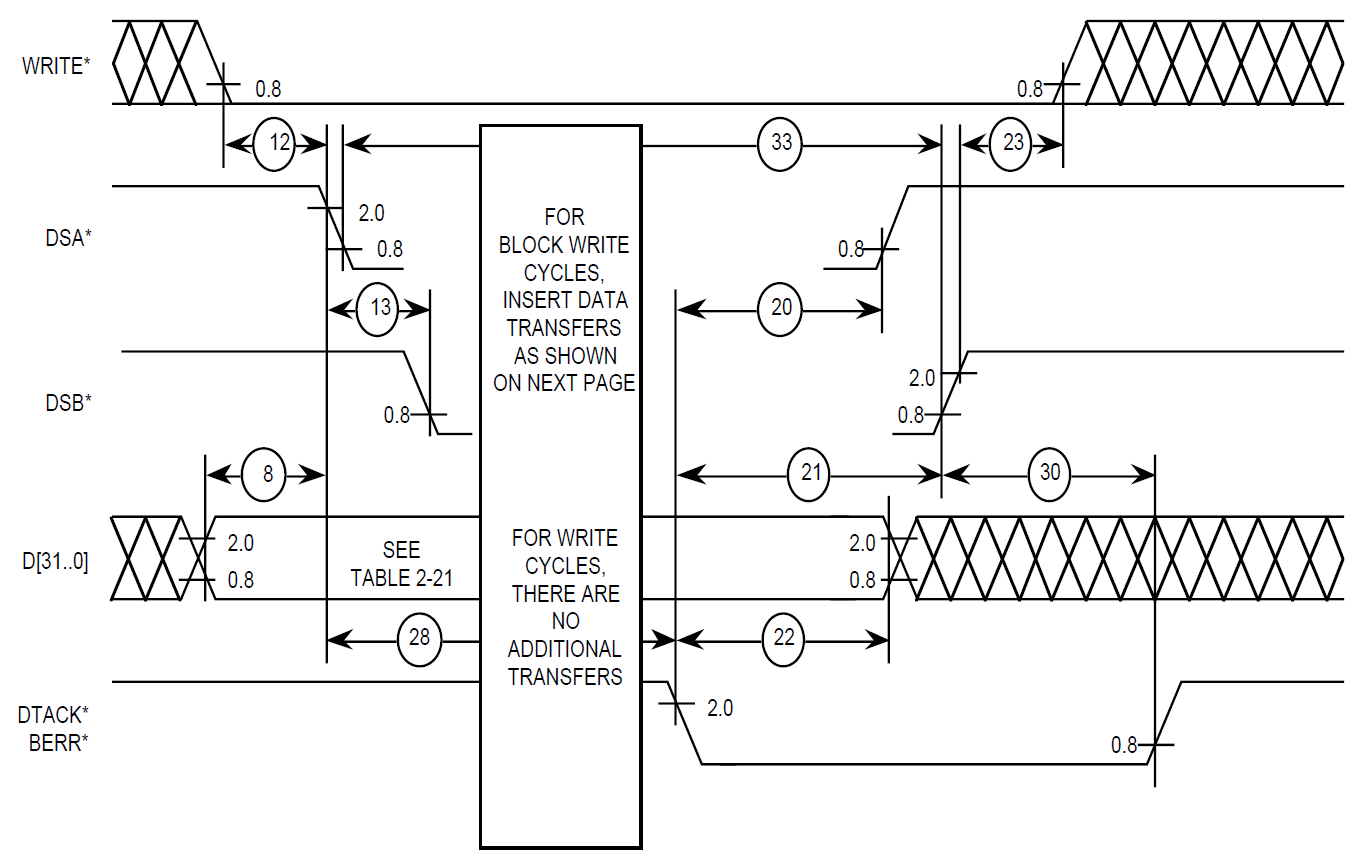


Figure -19: Data Write Transfer Cycle Timing

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Param** | **Description** | **Min** | **Max** | **Units** |
| 4 | AS\* low delay from Address group stable | 35 |  | nsec |
| 5 | AS\* Width (high time) | 40 |  | nsec |
| 7 | D[31:0] inactive delay to DS0\* or DS1\* low | 0 |  | nsec |
| 8 | DS0\* or DS1\* low delay from D[31:0] stable (write) | 35 |  | nsec |
| 10 | DS0\* or DS1\* low delay from AS\* low | 0 |  | nsec |
| 11 | DS0\* and DS1\* inactive | 40 |  | nsec |
| 12 | DS0\* or DS1\* delay from WRITE\* | 35 |  | nsec |
| 13 | DS0\* to DS1\* skew |  | 10 | nsec |
| 14, 15 | Address group hold from DTACK\* low | 0 |  | nsec |
| 16 | IACK\* hold from DTACK\* low | 0 |  | nsec |
| 17 | Address and Control hold from AS\* low | 40 |  | nsec |
| 18 | AS\* hold from DTACK\* low | 0 |  | nsec |
| 19 | AS\* Width (low time) | 40 |  | nsec |
| 20 | DS0\* or DS1\* hold from DTACK\* low | 0 |  | nsec |
| 23 | WRITE\* hold from DS0\* or DS1\* high | 10 |  | nsec |
| 27 | D[31:0] setup to DTACK\* low | -25 |  | nsec |
| 28 | DTACK\* delay from DS0\* or DS1\* low | 30 |  | nsec |
| 29 | D[31:0] hold from DS0\* or DS1\* high | 0 |  | nsec |
| 32 | IACK\* setup to DS0\* or DS1\* low | 10 |  | nsec |

Table 2-22: VME Master Timing Parameters

Timing Constraints based on VME Timing Parameters

*We could use a simulation screen shot of the VME IP to see clock delays here.*

## Output Port Timing Constraints

All output port (pin) signals are synchronous from a single clock (*u0|pcie\_hard\_ip\_0|\*|coreclkout*). So, the VME timing requirements will be functions of clock period delays and propagation delays. Since static timing analysis addresses propagation delays, the clock period delays are removed from the timing requirements leaving the propagation delays which are managed by the SDC timing constraints.

The following VME timing parameters are used to create Quartus Fitter timing constraints and TimeQuest timing checks for the FPGA. The reason behind the constraint and associated time values is included with each parameter.

**Parameter 4** – vme\_as\_n delay = 35ns min.

* There are 6 clock delays (48ns) from when the address is available to vme\_as\_n going low.
* Constrain propagation delays of output signals referenced to vme\_as\_n
  + Using the same min and max delays for all signals guarantees a maximum skew less than the max minus the min.
  + It also reduces the Fitter timing closure effort since the Fitter doesn’t have to compare each routing delay to every other routing delay in the set of signals.
  + Choose delays such that: (output delay max - output delay min) < 13

set\_max\_delay -to [get\_ports vme\_a\*] 16.0  
set\_min\_delay -to [get\_ports vme\_a\*] 3.5  
set\_max\_delay -to [get\_ports vme\_write\*] 16.0  
set\_min\_delay -to [get\_ports vme\_write\*] 3.5  
set\_max\_delay -to [get\_ports vme\_lword\_n] 16.0  
set\_min\_delay -to [get\_ports vme\_lword\_n] 3.5  
set\_max\_delay -to [get\_ports vme\_iack\*] 16.0  
set\_min\_delay -to [get\_ports vme\_iack\*] 3.5  
set\_max\_delay -to [get\_ports vme\_ds\*] 16.0  
set\_min\_delay -to [get\_ports vme\_ds\*] 3.5

* Alternately, constrain vme\_a and vme\_as\_n output skew
  + Choose a skew less than 13ns = (48ns – 35ns) [e.g. 12ns]

set\_max\_skew -from\_clock {u0|pcie\_hard\_ip\_0|\*|coreclkout} \  
 -to [get\_ports vme\*] 12.0

* + This increased the Quartus Fitter time by more than 10x.

**Parameter 5** – AS\* Width (high time) = 40ns min.

* No additional SDC constraint for AS\* needed since the delay is a function of the number of clock cycles that AS\* is inactive as defined by the state machine, not a propagation delay.

**Parameter 7** – D[31:0] inactive delay to DS0\* or DS1\* low = 0ns min.

* No additional SDC constraint for DS0\* or DS1\* needed since no extra delay is required.

**Parameter 8** – DS0\* or DS1\* low delay from D[31:0] stable (write) = 35ns min

* There are 7 clock delays (56ns) from when the data is available to vme\_ds0\_n and vme\_ds1\_n going low.
* Constrain propagation delays of data signals referenced to vme\_ds0\_n and vme\_ds1\_n
  + Delay variance must be less than 7 clocks – 35ns = 56ns - 35ns = 21.
  + Choose max delay such that: (vme\_db\* max delay – vme\_ds\* min delay) ≤ 21

set\_max\_delay -to [get\_ports vme\_a\*] 24.0

* Choose min delay ≥ vme\_ds\* min delay. Also see requirement from **Parameter 29**.

set\_min\_delay -to [get\_ports vme\_a\*] 7.0

**Parameter 10** – DS0\* or DS1\* low delay from AS\* = 0ns min

* No additional SDC constraint for DS0\* and DS1\* needed since this parameter is covered by the constraints for **Parameter 13**.

**Parameter 11** – DS0\* and DS1\* inactive = 40ns min

* No additional SDC constraint for DS0\* and DS1\* needed since the delay is a function of the number of clock cycles that DS0\* and DS1\* are inactive as defined by the state machine, not a propagation delay.

**Parameter 12** – DS0\* or DS1\* delay from WRITE\* = 35ns min

* No additional SDC constraint for DS0\* and DS1\* needed since this parameter is covered by the constraints for **Parameter 4**.

**Parameter 13** – DS0\* to DS1\* skew = 10ns max

* Use set\_max\_skew from the common reference clock to the signal set
* By including vme\_as\_n with vme\_ds\* and making the max skew value less than 8ns (1 clock cycle), vme\_ds0\_n and vme\_ds1\_n are guaranteed occur after vme\_as\_n.

set\_max\_skew -from\_clock {u0|pcie\_hard\_ip\_0|\*|coreclkout} -to \  
 [get\_ports {vme\_as\_n vme\_ds\*}] 7.0

**Parameter 14, 15, 16, 18, 20** – Address group, IACK\*, AS\*, DS0\*, DS1\* hold from DTACK\* low = 0ns min.

* No additional SDC constraint for these signals since no extra hold time is required.

**Parameter 17** – Address and Control hold from AS\* low = 40ns min

* This is a function of the number of clock cycles from AS\* low to DTACK\* low and the skew between the signals and AS\*. The minimum number of clocks is 5. If the feature was supported, the design should add margin and insure 6 clock cycles.
* No additional SDC constraint for these signals since the feature is not supported.

**Parameter 19** – AS\* Width (low time) = 40ns min

* This is a function of the number of clock cycles from AS\* low to DTACK\* low. The minimum number of clocks is 5. However, DTACK\* detection determines the number of needed clocks.
* No additional SDC constraint for these signals since AS\* is held low until DTACK\* is detected.

**Parameter 23** – WRITE\* hold from DS0\* or DS1\* high = 10ns min

* Based on simulations, WRITE\* is held for 3 clock cycles = 24ns from DS0\* or DS1\* high. Based on constraints for **Parameter 4**, the maximum skew between DS\* and WRITE\* is 14 – 3.5 = 10.5ns.
* No additional SDC constraint, min hold time is 24 – 10.5 = 13.5ns meeting the 10ns requirement.

**Parameter 27** – D[31:0] setup to DTACK\* low = -25ns min

* DS0\* or DS1\* delay from D[31:0] stable is 7 clocks (56ns) minus the maximum D[31:0] output delay (24ns max) plus **Parameter 28** (30ns min) = 56 - 24 + 30 = 40ns min setup.
* No additional SDC constraint, margin is 40 - (-25) = 65ns based on **Parameters 28** and **29**.

**Parameter 28** – DTACK\* delay from DS0\* or DS1\* low = 30ns min

* No additional SDC constraint since parameter is constrained by the slave device. It is informational.

**Parameter 29** – D[31:0] hold from DS0\* or DS1\* high = 0ns min

* D[31:0] is held for 1 clock cycle (8ns) after DS0\* or DS1\* go high. Therefore, DS0\* or DS1\* delay cannot be more than 8ns longer than the D[31:0] delay.
* Tighten the max delay in **Parameter 4** from 16.0 to 14.0. This should be a problem since vme\_ds0\_n and vme\_ds1\_n delays are short by design (direct connects from register to pin).
* Choose vme\_db\* min delay ≥ vme\_ds\* max delay – 8ns. See vme\_db\* constraint associated with **Parameter 8**.

**Parameter 32** – IACK\* setup to DS0\* or DS1\* low = 10ns min

* There are seven clock cycles (56ns) between IACK\* stable and DS0\* or DS1\*.
* No additional SDC constraint for IACK\*, DS0\*, or DS1\* needed since this parameter is covered by the constraints for **Parameter 4**.

## Input Port Timing Constraints