sSUHFIPTIVA0

HVQFN24

Rev. 1.0 — February 2023 **Data sheet**

REINDEER PROJECT ONLY

1 General description

The sSUHFIPTIVA0 in HVQFN24 package implements all minimum requirements for RF energy harvesting. It has to be noted that the harvesting core unit (RF frontend plus charge pump) is not optimized or has been redesigned for frequencies above 1GHz. Instead, a SUHF fronted is used to serve as power conversion unit. Therefore the harvesting efficiency will be less at 2.4 GHz compared to the designed UHF frequency range.

Next to the RF harvesting capabilities, this sSUHFIPTIVA0 IC also contains a demodulator and configuration pins for basic backscattering. It has to be noted that the IC is purely designed as test IC which should be kept in mind for all operations performed.

The IC requires an external power supply (two power rails, 3.3V and 1.1V) to function properly - no standalone RF harvesting without external supply is possible right now.

The RF port has a maximum power rating of P_{max} = 20dBm. This limit should not be exceeded to prevent Risk of damage/performance degradation due to overvoltage between RF input pins. The minimum power depends on the connected load. Validation measurements with a power of around -20dBm resulted in a charge-pump voltage (vdda) of up to 1.2V at 860MHz and 2.4GHz (no load – high impedance voltmeter). These results should only give a rough estimation about the RF harvesting capabilities and are not true reference values.

2 Block diagram

Following block diagram shows all available configuration input and status output pins in the HVQFN24 package.

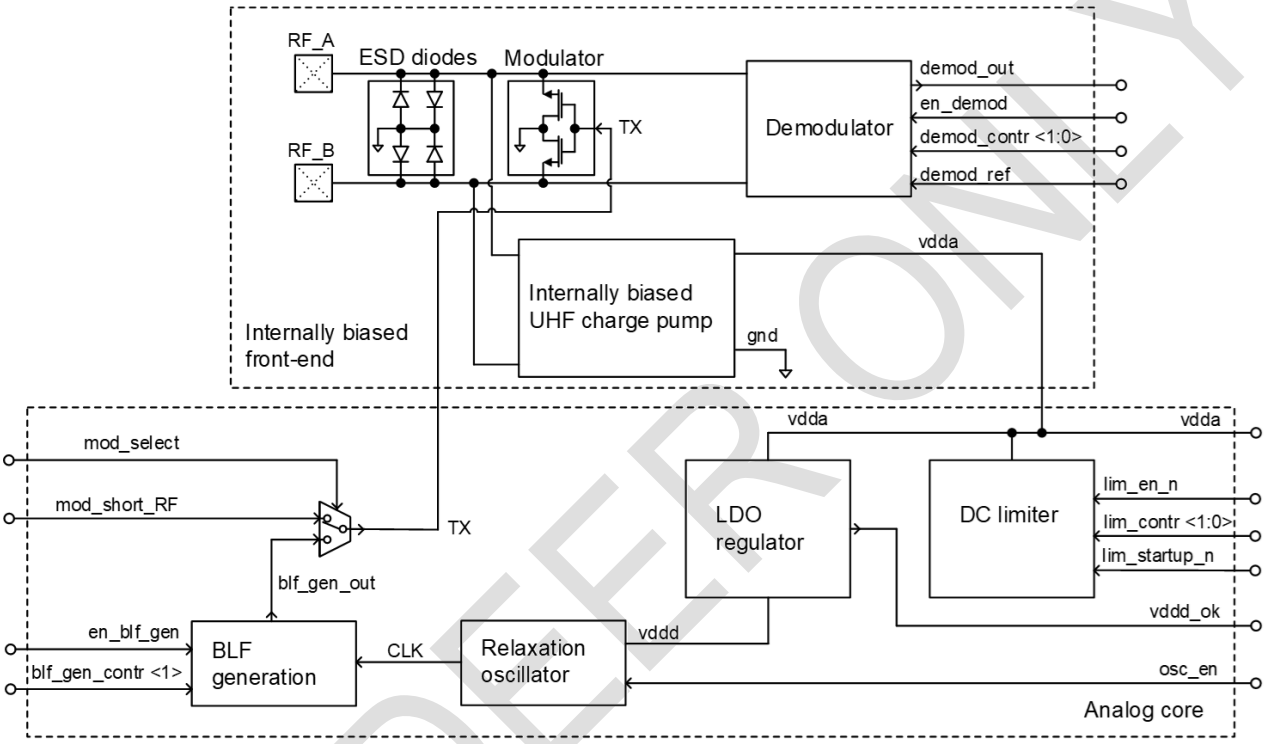


Figure 1. Block diagram

3 Pinning information

The pinout information for the sSUHFIPTIVA0 IC in HVQFN24 can be taken from following figure. Each pin was color-coded to provide some further information about the possible operations.

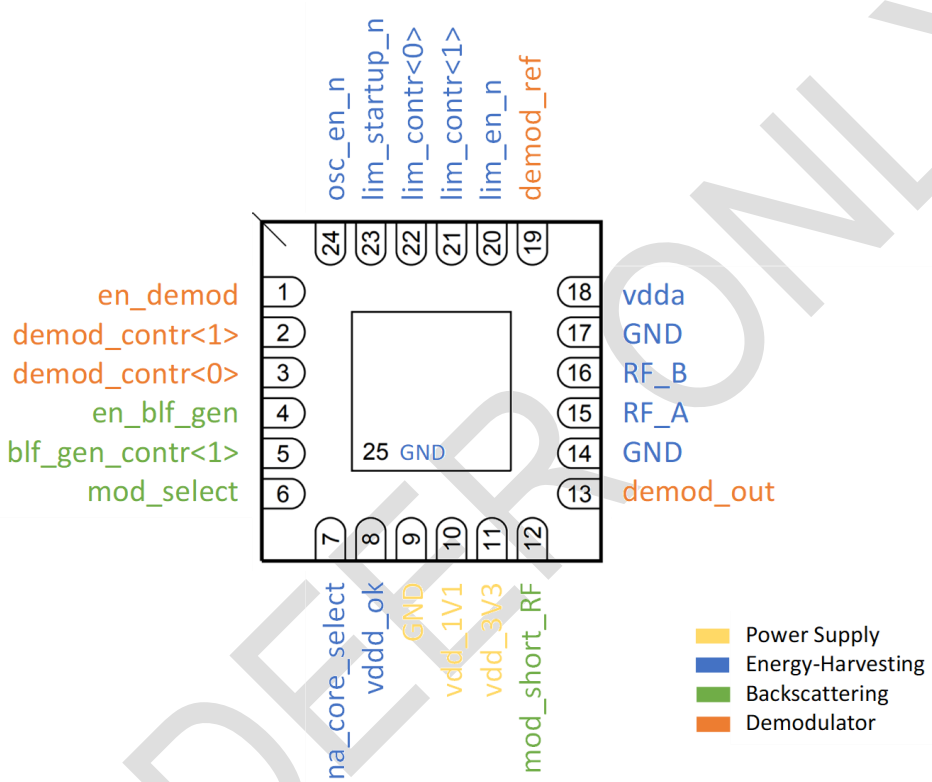


Figure 2. Pinout

Default states of digital inputs are defined by pull-up/pull-down resistors (34kΩ). The pull-down resistors are connected to GND. The pull-up resistors are connected to vdd_3V3. Therefore, pin states are changed by connecting them to GND or to a 3.3V rail.
Default states of digital input pads are indicated by the bit values in brackets (b0 or b1). All pin-names without values in brackets are either output pins or analog input pins (ref).

Table 1. Pin description

Pin	Signal	Description	Nature	I/O	Comments
1	en_demod	Demodulator enable signal	Digital	I	b0 Demodulator in power-down mode (default) b1 Demodulator enabled
2	demod_contr<1>	MSB demodulator configuration bit (RF detector gain control)	Digital	I	Further information in section 4.3 Demodulator configuration
3	demod_contr<0>	LSB demodulator configuration bit (RF detector gain control)	Digital	I	Further information in section 4.3 Demodulator configuration
4	en_blf_gen	BLF generation enable signal (BLF… Backscatter link frequency)	Digital	I	b0 BLF generation enabled (default) b1 BLF generation disabled
5	blf_gen_contr<1>	MSB BLF generation configuration bit	Digital	I	b0 clk/8, ~160kHz b1 clk/64, ~20kHz
6	mod_select	Selection of the modulator control input (internal modulator control signal mod_tx)	Digital	I	b0 External control signal (default) b1 BLF generator output
7	ana_core_select	Output multiplexing between the analog part incl. RF front-end and the stand-alone analog core	Digital	I	Should always be connected to vdd_3V3
8	vddd_ok	Signal indicating a regulated vddd supply voltage	Digital	O	The vddd regulator has entered regulation mode at vddd_ok = b1; bias_started is latched; reset by startup_vdda
9	gnd	Global chip ground	Supply	I	Main gnd bin for power supply
10	vdd_1V1	1.1V I/O pad ring core supply	Supply	I	0.8V ≤ vdd_1V1 ≤ 1.2V
11	vdd_3V3	3.3V I/O pad ring external supply	Supply	I	3.0V ≤ vdd_3V3 ≤ 3.6V
12	mod_short_RF	External modulator control signal	Digital	I	b0 High impedance state (default) b1 Low impedance state; vdd_1V1 driving voltage
13	demod_out	Demodulator output signal	Digital	O	Further information in section 4.3 Demodulator configuration
14	gnd	Global chip ground	Supply	I	Ground pin to keep a short and symmetrical ground loop on the RF side
15	RF_A	RF pad A connected to the UHF front-end	RF	I	Conatining anti-parallel diodes for ESD protection
16		RF pad B connected to the UHF front-end	RF	I	Conatining anti-parallel diodes for ESD protection
17	gnd	Global chip ground	Supply	I	Ground pin to keep a short and symmetrical ground loop on the RF side
18	vdda	Analog supply rail; analog part including an RF front-end	Voltage	I/O	Series resistor of 516Ω between DC limiter input vdda_raw and vdda
19	demod_ref	Demodulator comparator reference voltage	Voltage	I	Typ. value of about 80mV at Pmin Further information in section 4.3 Demodulator configuration
20	lim_en_n	DC limiter enable signal	Digital	I	b0 DC limiter enabled (default) b1 DC limiter disabled
21	lim_contr<1>	MSB of DC limiter trim bits	Digital	I	MSB ... LSB; binary encoded trim bits; typ. limiter trim range of 1.61V to 1.86V at 600µA; nonuniform step size: 40mV, 34mV, 174mV; default: b00; midrange, typ. vdda_max ≈ 1.7V: b10
22	lim_contr<0>	LSB of DC limiter trim bits	Digital	I	
23	lim_startup_n	DC limiter start-up mode signal (may be controlled by vddd_ok)	Digital	I	b0 Start-up mode, vdda_max_stup < 1.26V (default) b1 Normal mode, typ. vdda_max < 1.86V
24	osc_en_n	Oscillator enable signal	Digital	I	b0 The oscillators are enabled (default) b1 Oscillators are in power-down mode

4 Functional description.

This section provides some further information about the basic operation modes possible with the sSUHFIPTIVA0 in HVQFN24 package.

4.1 Basic RF harvesting operation

For basic RF harvesting operation, without using the demodulator and the backscattering options, pin configuration should look like following:

- **ana_core_select**: HIGH (vdd_3V3)
- **vddd_ok**: connected to lim_startup_n
- **lim_en_n**: either HIGH or LOW depending if chip-internal voltage limiting is desired. If the limiter is disabled (lim_en_n = HIGH), the resulting voltage at vdda must be monitored carefully to ensure that the limit of 2.0V is not surpassed!
- **lim_startup_n**: connected to vddd_ok
- **osc_en_n**: HIGH (vdd_3V3)

The power supply pins vdd_3V3 and vdd_1V1 should be supplied as stated in table 1: static characteristics. The DC charge-pump out pin vdda should be supplied with decoupling caps as mentioned in 5.1 PCB design-in information.
All other pins should be floating or supplied by their default supply voltage.

4.2 CLK and BLF generation sub-system

Signal ana_core_select must be set HIGH (connected to vdd_3V3). This selects the internal analog core plus front-end clk signal as clk source for the BLF generator.
By changing the state of blf_gen_contr<1>, the BLF generator clock can me modified. The default mode is highlighted in blue and results in a frequency of around 20kHz (clk divided by 64). The other possible frequency is around 160kHz (clk divided by 160) which can be set by setting the blf_gen_contr<1> signal LOW (connection to ground).

blf_gen_contr<1>: blf_gen_out	
0	clk/8 (~160kHz)
1	clk/64 (~20kHz)

With mod_select, the modulator input source can be selected. The default LOW state of this signal enables to inject an external modulation signal to the mod_short_RF pin. By setting the mod_select pin to HIGH (connected to vdd_3V3) the blf_gen_out (output signal of the BLF generator) signal is used as modulator signal.

mod_select: mod_tx	
0	mod_short_RF
1	blf_gen_out

4.3 Demodulator configuration

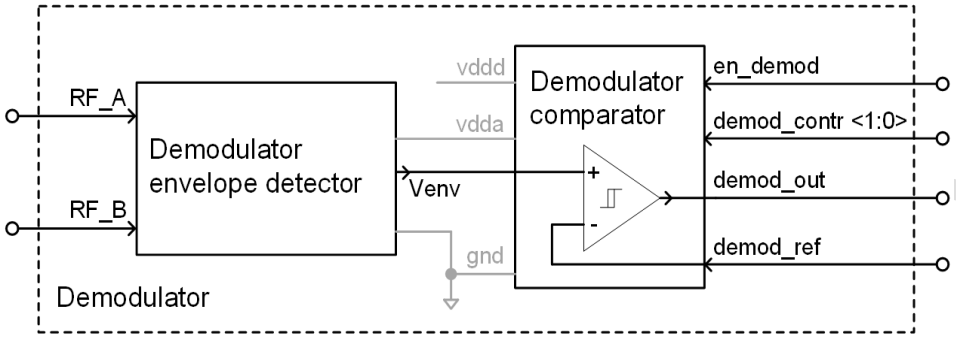


Figure 3. Demodulator

The voltage difference between RF_A and RF_B is called Vin.
Depending on the state of the configuration signal demod_contr, different envelope detector loads can be applied to the Venv voltage rail as presented in the following table.

Table 2. Envelope detector load

Configuration range, lower limit		Configuration range, higher limit		demod_contr configuration	Envelope detector load
Intb. FE, Pav (dBm)	Vin (V)	Intb. FE, Pav (dBm)	Vin (V)		
-	-	-17	0.3	b00	25nA constant current
-17	0.3	-5	0.45	b01	312nA constant current
-5	0.45	3	0.65	b10	250kΩ resistance
3	0.65		-	b11	100kΩ resistance

This adjustment of the envelope detector load results in different gain control values (Venv/Vin). This gain adjustment should be performed according to the Vin level or rather the available power Pav* to minimize distortions of Venv versus the Vin envelope.

The different demod_contr configurations therefore result in following average gain values:

Table 3. Average gain

Config. range	Vin range	demod_contr configuration	Average gain (Venv/Vin)
1	Vin < 0.3V	b00	0.77
2	0.3V < Vin < 0.45V	b01	0.65
3	0.45V < Vin < 0.65V	b10	0.54
4	0.65V < Vin	b11	0.35

*All values assume perfect matched impedance conditions at Pmin (reference load of vdda = 0.65V, idda = 3.1µA).

5 Application design-in information

This section should give some further information and design guidelines for the use of the sSUHFIPTIVA0 IC in a new design.

5.1 Known issues and limitations

- Signal demod_out has the wrong polarity with reference to the RF envelope.
- Demodulator: First modulation pulse is missed

5.2 PCB design-in information

The DC output pin of the charge pump vdda should be supplemented by an external capacitance of ~200pF on the PCB. Two parallel capacitors of values 10pF and 180pF are recommended and have been verified to work fine with this chip. These capacitors should be located as close to the vdda pad as possible. SMD MLCC capacitors of size 0402 are recommended.
Following figure represents a recommended PCB layout for decoupling caps. All vias are connected to ground (solid ground plane under the IC area is recommended).

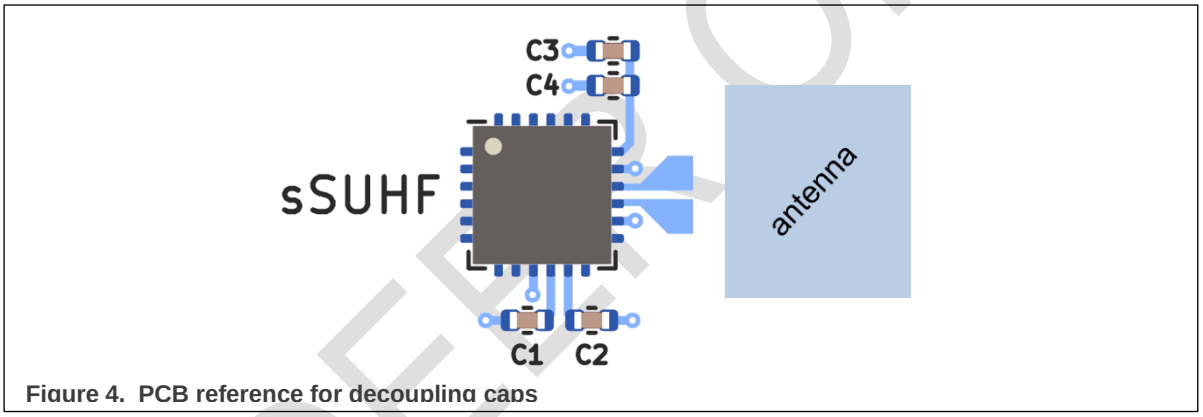


Figure 4. PCB reference for decoupling caps

Capacitor C1 is the decoupling capacitor for the vdd_1v1 rail, C2 for the vdd_3V3 rail.
Capacitors C3 and C4 are in parallel and have a capacity of 180pF and 10pF. If further connections to the pins on the upper side of the IC are made, the decoupling caps should be moved to the bottom side of the PCB to keep a very close distance to the vdda pin.

5.3 Power Supply

vdd_3V3 and vdd_1V1 should ramp up as contemporaneous as possible but an exact sequence is not relevant. The power rails should be free of overshoot and decoupling caps should be added to ensure low noise.
In exceptional cases the vdd_1V1 power rail can also be supplied by a resistive voltage divider fed by the vdd_3V3 line. Appropriate values must be chosen to ensure the desired lower and upper voltage limit.

5.4 Reference antenna designs

Following figures show two reference antenna designs for UHF (915MHz) and for WIFI (2.45GHz). The figure represents the true scale of the antennas and the sSUHFIPTIVA0 IC. The UHF antenna has a height of 90mm, the WIFI antenna has a height of 45mm. Both antennas are designed to match the input impedance of the RF port, but further tuning of the antenna length would be necessary to enhance the performance.

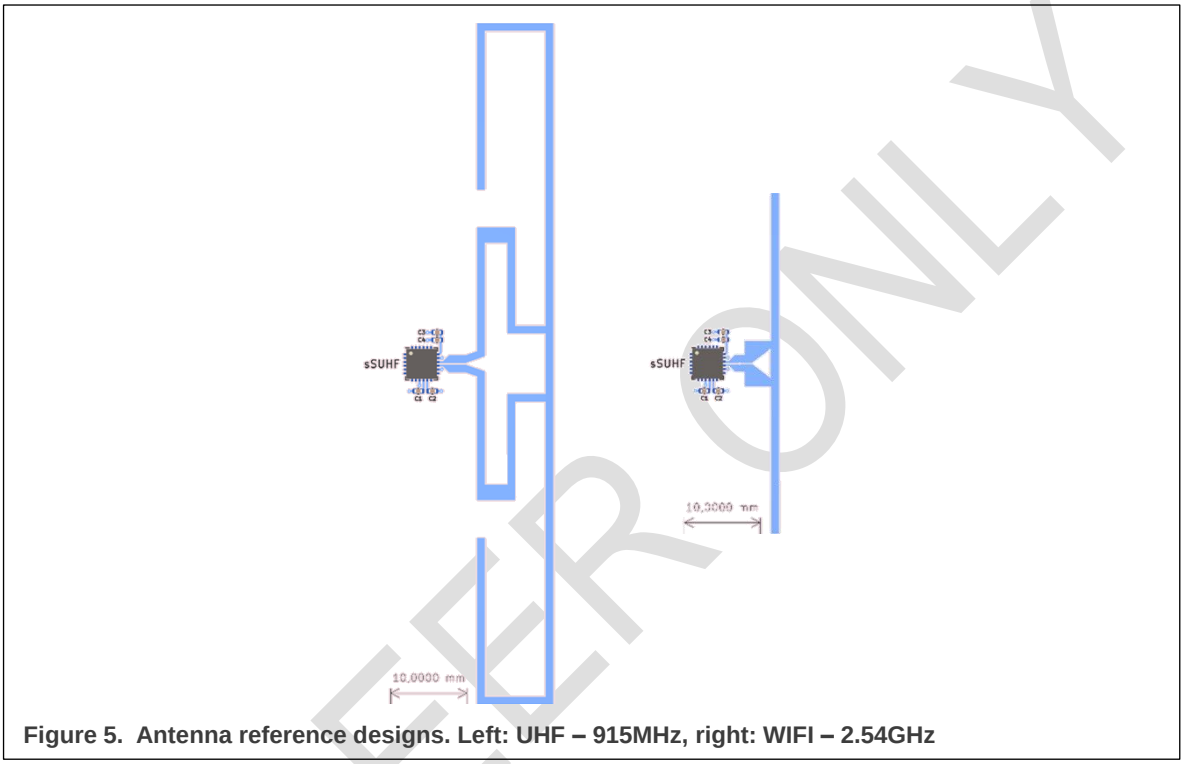


Figure 5. Antenna reference designs. Left: UHF – 915MHz, right: WIFI – 2.54GHz

6 Static characteristics

Table 4. Static characteristics

V_{DD_3V3} = 3.0 V to 3.6 V; V_{DD_1V1} = 0.8 V to 1.2 V; GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

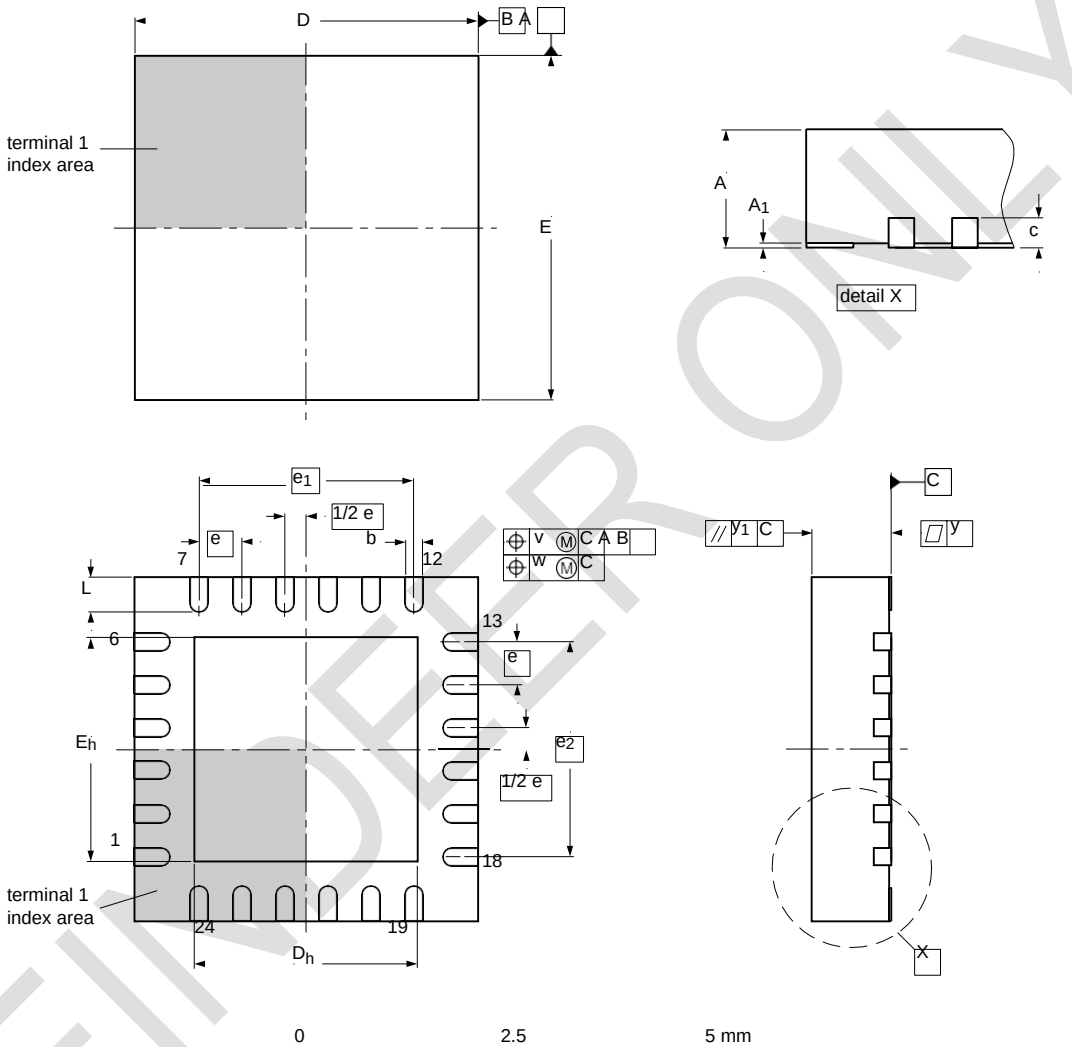
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD_3V3}	supply voltage			3.0	-	3.6	V
V_{DD_1V1}	supply voltage			0.8	-	1.2	V
I_{DD_3V3}	supply current	Operating mode; V_{DD_3V3} = 3.3 V; V_{DD_1V1} = 1.1 V; I/O = all floating		-	14	20	µA
I_{DD_1V1}	supply current	Operating mode; V_{DD_3V3} = 3.3 V; V_{DD_1V1} = 1.1 V		-	500	-	nA
RF Input Power							
P_{RF}	RF input power			-23.7*	-	20	dBm
I/Os							
V_{IL}	LOW-level input voltage			0.0	-	0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	3.3	V
I_{LIH}	HIGH-level input leakage current	V_{DD_3V3} = 3.3 V; V_{DD_1V1} = 1.1 V **		-	100	-	µA
I_{LIL}	LOW-level input leakage current	V_{DD_3V3} = 3.3 V; V_{DD_1V1} = 1.1 V **		-	100	-	µA
Charge pump Impedance (capacitance) @PoR							
Z_{in}	RF input impedance			-	25,7956 - j99,0028* (0.656155)	-	Ω (pF)
RF Power Ratings							
V_{Ref}	demod_ref			-	80	-	mV

*At Pmin (reference load of vdda = 0.65V, idda = 3.1µA). Input impedance has a high non-linearity in relation to the connected load.

**HIGH-level and LOW-level leakage currents only appear when pin is set to not-default state (leakage current = current through internal 34k pull-up/down resistor)

7 Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-3A**



Dimensions (mm are the original dimensions)

Unit(1)		A(1)	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	max	1	0.05	0.30	0.2	4.1	2.75	4.1	2.75	0.5	2.5	2.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		3.9	2.45	3.9	2.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot616-3a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT616-3A		MO-220				~~16-02-16~~ 16-02-17

Fig. 6. Package outline HVQFN24 (SOT616-3)

8 Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Supersedes
sSUHFIPTIVA0 v.1.0	2023/02	SUHF data sheet	-

9 Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
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