Specification For HINK 7.5"EPD

Model NO.: HINK-E075A12

Product VER:A1

Customer Approval

Customer	
Approval By	
Date Of Approval	

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Version	Content	Date	Producer
A0	New release	2017/11/30	Hu ting
A1	ADD Reliability condition	2018/1/5	Wang lin

CONTENTS

1. General Description

HINK-E075A12 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The7.5" active area contains 640×384 pixels, and has 1-bit B/W full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2.Features

- 640×384 pixels display
- White reflectance above 35%
- Contrast ratio above 10:1
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in flash memory
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C Signal Master Interface to read external temperature sensor/ built-in temperature sensor
- Available in COG package IC thickness 280um

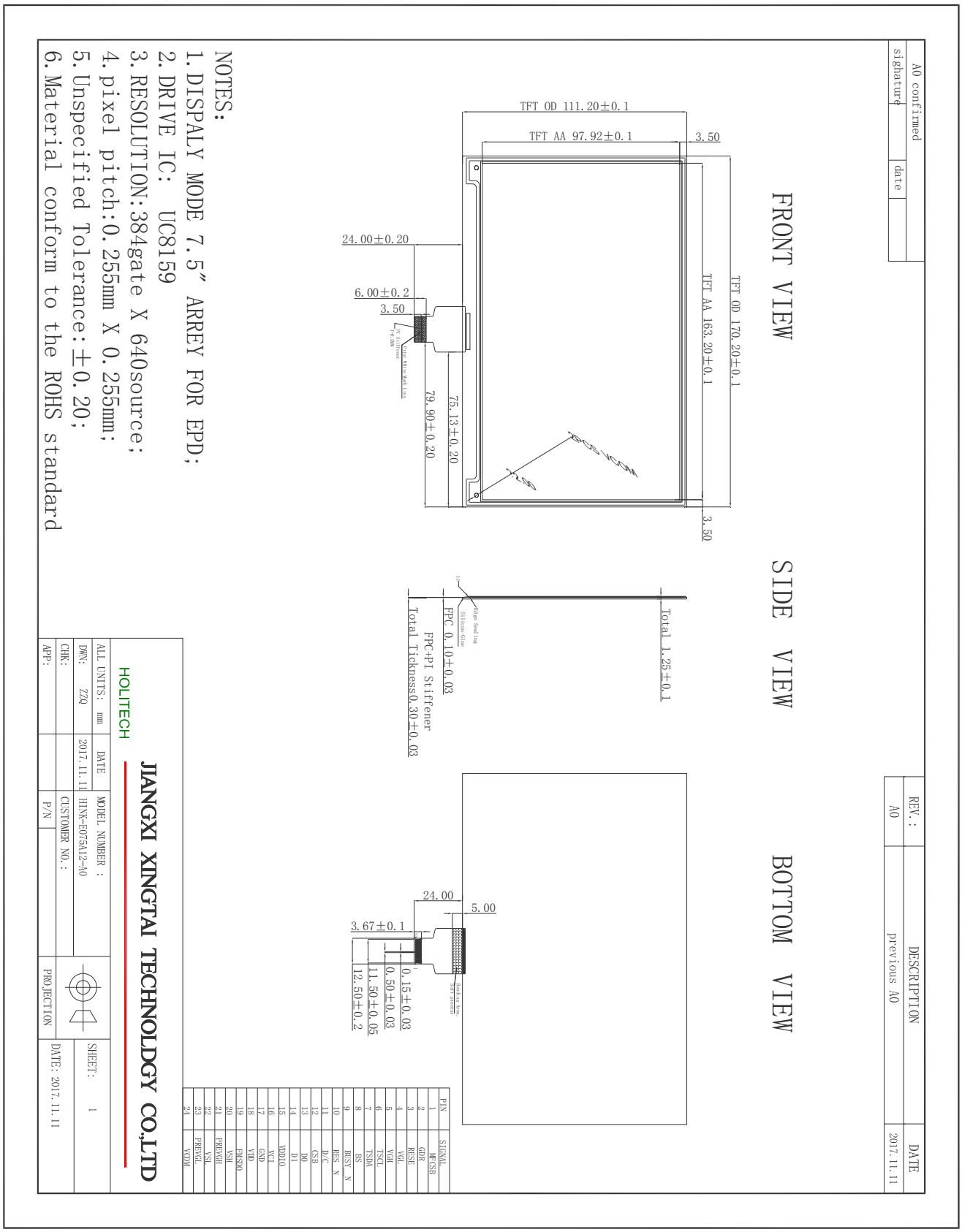
3. Application

Electronic Shelf Label System

4.Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	7.5	Inch	
Display Resolution	640(H)×384(V)	Pixel	Dpi:99
Active Area	163.20(H)×97.92(V)	mm	
Pixel Pitch	0.255×0.255	mm	
Pixel Configuration	Square		
Outline Dimension	170.20(H)×111.20 (V) ×1.25 (D)	mm	
Weight	40.4±0.2	g	

5. Mechanical Drawing of EPD module



6. Input/Output Terminals

Pin #	Single	Description	Remark
1	MFCSB	Serial communication chip select. It would bypass to MFCSB by R65H command.	
2	GDR	This pin is N-MOS gate control.	
3	RESE	Current Sense Input for the Control Loop	
4	VSL_LV	Negative source voltage (-3.0V ~ -15.0V).	
5	VSH_LV	Positive source voltage (+3.0V ~ +15.0V).	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS	Bus selection pin	Note 6-5
9	BUSY_N	Busy state output pin	Note 6-4
10	RST_N	Reset	Note 6-3
11	DC	Data /Command control pin	Note 6-2
12	CSB	Chip Select input pin	Note 6-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VDDA	Power Supply pin for the chip	
17	GND	Ground	
18	VDDD	Core logic power pin	
19	FMSDO	Serial communication data output . It would bypass to FMSDO by R65H command.	
20	VSH	Positive Source driving voltage	
21	VGH	Positive Gate driving voltage	
22	VSL	Negative Source driving voltage	
23	VGL	Negative Gate voltage.	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CSB is pulled LOW.

Note 6-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RST_N) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY_N) is Busy state output pin. When Busy_N is High the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy_N pin High when the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 6-5: This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected.

Table: Bus interface selection

BS	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

7. COMMAND TABLE

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel setting(PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	-	#	#	#	#	RES[1],RES[0], LUT_EN, UD,SHL,SHD_N,RST_N	0Fh
		0	1	-	-	-	#	-	-	-	-	VCM_HZ	00h
2	Power setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	-	-	#	#	-	#	#	#	EDATA_SEL, EDATA_SET, VSource_LV_EN, VSource _EN, VGate_EN	07h
		0	1	-	-	-	-	-	#	#	#	VGHL_LV[1:0]	01h
		0	1	-	-	#	#	#	#	#	#	VDPS_LV[5:0]	05h
		0	1	-	-	#	#	#	#	#	#	VDNS_LV[5:0]	05h
3	Power OFF(POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting(PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	-	-	#	#	-	-	-	-	T_VDS_OFF[1:0]	00h
5	Power ON(PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	00h
		0	1			#	#	#	#	#	#	BT_PHC[5:0]	00h
7	Deep sleep(DSLP)	0	0	0	0	0	0	0	1	1	1		07h
		0	1	1	0	1	0	0	1	0	1	Check code	A5h
8	Data Start Transmission 1 (DTM1) (x-byte command)	0	0	0	0	0	1	0	0	0	0		10h
		0	1	-	#	#	#	-	#	#	#	KPixel1[2:0], KPixel2[2:0]	00h
		0	1										
		0	1	-	#	#	#	-	#	#	#	Kpixel[2M-1][2:0], Kpixel[2M][2:0]	00h
9	Data Stop(DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	-	-	-	-	-	-	-	Data_flag	
10	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
11	Image Process Command (IPC)	0	0	0	0	0	1	0	0	1	1		13h
		0	1	-	-	-	#	-	#	#	#	IP_EN, IP_SEL[2:0]	00h
12	PLL control(PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	-	-	#	#	#	#	#	#	M[2:0], N[2:0]	3Ch
13	Temperature Sensor Command (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	D[10:3]/TS[7:1]	00h
		1	1	#	#	#	-	-	-	-	-	D[2:0]/TS[0]	00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
14	Temperature Sensor Calibration (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	-	-	-	-	-	-	-	TSE	00h
15	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h
16	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
17	Vcom and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h
		0	1	#	#	#	#	#	#	#	#	VBD[2:0], DDX, CDI[3:0]	F7h
18	Lower Power Detection(LPD)	0	0	0	1	0	1	0	0	0	1		51h
		1	-	-	-	-	-	-	-	-	#	LPD	01h
19	TCON Setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G[3:0],G2S[3:0]	22h
20	TCON resolution (TRES)	0	0	0	1	1	0	0	0	0	1		61h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	-	-	-	-	-	-	#	#	HRES[9:0]	00h
		0	1	-	-	-	-	-	-	-	#		00h
		0	1	#	#	#	#	#	#	#	#	VRES[8:0]	00h
21	SPI flash control (DAM)	0	0	0	1	1	0	0	1	0	1		65h
		0	1	-	-	-	-	-	-	-	#	DAM	00h
22	Revision(REV)	0	0	0	1	1	1	0	0	0	0		70h
		0	1	-	-	#	#	#	#	#	#	MAN,SHRK,LUT_ REV[3:0]	00h
23	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	-	-	#	#	#	#	#	#	I2C_ERR,I2C_BUS Y, DATA_FLAG, PON, POF, BUSY	02h
24	Auto Measurement Vcom (AMV)	0	0	1	0	0	0	0	0	0	0		80h
		0	1	-	-	#	#	#	#	#	#	AMVT[1:0],AMVX, AMVS, AMV,AMVE	10h
25	Read Vcom Value(VV)	0	0	1	0	0	0	0	0	0	1		81h
		1	1	-	#	#	#	#	#	#	#	VV[6:0]	00h
26	VCM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	-	#	#	#	#	#	#	#	VDCS[6:0]	02h

1)Panel Setting (PSR) (R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	RES1	RES0	LUT_EN	-	UD	SHL	SHD_N	RST_N

RES[1:0]: Display resolution setting (source×gate)

00b: 640×480 (default)

01b: 600×450

10b: 640×448

11b: 600×448

LUT_EN: LUT selection

0: Using LUT from external Flash.

1: Using LUT from register.

UD: Gate Scan Direction

0: Scan down First line to last: Gn→·····→G1

1: Scan up. (default) First line to last: G1→ ·····→Gn

SHL: Source shift direction

0: Shift left. First data to last data: Sn→·····→S1

1: Shift right First data to last data: S1→·····→Sn

SHD_N: Booster switch

0: DC-DC converter OFF.

1: DC-DC converter ON (Default)

When SHD_N become low, DC-DC will turn OFF. Register and SRAM data will keep until VDD OFF. SD output and VCOM will remain previous condition. It may have two conditions: 0v or floating.

RST_N: Soft Reset

0: The controller is reset. Reset all registers to their default value.

1: Normal operation (Default). Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V

When RST_N become low, driver will reset. All register will reset to default value. Driver all function will disable. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

VCM_HZ: VCOM Hi-Z function

0: VCOM normal output. (Default)

1: VCOM floating.

2) Power Setting (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1
	0	1	-	-	EDATA_SEL	EDATA_SET	-	VSource_LV_EN	VSource_EN	VGate_EN
	0	1	-	-	-	-	-		VGHL_LVL[1:0]	
	0	1	-	-	VDPS_LV [5:0]					
	0	1	-	-	VDNS_LV [5:0]					

EDATA_SEL: EDATA selection for pure driver mode

0 : When EDATA_SET=1, pixel bit =2`b11 output VDPS_L level

1 : When EDATA_SET=1, pixel bit =2`b11 output VDNS_L level (default)

EDATA_SET: EDATA setting for pure driver mode

0: 3-bit data mode for pure driver

1: 2-bit data mode for pure driver (default)

Vsource_LV_EN: VSource LV power selection.

0: External source power from VSH_LV and VSL_LV pin.

1: Internal DCDC function for generate source power. (default)

VSource_EN: VSource power selection.

0: External source power from VSH and VSL pin.

1: Internal DCDC function for generate source power. (default)

VGate_EN: VGate power selection.

0: External gate power from VGH and VGL pin.

1: Internal DCDC function for generate gate power. (default)

VGHL_LVL[1:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage level
00	VGH=20V, VGL= -20V
01 (Default)	VGH=19V, VGL= -19V
10	VGH=18V, VGL= -18V
11	VGH=17V, VGL= -17V

VDPS_LV[5:0]: Internal VDH power selection for Red LUT.

VDPS_LV	VDH_V
000000	3.0V
000001	3.2V
000010	3.4V
000011	3.6V
000100	3.8V
000101	4.0V (Default)
..	..
111100	15.0V

VDNS_LV[5:0]: Internal VDL power selection for Red LUT.

VDNS_LV	VDL_V
000000	-3.0V
000001	-3.2V
000010	-3.4V
000011	-3.6V
000100	-3.8V
000101	-4.0V (Default)
111100	-15.0V

3) Power OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After power off command, driver will power off based on the Power OFF Sequence, BUSY signal will become “0”.

The Power OFF command will turn off DCDC, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off.

SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

4) Power OFF Sequence Setting(PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	T_VDS_OFF[1:0]					

T_VDS_OFF[1:0]: Power OFF Sequence of VDH and VDL.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

5) Power ON (PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, driver will power on based on the Power ON Sequence.

After power on command and all power sequence are ready, then BUSY signal will become “1”.

6) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	0	0	1	1	0
	0	1	BTPHA7	BTPHA6	BTPHA5	BTPHA4	BTPHA3	BTPHA2	BTPHA1	BTPHA0
	0	1	BTPHB7	BTPHB6	BTPHB5	BTPHB4	BTPHB3	BTPHB2	BTPHB1	BTPHB0
	0	1	-	-	BTPHC5	BTPHC4	BTPHC3	BTPHC2	BTPHC1	BTPHC0

BTPHA7[7:6] **BTPHB7[7:6]**	**BTPHA[5:3],** **BTPHB[5:3],** **BTPHC[5:3],**	**BTPHA[2:0]** **BTPHB[2:0]** **BTPHC[2:0]**
Soft Start Phase Period (mS)	**Driving Strength**	**Minimum OFF Time (uS)**
00b: 10 mS **01b: 20** **10b: 30** **11b: 40**	**000b: (reserved)** **001b: (reserved)** **010b: 1** **011b: 2** **100b: 3** **101b: 4** **110b: 5** **111b: 6 (strongest)**	**000b: 0.26 uS** **001b: 0.31** **010b: 0.36** **011b: 0.52** **100b: 0.77** **101b: 1.61** **110b: 3.43** **111b: 6.77**

7) Deep sleep (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hard ward reset assertion.

The only one parameter is a check code, the command would be executed if check code is A5h.

8) Data Start Transmission 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Dummy	KPixel12	KPixel11	KPixel10	Dummy	KPixel22	KPixel21	KPixel20
	0	1	…	…	…	…	…	…	…	…
	0	1	Dummy	Kpixel	Kpixel	Kpixel	Dummy	Kpixel	Kpixel	Kpixel

This Command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Datastop command (R11H). Then the chip will start to send data/VCOM for panel.

Kpixel[1~2M][2:0] :

Kpixel [2:0]	Source Driver Output	
	DDX=1(default)	DDX=0
	LUT	LUT
000	Black	White
001	Gray1	Gray2
010	Gray2	Gray1
011	White	Black
100	Red0	Red3
101	Red1	Red2
110	Red2	Red1
111	Red3	Red0

9) Data stop (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	0	0	1
	1	1	data-flag	-	-	-	-	-	-	-

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (10h) or “Data Stop” (11h) commands, BUSY signal will become “0” until display update is finished.

10) Display Refresh (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY signal will become “0” until display update is finished.

11) Image Process Command (IPC) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Image Process Setting	0	0	0	0	1	0	0	0	1	1
	0	1	-	-	-	IP_EN		IP_SEL[2:0]		

After this command is issued, image process engine will find thin lines/pixels from frame SRAM and update the frame SRAM for applying new gray level waveform.

IP_EN: Image process enable.

0: No action.

1: Image process enable (auto return to ‘0’ after image process is finished.

IP_SEL[2:0]: Image process selection.

000 : Deal with 1-pixel width

001 : Deal with 2-pixel width

010 : Deal with 3-pixel width

011 : Deal with 1-pixel and 2-pixel width

100 : Deal with 1-pixel, 2-pixel and 3-pixel width

Others : Deal with 1-pixel width

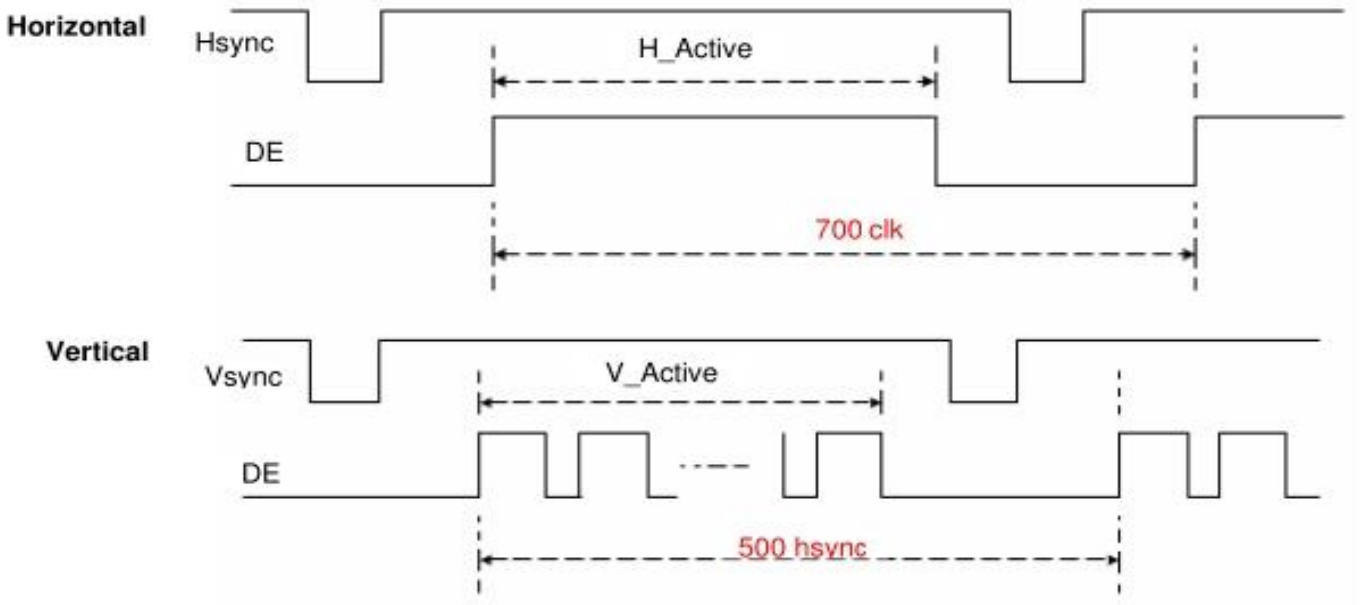
After “Image Process Command” (13h), BUSY_N signal will become “0” until image process is finished

12) PLL Control (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	M[2:0]			N[2:0]		

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

M	N	FR	M	N	FR	M	N	FR	M	N	FR
1	1	29	3	1	86	5	1	143	7	1	200
	2	14		2	43		2	71		2	100
	3	10		3	29		3	48		3	67
	4	5		4	21		4	36		4	50
	5	7		5	17		5	29		5	40
	6	6		6	14		6	24		6	33
	7	5		7	12		7	20		7	29
2	1	57	4	1	114	6	1	171			
	2	29		2	57		2	86			
	3	19		3	38		3	57			
	4	14		4	29		4	43			
	5	11		5	23		5	34			
	6	10		6	19		6	29			
	7	8		7	16		7	24			



13) Temperature Sensor Command(TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10	D9/TS7	D8/TS6	D7/TS5	D6/TS4	D5/TS3	D4/TS2	D3/TS1
	1	1	D2/TS0	D1	D0					

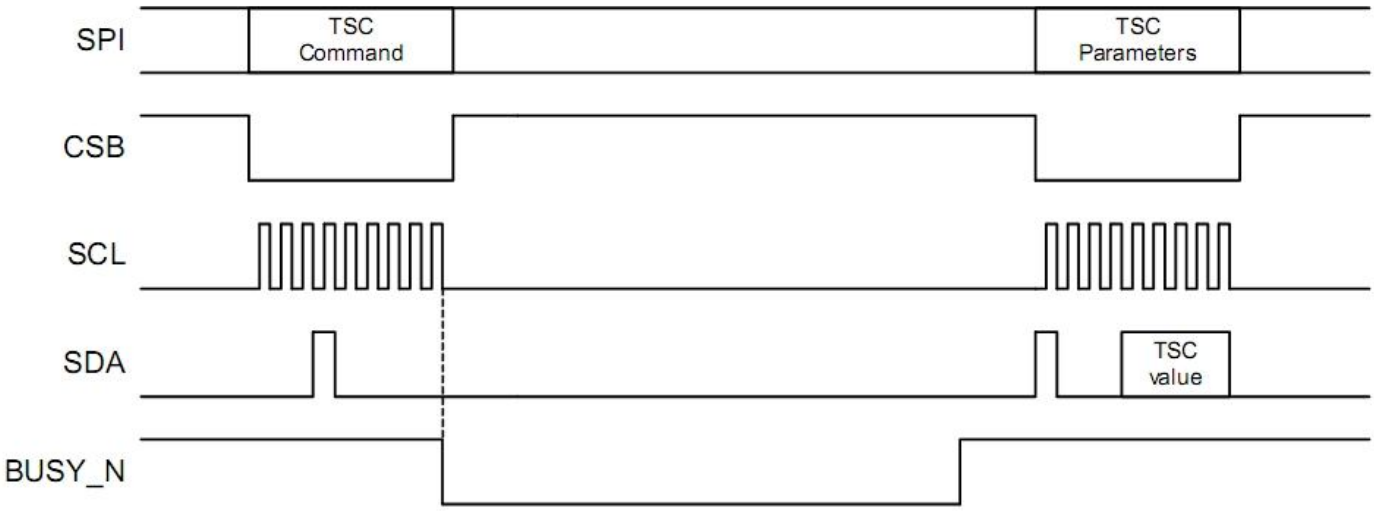
This command reads the temperature sensed by the temperature sensor.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

Bit 7~0	Temperature(℃)
0000 0000b	0
0000 0001b	0.5
0000 0010b	1
..	..
0101 1010b	45
..	..
0110 0100b	50
..	..
1100 1110b	-25
..	..
1111 1110b	-1
1111 1111b	-0.5

BUSY become low after TSC command. When BUSY become high, Parameter can be read.



14) Temperature Sensor Calibration (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Sensor Selection	0	0	0	1	0	0	0	0	0	1
	0	1	TSE	-						

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Select internal temperature sensor (default) 1: Select external temperature sensor.

15) Temperature Sensor Write (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Sensor Selection	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]-							
	0	1	WMSB[7:0]							
	0	1	WLSB[7:0]							

This command could write data to the external temperature sensor.

WATTR: D[7:6]: I2C Write Byte Number

00: 1 byte (head byte only)

01: 2 bytes (head byte + pointer)

10: 3 bytes (head byte + pointer + 1stparameter)

11: 4 bytes (head byte + pointer + 1stparameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor.

16) Temperature Sensor Read (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Sensor Selection	0	0	0	1	0	0	0	0	1	1
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command could read data from the external temperature sensor.

RMSB[7:0]: MSByte of read-data from external temperature sensor.

RLSB[7:0]: LSByte of read-data from external temperature sensor.

17) VCOM and Data Interval Setting(CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval between Vcom and Data	0	0	0	1	0	1	0	0	0	0
	0	1	VBD[2:0]			DDX	CDI[3:0]			

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[2:0]: Border output selection.

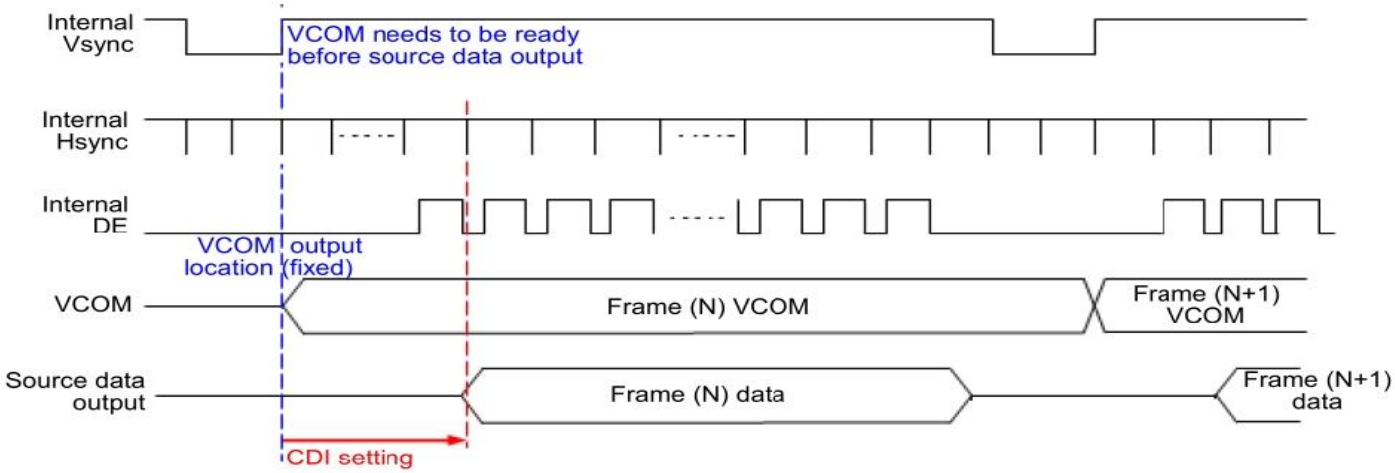
DDX: Data polality.

The mapping table of VBD[2:0] and DDX is listed as below.

VBD[2:0]	Border Output	
	DDX=1(default)	DDX=0
	LUT	LUT
000	Black	White
001	Gray1	Gray2
010	Gray2	Gray1
011	White	Black
100	Red0	Floating
101	Red1	Red2
110	Red2	Red1
111	Floating	Red0

CDI[3:0]: Vcom and data interva

CDI[3:0]	Vcom and Data Interval	CDI[3:0]	Vcom and Data Interval
0000b	17 hsync	1000	9
0001	16	1001	8
0010	15	1010	7
…			
0110	11	1110	3
0111	10(Default)	1111	2



Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal temperature sensor switch

0: Low power input (VDD<2.5V) 1: Normal status (default)

19) TCON Setting(TCON) (R60h)

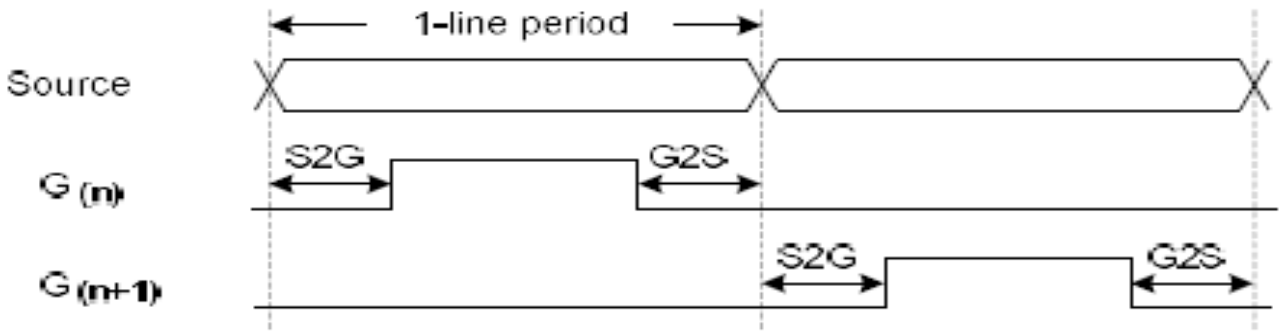
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing	0	0	0	1	1	0	0	0	0	0
Temperature	0	1	S2G[3:0]				G2S[3:0]			

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period		S2G[3:0] or G2S[3:0]	Period
0000b	4		…	…
0001	8		1011	48
0010	12(Default)		1100	52
0011	16		1101	56
0100	20		1110	60
0101	24		1111	64

Period = 660 nS.



20) Resolution Setting(TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	0	0	0	1	1	0	0	0	0	1
	0	1	HRES[7:0]							
	0	1	-	-	-	-	-	-	HRES[9:8]	
	0	1	VRES[7:0]							
	0	1	-	-	-	-	-	-	-	VRES[8]

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[9:0]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Resolution setting (R61H) has higher priority than RES[1:0] (R00H). Resolution should be even number.

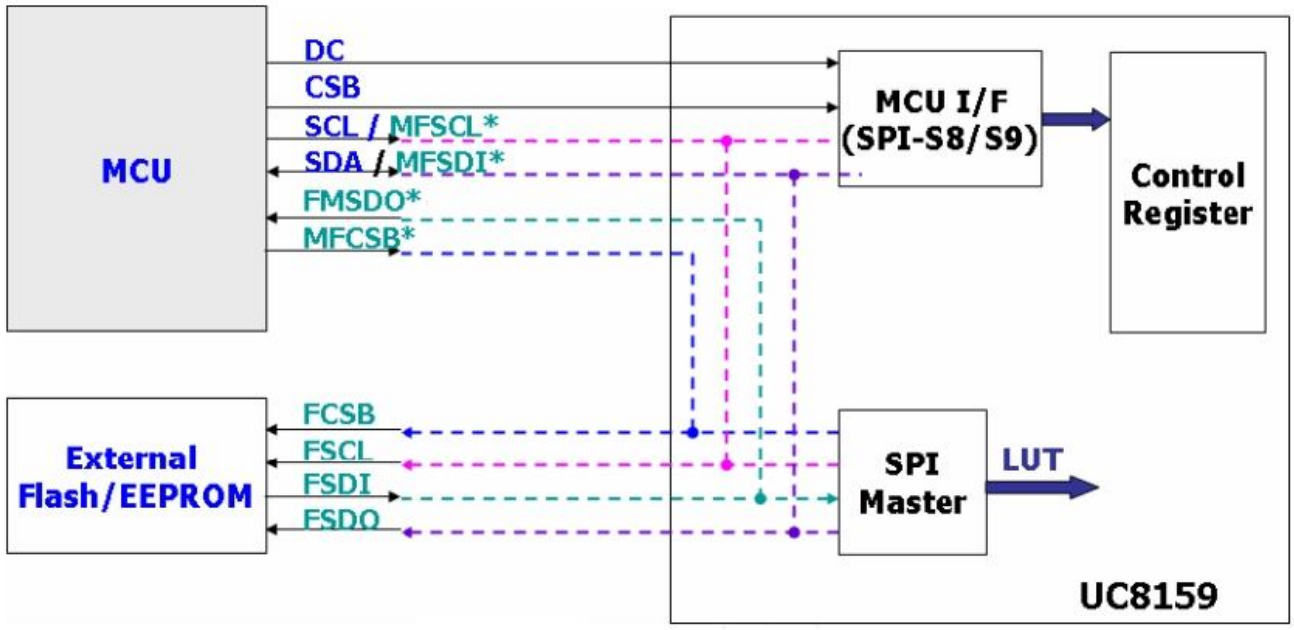
21) SPI Flash Control(DAM) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	1	0	0	0	0	1
	1	1	-	-	-	-	-	-	-	DAM

This command defines MCU host direct access external memory mode.

DAM: 0: Disable (default)

1: Enable. By pass MFSCL*, MFSDI*, MFSDO*, AND MFCSB* to external flash.



22) Revision(REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
RLUT/Chip Revision	0	0	0	1	1	1	0	0	0	0
	1	1	LUTVER[7:0]							
	1	1	LUTVER[15:8]							
	1	1	0	0	0	0	CHREV[3:0]			

The LUTVER[15:0] is read from OTP address = 25001 and 25000.

LUTVER[15:0]: LUT versionL.

CHREV [3:0]: Chip Revision.

23) Get status(FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	-	-	I2C_ERR	I 2C_ BUSY	data_ flag	PON	POF	BUSY

This command reads the IC status.

I2C_ERR: I2C master error status

I2C_BUSY: I2C master busy status (low active)

Data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY: Driver busy status (low active)

24) Auto measure vcom(AMV) (R80h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure vcom	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		AMVX	AMVS	AMV	AMVE

This command implements related VCOM sensing setting.

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s 01b: 5s (default)

10b: 8s 11b: 10s

AMVX: Auto Measure VCOM without XON function

0: Measure VCOM without XON function. (Gate scanning) (default)

1: Measure VCOM without XON function. (All Gate ON)

AMVS: Source output of AMV

0: Set Source output to 0V during Auto Measure VCOM period. (default)

1: Set Source output to 3V (or VDPS_L) during Auto Measure VCOM period.

AMV: Analog signal

0: Get Vcom value with the VV command (R81h) (default)

1: Get Vcom value in analog signal.

AMVE: Auto Measure Vcom Enable (/Disable)

0: Disabled 1: Enabled

25) VCOM Value(VV) (R81h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure vcom	0	0	1	0	0	0	0	0	0	1
	1	1	-	VV [6:0]						

This command gets the Vcom value.

VV[6:0]: Vcom Value Output

VV[60]	VCOM Value
000 0000b	0V
000 0001b	-0.05V
000 0010b	-0.10V
000 0011b	-0.15V
101 0000b:	-4.00V
(Others)	-4.00V

26) VCOM-DC Setting(VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	VDCS[6:0]						

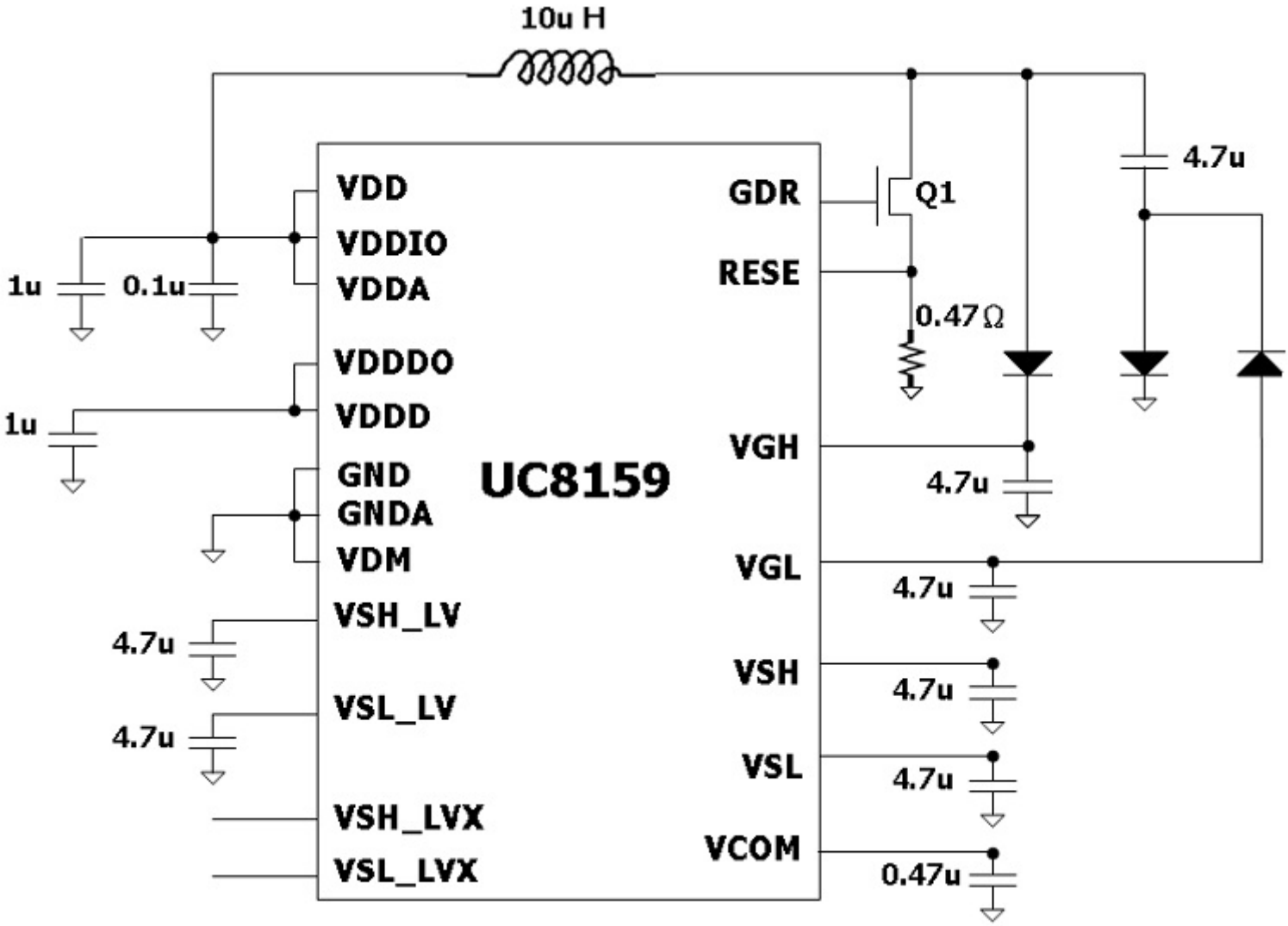
This command sets VCOM_DC value.

VDCS[6:0]: VCOM_DC Setting

VDCS[6:0]	VCOM_DC Value
000 0000b	(Reserved)
000 0001b	(Reserved)
000 0010b	-0.10v
000 0011b	-0.15v
000 0100b	-0.20v
..	..
101 0000b	-4.0v
(others)	-4.0v

8. Electrical Characteristics

8-1) Reference Circuit



8-2) Absolute maximum rating

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.3 to +3.6	V
T_{OPR}	Operation temperature range	-25 to 25	℃
T_{STG}	Storage temperature range	-25 to 60	℃

8-3) Panel DC Characteristics

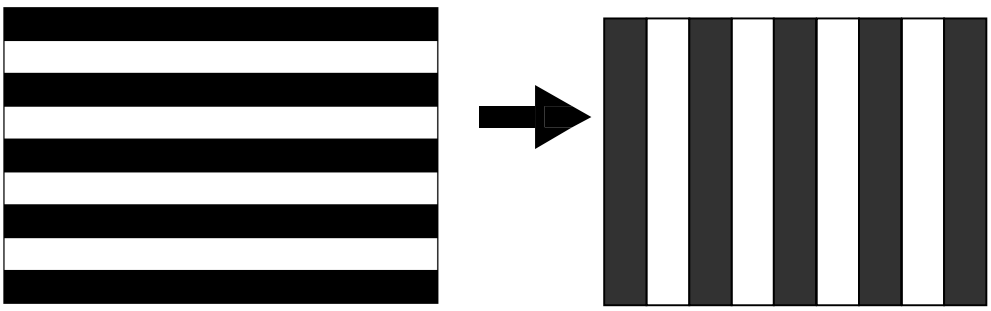
The following specifications apply for: VSS = 0V, VCI = 3.3V, TA = 25℃

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCI	Logic Supply Voltage	-	2.3	3.3	3.6	V
VIH	High level input voltage	Digital input pins	0.8xV DDIO	-	V DDIO	V
VIL	Low level input voltage	Digital input pins	GND	-	0.2xV DDIO	V
VOH	High level output voltage	IOH= 400uA	0.8xV DDIO	-	-	V
VOL	Low level output voltage	IOH= -400uA	GND	-	0.2xV DDIO	V
Iupdate	Module operating current	-	-	27	-	mA
Isleep	Deep sleep mode	VCI = 3.3V	-	7	-	uA

- The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 8-3)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 8-3

The Typical power consumption



8-4) Panel AC Characteristics

8-4-1) MCU Interface

8-4-1-1) MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS pins. When it is "Low", 4-wire SPI is selected. When it is "High", 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CSB	DC	RST_N
SPI4	SDIN	SCLK	CSB	DC	RST_N
SPI3	SDIN	SCLK	CSB	L	RST_N

Table 8-4-1-1: MCU interface assignment under different bus interface mode

Note 8-2: L is connected to GND

Note 8-3: H is connected to VCI

8-4-1-2) MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, DC, CSB. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Function	CSB	DC	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Table 8-4-1-2: Control pins of 4-wire Serial Peripheral interface

Note8-4: ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

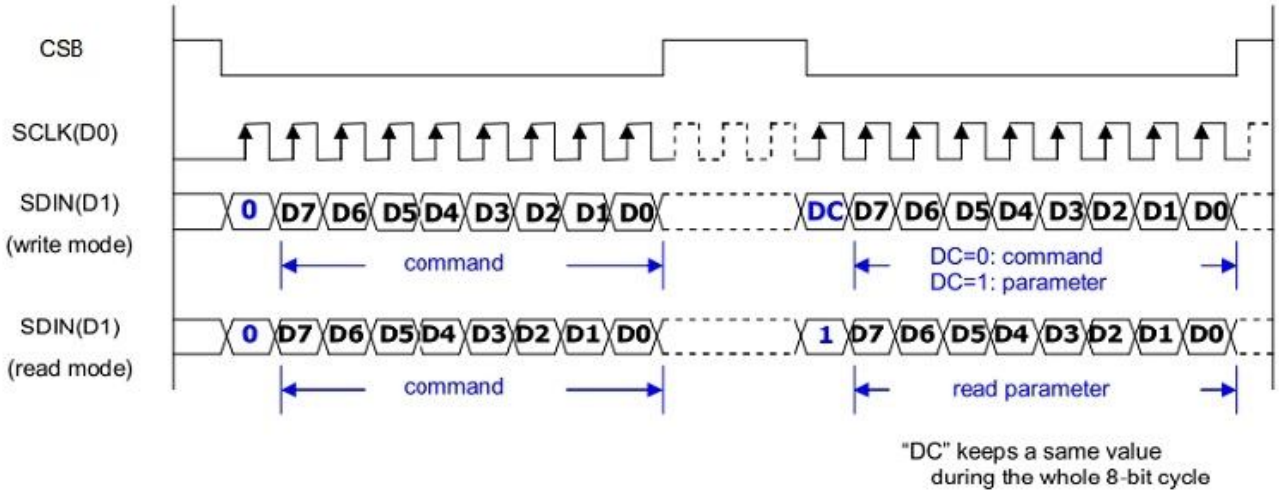


Figure8-4-1-2: Write procedure in 4-wire Serial Peripheral Interface mode

8-4-1-3) MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CSB.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN, The pin DC can be connected to an external ground.

The operation is similar to 4-wire serial interface while DC pin is not used. There are altogether 9-bits will be shifted into the shift register on each ninth clock in sequence: DC bit, D7 to D0 bit. The DC bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (DC bit = 1) or the command register (DC bit = 0).Under serial mode,

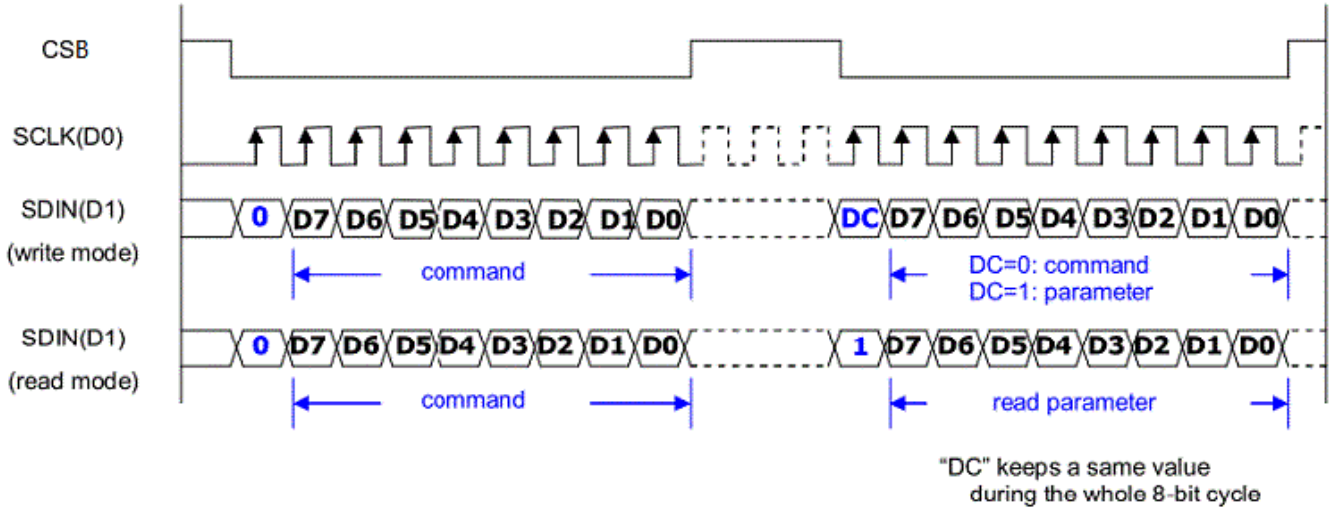
only write operations are allowed.

Function	CSB	DC	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

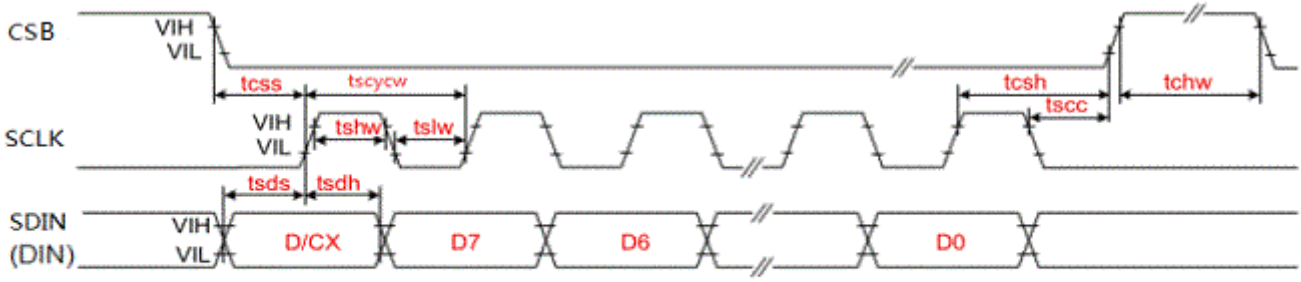
Table 8-4-1-3: Control pins of 3-wire Serial Peripheral Interface

Note 8-5: ↑ stands for rising edge of signal

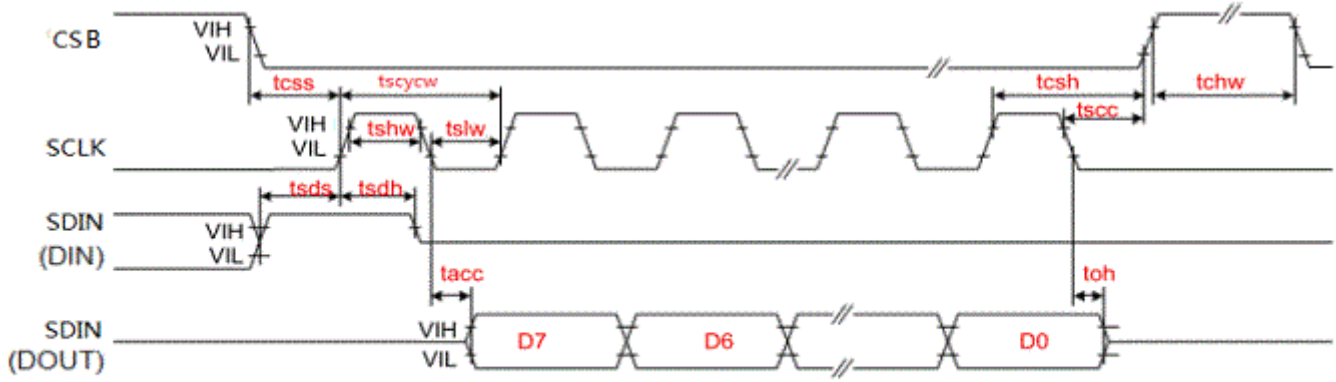
Figure 8-4-1-3: Write procedure in 3-wire Serial Peripheral Interface mode



8-4-2) Timing Characteristics of Series Interface



3-wire Serial Interface – Write



3-wire Serial Interface – Read

Symbol	Signal	Parameter	Min	Typ	Max	Unit
Tcss	CSB	Chip Select Setup Time	60	-	-	ns
Tcsh		Chip Select Hold Time	65	-	-	ns
Tscc		Chip Select Setup Time	20	-	-	ns
Tchw		Chip Select Setup Time	40	-	-	ns
Tscycw	SCLK	Serial clock cycle (write)	100	-	-	ns
Tshw		SCL “H” pulse width (write)	35	-	-	ns
Tslw		SCL “L” pulse width (write)	35	-	-	ns
Tscycr		Serial clock cycle (Read)	150	-	-	ns
Tshr		SCL “H” pulse width (Read)	60	-	-	ns
Tslr		SCL “L” pulse width (Read)	60	-	-	ns
Tsds	SDIN (DIN) (DOUT)	Data setup time	30	-	-	ns
Tsdh		Data hold time	30	-	-	ns
Tacc		Access time	10	-	-	ns
toh		Output disable time	15	-	-	ns

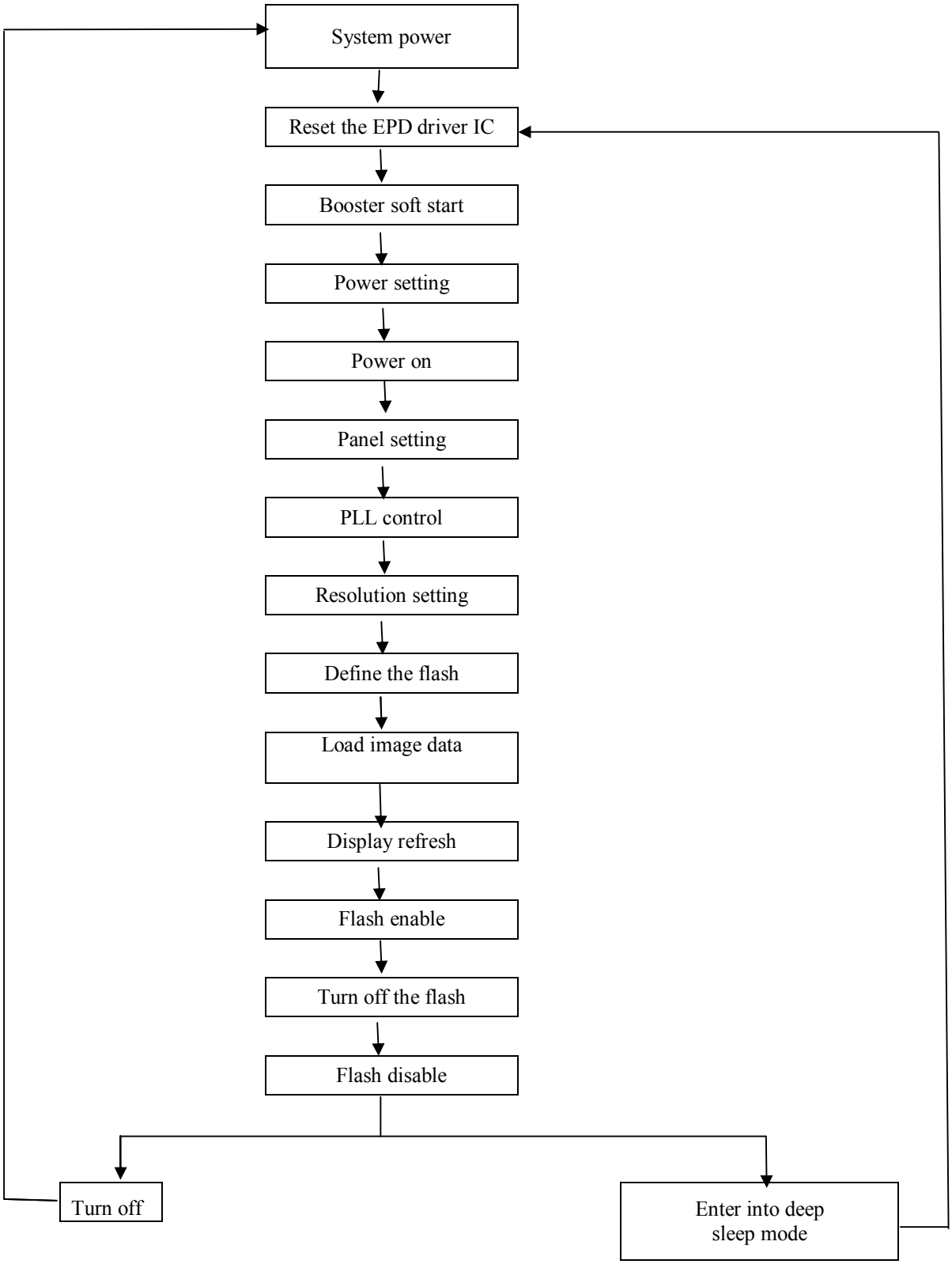
8-5) Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	-25℃	1326	-	mAs	-
Deep sleep mode	-	-25℃	7	-	uA	-

9. Typical Operating Sequence

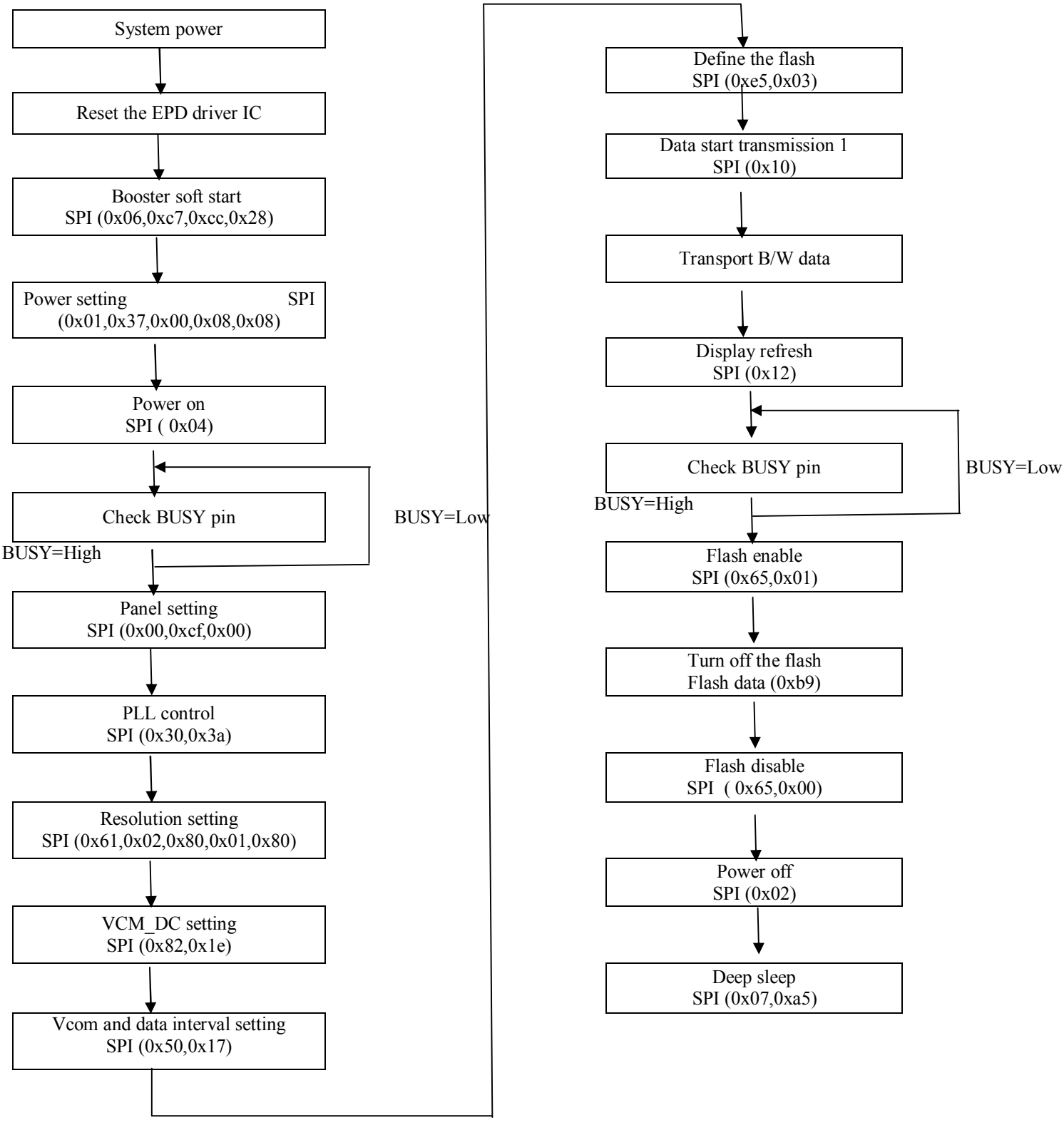
9-1) Normal Operation Flow

1. LUT from flash



9-2) Reference Program Code

1.LUT from flash



10. Optical characteristics

10.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 10-1
Gn	2Grey Level	-	-	DS+(WS-DS)×n(m-1)	-	L*	-
CR	Contrast Ratio	indoor	-	10	-	-	-
Panel's life	-	-25℃～25℃		5years or 1000000 times	-	-	Note 10-2

WS: White state, DS : Dark state

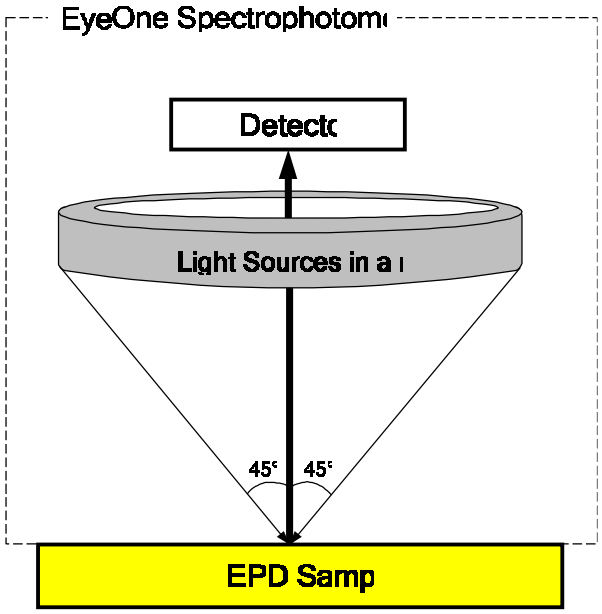
m: 2

Note 10-1: Luminance meter : Eye - One Pro Spectrophotometer

10.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

CR = Rl/Rd

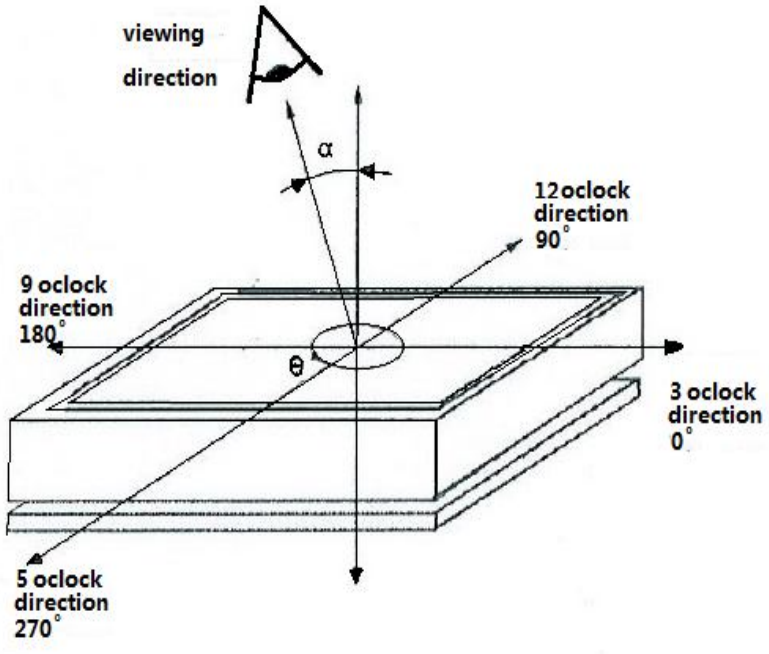


10.3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



11. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Product specification	The data sheet contains final product specifications.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification

ROHS

REMARK

All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

12. Reliability test

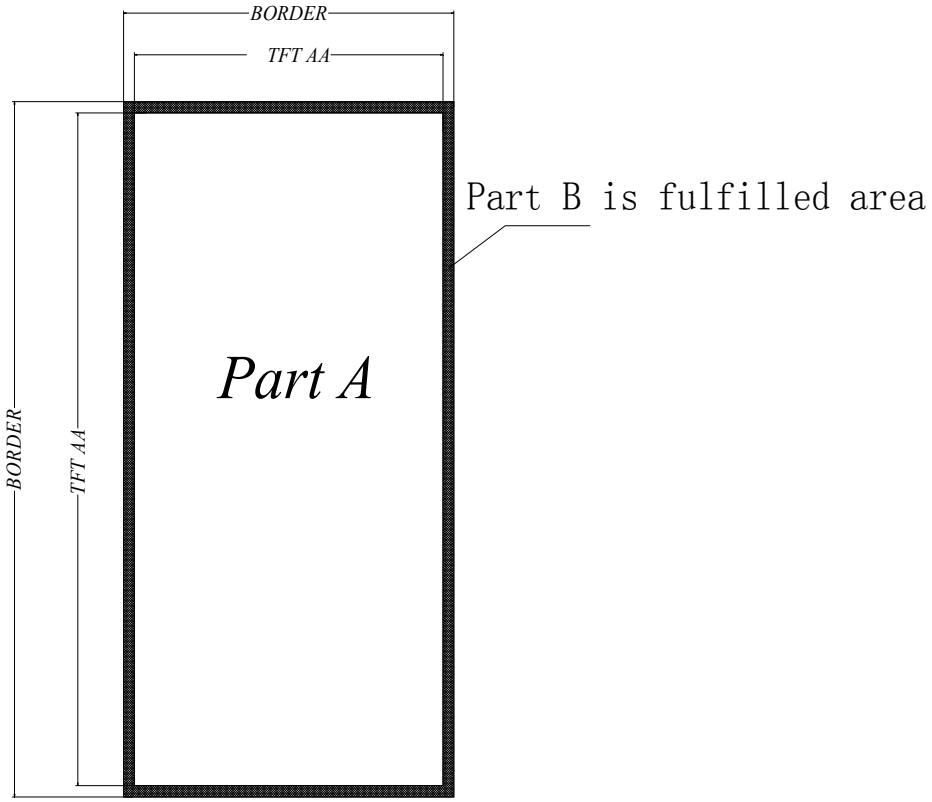
	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T=25℃，For 240Hr	IEC 60 068-2-2Bb	
2	Low-Temperature Operation	T = -25℃ for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T=70℃ RH=40%RH For 240Hr Test in white pattern	IEC 60 068-2-2Bb	
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Storage	T=60℃，RH=80%RH，For 480Hr Test in white pattern	IEC 60 068-2-3CA	
6	Temperature Cycle	-25℃(30min)~60℃(30min)，50 Cycle Test in white pattern	IEC 60 068-2-14NB	
7	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
8	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	
9	UV exposure Resistance	765 W/㎡ for 168hrs,40℃	IEC 60068-2-5 Sa	
10	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	IEC61000-4-2	

Actual EMC level to be measured on customer application.

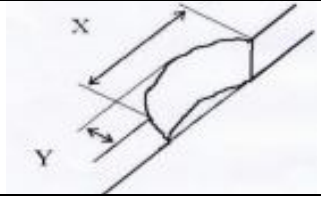
Note1: The protective film must be removed before temperature test.

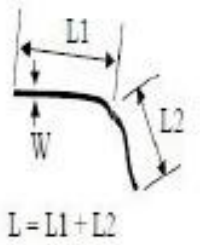
Note2： Stay white pattern for storage and non-operation test.

13. PartA/PartB specification

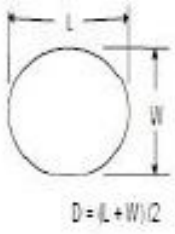


14. Point and line standard

Shipment Inspection Standard						
Equipment：Electrical test fixture, Point gauge						
Outline dimension	170.20 (H) × 111.20(V) × 1.25(D)	Unit：㎜	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19℃～25℃	55%±5%RH	800～1300Lux	300 ㎜	35Sec	
Defet type	Inspection method	Standard		Part-A		Part-B
Spot	Electric Display	D≤0.25 ㎜		Ignore		Ignore
		0.25 ㎜<D≤0.4 ㎜		N≤4		Ignore
		0.40 ㎜<D≤0.5 ㎜		N≤1		Ignore
		D>0.5 ㎜		Not Allow		Ignore
Display unwork	Electric Display	Not Allow		Not Allow		Ignore
Display error	Electric Display	Not Allow		Not Allow		Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2 ㎜，W≤0.2 ㎜		Ignore		Ignore
		2.0mm<L≤8.0mm，0.2<W≤0.5mm,		N≤2		Ignore
		L>8.0 ㎜，W>0.5 ㎜		Not Allow		Ignore
PS Bubble	Visual/Film card	D≤0.25mm		Ignore		Ignore
		0.25mm≤D≤0.40mm		N≤4		Ignore
		D>0.40 mm		Not Allow		Ignore
Side Fragment	Visual/Film card	X≤6mm，Y≤0.5mm, Do not affect the electrode circuit , Ignore				
						
Remark	1.Cannot be defect & failure cause by appearance defect；					
	2.Cannot be larger size cause by appearance defect；					
	L=long W=wide D=point size N=Defects NO					

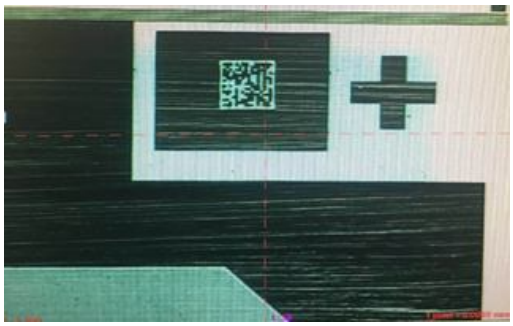


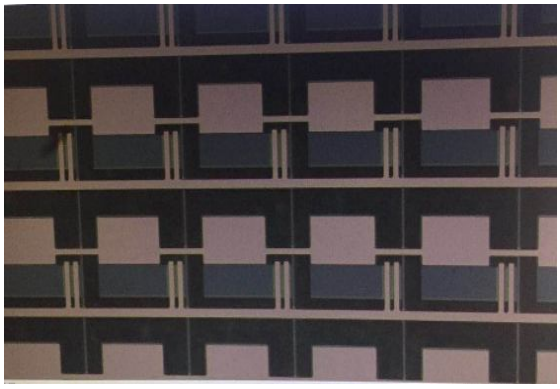
Line Defect

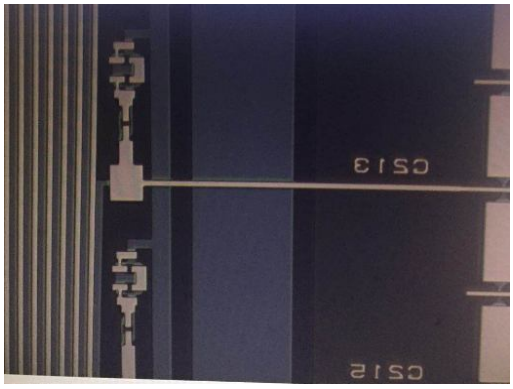


Spot Defect de D=point size

14.1 TFT Glass.







15.Barcode

AAAAAAA B CCCC DD

EEE FFF GGG HH III

AAAAAAA	B	CCCC	DD	EEE	FFF	GGG	HH	III
①	②	③	④	⑤	⑥	⑦	⑧	⑨

① AAAAAAA——Module of EPD
② B—— Normal Lot
③ CCCC——Date of production
④ DD——Production lot
⑤ EEE—— FPL
⑥ FFF——TFT
⑦ GGG——PS
⑧ HH——Edge sealing Adhesive
⑨ III——NO.

16.P acking

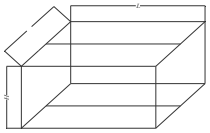
Packing Spec

Sheet No:

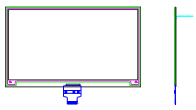
HOLITECH	Part No	HINK-E075A12-A1	DATE	2018.1.5	VER	A1	Page	2-1

一, Package Type: Box

Box No	HINK-E029A01-ZX-A0
Box size	515*322*170
Containment	48PCS

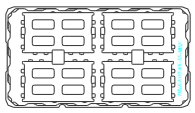


PRODUCT DRAWING

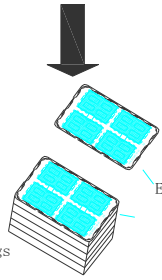


二, Inside package type:Plastic Tray unit: mm

Plastic Tray	465*280*15	13 pcs
Anti-static foil bags	700*530*0.1	1 pcs
EPE(inside)	408.17*114.75*2	24 pcs
EPE(Up-Down)	485*145*10	2 pcs
EPE(Left-Right)	285*480*10	2 pcs
EPE(Front-back)	310*145*10	2 pcs
Chip board	500*306*5	2 pcs
Quantity/tray	4 pcs	
Tray number/sheet	12+1 Sheets	
Box	1	

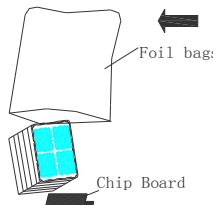


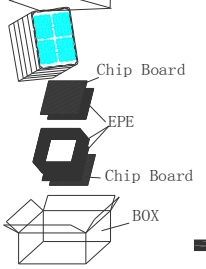
Step 1:
Material: Tray, EPE
Put the product in to the tray and keep the dispaly side up. Then put anti-static EPE in to each holes.



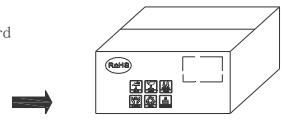
Step 2:
1) Must keep the angle 180 degree placed between the neighboring Plastic trays.
2) There are 12 layers product, total 4*12=48 pcs。
3) An empty Plastic tray intersects put on the top of the plastic trays.

Step 3
1) In each case, put 2 bags of desiccant. then seal the trays with adhesive tapes.
2) Put the trays into foil bags.
3) heat seal the foil bags.





Step 4:
1)First put a chip board on the buttom of the box, then placed the down EPE, the left - right and front -back EPE.
2) Placed the sealed products into the box.
3) The last placed the up EPE on the top of the trays, and place a chip board on it.



Step 5:
1) Seal the box with adhensive tapes 。
2) Paste the lable onto the exterior box, and the lable can't cover the safety , transfer and RoSH sign。

Design	Z.Z.Q	Approve	J.P.F	Confirm	X.X.M
Date	2018.1.5	Date	2018.1.5	Date	2018.1.5

Packing Spec

Sheet No

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The label outside the carton print as below

合力泰 HOLITECH	Packing Label 出货包装标签		
CUSTOMER: 客户名称:			
CUSTOMER P/N: 客户产品编码:			
CUSTOMER P/O: 客户订单号:			
HOLITECH P/N: 合力泰产品编码:			
N/W: 净重:	KG	G/W: 毛重:	KG
C/N: 箱号:	of		
QTY: 数量:	PCS	DATE: 日期:	
REMARK: 备注:			
SHIP FROM: 发货地址:			
SHIP TO: 收货地址:			
PACKAGE-ID: 外箱 ID:			

Design	X.Z.P	Approve	J.P.F	Confirm	X.X.M
Date	2018.1.6	Date	2018.1.6	Date	2018.1.6