Amiga 1000 Rejuvenator PALs "Best Guess"

I = Input, **O** = Combinatorial Output, **R** = Registered Output.

U28

A23	A23	1	I	+5V	20	VCC	VCC +5V
A22	A22	2	I	O	19	REJ3	ROME?
A21	A21	3	I	I/O	18	BLS	Blitter Slowdown
Address Strobe	AS	4	I	R - I/O	17	DTACK	Data Transfer Ack
?	REJ1	5	I	I/O	16	RE	RAM Enable
Overlay ROM over RAM	OVL	6	I	I/O	15	A20	A20
Override System Decoding	OVR	7	I	I/O	14	A19	A19
External Data Ready	XRDY	8	I	R - I/O	13	MYRAME	ROME?
C3 Clock (3.58Mhz rising edge)	C3	9	I	O	12	VPA	Valid Peripheral Address
GND	GND	10	I	I	11	C1	C1 Clock (3.58MHz falling edge)

PAL analyser shows fixed high output for 14,15,16,18 indicating those pins are inputs.
PAL analyser shows registered output for 13,17 indicating those pins are tri-state or feedback enabled.

U29

ROME?	REJ3	1	I	+5V	20	VCC	VCC +5V
A18	A18	2	I	O	19	XOE	Enable Rejuve ROM (_ROMEN)
RESET	RESET	3	I	I/O	18	CDW	Chip RAM Direction Write
Processor Read/Write	RW	4	I	I/O	17	CDR	Chip RAM Direction Read
Upper Data Strobe	UDS	5	I	I/O	16	UCEN	Upper CAS Enable
Lower Data Strobe	LDS	6	I	I/O	15	LCEN	Lower CAS Enable
(from jumper)	REJ.KICK	7	I	I/O	14	RRW	RAM Expansion RW
RAM Enable	RE	8	I	I/O	13	x	n.c. (internal use equation?)
C1 Clock (3.58MHz falling edge)	C1	9	I	O	12	ROM01	(enable MB ROMs for disk KS)
GND	GND	10	I	I	11	AS	Address Strobe

Even though pin 13 is n.c., the PAL analyser shows an active equation, indicating it might be used internally.

U30

Data Transfer Ack	DTACK	1	I	+5V	24	VCC	VCC +5V
RAM Enable	RAMEN	2	I	I	23	REGEN	Chip Register Enable
(possibly CLKE) ?	REJ.2	3	I	O	22	RTC.WR	Realtime Clock Write
(Chip RAM Enable) DAE?	REJ.CE	4	I	R - I/O	21	x	n.c. (internal use equation?)
Address Strobe	AS	5	I	R - I/O	20	x	n.c. (internal use equation?)
Upper Data Strobe	UDS	6	I	R - I/O	19	REJ4	CNT?
Overlay ROM over RAM	OVL	7	I	R - I/O	18	REJ1	?
Override System Decoding	OVR	8	I	R - I/O	17	REJ.OE2	(LS244 output enable)
Lower Data Strobe	LDS	9	I	R - I/O	16	REJ.OE1	(LS373 output enable)
C1 Clock (3.58MHz falling edge)	C1	10	I	O	15	RTC.RD	Realtime Clock Read
C3 Clock (3.58Mhz rising edge)	C3	11	I	I	14	PRW	Processor RW
GND	GND	12	GND	I	13	BLIT	Chip Memory Enable (DBR replace?)

PAL analyser shows registered output for 16,17,18,19,20,21
Even though pins 20,21 are n.c., the PAL analyser shows active equations, indicated they might be used internally.

U31

(memory cfg jumper)	MCFG2	1	I	+5V	24	VCC	VCC +5V
A23	A23	2	I	I	23	MCFG1	(memory cfg jumper)
A22	A22	3	I	O	22	RAMEN	RAM Enable
A21	A21	4	I	I/O	21	REJ.KICK	(kickstart select jumper)
Address Strobe	AS	5	I	R - I/O	20	REJ.CE	DAE? (Chip RAM Enable)
A20	A20	6	I	I/O	19	REGEN	Chip Register Enable
Overlay ROM over RAM	OVL	7	I	I/O	18	DTACK	Data Transfer Ack
Override System Decoding	OVR	8	I	I/O	17	x	n.c. (internal use equation?)
A19	A19	9	I	R - I/O	16	RE	RAM Enable
C1 Clock (3.58MHz falling edge)	C1	10	I	O	15	REJ.2	(possibly CLKE)?
A18	A18	11	I	I	14	C3	C3 Clock (3.58Mhz rising edge)
GND	GND	12	GND	I	13	A17	A17

PAL analyser shows fixed high output for 18,21 indicating those pins are inputs.
PAL analyser shows registered output for 16,20 indicating those pins are tri-state or feedback enabled.
Even though pin 17 is n.c., the PAL analyser shows an active equation, indicating it might be used internally.

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