Amiga 1000 Rejuvenator PALs "Best Guess"

I = Input, **O** = Combinatorial Output, **R** = Registered Output.

U28

A23	A23	1	I	+5V	20	VCC	VCC +5V
A22	A22	2	I	O	19	REJ3	?
A21	A21	3	I	I/O	18	_BLS	Blitter Slowdown
Address Strobe	_AS	4	I	R - I/O	17	_DTACK	Data Transfer Ack
?	REJ1	5	I	I/O	16	_RE	RAM Enable
Overlay ROM over RAM	OVL	6	I	I/O	15	A20	A20
Override System Decoding	_OVR	7	I	I/O	14	A19	A19
External Data Ready	XRDY	8	I	R - I/O	13	_ROME	Is unconnected, no longer used
C3 Clock (3.58Mhz rising edge)	_C3	9	I	O	12	_VPA	Valid Peripheral Address
GND	GND	10	I	I	11	_C1	C1 Clock (3.58MHz falling edge)

PAL analyser shows fixed high output for 14,15,16,18 indicating those pins are inputs.
PAL analyser shows registered output for 13,17 indicating those pins are tri-state or feedback enabled.

U29

?	REJ3	1	I	+5V	20	VCC	VCC +5V
A18	A18	2	I	O	19	_XOE	Enable Rejuve ROM
RESET	_RESET	3	I	I/O	18	_CDW	RAM Direction Write for mainboard
Processor Read/Write	_PRW	4	I	I/O	17	_CDR	RAM Direction Read for Mainboard
Upper Data Strobe	_UDS	5	I	I/O	16	UCEN	Upper CAS Enable
Lower Data Strobe	_LDS	6	I	I/O	15	LCEN	Lower CAS Enable
(from jumper)	REJ.KICK	7	I	I/O	14	_RRW	RAM Read/Write for Mainboard
RAM Enable	_RE	8	I	I/O	13	x	n.c. (internal use equation?)
C1 Clock (3.58MHz falling edge)	_C1	9	I	O	12	_ROM01	(enable MB ROMs for disk KS)
GND	GND	10	I	I	11	_AS	Address Strobe

Even though pin 13 is n.c., the PAL analyser shows an active equation, indicating it might be used internally.

U30

Data Transfer Ack	_DTACK	1	I	+5V	24	VCC	VCC +5V
RAM Enable	_RAMEN	2	I	I	23	_REGEN	Chip Register Enable
(most likely _CLKE)	REJ2	3	I	O	22	_CLKW	Realtime Clock Write
DMA Address Enable	_DAE	4	I	R - I/O	21	x	n.c. (internal use equation?)
Address Strobe	_AS	5	I	R - I/O	20	x	n.c. (internal use equation?)
Upper Data Strobe	_UDS	6	I	R - I/O	19	_CNT	counter
Overlay ROM over RAM	OVL	7	I	R - I/O	18	REJ1	?
Override System Decoding	_OVR	8	I	R - I/O	17	_CDWREJ	(_CDW for Rejuve RAM)
Lower Data Strobe	_LDS	9	I	R - I/O	16	_CDRREJ	(_CDR for Rejuve RAM)
C1 Clock (3.58MHz falling edge)	_C1	10	I	O	15	_CLKR	Realtime Clock Read
C3 Clock (3.58Mhz rising edge)	_C3	11	I	I	14	_PRW	Processor RW
GND	GND	12	GND	I	13	_BLIT	Chip Memory Enable (_DBR replace?)

PAL analyser shows registered output for 16,17,18,19,20,21
Even though pins 20,21 are n.c., the PAL analyser shows active equations, indicated they might be used internally.

U31

(memory cfg jumper)	MCFG2	1	I	+5V	24	VCC	VCC +5V
A23	A23	2	I	I	23	MCFG1	(memory cfg jumper)
A22	A22	3	I	O	22	_RAMEN	RAM Enable
A21	A21	4	I	I/O	21	REJKICK	(kickstart select jumper)
Address Strobe	_AS	5	I	R - I/O	20	_DAE	DMA Address Enable
A20	A20	6	I	I/O	19	_REGEN	Chip Register Enable
Overlay ROM over RAM	OVL	7	I	I/O	18	_DTACK	Data Transfer Ack
Override System Decoding	_OVR	8	I	I/O	17	x	n.c. (internal use equation?)
A19	A19	9	I	R - I/O	16	_RE	RAM Enable
C1 Clock (3.58MHz falling edge)	_C1	10	I	O	15	REJ2	(most likely _CLKE)
A18	A18	11	I	I	14	_C3	C3 Clock (3.58Mhz rising edge)
GND	GND	12	GND	I	13	A17	A17

PAL analyser shows fixed high output for 18,21 indicating those pins are inputs.
PAL analyser shows registered output for 16,20 indicating those pins are tri-state or feedback enabled.
Even though pin 17 is n.c., the PAL analyser shows an active equation, indicating it might be used internally.

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