Since the same FAT GARY chip as in the A3000 is being used, some external logic was required to provide the required functionality. Since FAT GARY terminates ROM accesses with *STERM, an external PAL is required to convert this to synchronous *DSACKs for use with a 68020.

Writes to the ROM address range will cause a bus timeout to occur.

Real Time Clock

- Ricoh RTC with 26 x 4-bit battery backed RAM
- The A4000 uses the same Ricoh RTC as in the A3000

Floppy Disks

- One internal floppy drive standard (2 speed, high density, 1.7 MB)
- Up to two internal floppy drives (DF0: and DF1:)
- Up to two external floppy drives (DF2: and DF3:)

A single 1.7 MB internal floppy disk comes installed in the machine. The circuitry on the motherboard can support two internal drives. The standard disk is installed in the topmost drive bay, and uses the front bezel as its faceplate (32 mm or 25 mm). A second drive can be added in either of the lower two bays. Drives in these two bays require their own bezels. Also, the lowest bay is limited to a 25 mm drive only.

External drives (DF2: and DF3:) must be installed via the 23-pin external connector. A jumper is provided on the motherboard to redirect DF0: out the external connector. The first external drive would then be DF0:, and the second external drive would be DF3:.

The internal floppy connector is wired such that DF0: is connected before the twist in the floppy cable wire. DF1: would be after the twist.

Hard Disk

- Built in 16-bit IDE interface (internal connections only)
- Two drive support

An internal 40-pin connector is provided for the addition of up to two 16-bit AT IDE compatible hard disk drives.

Hard drives can be installed in two places. A single slim line (low profile) hard disk can be mounted in the lower bay of the bracket in the front of the machine (below the floppy). In addition, a single half height, or two low profile hard disks can be installed alongside the power supply in the back of the machine.

The IDE (AT) hard drive requires two mutually exclusive chip selects. Refer to the following tables for address range in which each is active. The state machine shown in Figure 6-2 is used for IDE accesses. Note that consecutive accesses cannot be performed nearly as fast as a single access. This would suggest that the optimum algorithm for access of IDE data would consist of single accesses of IDE data interleaved with single accesses of the target/source data buffer.

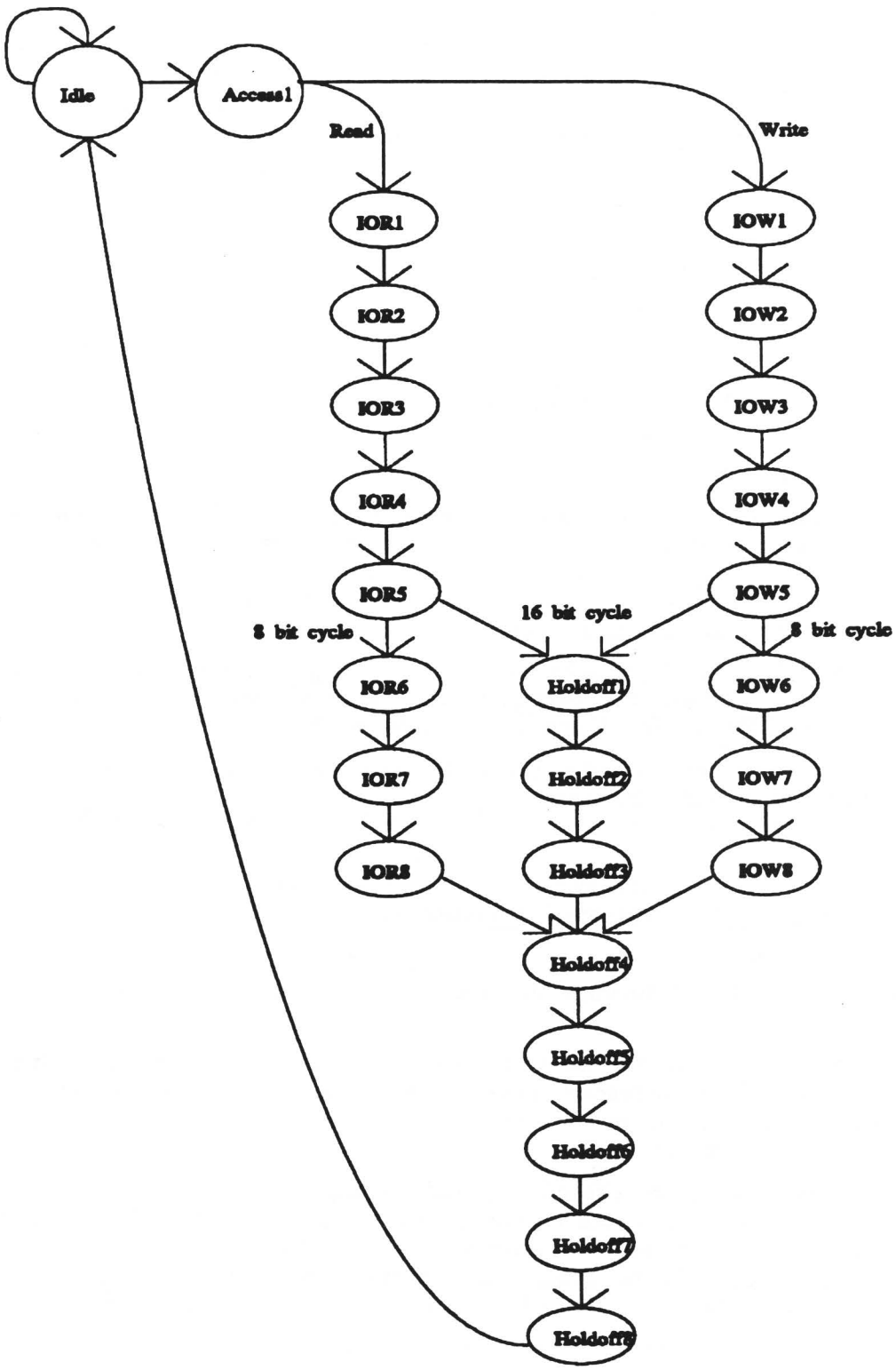

Figure 6-2. State Machine

Data register accesses can be performed faster than control register accesses. Accesses to the control registers are called "8-bit accesses" while those to the data register are called "16-bit accesses". Shown below is a table that gives addresses for all registers related to the IDE sub-system.

A13	A12	A5	A1	Address	Function
0	0	1	X	$0DD0XXX	Reserved for SCSI
0	1	1	0	$0DD1XX0	Reserved for mode register 0
0	1	1	1	$0DD1XX2	Reserved for mode register 1
1	0	1	0	$0DD2XX0	_CS1, 16-bit speed
1	0	1	1	$0DD2XX2	_CS1, 8-bit speed
1	1	1	0	$0DD3XX0	IDE interrupt register
1	1	1	1	$0DD3XX2	_CS2, 8-bit speed

Note that A5 must be high for all accesses. This is because contention with RAMSEY results if this is not done.

The A4000 supports four different timings. They represent reads and writes at 8-bit and 16-bit speeds. These timings are shown on the following pages.

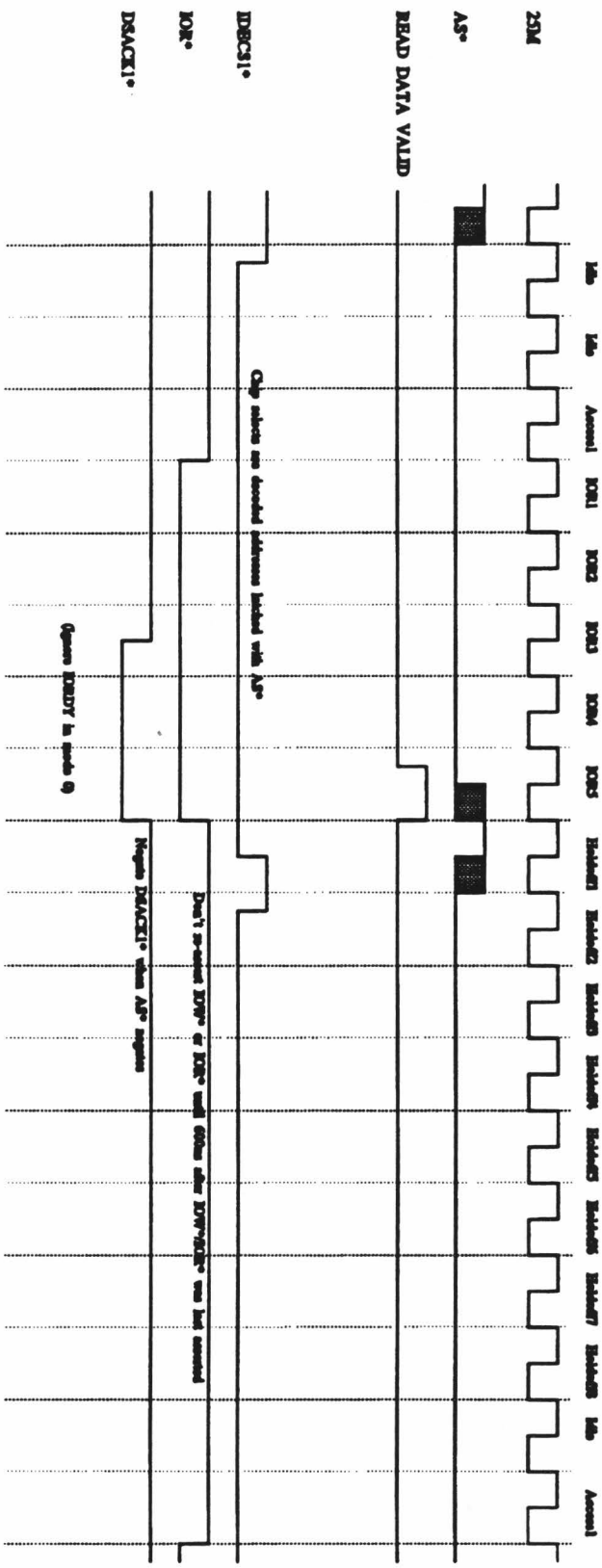

Figure 6-3. Timing Table 1

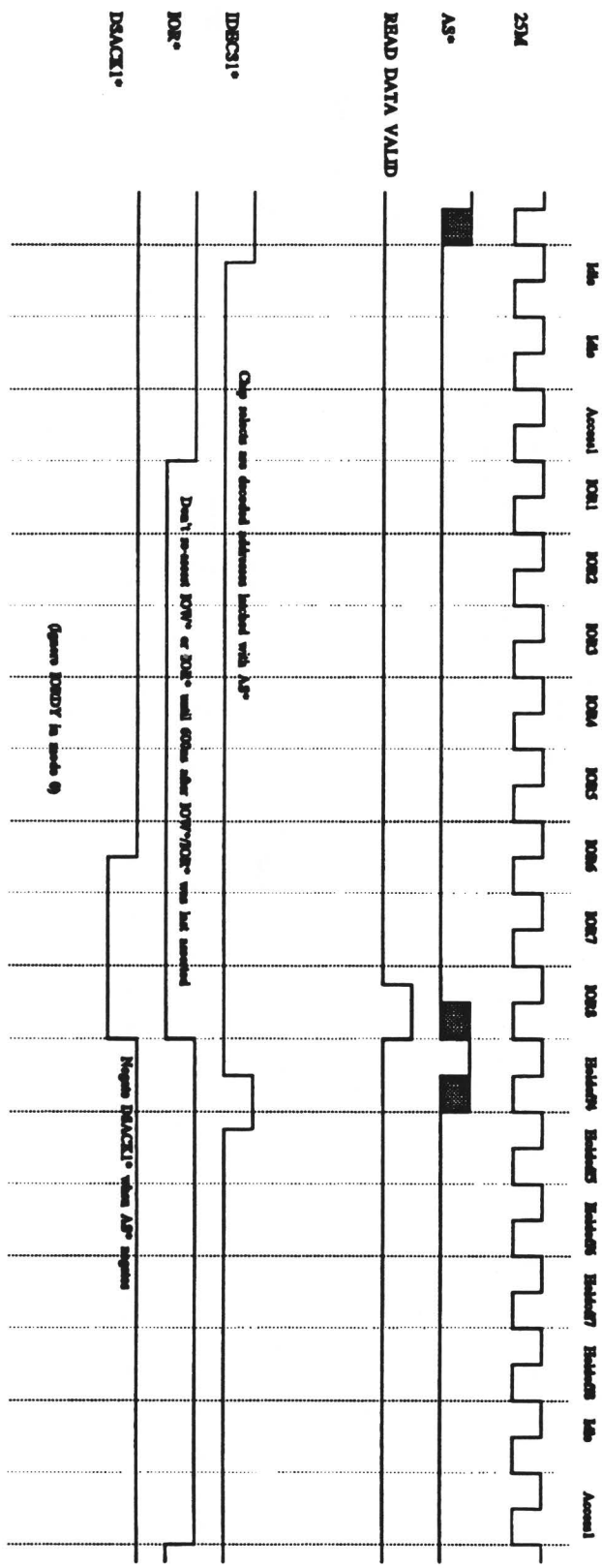

Figure 6-4. Timing Table 2

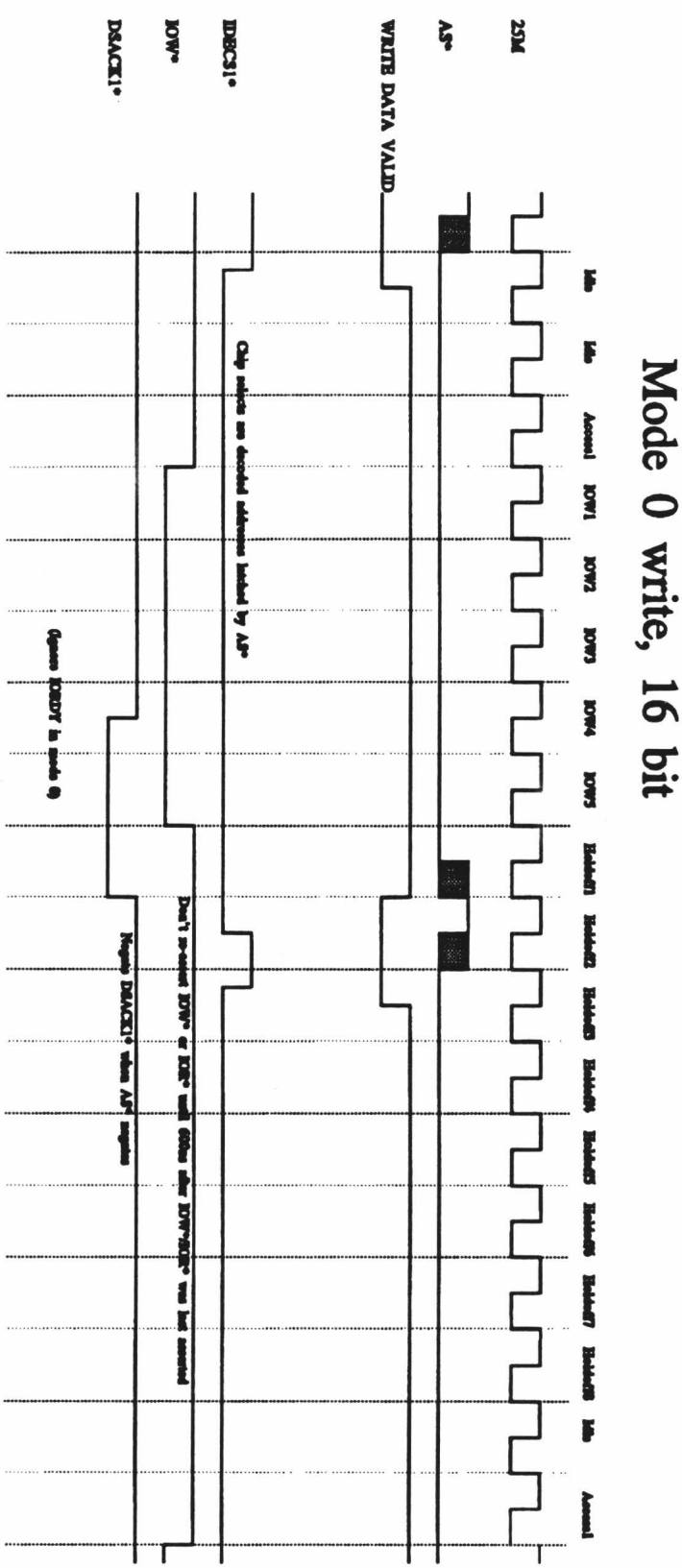

Figure 6-5. Timing Table 3

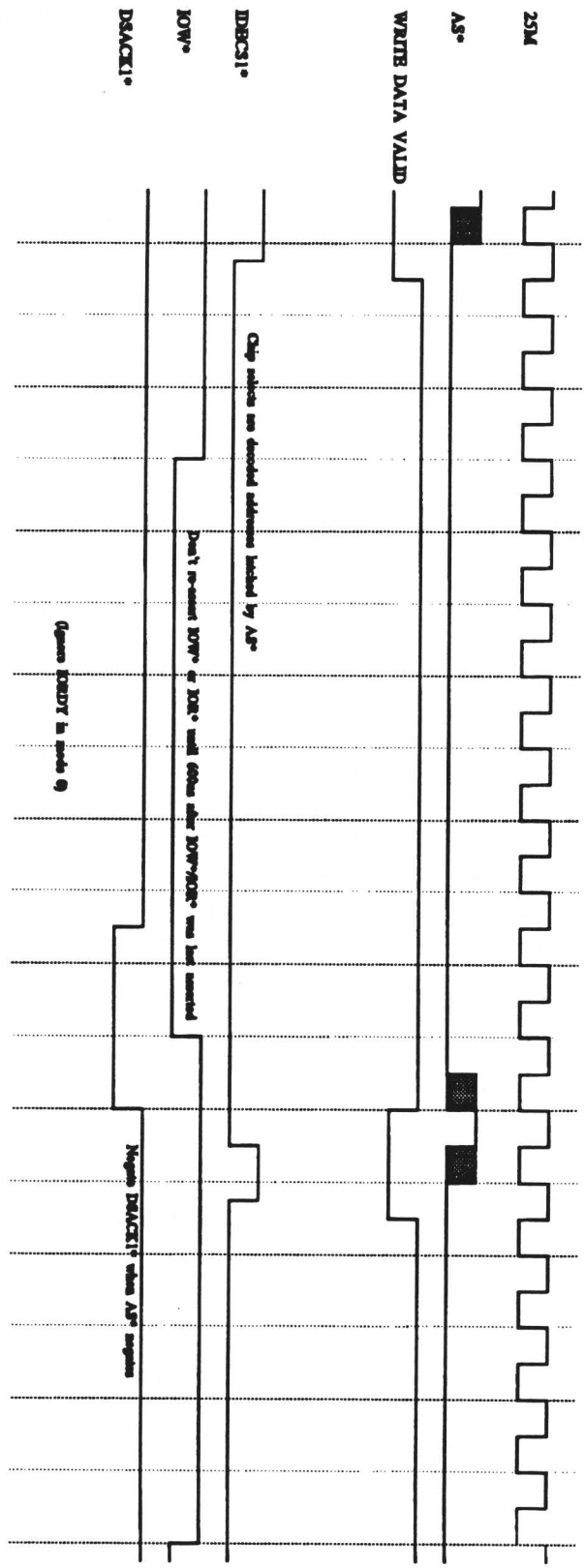

Figure 6-6. Timing Table 4

The disk drive address lines DA0, DA1, and DA2 are connected to processor address lines A2, A3, and A4, respectively. This results in the following memory map.

A1000 Address	Addr on AT Address	Valid Data	Read Function	Write Function
$0DD1020	-	D31	None	Mode Reg0 (reserved)
$0DD1022	-	D31	None	Mode Reg1 (reserved)
$0DD3020	-	D31	IDE int reg	None
$0DD303A	3F6	8 bits	Alternate Status	Device Control
$0DD303E	3F7	8 bits	Drive address	Not used
$0DD2026	1F1	8 bits	Error Register	Features
$0DD202A	1F2	8 bits	Sector Count	Sector Count
$0DD202E	1F3	8 bits	Sector Number	Sector Number
$0DD2032	1F4	8 bits	Cylinder Low	Cylinder Low
$0DD2036	1F5	8 bits	Cylinder High	Cylinder High
$0DD203A	1F6	8 bits	Drive/Head	Drive/Head
$0DD203E	1F7	8 bits	Status	Command
$0DD2020	1F0	16 bits	Data	Data

Locations $0DD1020 and $0DD1022 are reserved for the mode registers. These are currently not implemented. When implemented, they will allow faster transfer rates from hard drives that support such rates. Part of the ID of a drive is information that allows the driver to decide which 'mode' is the fastest the drive supports. Modes are defined as follows.

Mode Reg1	Mode Reg0	Mode Type	Maximum Transfer Rate
0	0	mode 0	3.3 MB/sec
0	1	mode 1	5.2 MB/sec
1	0	mode 2	8.3 MB/sec
1	1	Undefined	Undefined

As currently implemented, only mode 0 is available.

Location $0DD3000 contains the IDE interrupt register. This register returns a value of 1 if an interrupt is pending from the IDE hard disk, and a value of 0 if an interrupt is not pending from this source. Writing to this register has no effect.

Audio

Two external RCA jacks are provided for stereo audio output (pre-amp levels). As in the A3000, right and left channels are shorted together to provide combined monoraul audio if only a single RCA plug is installed. Separate right and left stereo is provided when male RCA plugs are inserted into both of the RCA jacks.

External audio in is provided on pin 18 of the RS-232 DB25 connector. This audio is mixed into the right channel. Audio out is also provided on the DB25 connector on pin 11, which is sent from the left audio channel.

An internal connector on the PCB allows for additional Right and Left audio to be mixed in. This allows internal expansion devices (such as a DSP) to provide stereo audio as well.