AM Control Operation & Timing

DRAM memory operating in a synchronous manner, the timing and operation control signals are crucial.

Memory Tutorial Includes:

SDRAM memory SDRAM architecture SDRAM timing & control DDR / DDR1 SDRAM DDR2 DDR3 SDRAM DDR4 SDRAM JEDEC 79 Standard

Memory types & technologies

ous DRAM offers many advantages in terms of its speed and operation. The timing and operation of the gnals is key to the smooth operation of this form of memory.

or the SDRAM to operate correctly, the control line timing needs to handled correctly for accurate operation.

naturally issues of operation and timing that are different to other forms of memory.

AM control signal operation

chronous operation of DRAM caused many design challenges because it interfaced to a synchronous system. These issues became more apparent as the processor speeds increased.

ous dynamic random access memory, SDRAM runs in a synchronous fashion with the commands are sed to the rising edge of the clock.

various actions that can be taken by the memory. These are determined by the state of the command the rising edge of the clock.

six control signals that are used for SDRAM operation.

Column Address Strobe Along with /RAS and /WE, this control line on the SDRAM selects one of 8 ands.

Clock Enable When this signal is low, and after one clock cycle, the SDRAM is inhibited and no commands erpreted despite the state of other lines.

DRAM is made active on the rising edge of the clock after CKE is made high.

hip Select This line is used when several chips are used together and it enables selection of a particular M. When this line is high, the chip ignores all other inputs except for CKE.

Data Mask The DQM line is used to suppress the I/O data when it is high. For read actions, when the ine is asserted high two cycles before a read cycle, the read data is not output from the chip.

is one DQM line per 8 bits on a x16 memory chip or DIMM

Row Address Strobe The /RAS line is a command bit which enables election of one of eight commands t is asserted along with /CAS and /WE.

Write enable This line is generally used in conjunction with /CAS and /RAS, but it normally distinguishes ke from write-like commands.

many commands that can be sent. Most operations comprise a number of different commands. For a typical sequence may comprise the following commands:

te: This sends a row address to the SDRAM to open a row, i.e. page.

ect commands: These commands within the overall SDRAM operation satisfy the timing requirements for emory.

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Quote:

However bad life may seem, there is always something you can do and succeed at. Where there's life, there's hope.

Stephen Hawking

The way things are: Old age and treachery will always overcome youth and enthusiasm.

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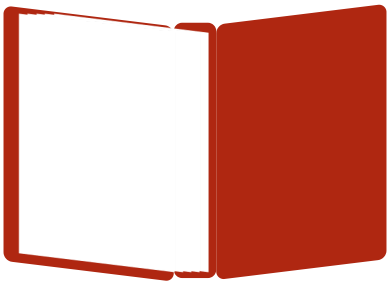

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EVENTS

or Write: This is sent with the column address. With a row open, several read or write commands can be aken. This enables much faster activity as new rows do not need to be opened or deactivated.

arge : A precharge command is required to close a row before a new row can be opened.

AM timing

ıas significant advantages over the more traditional RAM. One of the ways it has been able to achieve this sing the timing of the system to achieve more efficient usage of time. Hence SDRAM timing is of great :e.

a number of SDRAM timings that are of great importance:

atency: The CAS latency is the time between supplying a column address and then receiving back the ponding data. For any system, the CAS latency is programmed into the SDRAM's mode register and :ed by the DRAM controller. It is defined in terms of a specific number of clock cycles.

cycle time: This element of SDRAM timing is the time between successive read operations to an open ypical figures are of the order of 5 ns.

e the main controls and timing elements that are used for SDRAM operation. These controls and the timing enable the SDRAM to interface to the timing of the processor and in this way operate in an effective

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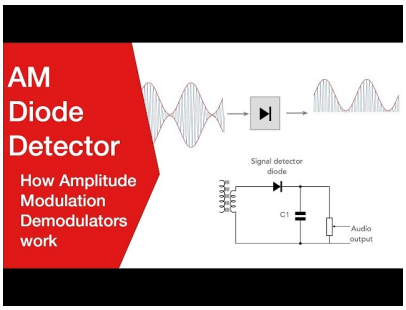

AM Diode Detector / Demodulator

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