APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	AMIGA	A	PRODUCTION RELEASE	4/5/86	YN
	1571, 1581	B	REVISED PER ECO 860687	12-23-86	YN
		C	REVISED PER ECO 870248	8-7-87	R. Burke

1.0 DESCRIPTION/PART #318029-01

The complex Interface Adapter (CIA) is a 65xx Bus compatible peripheral interface device with extremely flexible timing and I/O capabilities. See Figure 2 for block diagram.

1.1 CONFIGURATION

The CIA shall come in a standard 40 pin package. See Figure 1 for pin configuration.

1.2 SOURCES: SEE APPPROVED VENDOR'S LIST FOR APPROVED SOURCES.

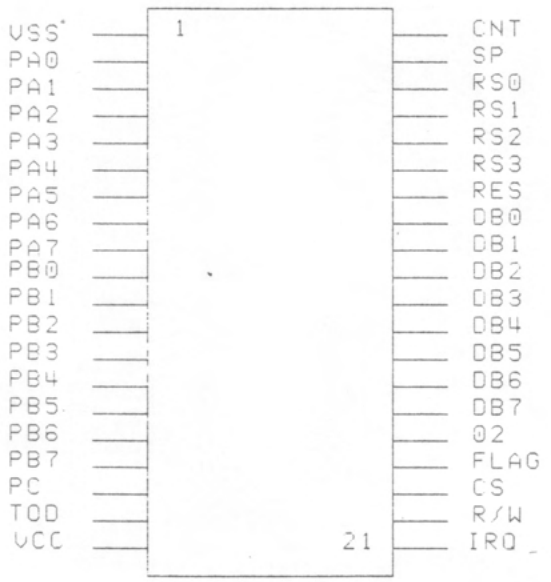


Figure 1. PIN CONFIGURATION

COMMODORE PART #	STATUS				
318029-01	INACTIVE				
318029-02	ACTIVE				
318029-03	ACTIVE				

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES
ANGLES ±1°
2 PLACE DECIMALS ±.02
3 PLACE DECIMALS ±.010

DRWN	M A Fagan	1/13/88
SYSTEMS ENG	A. Berlin	1/13/88
TEST ENG		1/13/88
CIRCUIT ENG	Victor T. Medrado	1/13/88
COMP ENG	R. Burke	

COMMODORE

TITLE IC, LSI, Complex Interface Adapter 8520

SIZE A | DRAWING NO. 318029

SCALE — | SHEET 1 OF 15

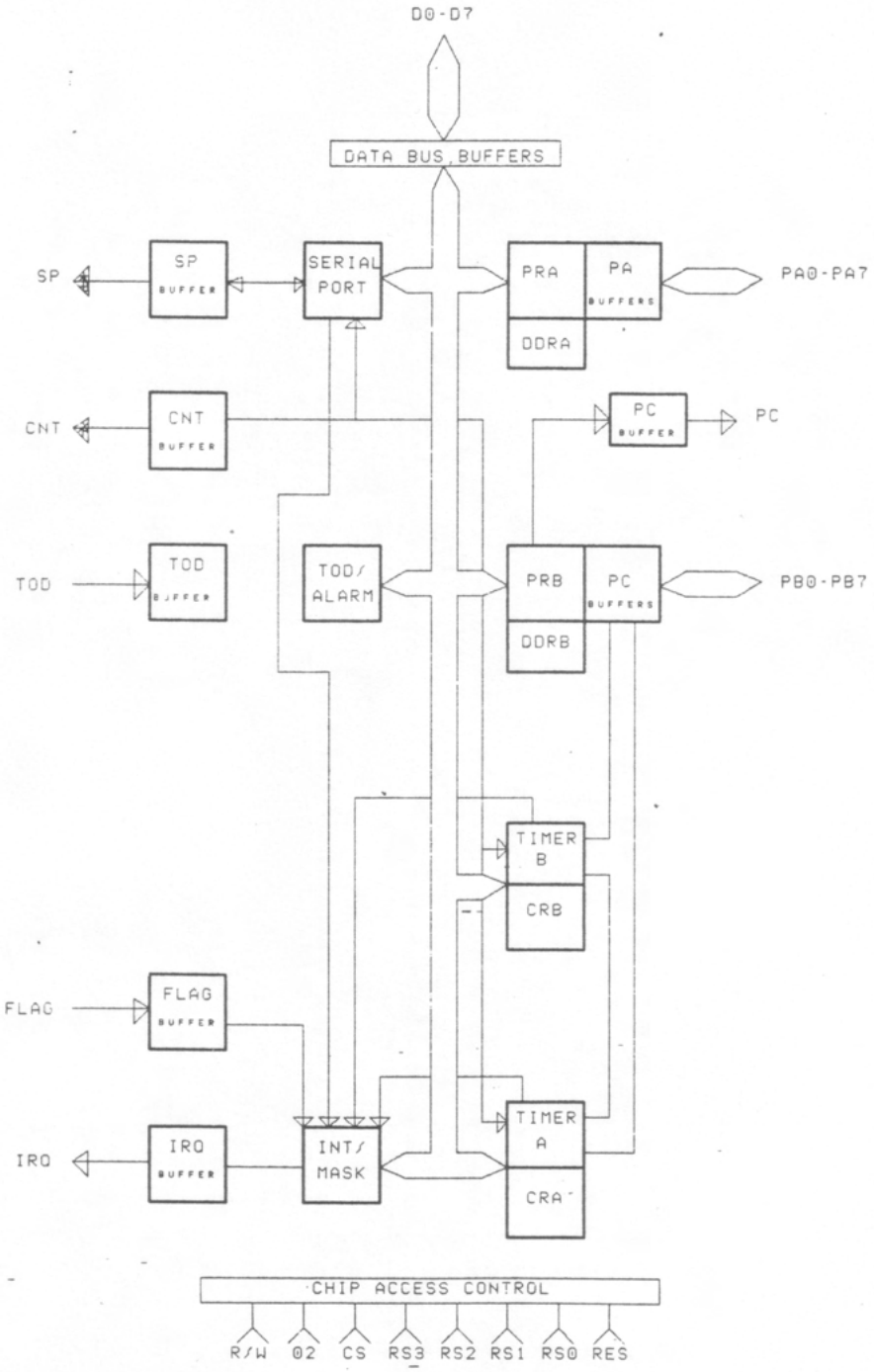
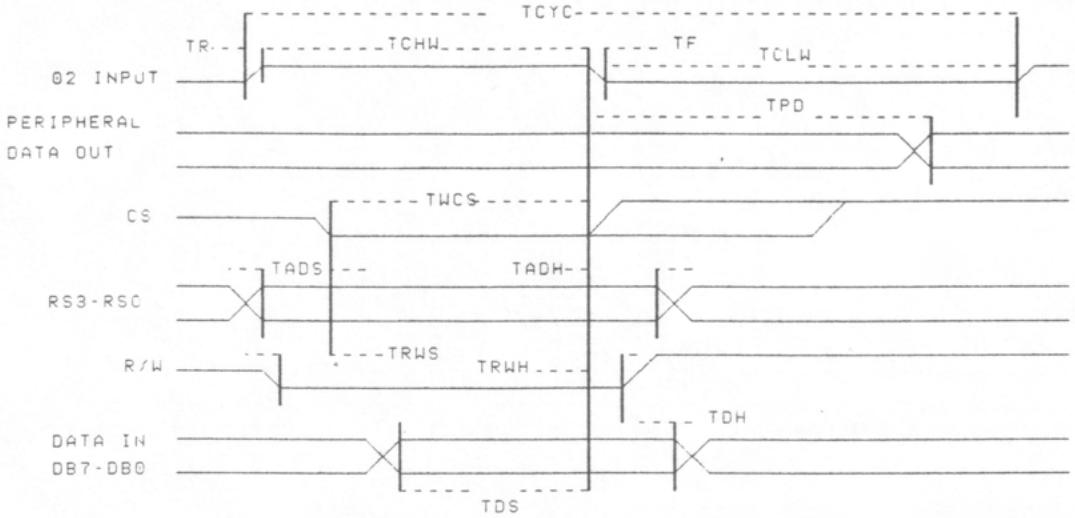


Figure 2. BLOCK DIAGRAM

COMMODORE			TITLE	IC,LSI COMPLEX INTERFACE ADAPTER 8520	
SIZE A	DRAWING NO. 318029	REV C	SCALE ——	SHEET 2	OF 15

WRTIE TIMING DIAGRAM



READ TIMING DIAGRAM

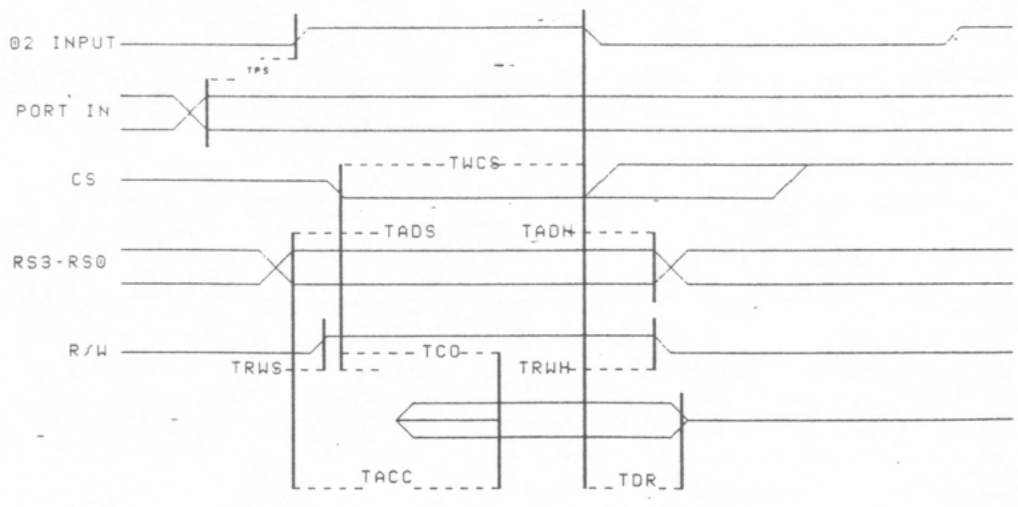


Figure 3. TIMING DIAGRAMS

COMMODORE			TITLE: IC, LSI, COMPLEX INTERFACE ADAPTER 8520
SIZE: A	DRAWING NO.: 318029	REV: C	SCALE: — SHEET: 3 OF: 15

1.3 INTERFACE SIGNALS

1.3.1 Ø2-Clock Input

The Ø2 clock is a TTL compatible input used for internal device operation and as a timing reference for communicating with the system data bus.

1.3.2 CS-Chip Select Input

The CS input controls the activity of the 8520. A low level on CS while Ø2 is high causes the device to respond to signals on the R/W and address (RS) lines. A high on CS prevents these lines from controlling the 8520. The CS line is normally activated (low) at Ø2 by the appropriate address combination.

1.3.3 R/W-Read/Write Input

The R/W signal is normally supplied by the microprocessor and controls the direction of data transfers of the 8520. A high on R/W indicates a read (data transfer out of the 8520), while a low indicates a write (data transfer into the 8520).

1.3.4 RS3-RS0 - Address Inputs

The address inputs select the internal registers as described by the Register Map.

1.3.5 DB7-DB0 - Data Bus Inputs/Outputs

The eight bit data bus transfers information between the 8520 and the system data bus. These pins are high impedance inputs unless CS is low and R/W and Ø2 are high, to read the device. During this read, the data bus output buffers are enabled, driving the data from the selected register onto the system data bus.

1.3.6 IRQ-Interrupt Request Output

IRQ is an open drain output normally connected to the processor interrupt input. An external pullup resistor holds the signal high, allowing multiple IRQ-outputs to be connected together. The IRQ output is normally off (high impedance) and is activated low as indicated in the functional description.

1.3.7 RES-Reset Input

A low on the RES pin resets all internal registers. The port pins are set as inputs and port registers to zero (although a read of the ports will return all highs because of passive pullups). The timer control registers are set to zero and the timer latches to all ones. All other registers are reset to zero.

1.4 REGISTER MAP

RS3	RS2	RS1	RS0	REG		
0	0	0	0	0	PRA	Peripheral Data Reg. A
0	0	0	1	1	PRB	Peripheral Data Reg. B
0	0	1	0	2	DDRA	Data Direction Reg. A
0	0	1	1	3	DDRB	Data Direction Reg. B
0	1	0	0	4	TA LO	Timer A Low Register
0	1	0	1	5	TA HI	Timer A High Register
0	1	1	0	6	TB LO	Timer B Low Register
0	1	1	1	7	TB Hi	Timer B High Register
1	0	0	0	8		Event LSB
1	0	0	1	9		Event 8-15
1	0	1	0	A		Event MSB
1	0	1	1	B		No Connect
1	1	0	0	C	SDR	Serial Data Register
1	1	0	1	D	ICR	Interrupt Control Register
1	1	1	0	E	CRA	Control Register A
1	1	1	1	F	CRB	Control Register B

1.5 FUNCTIONAL DESCRIPTION

1.5.1 I/O Ports (PRA, PRB, DDRA, DDRB)

Ports A and B each consist of an 8-bit Peripheral Data Register (PR) and an 8-bit Data Direction Register (DDR). If a bit in the DDR is set to the corresponding bit in the PR is an output if a DDR bit is set to zero, the corresponding PR bit is defined as an input. On a READ, the PR reflects the information present on the actual port pins (PA0-PA7, PB0-PB7) for both input and output bits. Port A has both passive and active pullup devices, providing both CMOS and TTL compatibility. It can drive 2 TTL loads. Port B has only passive pullup devices and has a much higher current-sinking capability.

1.5.2 HANDSHAKING

Handshaking on data transfers can be accomplished using the PC output pin and the FLAG input pin. PC will go low on the 3rd cycle after a PORT B access. This signal can be used indicate "data ready" at PORT B or "data accepted" from PORT B. Handshaking on a 16-bit data transfers (using both PORT A and PORT B) is possible by always reading or writing PORT A first. FLAG is a negative edge sensitive input which can be used for recieving the PC output from another 8520 or as a general purpose interrupt input. Any negative transistion on FLAG will set the FLAG interrupt bit.

Reg	Name	D7	D6	D5	D4	D3	D2	D1	D0
0	PRA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
1	PPB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
2	DDRA	DPA7	DPA6	DPA5	DPA4	DPA3	DPA2	DPA1	DPA0
3	DDRB	DPB7	DPB6	DPB5	DPB4	DPB3	DPB2	DPB1	DPB0

1.5.3 Interval Timers (Timer A, Timer B)

Each interval timer consists of a 16-bit read-only Timer Counter and a 16-bit write-only Timer Latch. Data written to the timer are latched in the Timer Latch, while data read from the timer are the present contents of the Timer Counter. The timers can be used independently or linked for extended operations. The various timer modes allow generation of long time delays, variable width pulses, pulse trains and variable frequency waveforms. Utilizing the CNT input, the timers can count external pulses or measure frequency, pulse width and delay times of external signals. Each timer has an associated control register, providing independent control of the following functions:

1.5.4 Start/Stop

A control bit allows the timer to be started or stopped by the microprocessor at any time.

1.5.5 PB On/Off

A control bit allows the timer output to appear on a PORT B output line (PB6 for TIMER A and PB7 for TIMER B). This function overrides the DDRB control bit and forces the appropriate PB line to an output.

1.5.6 Toggle/Pulse

A control bit selects the output applied to PORT B. On every timer underflow the output can either toggle or generate a single positive pulse of one cycle duration. The toggle output is set high whenever the timer is started and is set low by RES.

1.5.7 One-Shot/Continuous

A control bit selects either timer mode. In one-shot mode, the timer will count down from the latched value to zero, generate an interrupt, reload the latched value, then stop. In continuous mode, the timer will count from the latched value to zero, generate an interrupt, reload the latched value and repeat the procedure continuously. In one-shot mode; a write to Timer High (registers 5 for TIMER A, 7 for TIMER B) will transfer the timer latch to the counter and initiate counting regardless of the start bit.

1.5.8 Force Load

A strobe bit allows the timer latch to be loaded into the timer counter at any time, whether the timer is running or not.

1.5.9 Input Mode

Control bits allow selection of the clock used to decrement the timer. TIMER A can count 02 pulses or external pulses applied to the CNT pin. TIMER B can count 02 pulses, external CNT pulses, TIMER A underflow pulses or TIMER A underflow pulses while the CNT pin is held high.

The timer latch is loaded into the timer on any timer underflow, on a force load or following a write to the high byte of the prescaler while the timer is stopped. If the timer is running, a write to the high byte will load the timer latch, but not reload the counter.

READ (TIMER)

REG	Name								
4	TA LO	TAL7	TAL6	TAL5	TAL4	TAL3	TAL2	TAL1	TAL0
5	TA HI	TAH7	TAH6	TAH5	TAH4	TAH3	TAH2	TAH1	TAH0
6	TB LO	TBL7	TBL6	TBL5	TBL4	TBL3	TBL2	TBL1	TBL0
7	TB HI	TBH7	TBH6	TBH5	TBH4	TBH3	TBH2	TBH1	TBH0

WRITE (PRESCALER)

REG	Name								
4	TA LO	PAL7	PAL6	PAL5	PAL4	PAL3	PAL2	PAL1	PAL0
5	TA HI	PAH7	PAH6	PAH5	PAH4	PAH3	PAH2	PAH1	PAH0
6	TB LO	PBL7	PBL6	PBL5	PBL4	PBL3	PBL2	PBL1	PBL0
7	TB HI	PBH7	PBH6	PBH5	PBH4	PBH3	PBH2	PBH1	PBH0

1.5.10 TOD

TOD consists of a 24 bit binary counter. Posistive edge transitions on this pin cause the binary counter to increment. The TOD pin has a passive pull-up on it. A programmable ALARM is provided for generating an interrupt at a desired time. The ALARM registers are located at the same addresses as the corresponding TOD register. Access to the ALARM is governed by a Control Register bit. The ALARM is write-only; any read of a TOD address will read time regardless of the state of the ALARM access bit.

A specific sequence of events must be followed for proper setting and reading of TOD. TOD is automatically stopped whenever a write to the register occurs. The clock will not start again until after a write to the LSB Event Register. This assures TOD will always start at the desired time. Since a carry from one stage to the next can occur at any time with respect to a read operation, a latching function is included to keep all Time of Day information constant during a read sequence. All TOD registers latch on a read of MSB event and remain latched until after a read of LSB Event. The TOD clock continues to count when the output registers are latched. if only one register is to be read, there is no carry problem and the register can be read "on the fly", provided that any read of MSB Event is followed by a read of LSB Event to disable the latching.

READ

REG	NAME								
8	LSB EVENT	E7	E6	E5	E4	E3	E2	E1	E0
9	EVENT 8-15	E15	E14	E13	E12	E11	E10	E9	E8
A	MSB EVENT	E23	E22	E21	E20	E19	E18	E17	E16

WRITE
CRB7=0
CRB7=1 ALARM
(SAME FORMAT AS READ)

1.5.11 Serial Port (SDR)

The serial port is a buffered, 8-bit synchronous shift register system. A control bit selects input or output mode. In input, mode, data on the SP pin is shifted into the shift register on the rising edge of the signal applied to the CNT pin. After 8 CNT pulses, the data in the shift register is dumped into the Serial Data Register and an interrupt is generated. In the output mode, TIMER A is used for the baud rate generator. Data is shifted out on the SP pin at 1/2 the underflow rate of TIMER A. The maximum baud rate possible is 02 divided by 6, but the maximum useable baud rate will be determined by line loading and the speed at which the reciever responds to input data. Transmission will start following a write to the Serial Data Register (provided TIMER A is running and in continuous mode). The clock signal derived from TIMER A appears as an output on the CNT pin. The data in the Serial Data Register will be loaded into the shift register then shift out to the SP pin when a CNT pulse occurs. Data shifted out becomes valid on the falling edge of CNT and remains valid until the next falling edge. After 8 CNT pulses, an interrupt is generated to indicate more data can be sent. If the Serial Data Register was loaded with new information prior to this interrupt, the new data will automatically be loaded into the shift register and transmission will be continuous. If no further data is to be transmitted, after the 8th CNT pulse, CNT will return high and SP will remain at the level of the last data bit transmitted. SDR data is shifted out MSB first and serial input data should also appear in this format.

The bidirectional capabiltiy of the Serial Port and CNT clock allows several devices to be connected to a common serial communication bus on which one acts as a master, sourcing data and shift clock, while all other chips act as slaves. Both CNT and SP outputs are open drain, with passive pullups, to allow such a common bus. Protocol for slave/master selection can be transmitted over the serial bus, or via dedicated handshaking lines.

REG	NAME								
C	SDR	S7	S6	S5	S4	S3	S2	S1	S0

1.5.12 Interrupt Control (ICR)

There are five sources of interrupts on the 8520: underflow from TIMER A, underflow from TIMER B, TOD ALARM, Serial Port full/empty and FLAG. A single register provides masking and interrupt information. The Interrupt Control Register consists of a write-only MASK register and a read-only DATA register. Any interrupt which is enabled by the MASK register will set the IR bit (MSB) of the DATA register and bring the IRQ pin low. In a multi-chip system, the IR bit can be polled to detect which chip has generated an interrupt request.

The interrupt DATA register is cleared and the IRQ line returns high following a read of the DATA register. Since each interrupt sets an interrupt bit regardless of the MASK, and each interrupt bit can be selectively masked to prevent the generation of a processor interupt, it is possible to intermix polled interrupts with true interrupts. However, polling the IR bit will cause the DATA register to clear, therefore, it is up to the user to preserve the information contained in the DATA register if any polled interrupts were present.

The MASK register provides convenient control of individual mask bits. When writing to the MASK register, if bit 7 (SET/CLEAR) of the data written is a ZERO, any mask bit written with a one will be cleared, while those mask bits written with a zero will be unaffected. If bit 7 of the data written is a ONE, any mask bit written with a one will be set, while those mask bits written with a zero will be unaffected. In order for an interrupt flag to set IR and generate an Interrupt Request, corresponding MASK bit must be set.

READ (INT DATA)

REG	NAME								
D	IRC	IR	0	0	FLG	SP	ALRM	TB	TA

WRITE (INT MASK)

REG	NAME								
D	IRC	S/C	X	X	FLG	SP	ALRM	TB	TA

1.5.13 Control Registers

There are two control registers in the 8520: CRA and CRB, CRA is associated with TIMER A and CRB is associated with TIMER B.

The register format is as follows:

CRA:

BIT	NAME	FUNCTION
0	START	1=START TIMER A, 0=STOP TIMER A. This bit is automatically reset when underflow occurs during one-shot mode.
1	PBON	1=TIMER A output appears on PB6, 0=PB6 normal operation
2	OUTMODE	1=TOGGLE, 0=PULSE
3	RUNMODE	1=ONE-SHOT, 0=CONTINUOUS
4	LOAD	1=FORCE LOAD (this is a STROBE input, there is no data storage, bit 4 will always read back a zero and writing a zero has no effect.
5	INMODE	1=TIMER A counts positive CNT transitions, 0=TIMER A counts 02 pulses.
6	SPMODE	1=SERIAL PORT output (CNT sources shift clock). 0=SERIAL PORT input (external shift clock required).
7	TODIN	1=50 Hz clock required on TOD pin for accurate time. 0=60 Hz clock required on TOD pin for accurate time.

CRB:

BIT	NAME	FUNCTION
		(Bits CRB0-CRB4 are identical to CRA0-CRA4 for TIMER B with the exception that bit 1 controls the output of TIMER B on PB7).
5,6	INMODE	Bits CRB5 and CRB6 select one of four input modes for TIMER B as:

CRB6	CRB5	
0	0	TIMER B counts 02 pulses.
0	1	TIMER B counts positive CNT transitions
1	0	TIMER B counts TIMER A underflow pulses
1	1	TIMER B counts TIMER A underflow pulses while CNT is high.

7	ALARM	1=writing to TOD registers set ALARM, 0=writing to TOD registers sets TOD clock.

2.0 ELECTRICAL PARAMETERS

2.1 Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the circuit. Functional operation of the device at these or any conditions other than those indicated in the operating conditions of the specification is not implied. Exposure to the maximum ratings for extended periods may adversely affect device reliability.

Supply Voltage	Vcc	-0.3V to 7.0V
Input/Output Voltage	Vin	-0.3V to 7.0V
Operating Temp.	Top	0 C to 70·C
Storage Temp.	Tstg	-55 C to 150·C

* All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

ELECTRICAL CHARACTERISTICS (VCC +/- 5%, VSS = 0v, TA = 0.70 C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	Vih	+2.4	-	Vcc	V
Input Low Voltage	Vil	-3.0	-	+0.8	V
Input leakage current VIN=VSS + 5V (TOD,R/W, 02,RES,RS0-RS3,CS)	Iin	-	1.0	2.5	µA
PA0-7, PB0-7, TOD, FLAG, SP, CNT	Rpi	3.1	5.0	-	KΩ
Output leakage current for High Impedance State VIN=4V to 2.4V (DB0-DB7, IRQ)	Itsi	-	±1.0	±10.0	µA
Output High Voltage VCC=MIN, LOAD <-200µA (PA0-PA7,DB0-DB7)	Voh	+2.4	-	Vcc	V
Output Low Voltage (PA0-PA7,DB0-DB7)	Vol	-	-	+0.40	V

VCC=MIN, LOAD <3.2mA

Output High Current(sourcing) Ioh VOH > 2.4V(PA0-PA7, DB0-DB7)		-200	-1000	-	μA
Output Low Current (sinking) Iol VOL< .4V (PA0-PA7, DB0-DB7)		3.2	-	-	mA
Output Low Current (sinking) Iol VOL< .4V (PC, PB0-PB7)		13.0	-	-	mA
Input Capacitance	Cin	-	7	10	pf
Output Capacitance	Cout	-	7	10	pf
Power Supply Current	Icc	-	70	100	mA

2.2 Timing Characteristics

		318029-02		318029-03	
		1MHZ		2MHZ	
SYMBOL	CHARACTERISTIC	MIN	MAX	MIN	MAX
	Ø2 CLOCK				
TCYC	Cycle Time	1000	10,000	500	10,000
TR, TF	Rise and Fall Time	--	25	- -	25
TCHW	Clock Pulse Width (High)	440	5,000	240	5,000
TCLW	Clock Pulse Width (Low)	440	5,000	240	5,000
	WRITE CYCLE				
TPD	Output Delay From Ø2	--	960	- -	460
TWCS	CS low while Ø2 high	280	--	255	- -
TADS	Address setup time	58	--	20	- -
TADH	Address hold time	10	--	10	- -
TRWS	R/W setup time	58	--	20	- -
TRWH	R/W hold time	10	--	15	- -
TDS	Data bus setup time	200	--	75	- -
TDH	Data bus hold time	15	--	15	- -
	READ CYCLE				
TPS	Port setup time	300	--	155	- -
TWCS(2)	CS low while Ø2 high	280	--	255	- -
TADS	Address setup time	58	--	20	- -
TADH	Address hold time	10	--	10	- -
TRWS	R/W setup time	58	--	20	- -
TRWH	R/W hold time	10	--	15	- -
TACC	Data access frrom RS3-RS0	--	300	200	- -
TCO(3)	Data access from CS	--	240	180	- -
TDR	Data release time	50	--	25	- -

* See figure 3 for timing relationships.

*NOTES:
1- All timings are referenced from VIL max and VIH min on inputs and VOL max and VOH min on outputs.
2- TWCS is measured from the later of Ø2 high or CS low. Cs must be low at least until the end of Ø2 high.
3- TCO is measured from the later of Ø2 high or CS low. Valid data is available only after the later of TACC of TCO.

3.0 MECHANICAL REQUIREMENTS

3.1 Marking

Parts shall be marked with Commodore part number, manufacturers identification and EIA data code. Pin 1 shall be identified.

3.2 Packaging

Parts shall be packaged in a standard 40 pin dual-in-line ceramic or plastic package.

APPROVED VENDORS LIST

THIS PAGE MUST BE DETACHED FROM THE REMAINDER OF THE DRAWING WHENEVER THIS DRAWING IS SHOWN OR TRANSMITTED TO VENDORS.

VENDORS	VENDOR PART NO.	COMMODORE PART NO.
MOS TECHNOLOGY	8520R3	318029-01
MOS TECHOLOGY	8520R4	318029-02
MOS TECHOLOGY	8520A-1	318029-03

commodore

TITLE IC, LSI COMPLEX INTERFACE ADAPTER 8520

SIZE	DRAWING NO.	REV
A	318029	C

SCALE —— SHEET 15 OF 15