CS2292 Project Phase 3

April 10, 2021

- Extend the simulator that you developed in Phase 2 to incorporate Caches.
- A memory access will now first search for the address in the cache(s). On a miss, the data will be fetched from the main memory.
- This effectively means that the memory instructions (load and stores) will not be completed in one cycle.
- Loads and Stores will have variable latency, and hence the penalty (stalls) due to the memory access is variable.
- The simulator should be able to simulate 2 levels of cache, with LRU replacement policy.
- The input along with the assembly code will include cache size, block size, associativity, and access latency of the caches. These parameters can be provided in a separate file as input.
- The input will also include main memory access time.
- At the end of the execution, the simulator should output the number of stalls, cache miss rate(s), and the IPC (Instructions per Cycle).
- If you are unable to complete the project, do prepare a document detailing what you tried, and what did not work etc. The document along with the incomplete code will be evaluated.
- Any kind of malpractice will fetch you a straight *F*. Malpractice also includes sharing your code with someone else, so don't try to be a hero/heroine or saviour!
- Individual members of a team will be evaluated based on their contribution.
- This is "your" project.
- Deadline: 30 April, 11:59PM
- Have fun!