* Generated for: PrimeSim

* Design library name: AMIT

* Design cell name: FOUR_QUADRANT_ANALOG_MULTIPLIER_tb

* Design view name: schematic

.lib 'saed32nm.lib' TT

*Custom Compiler Version S-2021.09

*Sun Feb 20 07:19:57 2022

.global gnd!

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* Library   : AMIT

* Cell   : FOUR_QUADRANT_ANALOG_MULTIPLIER

* View   : schematic

* View Search List : hspice hspiceD schematic spice veriloga

* View Stop List   : hspice hspiceD

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.subckt four_quadrant_analog_multiplier gnd_1 v1 v2 v3 v4 vdd voneg vopos

xm8 net35 v2 net18 vdd p105 w=0.1u l=0.03u nf=1 m=1

xm7 net32 v1 net18 vdd p105 w=0.1u l=0.03u nf=1 m=1

xm6 net32 v2 net5 vdd p105 w=0.1u l=0.03u nf=1 m=1

xm12 net35 v1 net5 vdd p105 w=0.1u l=0.03u nf=1 m=1

xm4 net46 v1 net18 vdd p105 w=0.1u l=0.03u nf=1 m=1

xm2 net18 net46 vdd vdd p105 w=0.1u l=0.03u nf=1 m=1

xm1 net37 v1 net5 vdd p105 w=0.1u l=0.03u nf=1 m=1

xm0 net5 net37 vdd vdd p105 w=0.1u l=0.03u nf=1 m=1

xm11 net46 v4 gnd_1 gnd_1 n105 w=0.1u l=0.03u nf=1 m=1

xm9 net37 v3 gnd_1 gnd_1 n105 w=0.1u l=0.03u nf=1 m=1

r15 net32 net60 r=10k

r14 net35 net61 r=10k

e16 vopos voneg vcvs net60 net61 1 abs=0

.ends four_quadrant_analog_multiplier

* Library   : AMIT

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* View   : schematic

* View Search List : hspice hspiceD schematic spice veriloga

* View Stop List   : hspice hspiceD

xi0 gnd! net9 net18 net13 net21 net16 outn outp four_quadrant_analog_multiplier

v9 gnd! net21 dc=0 sin (0 100m 1meg 0 0 0)

v7 gnd! net18 dc=0 sin (0 100m 50meg 0 0 0)

v3 net13 gnd! dc=0 sin (0 100m 1meg 0 0 0)

v1 net9 gnd! dc=0 sin (0 100m 50meg 0 0 0)

v4 net16 gnd! dc=1.8

.tran '0.1u' '3u' name=tran

.option primesim_remove_probe_prefix = 0

.probe v(*) i(*) level=1

.probe tran v(net13) v(net9) v(outp)

```
.temp 25

.option primesim_output=wdf

.option parhier = LOCAL

.end
```