Four-Quadrant Analog Multiplier based on square rooting circuit

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***Abstract*—** An analog multiplier is an important component for many signal processing algorithms, artificial neural network mapped into hardware. It has been proven that analog multipliers are used for application like neural network where we don't require a very high level of accuracy. Analog multipliers provide high synapse density and high computational speed than a digital multiplier. A CMOS four quadrant analog multiplier design is shown in this report. The designed circuit will be simulated using 28nm CMOS process. It is applicable for a wide range of applications like variable-gain amplifiers, peak detectors, modulators, phase detectors, artificial neural networks etc.

***Keywords*—**Analog multiplier, Synopsis tool

1. Reference Circuit details:

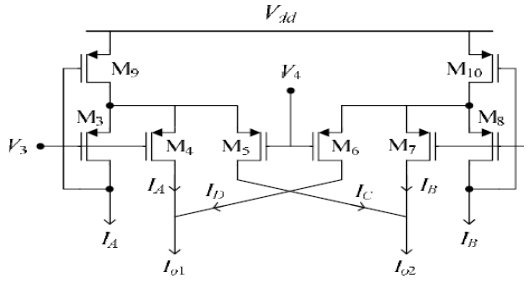

Figure 1: Square rooting circuit

Figure 1 shows a square rooting circuit, setting M3-M8 to be identical, the currents I_C and I_D are found to be

$$I_C = \beta_P (V_{34} + \sqrt{I_A/\beta_P})^2$$

$$I_D = \beta_P (V_{34} + \sqrt{I_B/\beta_P})^2$$

Where $\beta_P = 0.5 * \mu_n CoxW/L$

It can be easily shown that

$$I_{OUT} = I_{O1} - I_{O2} = 2V_{34}\sqrt{\beta_P}(\sqrt{I_A} - \sqrt{I_B})$$

Figure 2 shows the analog multiplier circuit and the output voltage is given by

$$Vout = V_{O1} - V_{O2} = R(I_{O1} - I_{O2})$$

Substituting the values of I_{O1} and I_{O2} it can be derived that

$$Vout = 2R\sqrt{\beta_P \beta_N} V_{12} V_{34}$$

Thus, the analog multiplier is designed where the gain can be changed by changing resistance values and the dimensions of MOSFET

2. Reference Circuit design

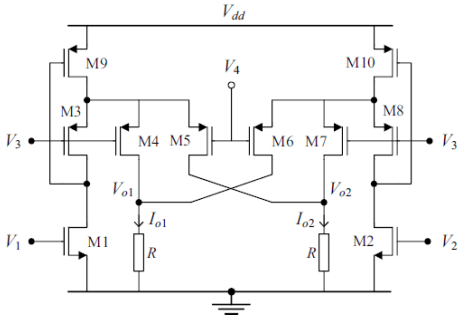

Figure 2: Four quadrant analog multiplier circuit.

3. Reference Waveform and Area estimate

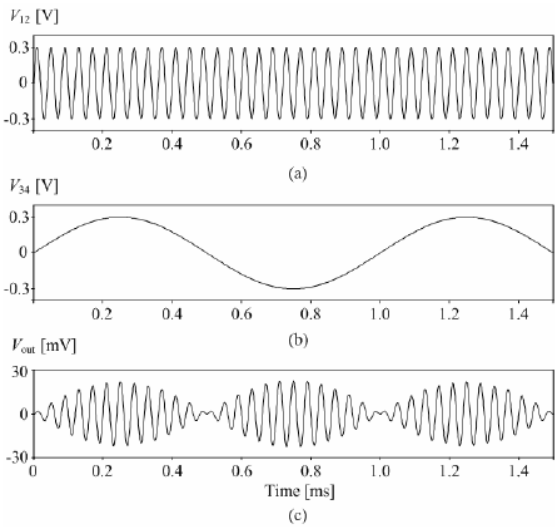

Figure: Transient analysis of Analog Multiplier

Parameter	**Referenced Analog multiplier [1]**
CMOS Technology	**0.35 micron**
Power consumption	**165µW**
Area	**103µ m²**

References:

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[4] S. Satyanarayana, Y. Tsividis and H. P. Graf, "A reconfigurable analog VLSI neural network chip" in Advances in Neural Information Processing Systems 2, CA, San Mateo:Morgan Kaufmann, vol. 2, pp. 758-768, 1990.