بسم الله الرحمن الرحيم

وزارة التعليم العالي والبحث العلمي

جامعة إقليم سبأ

كلية تكنلوجيا المعلومات وعلوم الحاسوب

قسم تكنلوجيا المعلومات والاتصالات

مستوى ثاني

- Four and five chapters solving

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Chapter 4

1. A half-adder adds two binary bits => true

2. A half-adder has a carry output only => false

3. A full adder adds two bits and produces two outputs => false

4. A full-adder can be realized only by using 2-input XOR gates. false

5. When the input bits are both 1 and the input carry bit is 1, the sum output of a full adder is 1. true

6. The output of a comparator is 0 when the two binary inputs given are equal. false

7. A decoder detects the presence of a specified combination of input bits. true

8. The 4-line-to-10-line decoder and the 1-of-10 decoder are two different types. false

9. An encoder essentially performs a reverse decoder function. true

10. A multiplexer is a logic circuit that allows digital information from a single source to be routed onto several lines. false

1. A half-adder is characterized by
   (a) two inputs and two outputs (b) three inputs and two outputs
   (c) two inputs and three outputs (d) two inputs and one output

2. A full-adder is characterized by
   (a) two inputs and two outputs (b) three inputs and two outputs
   (c) two inputs and three outputs (d) two inputs and one output

3. The inputs to a full adder are A = 1, B = 0, Cin = 1. The outputs are

(a) © = 0, Cout = 1 (b) © = 1, Cout = 0

(c) © = 0, Cout = 0 (d) © = 1, Cout = 1

4. A 3-bit parallel adder can add

(a) three 2-bit binary numbers (b) two 3-bit binary numbers

(c) three bits at a time (d) three bits in sequence

5. To expand a 2-bit parallel adder to a 4-bit parallel adder, you must

(a) use two 2-bit adders with no interconnections

(b) use two 2-bit adders and connect the sum outputs of one to the bit inputs of the other

(c) use four 2-bit adders with no interconnections

(d) use two 2-bit adders with the carry output of one connected to the carry input of the other

6. If a 74HC85 magnitude comparator has A = 1000 and B = 1010, the outputs are

(a) A 7 B = 0, A 6 B = 0, A = B = 0 (b) A 7 B = 0, A 6 B = 0, A = B = 1

(c) A 7 B = 0, A 6 B = 1, A = B = 0 (d) A 7 B = 0, A 6 B = 1, A = B = 1

7. If a 1-of-16 decoder with active-LOW outputs exhibits a LOW on the decimal 12 output, what are the inputs?

(a) A3A2A1A0 = 1010 (b) A3A2A1A0 = 1110

(c) A3A2A1A0 = 1100 (d) A3A2A1A0 = 0100

8. A BCD-to-7 segment decoder has 0100 on its inputs. The active outputs are

(a) a, c, f, g (b) b, c, f, g

(c) b, c, e, f (d) b, d, e, g

9. If an octal-to-binary priority encoder has its 0, 2, 5, and 6 inputs at the active level, the activeHIGH binary output is

(a) 110 (b) 010

(c) 101 (d) 000

10. In general, a multiplexer has

(a) one data input, several data outputs, and selection inputs

(b) one data input, one data output, and one selection input

(c) several data inputs, several data outputs, and selection inputs

(d) several data inputs, one data output, and selection inputs

11. Data distributors are basically the same as

(a) decoders (b) demultiplexers

(c) multiplexers (d) encoders

12. Which of the following codes exhibit even parity?

(a) 10011000 (b) 01111000 (c) 11111111

(d) 11010101 (e) all (f) both answers (b) and (c)

Section 6–1 Half and Full Adders

1. For the full-adder of Figure 6–4, determine the outputs for each of the following inputs

(a) $A = 0, B = 1, C_{in} = 0$ **(b)** $A = 1, B = 0, C_{in} = 1$
(c) $A = 0, B = 0, C_{in} = 0$

2. What are the half-adder inputs that will produce the following outputs:

(a) $\Sigma = 0, C_{out} = 0$ **(b)** $\Sigma = 1, C_{out} = 0$
(c) $\Sigma = 0, C_{out} = 1$

3. Determine the outputs of a full-adder for each of the following inputs:

(a) $A = 1, B = 0, C_{in} = 0$ **(b)** $A = 0, B = 0, C_{in} = 1$
(c) $A = 0, B = 1, C_{in} = 1$ **(d)** $A = 1, B = 1, C_{in} = 1$

Section 6–1 Half and Full Adders

1. (a) $\Sigma = 1, C_{out} = 0$
(b) $\Sigma = 0, C_{out} = 0$
(c) $\Sigma = 1, C_{out} = 0$
(d) $\Sigma = 0, C_{out} = 1$

2. $\Sigma = 1, C_{out} = 1$

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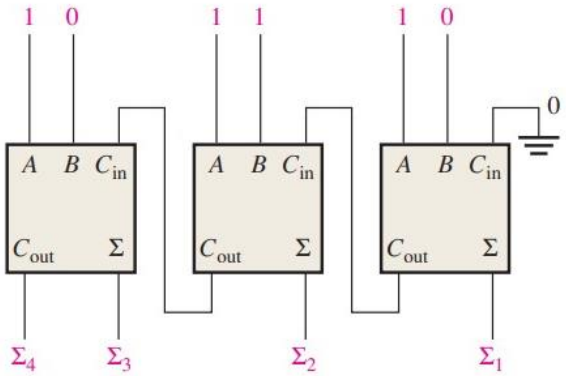
Section 6–2 Parallel Binary Adders

4. For the parallel adder in Figure 6–69, determine the complete sum by analysis of the logical operation of the circuit. Verify your result by longhand addition of the two input numbers.



Section 6–2 Parallel Binary Adders

1. $C_{out}\Sigma_4\Sigma_3\Sigma_2\Sigma_1 = 11001$

Section 6–8 Multiplexers (Data Selectors)

28. For the multiplexer in Figure 6–79, determine the output for the following input states: $D_0 = 1$, $D_1 = 0$, $D_2 = 0$, $D_3 = 1$, $S_0 = 0$, $S_1 = 1$.

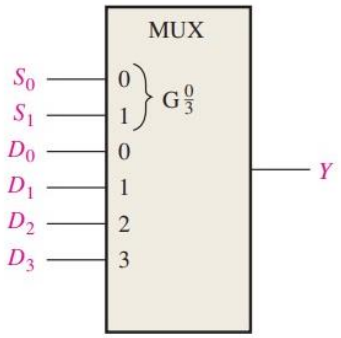
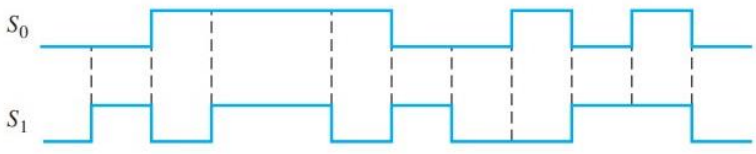


FIGURE 6–79

29. If the data-select inputs to the multiplexer in Figure 6–79 are sequenced as shown by the waveforms in Figure 6–80, determine the output waveform with the data inputs specified in Problem 28.



30. The waveforms in Figure 6–81 are observed on the inputs of a 74HC151 8-input multiplexer. Sketch the *Y* output waveform.

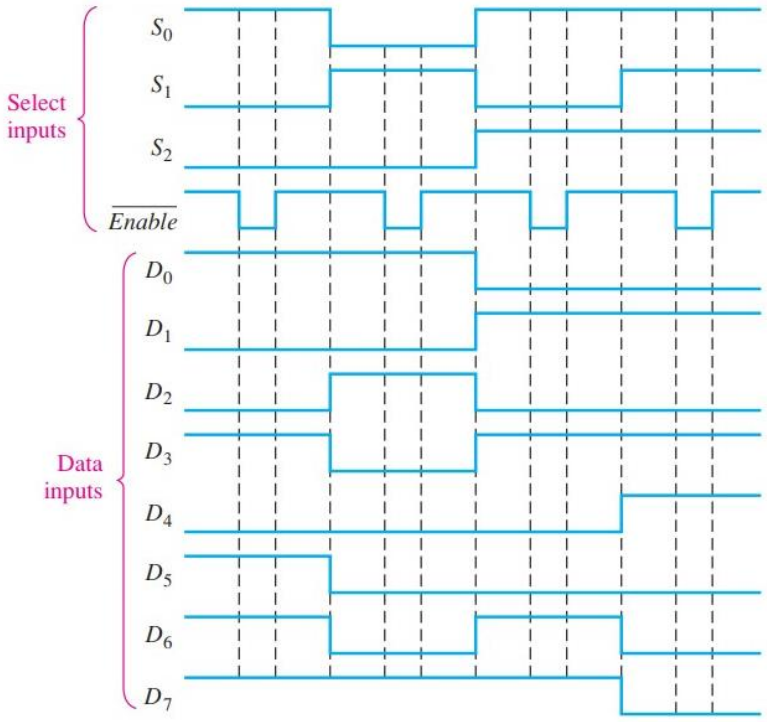


FIGURE 6–81

Section 6–8 Multiplexers (Data Selectors)

1. The output is 0.

2. **(a)** 74HC153: Dual 4-input data selector/multiplexer

(b) 74HC151: 8-input data selector/multiplexer

3. The data output alternates between LOW and HIGH as the data-select inputs sequence through the binary states.

4. **(a)** The 74HC157 multiplexes the two BCD codes to the 7-segment decoder.

(b) The 74HC47 decodes the BCD to energize the display.

(c) The 74HC139 enables the 7-segment displays alternately.

Section 6–9 Demultiplexers

31. Develop the total timing diagram (inputs and outputs) for a 74HC154 used in a demultiplexing application in which the inputs are as follows: The data-select inputs are repetitively sequenced through a straight binary count beginning with 0000, and the data input is a serial data stream carrying BCD data representing the decimal number 2468. The least significant digit (8) is first in the sequence, with its LSB first, and it should appear in the first 4-bit positions of the output.

Section 6–9 Demultiplexers

1. A decoder can be used as a multiplexer by using the input lines for data selection and an Enable line for data input. 2. The outputs are all HIGH except D10, which is LOW.

Chapter 5

1. A latch has one stable state. F

2. A latch is considered to be in the RESET state when the Q output is low. T

3. A gated D latch cannot be used to change state. F

4. Flip-flops and latches are both bistable devices. T

5. An edge-triggered D flip-flop changes state whenever the D input changes. F

6. A clock input is necessary for an edge-triggered flip-flop. T

7. When both the J and K inputs are HIGH, an edge-triggered J-K flip-flop changes state on each clock pulse. T

8. A one-shot is also known as an astable multivibrator. F

9. When triggered, a one-shot produces a single pulse. T

10. The 555 timer cannot be used as a pulse oscillator. F

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1. An active HIGH input S-R latch is formed by the cross-coupling of
   (a) two NOR gates (b) two NAND gates
   c) two OR gates (d) two AND gates

2. Which of the following is not true for an active LOW input S-R latch?

   (a) S = 1, R = 1, Q = NC, Q = NC (b) S = 0, R = 1, Q = 1, Q = 0

   (c) S = 1, R = 0, Q = 1, Q = 0 (d) S = 0, R = 0, Q = 1, Q = 1

3. For what combinations of the inputs D and EN will a D latch reset?

   (a) D = LOW, EN = LOW

   (b) D = LOW, EN = HIGH

   (c) D = HIGH, EN = LOW

   (d) D = HIGH, EN = HIGH

   4. A flip-flop changes its state during the

   (a) complete operational cycle

   (b) falling edge of the clock pulse

   (c) rising edge of the clock pulse

   (d) both answers (b) and (c)

5. The purpose of the clock input to a flip-flop is to

(a) clear the device

(b) set the device

(c) always cause the output to change states

(d) cause the output to assume a state dependent on the controlling (J-K or D) inputs.

6. For an edge-triggered D flip-flop,

(a) a change in the state of the flip-flop can occur only at a clock pulse edge

(b) the state that the flip-flop goes to depends on the D input

(c) the output follows the input at each clock pulse

(d) all of these answers

7. A feature that distinguishes the J-K flip-flop from the D flip-flop is the

(a) toggle condition (b) preset input

(c) type of clock (d) clear input

8. A flip-flop is SET when

(a) J = 0, K = 0 (b) J = 0, K = 1

(c) J = 1, K = 0 (d) J = 1, K = 1

9. A J-K flip-flop with J = 1 and K = 1 has a 10 kHz clock input. The Q output is

(a) constantly HIGH (b) constantly LOW

(c) a 10 kHz square wave (d) a 5 kHz square wave

10. A one-shot is a type of

(a) monostable multivibrator (b) astable multivibrator (c) timer

(d) answers (a) and (c) (e) answers (b) and (c)

11. The output pulse width of a nonretriggerable one-shot depends on

(a) the trigger intervals (b) the supply voltage

(c) a resistor and capacitor (d) the threshold voltage

12. An astable multivibrator

(a) requires a periodic trigger input (b) has no stable state

(c) is an oscillator (d) produces a periodic pulse output (e) answers (a), (b), (c), and (d) (f) answers (b), (c), and (d) only

Section 7–1 Latches

1. If the waveforms in Figure 7–70 are applied to an active-HIGH S-R latch, draw the resulting Q output waveform in relation to the inputs. Assume that Q starts LOW.

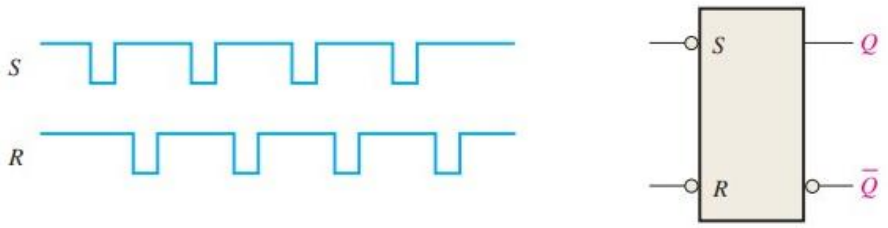

FIGURE 7–70

2. Solve Problem 1 for the input waveforms in Figure 7–71 applied to an active-LOW $\overline{S} - \overline{R}$ latch.

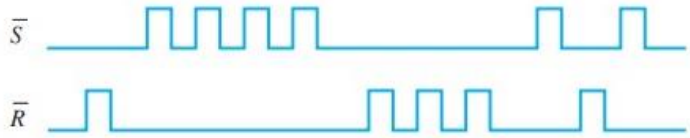

FIGURE 7–71

3. Solve Problem 1 for the input waveform in Figure 7–72.

FIGURE 7–72

Section 7–1 Latches

1. Three types of latches are S-R, gated S-R, and gated D.

2. $SR = 00$, NC; $SR = 01$, $Q = 0$; $SR = 10$, $Q = 1$; $SR = 11$, invalid

3. $Q = 1$

Section 7–2 Flip-Flops

8. Two edge-triggered J-K flip-flops are shown in Figure 7–77. If the inputs are as shown, draw the Q output of each flip-flop relative to the clock, and explain the difference between the two. The flip-flops are initially RESET.

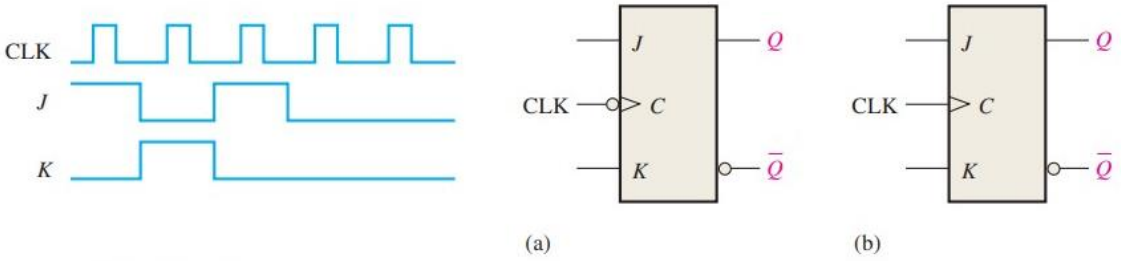

FIGURE 7–77

9. The Q output of an edge-triggered D flip-flop is shown in relation to the clock signal in Figure 7–78. Determine the input waveform on the D input that is required to produce this output if the flip-flop is a positive edge-triggered type.

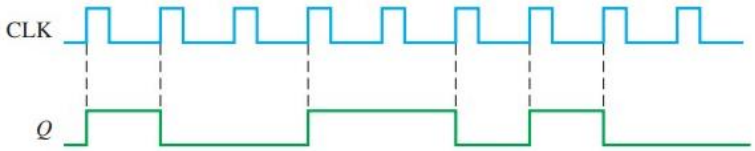

FIGURE 7–78

10. Draw the Q output relative to the clock for a D flip-flop with the inputs as shown in Figure 7–79. Assume positive edge-triggering and Q initially LOW.

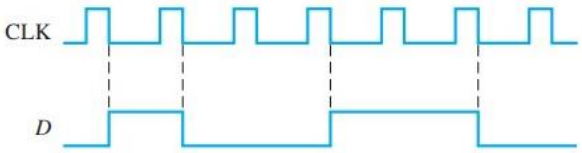

FIGURE 7–79

Section 7–2 Flip-Flops

1. The output of a gated D latch can change any time the gate enable (*EN*) input is active. The output of an edge-triggered D flip-flop can change only on the triggering edge of a clock pulse.
2. The output of a J-K flip-flop is determined by the state of its two inputs whereas the output of a D flip-flop follows the input.
3. Output Q goes HIGH on the trailing edge of the first clock pulse, LOW on the trailing edge of the second pulse, HIGH on the trailing edge of the third pulse, and LOW on the trailing edge of the fourth pulse.